FLEX 8000

Programmable Logic Device Family

January 2003, ver. 11.1 **Data Sheet**

Features...

- Low-cost, high-density, register-rich CMOS programmable logic device (PLD) family (see Table 1)
  - 2,500 to 16,000 usable gates
  - 282 to 1,500 registers
- System-level features
  - In-circuit reconfigurability (ICR) via external configuration devices or intelligent controller
  - Fully compliant with the peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 5.0-V operation
  - Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990 on selected devices
  - MultiVolt™ I/O interface enabling device core to run at 5.0 V, while I/O pins are compatible with 5.0-V and 3.3-V logic levels
  - Low power consumption (typical specification is 0.5 mA or less in standby mode)
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state nets
- Powerful I/O pins
- Programmable output slew-rate control reduces switching noise

Table 1. FLEX 8000 Device Features

Feature	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
Usable gates	2,500	4,000	6,000	8,000	12,000	16,000
Flipflops	282	452	636	820	1,188	1,500
Logic array blocks (LABs)	26	42	63	84	126	162
Logic elements (LEs)	208	336	504	672	1,008	1,296
Maximum user I/O pins	78	120	136	152	184	208

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes

...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

Table 2. FLEX 8000 Package Options & I/O Pin Count Note (1)

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

Note:

(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance and LE requirements for typical applications.

Table 3. FLEX 8000 Performance

Application	LEs Used	Speed Grade			Units
		A-2	A-3	A-4	
16-bit loadable counter	16	125	95	83	MHz
16-bit up/down counter	16	125	95	83	MHz
24-bit accumulator	24	87	67	58	MHz
16-bit address decode	4	4.2	4.9	6.3	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	ns

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

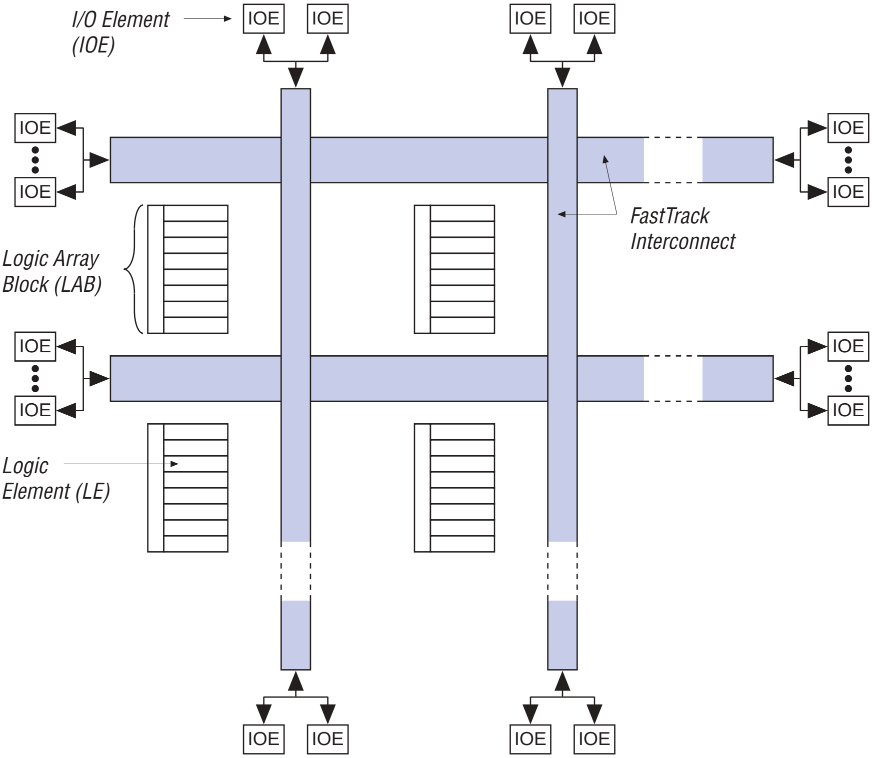
Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

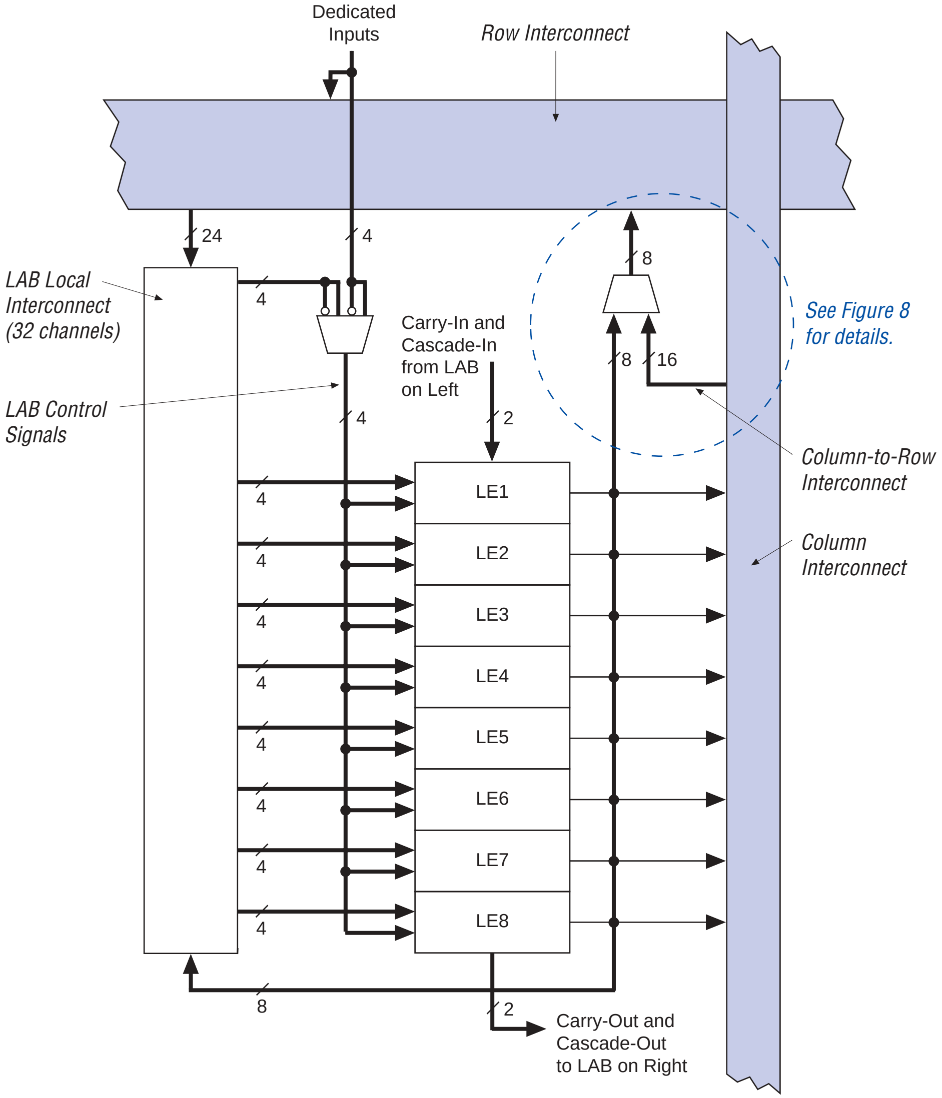


Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

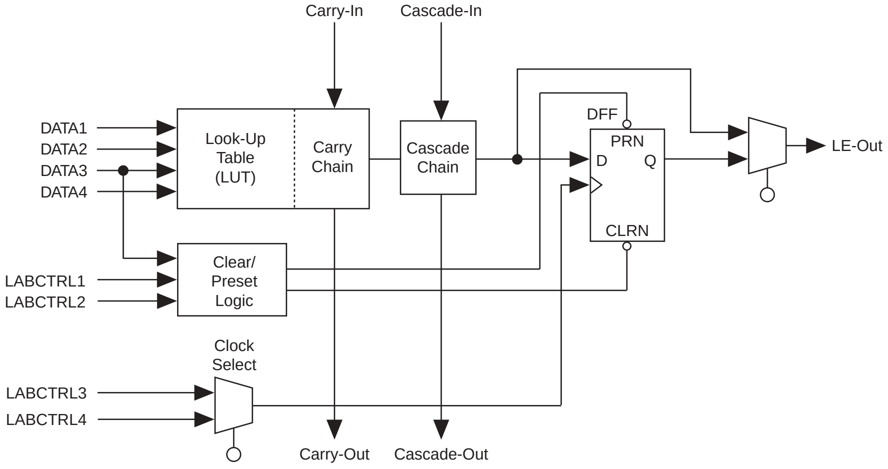


Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

Figure 3. FLEX 8000 LE



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

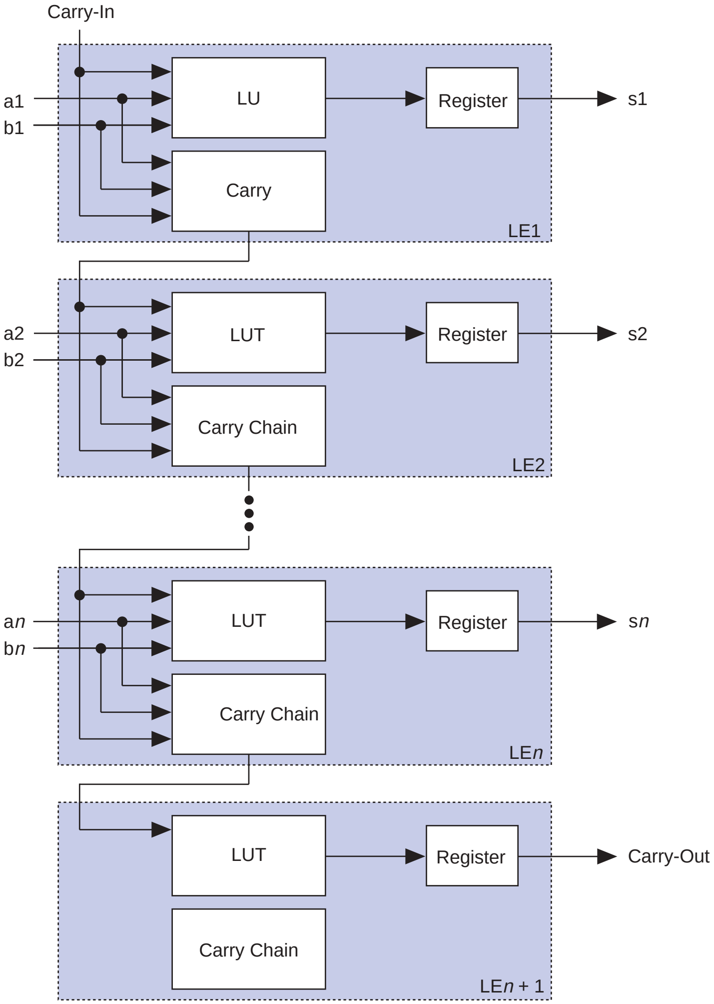
The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce routing flexibility. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 4 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to another LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

Figure 4. FLEX 8000 Carry Chain Operation



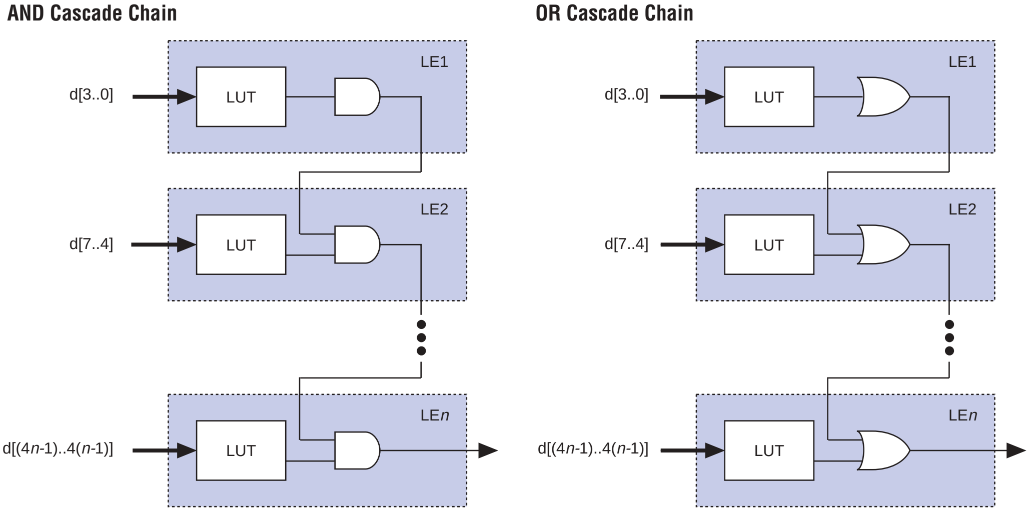
Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical `AND` or logical `OR` (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 5. FLEX 8000 Cascade Chain Operation

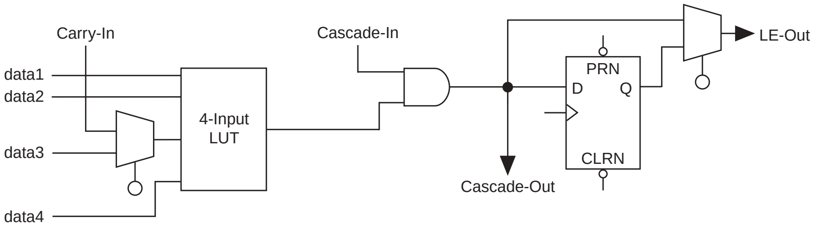


LE Operating Modes

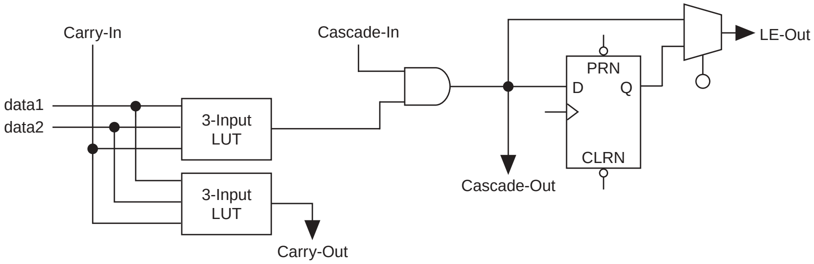
The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 6. FLEX 8000 LE Operating Modes

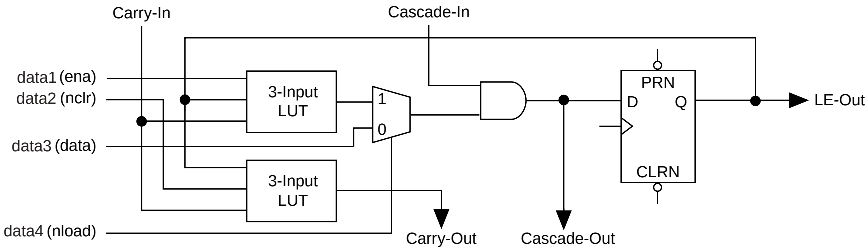
Normal Mode



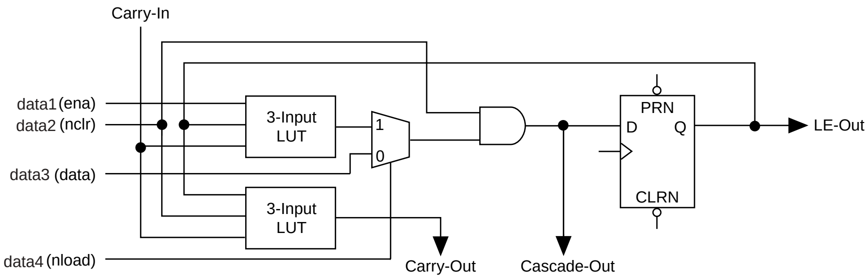
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the `DATA3` signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The `LE-Out` signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (`Q`)of the programmable register.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: `a`, `b`, and the carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is `AND`ed with a synchronous clear.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

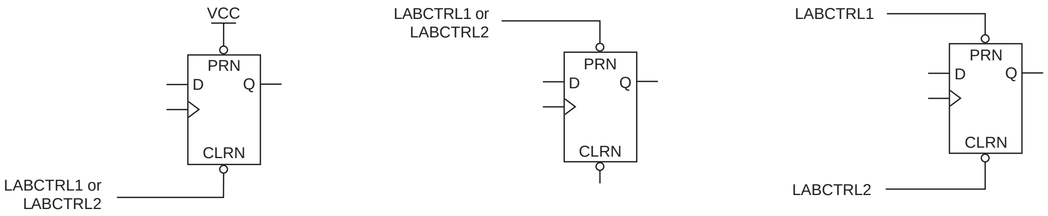
Logic for the programmable register's clear and preset functions is controlled by the `DATA3`, `LABCTRL1`, and `LABCTRL2` inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that `LABCTRL1` implements an asynchronous load. The data to be loaded is driven to `DATA3`; when `LABCTRL1` is asserted, `DATA3` is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

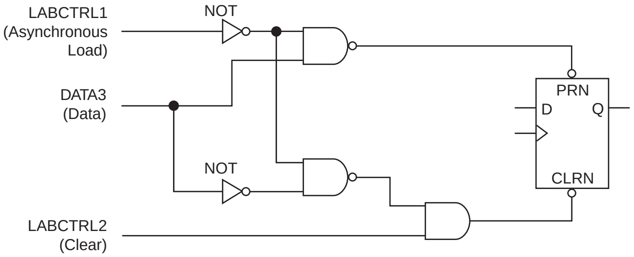


Asynchronous Clear

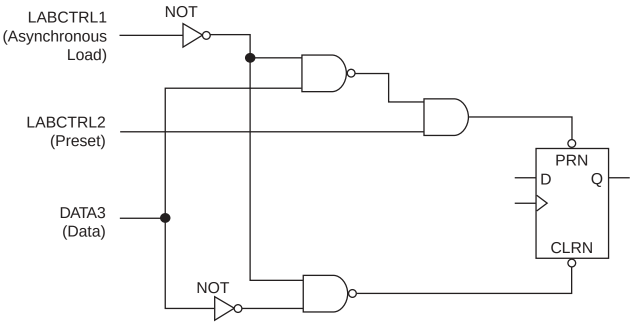
Asynchronous Preset

Asynchronous Clear & Preset

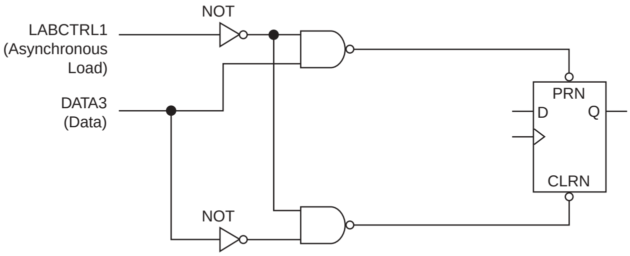
Asynchronous Load with Clear



Asynchronous Load with Preset



Asynchronous Load without Clear or Preset



Asynchronous Clear

A register is cleared by one of the two `LABCTRL` signals. When the `CLRn` port receives a low signal, the register is set to zero.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If `DATA3` is tied to `VCC`, asserting `LABCTRLl` asynchronously loads a `1` into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two `LABCTRL` signals, the `DATA3` input is not needed and can be used for one of the LE operating modes.

Asynchronous Clear & Preset

When implementing asynchronous clear and preset, `LABCTRL1` controls the preset and `LABCTRL2` controls the clear. The `DATA3` input is tied to `VCC`; therefore, asserting `LABCTRL1` asynchronously loads a `1` into the register, effectively presetting the register. Asserting `LABCTRL2` clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load with the clear, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear. `LABCTRL2` implements the clear by controlling the register clear.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting `LABCTRL2` clears the register, while asserting `LABCTRL1` loads the register. The MAX+PLUS II software inverts the signal that drives the `DATA3` signal to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

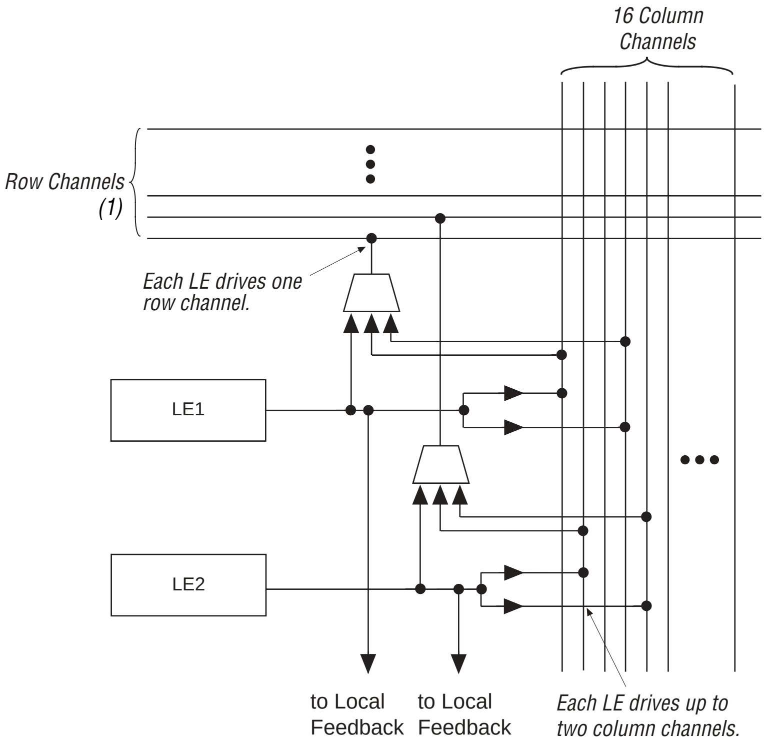
When implementing an asynchronous load without the clear or preset, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal (row) and vertical (column) routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing structure in FPGAs requires switch matrices to connect a variable number of routing paths, which increases the delays between logic resources and reduces performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

Figure 8. FLEX 8000 LAB Connections to Row & Column Interconnect



Note:
(1) See Table 4 for the number of row channels.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

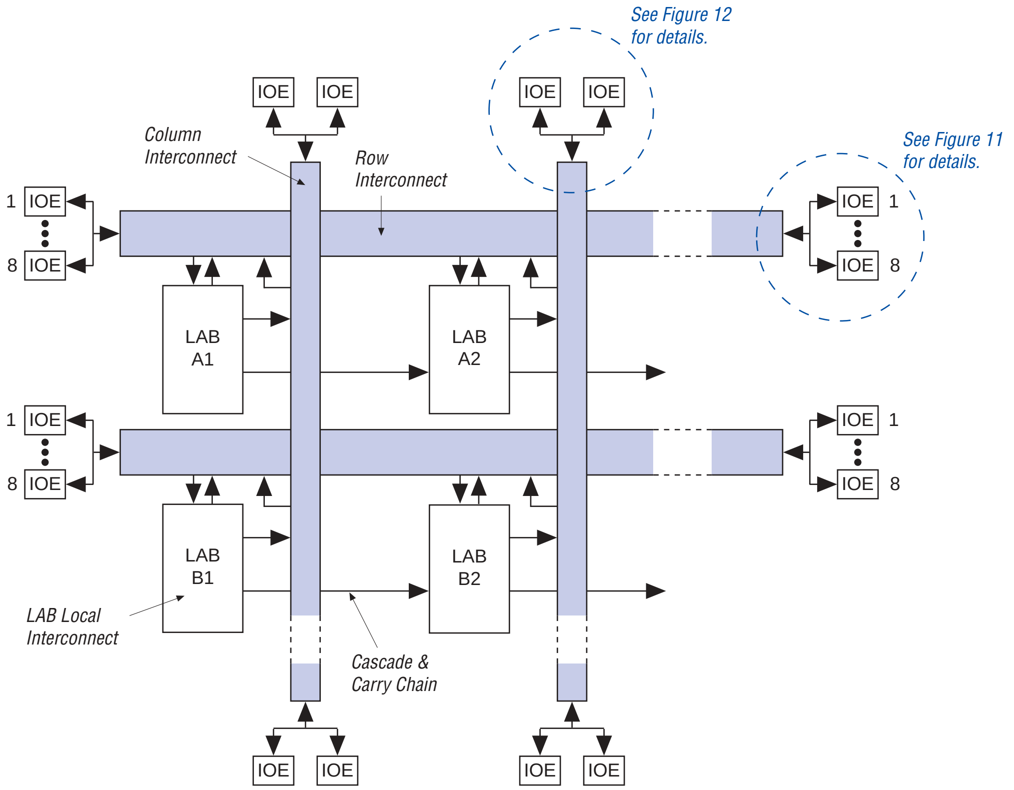
Table 4. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 9. FLEX 8000 Device Interconnect Resources

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.

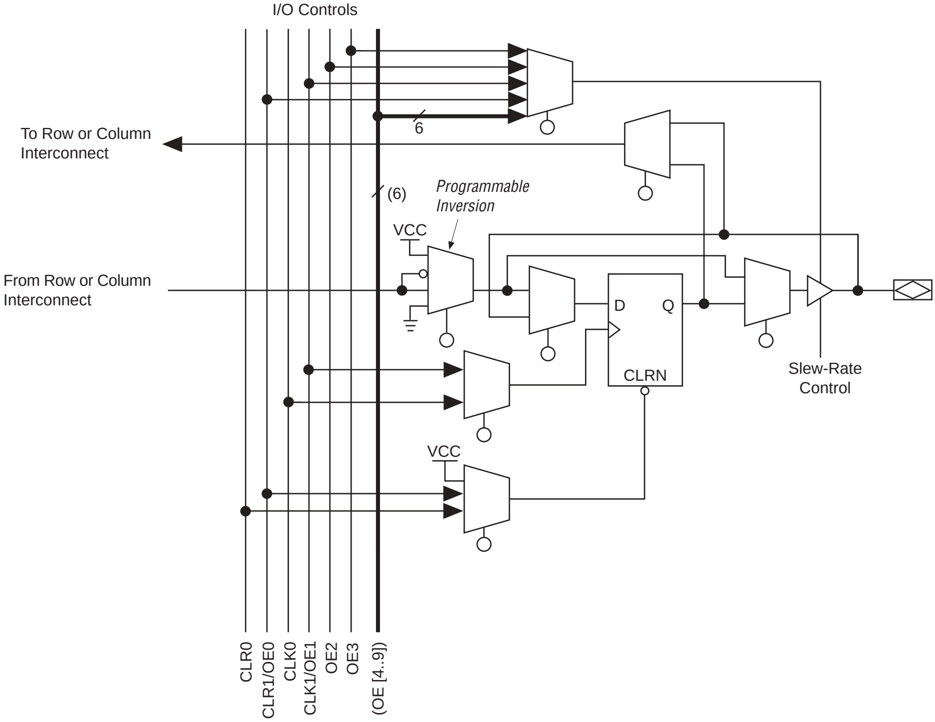


I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

Figure 10. FLEX 8000 IOE

Numbers in parentheses are for EPF81500A devices only.

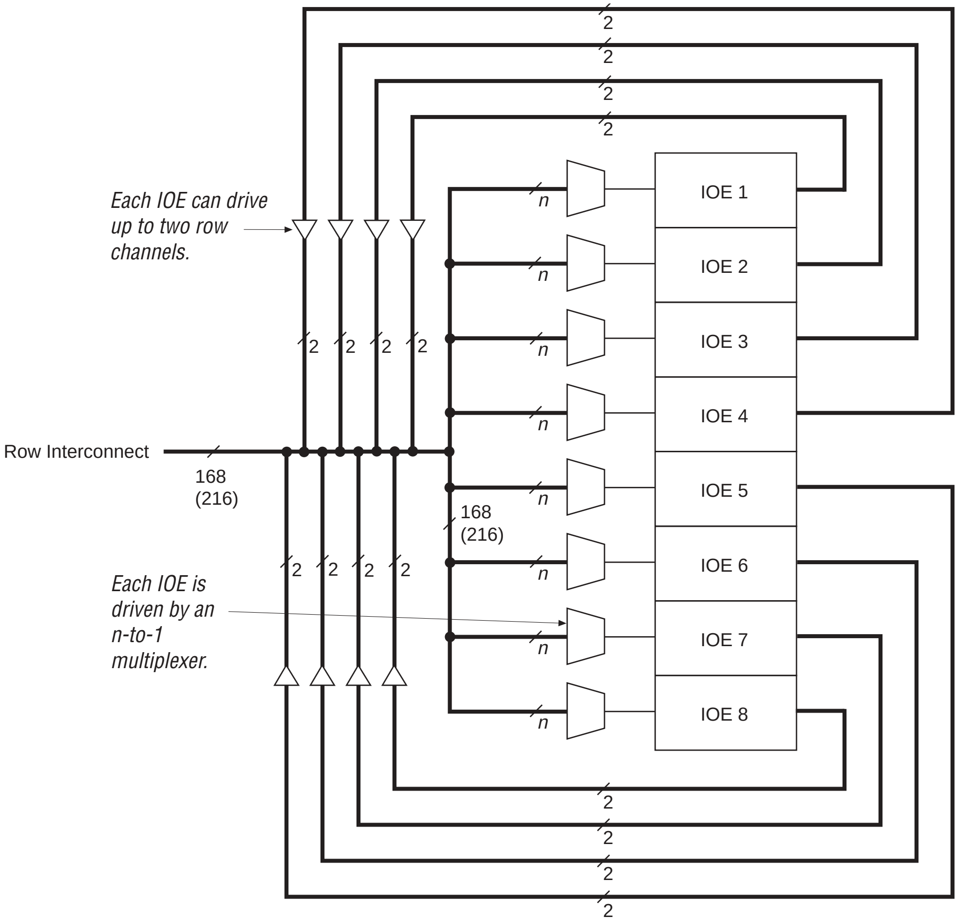


Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Figure 11. FLEX 8000 Row-to-IOE Connections

Numbers in parentheses are for EPF81500A devices. See Note (1).



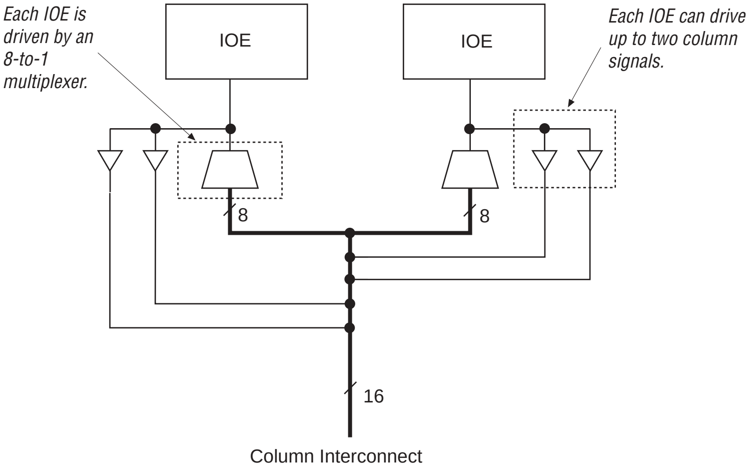
Note:

(1) n = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
n = 27 for EPF81500A devices.

Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see Figure 12). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

Figure 12. FLEX 8000 Column-to-IOE Connections



In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

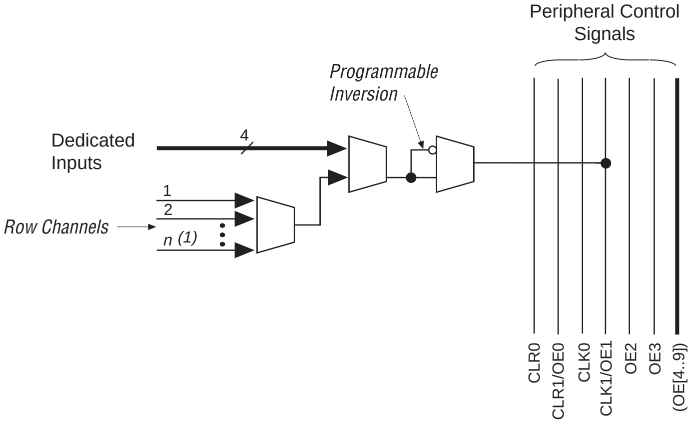
I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This “peripheral bus” can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. Figure 13 on page 22 shows how two output enable signals are shared with one clock and one clear signal.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500A devices.



Note:

(1) *n* = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
n = 27 for EPF81500A devices.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 5. Row Sources of FLEX 8000 Peripheral Control Signals

Peripheral Control Signal	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
`CLK0`	Row A	Row A	Row A	Row A	Row E	Row E
`CLK1/OE1`	Row B	Row B	Row C	Row C	Row B	Row B
`CLR0`	Row A	Row A	Row B	Row B	Row F	Row F
`CLR1/OE0`	Row B	Row B	Row C	Row D	Row C	Row C
`OE2`	Row A	Row A	Row A	Row A	Row D	Row A
`OE3`	Row B	Row B	Row B	Row B	Row A	Row A
`OE4`	–	–	–	–	–	Row B
`OE5`	–	–	–	–	–	Row C
`OE6`	–	–	–	–	–	Row D
`OE7`	–	–	–	–	–	Row D
`OE8`	–	–	–	–	–	Row E
`OE9`	–	–	–	–	–	Row F

Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

For more information on high-speed system design, go to *Application Note 75 (High-Speed Board Designs)*.

MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCINT` pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. See Table 8 on page 26.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

The instruction register length for FLEX 8000 devices is three bits. Table 7 shows the boundary-scan register length for FLEX 8000 devices.

Table 7. FLEX 8000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF8282A, EPF8282AV	273
EPF8636A	417
EPF8820A	465
EPF81500A	645

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. Figure 14 shows the timing requirements for the JTAG signals.

Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms

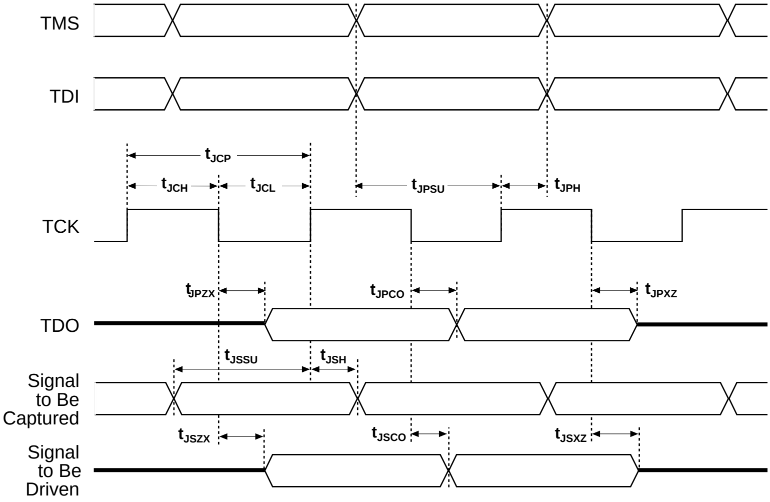


Table 8 shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.

Table 8. JTAG Timing Parameters & Values

Symbol	Parameter	EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A		Unit
		Min	Max	
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high-impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high-impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high-impedance		35	ns

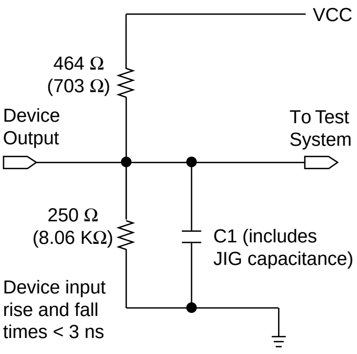
For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Designers can use multiple test patterns to configure devices during all stages of the production flow.

Figure 15. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers without parentheses are for 5.0-V devices or outputs.



Operating Conditions

Tables 9 through 12 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V FLEX 8000 devices.

Table 9. FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP, under bias		135	° C

Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 11. FLEX 8000 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC (7) V_{CCIO} = 4.75 V	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC (7) V_{CCIO} = 3.00 V	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC (7) V_{CCIO} = 3.00 V	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC (7) V_{CCIO} = 4.75 V			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC (7) V_{CCIO} = 3.00 V			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC (7) V_{CCIO} = 3.00 V			0.2	V
I_I	Input leakage current	V_I = V_{CC} or ground	–10		10	μA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or ground	–40		40	μA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	10	mA

Table 12. FLEX 8000 5.0-V Device Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum V_{CC} rise time is 100 ms.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified in Table 10 on page 28.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL or CMOS output current.
(8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	5.3	V
V_I	DC input voltage		–2.0	5.3	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Plastic packages, under bias		135	° C

Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*(3)*	3.0	3.6	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 15. FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC *(5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(5)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or ground	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or ground	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load *(6)*		0.3	10	mA

Table 16. FLEX 8000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(4) These values are specified in Table 14 on page 29.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)

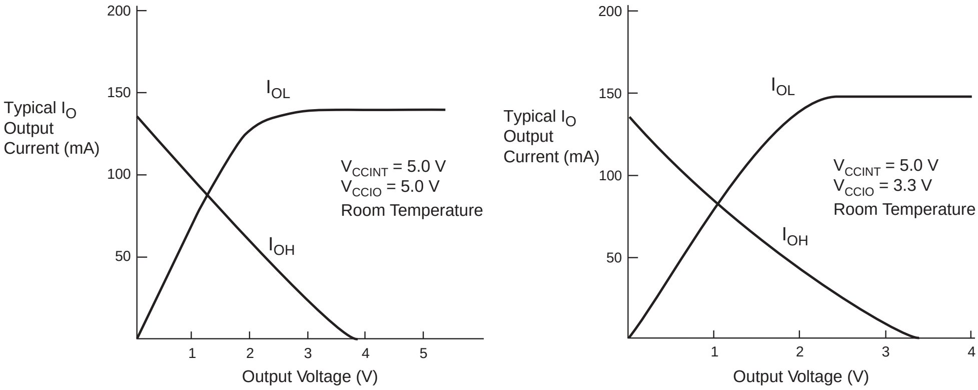


Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO}

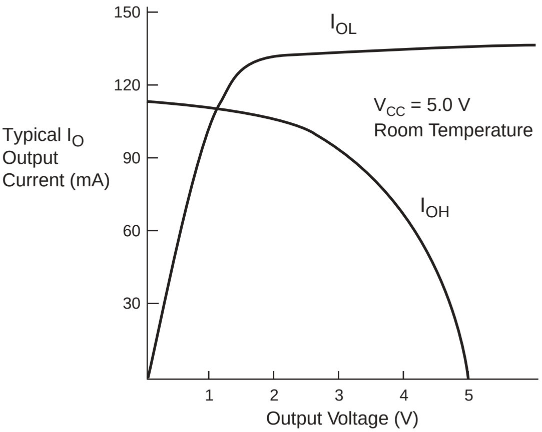
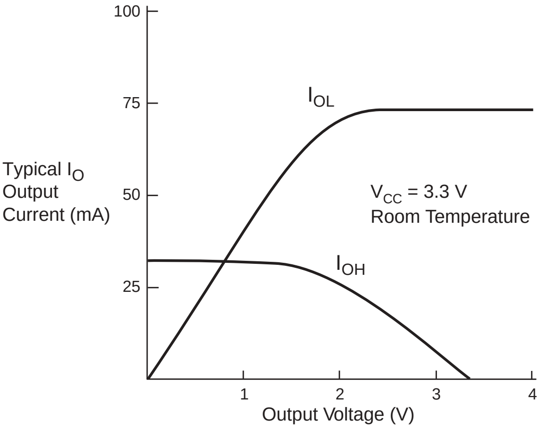


Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

Figure 18. Output Drive Characteristics of EPF8282AV Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

Table 17. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock; IOE register recovery time after asynchronous clear
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V C1 = 35 pF *(2)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF *(2)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)*

Table 18. FLEX 8000 LE Timing Parameters *Note (1)*

Symbol	Parameter
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	LE register clock high time
t_{CL}	LE register clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 19. FLEX 8000 Interconnect Timing Parameters *Note (1)*

Symbol	Parameter
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay *(4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay *(4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 20. FLEX 8000 External Reference Timing Characteristics *Note (5)*

Symbol	Parameter
$\mathbf{t_{DRR}}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)*
$\mathbf{t_{ODH}}$	Output data hold time after clock *(7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.

(3) For the t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.

(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.

(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.

(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

Figure 19. FLEX 8000 Timing Model

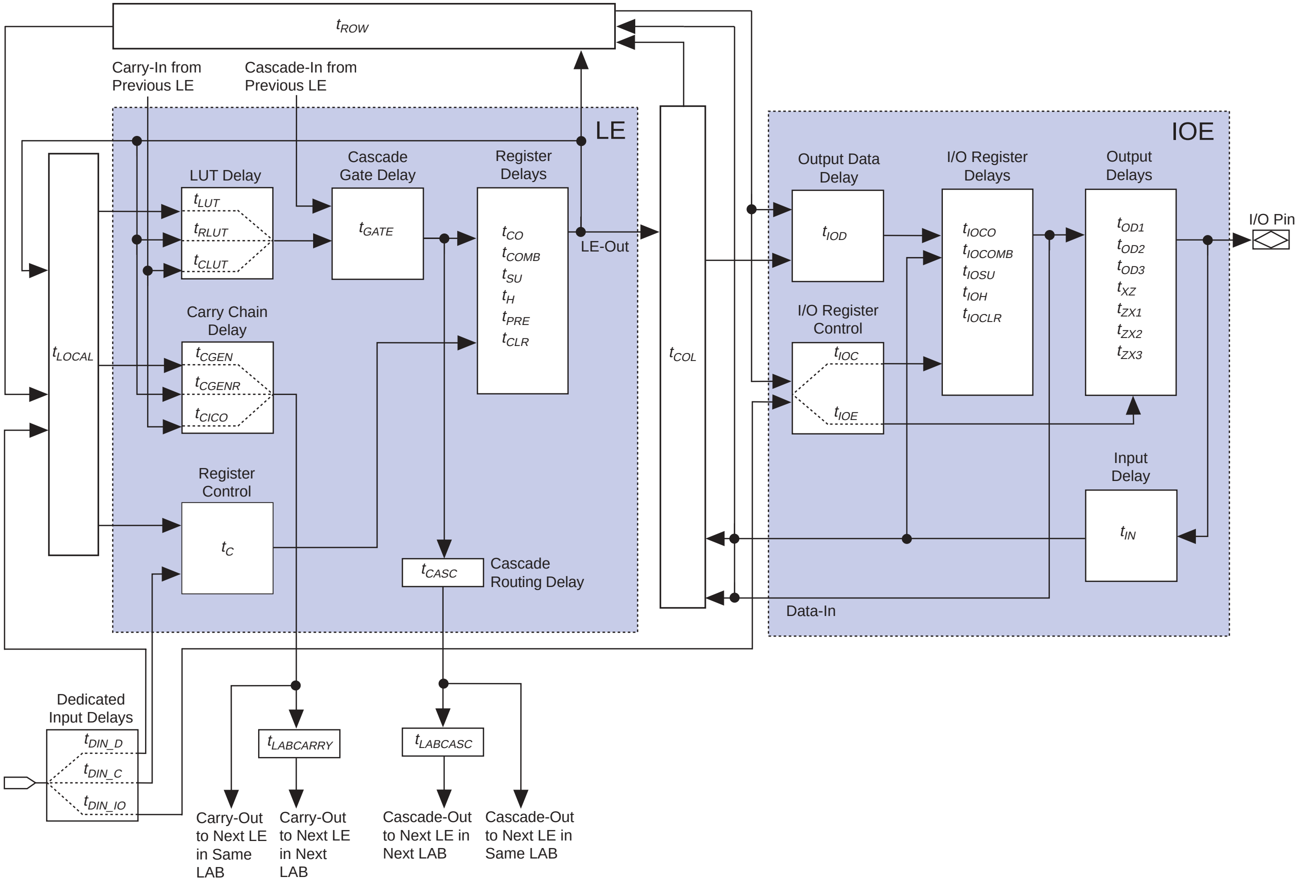


Table 21. FLEX 8000 Timing Model Interconnect Paths

Source	Destination	Total Delay
LE-Out	LE in same LAB	t_{LOCAL}
LE-Out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-Out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-Out	IOE on column	t_{COL}
LE-Out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

Table 22. EPF8282A Internal I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 23. EPF8282A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 24. EPF8282A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 25. EPF8282A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.8		19.8		24.8	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 26. EPF8282AV I/O Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{IOD}		0.9		2.2	ns
t_{IOC}		1.9		2.0	ns
t_{IOE}		1.9		2.0	ns
t_{IOCO}		1.0		2.0	ns
t_{IOCOMB}		0.1		0.0	ns
t_{IOSU}	1.8		2.8		ns
t_{IOH}	0.0		0.2		ns
t_{IOCLR}		1.2		2.3	ns
t_{IN}		1.7		3.4	ns
t_{OD1}		1.7		4.1	ns
t_{OD2}		–		–	ns
t_{OD3}		5.2		7.1	ns
t_{XZ}		1.8		4.3	ns
t_{ZX1}		1.8		4.3	ns
t_{ZX2}		–		–	ns
t_{ZX3}		5.3		8.3	ns

Table 27. EPF8282AV Interconnect Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
$t_{LABCASC}$		0.4		1.3	ns
$t_{LABCARRY}$		0.4		0.8	ns
t_{LOCAL}		0.8		1.5	ns
t_{ROW}		4.2		6.3	ns
t_{COL}		2.5		3.8	ns
t_{DIN_C}		5.5		8.0	ns
t_{DIN_D}		7.2		10.8	ns
t_{DIN_IO}		5.5		9.0	ns

Table 28. EPF8282AV Logic Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{LUT}		3.2		7.3	ns
t_{CLUT}		0.0		1.4	ns
t_{RLUT}		1.5		5.1	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		0.9		2.8	ns
t_{CICO}		0.6		1.5	ns
t_{CGEN}		0.7		2.2	ns
t_{CGENR}		1.5		3.7	ns
t_{C}		2.5		4.7	ns
t_{CH}	4.0		6.0		ns
t_{CL}	4.0		6.0		ns
t_{CO}		0.6		0.9	ns
t_{COMB}		0.6		0.9	ns
t_{SU}	1.2		2.4		ns
t_{H}	1.5		4.6		ns
t_{PRE}		0.8		1.3	ns
t_{CLR}		0.8		1.3	ns

Table 29. EPF8282AV External Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
$\mathbf{t_{DRR}}$		24.8		50.1	ns
$\mathbf{t_{ODH}}$	1.0		1.0		ns

Table 30. EPF8452A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 31. EPF8452A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 32. EPF8452A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_C		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_H	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 34. EPF8636A I/O Element Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 35. EPF8636A Interconnect Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 36. EPF8636A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_C		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_H	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 37. EPF8636A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 38. EPF8820A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 39. EPF8820A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 40. EPF8820A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 41. EPF8820A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 42. EPF81188A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 43. EPF81188A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$\mathbf{t_{DRR}}$		16.0		20.0		25.0	ns
$\mathbf{t_{ODH}}$	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 48. EPF81500A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 49. EPF81500A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.1		20.1		25.1	ns
t_{ODH}	1.0		1.0		1.0		ns

Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in Table 11 on page 28 and Table 15 on page 30. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock
K = Constant, shown in Table 50

Table 50. Values for Constant K

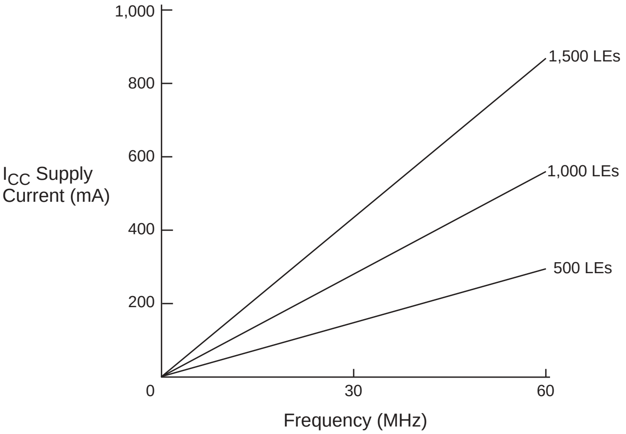
Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

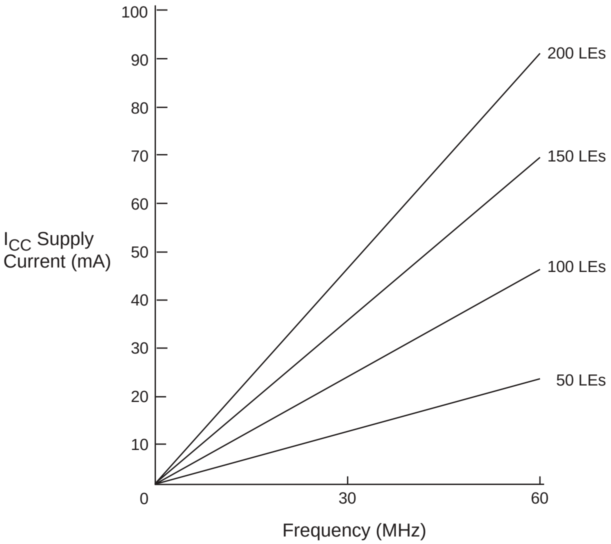
Figure 20 shows the relationship between I_{CC} and operating frequency for several LE utilization values.

Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. Table 51 shows the data source for each of the six configuration schemes.

Table 51. Data Source for Configuration

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
`nSP` *(2)*	75	75	75	76	110	R1	1
`MSEL0` *(2)*	74	74	74	75	109	P2	2
`MSEL1` *(2)*	53	53	51	51	72	A1	44
`nSTATUS` *(2)*	32	32	24	25	37	C13	82
`nCONFIG` *(2)*	33	33	25	26	38	A15	81
`DCLK` *(2)*	10	10	100	100	143	P14	125
`CONF_DONE` *(2)*	11	11	1	1	144	N13	124
`nWS`	30	30	22	23	33	F13	87
`nRS`	48	48	42	45	31	C6	89
`RDCLK`	49	49	45	46	12	B5	110
`nCS`	29	29	21	22	4	D15	118
`CS`	28	28	19	21	3	E15	121
`RDYnBUSY`	77	77	77	78	20	P3	100
`CLKUSR`	50	50	47	47	13	C5	107
`ADD17`	51	51	49	48	75	B4	40
`ADD16`	36	55	28	54	76	E2	39
`ADD15`	56	56	55	55	77	D1	38
`ADD14`	57	57	57	57	78	E1	37
`ADD13`	58	58	58	58	79	F3	36
`ADD12`	60	60	59	60	83	F2	32
`ADD11`	61	61	60	61	85	F1	30
`ADD10`	62	62	61	62	87	G2	28
`ADD9`	63	63	62	64	89	G1	26
`ADD8`	64	64	64	65	92	H1	22
`ADD7`	65	65	65	66	94	H2	20
`ADD6`	66	66	66	67	95	J1	18
`ADD5`	67	67	67	68	97	J2	16
`ADD4`	69	69	68	70	102	K2	11
`ADD3`	70	70	69	71	103	K1	10
`ADD2`	71	71	71	72	104	K3	8
`ADD1`	76	72	76	73	105	M1	7

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
`ADD0`	78	76	78	77	106	N3	6
`DATA7`	3	2	90	89	131	P8	140
`DATA6`	4	4	91	91	132	P10	139
`DATA5`	6	6	92	95	133	R12	138
`DATA4`	7	7	95	96	134	R13	136
`DATA3`	8	8	97	97	135	P13	135
`DATA2`	9	9	99	98	137	R14	133
`DATA1`	13	13	4	4	138	N15	132
`DATA0`	14	14	5	5	140	K13	129
`SDOUT` *(3)*	79	78	79	79	23	P4	97
`TDI` *(4)*	55	45 *(5)*	54	–	96	–	17
`TDO` *(4)*	27	27 *(5)*	18	–	18	–	102
`TCK` *(4)*, *(6)*	72	44 *(5)*	72	–	88	–	27
`TMS` *(4)*	20	43 *(5)*	11	–	86	–	29
`TRST` *(7)*	52	52 *(8)*	50	–	71	–	45
Dedicated Inputs *(10)*	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
`VCCINT`	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
`VCCIO`	–	–	–	–	16, 40, 60, 69, 91, 112, 122, 141	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
`GND`	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100,101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155
No Connect (N.C.)	–	–	–	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	–	–	–
Total User I/O Pins *(9)*	64	64	74	64	108	116	116

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
nSP *(2)*	120	1	R15	207	207	5
MSEL0 *(2)*	117	3	T15	4	4	21
MSEL1 *(2)*	84	38	T3	49	49	33
nSTATUS *(2)*	37	83	B3	108	108	124
nCONFIG *(2)*	40	81	C3	103	103	107
DCLK *(2)*	1	120	C15	158	158	154
CONF_DONE *(2)*	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
`DATA4`	154	127	E17	165	172	170
`DATA3`	157	124	G15	162	171	168
`DATA2`	159	122	F15	160	167	166
`DATA1`	11	115	E16	149	165	163
`DATA0`	12	113	C16	147	162	161
`SDOUT` *(3)*	128	152	C7 *(11)*	198	124	119
`TDI` *(4)*	–	55	R11	72	20	–
`TDO` *(4)*	–	95	B9	120	129	–
`TCK` *(4)*, *(6)*	–	57	U8	74	30	–
`TMS` *(4)*	–	59	U7	76	32	–
`TRST` *(7)*	–	40	R3	54	54	–
Dedicated Inputs *(10)*	5, 36, 85, 116	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146
`VCCINT` (5.0 V)	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147
`VCCIO` (5.0 V or 3.3 V)	–	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192
`GND`	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201
No Connect (N.C.)	2, 3, 38, 39, 70, 82, 83, 118, 119, 148	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 *(12)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208
Total User I/O Pins *(9)*	116	114	132, 148 *(13)*	132	148	144

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(2)*	A15	C14	237	237	W1	304
MSEL0 *(2)*	B14	G15	21	19	N1	26
MSEL1 *(2)*	R15	L15	40	38	H3	51
nSTATUS *(2)*	P2	L3	141	142	G19	178
nCONFIG *(2)*	R1	R4	117	120	B18	152
DCLK *(2)*	B2	C4	184	183	U18	230
CONF_DONE *(2)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
`DATA4`	A5	C7	198	194	W16	248
`DATA3`	B5	D7	196	193	W17	246
`DATA2`	E6	B5	194	190	V16	243
`DATA1`	D5	A3	191	189	U16	241
`DATA0`	C4	A2	189	187	V17	239
`SDOUT` *(3)*	K1	N2	135	136	F19	169
`TDI`	F15 *(4)*	–	–	63 *(14)*	B1 *(14)*	80 *(14)*
`TDO`	J2 *(4)*	–	–	117	C17	149
`TCK` *(6)*	J14 *(4)*	–	–	116 *(14)*	A19 *(14)*	148 *(14)*
`TMS`	J12 *(4)*	–	–	64 *(14)*	C2 *(14)*	81 *(14)*
`TRST` *(7)*	P14	–	–	115 *(14)*	A18 *(14)*	145 *(14)*
Dedicated Inputs *(10)*	F4, L1, K12, E15	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
`VCCINT` (5.0 V)	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
`VCCIO` (5.0 V or 3.3 V)	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
`GND`	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	–	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins *(9)*	148	180	180	177	204	204

Notes to tables:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) `SDOUT` will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use `SDOUT` as a user I/O pin; the user can override the MAX+PLUS II software and use `SDOUT` as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) `TRST` is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) `SDOUT` does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, `TDI`, `TCK`, `TMS`, and `TRST` should be tied to `GND`.

Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.