System-Side Impedance Track™ Fuel Gauge With Integrated LDO

Check for Samples: bq27520-G4

FEATURES

- **Single series cell Li-Ion battery fuel gauge resides on system board**
  - **Integrated 2.5 VDC LDO**
  - **External low-value 10 mΩ sense resistor**
- **Patented Impedance Track™ technology**
  - **Adjusts for battery aging, self-discharge, temperature, and rate changes**
  - **Reports Remaining Capacity, State of Charge (SOC), and Time-to-Empty**
    - **Optional Smoothing Filter**
  - **Battery State of Health (aging) estimation**
  - **Supports embedded or removable packs with up to 32Ahr capacity**
    - **Accomodates pack swapping with 2 separate battery profiles**
- **Microcontroller peripheral supports:**
  - **400-kHz I²C ™ serial interface**
  - **32 Bytes of Scratch-Pad FLASH NVM**
  - **Battery Low digital ouptut warning**
  - **Configurable SOC Interrupts**
  - **External thermistor, internal sensor, or host reported temperature options**
- **Tiny 15-pin 2610 × 1956 µm, 0.5 mm pitch NanoFree™ (CSP) package**

APPLICATIONS

- **Smartphones, Feature phones and Tablets**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

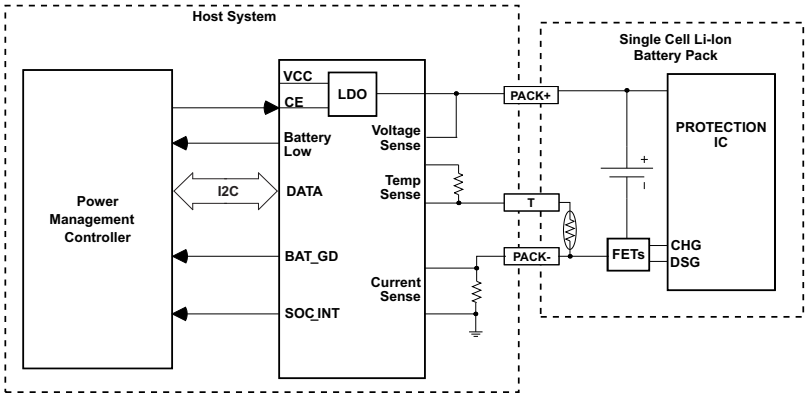
DESCRIPTION

The Texas Instruments bq27520-G4 system-side Li-Ion battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell Li-Ion battery packs. The device requires little system microcontroller firmware development. The bq27520-G4 resides on the system's main board and manages an embedded battery (non-removable) or a removable battery pack.

The bq27520-G4 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), run-time to empty (min), battery voltage (mV), temperature (°C) and state of health (%).

Battery fuel gauging with the bq27520-G4 requires only PACK+ (P+), PACK– (P–), and optional Thermistor (T) connections to a removable battery pack or embedded battery circuit. The device uses a 15-ball NanoFree™ (CSP) package in the nominal dimensions of 2610 × 1956 µm with 0,5 mm lead pitch. It is ideal for space constrained applications.

TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

AVAILABLE OPTIONS

PART NUMBER	FIRMWARE VERSION(1)	PACKAGE(2)	T_A	COMMUNICATION FORMAT	TAPE and REEL QUANTITY
bq27520YZFR-G4	3.29 (0x0329)	CSP-15	–40°C to 85°C	I^2C	3000
bq27520YZFT-G4					250

(1) Refer to the *FW_VERSION* subcommand to confirm the firmware version.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		bq27520-G4 YZF(15 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	70	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17	
θ_{JB}	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	18	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

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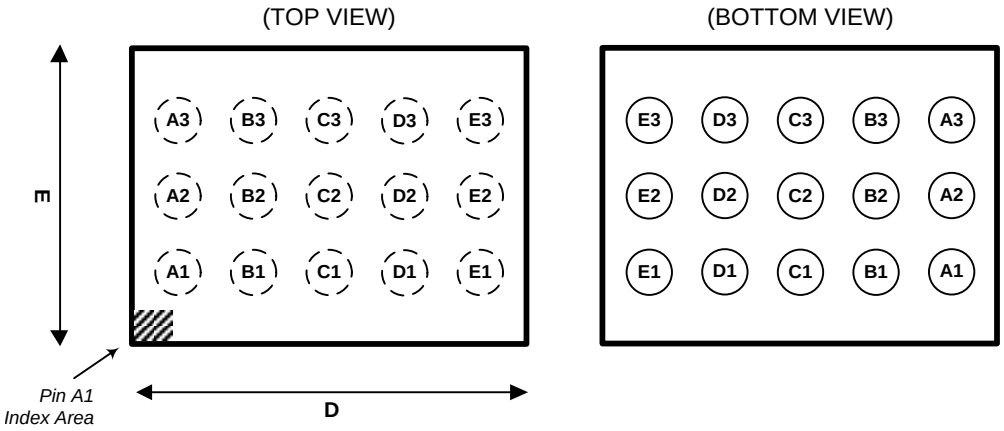
PIN ASSIGNMENT AND PACKAGE DIMENSIONS



DIM	MIN	TYP	MAX	UNITS
D	2580	2610	2640	µm
E	1926	1956	1986	

Table 1. PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SRP	A1	IA	Analog input pin connected to the internal coulomb counter with a Kelvin connection where SRP is nearest the PACK– connection. Connect to 5-mΩ to 20-mΩ sense resistor.
SRN	B1	IA	Analog input pin connected to the internal coulomb counter with a Kelvin connection where SRN is nearest the Vss connection. Connect to 5-mΩ to 20-mΩ sense resistor.
V_{SS}	C1, C2	P	Device ground
V_{CC}	D1	P	Regulator output and bq27520-G4 processor power. Decouple with 1µF ceramic capacitor to Vss.
REGIN	E1	P	Regulator input. Decouple with 0.1µF ceramic capacitor to Vss.
SOC_INT	A2	O	SOC state interrupts output. Generates a pulse under the conditions specified by (1). Open drain output.
BAT_GD	B2	O	Battery Good push-pull indicator output. Active-low and output disabled by default. Polarity is configured via ***Op Config [BATG_POL]*** and the output is enabled via ***OpConfig C [BATGSPUEN]***.
CE	D2	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low. **Note:** CE has an internal ESD protection diode connected to REGIN. Recommend maintaining $V_{CE} \le V_{REGIN}$ under all conditions.
BAT	E2	I	Cell-voltage measurement input. ADC input. Recommend 4.8V maximum for conversion accuracy.
SCL	A3	I	Slave I^2C serial communications clock input line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical).
SDA	B3	I/O	Slave I^2C serial communications data line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical).
BAT_LOW	C3	O	Battery Low push-pull output indicator. Active high and output enabled by default. Polarity is configured via ***Op Config [BATL_POL]*** and the output is enabled via ***OpConfig C [BATLSPUEN]***.
TS	D3	IA	Pack thermistor voltage sense (use 103AT-type thermistor). ADC input.
BI/TOUT	E3	I/O	Battery-insertion detection input. Power pin for pack thermistor network. Thermistor-multiplexer control pin. Use with pull-up resistor >1MΩ (1.8 MΩ typical).

(1) I/O = Digital input/output, IA = Analog input, P = Power connection

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		VALUE	UNIT
V_{REGIN}	Regulator input range	–0.3 to 5.5	V
		–0.3 to 6.0 (2)	V
V_{CE}	CE input pin	–0.3 to V_{REGIN} + 0.3	V
V_{CC}	Supply voltage range	–0.3 to 2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, SOC_INT)	–0.3 to 5.5	V
V_{BAT}	BAT input pin	–0.3 to 5.5	V
		–0.3 to 6.0 (2)	V
V_I	Input voltage range to all other pins (BI/TOUT , TS , SRP, SRN, BAT_GD)	–0.3 to V_{CC} + 0.3	V
ESD	Human-body model (HBM), BAT pin	1.5	kV
	Human-body model (HBM), all other pins	2	
T_A	Operating free-air temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Condition not to exceed 100 hours at 25 °C lifetime.

RECOMMENDED OPERATING CONDITIONS

T_A = -40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGIN}	Supply voltage	No operating restrictions	2.8		4.5	V
		No FLASH writes	2.45		2.8	
C_{REGIN}	External input capacitor for internal LDO between REGIN and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between V_{CC} and V_{SS}		0.47	1		µF
t_{PUCD}	Power-up communication delay			250		ms

SUPPLY CURRENT

T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} (1)	Normal operating-mode current	Fuel gauge in NORMAL mode. I_{LOAD} > ***Sleep Current***		118		µA
I_{SLP+} (1)	Sleep+ operating mode current	Fuel gauge in SLEEP+ mode. I_{LOAD} < ***Sleep Current***		62		µA
I_{SLP} (1)	Low-power storage-mode current	Fuel gauge in SLEEP mode. I_{LOAD} < ***Sleep Current***		23		µA
I_{HIB} (1)	Hibernate operating-mode current	Fuel gauge in HIBERNATE mode. I_{LOAD} < ***Hibernate Current***		8		µA

(1) Specified by design. Not production tested.

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DIGITAL INPUT AND OUTPUT DC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 25°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage, low (SCL, SDA, SOC_INT , BAT_LOW , BAT_GD)	I_{OL} = 3 mA			0.4	V
$V_{OH(PP)}$	Output voltage, high (BAT_LOW , BAT_GD)	I_{OH} = –1 mA	V_{CC} – 0.5			V
$V_{OH(OD)}$	Output voltage, high (SDA, SCL, SOC_INT)	External pullup resistor connected to V_{CC}	V_{CC} – 0.5			
V_{IL}	Input voltage, low (SDA, SCL)		–0.3		0.6	V
	Input voltage, low (BI/TOUT)	BAT INSERT CHECK MODE active	–0.3		0.6	
V_{IH}	Input voltage, high (SDA, SCL)		1.2			V
	Input voltage, high (BI/TOUT)	BAT INSERT CHECK MODE active	1.2		V_{CC} + 0.3	
$V_{IL(CE)}$	Input voltage, low (CE)	V_{REGIN} = 2.8 to 4.5V			0.8	V
$V_{IH(CE)}$	Input voltage, high (CE)		2.65			
I_{lkg} (1)	Input leakage current (I/O pins)				0.3	µA

(1) Specified by design. Not production tested.

POWER-ON RESET

T_A = –40°C to 85°C, typical values at T_A = 25°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at V_{CC}		2.05	2.15	2.20	V
V_{HYS}	Power-on reset hysteresis		45	115	185	mV

2.5V LDO REGULATOR

T_A = –40°C to 85°C, C_{LDO25} = 1µF, V_{REGIN} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{REG25}	Regulator output voltage (V_{CC})	2.8V ≤ V_{REGIN} ≤ 4.5V, I_{OUT} ≤ 16mA	2.3	2.5	2.6	V
		2.45V ≤ V_{REGIN} < 2.8V (low battery), I_{OUT} ≤ 3mA	2.3			V

INTERNAL CLOCK OSCILLATORS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	High Frequency Oscillator			2.097		MHz
f_{LOSC}	Low Frequency Oscillator			32.768		kHz

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ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{A1}	Input voltage range (TS)		V_{SS} – 0.125		2	V
V_{A2}	Input voltage range (BAT)		V_{SS} – 0.125		5	V
$V_{IN(ADC)}$	Input voltage range		0.05		1	V
G_{TEMP}	Internal temperature sensor voltage gain			–2		mV/°C
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
Z_{ADC1} (1)	Effective input resistance (TS)		8			MΩ
Z_{ADC2} (1)	Effective input resistance (BAT)	bq27520-G4 not measuring cell voltage	8			MΩ
		bq27520-G4 measuring cell voltage		100		kΩ
$I_{lkg(ADC)}$ (1)	Input leakage current				0.3	µA

(1) Specified by design. Not tested in production.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$	V_{SR} = $V_{(SRN)}$ – $V_{(SRP)}$	–0.125		0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
INL	Integral nonlinearity error			±0.007	±0.034	% FSR
$Z_{IN(SR)}$ (1)	Effective input resistance		2.5			MΩ
$I_{lkg(SR)}$ (1)	Input leakage current				0.3	µA

(1) Specified by design. Not tested in production.

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DATA FLASH MEMORY CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR} (1)	Data retention		10			Years
	Flash-programming write cycles (1)		20,000			Cycles
$t_{WORDPROG}$ (1)	Word programming time				2	ms
I_{CCPROG} (1)	Flash-write supply current			5	10	mA
$t_{DFERASE}$ (1)	Data flash master erase time		200			ms
$t_{IFERASE}$ (1)	Instruction flash master erase time		200			ms
$t_{PGERASE}$ (1)	Flash page erase time		20			ms

(1) Specified by design. Not production tested

I²C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse duration (high)		600			ns
$t_{w(L)}$	SCL pulse duration (low)		1.3			µs
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
$t_{(BUF)}$	Bus free time between stop and start		66			µs
f_{SCL}	Clock frequency (1)				400	kHz

(1) If the clock frequency (f_{SCL}) is > 100 kHz, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to I²C INTERFACE and I²C Command Waiting Time)

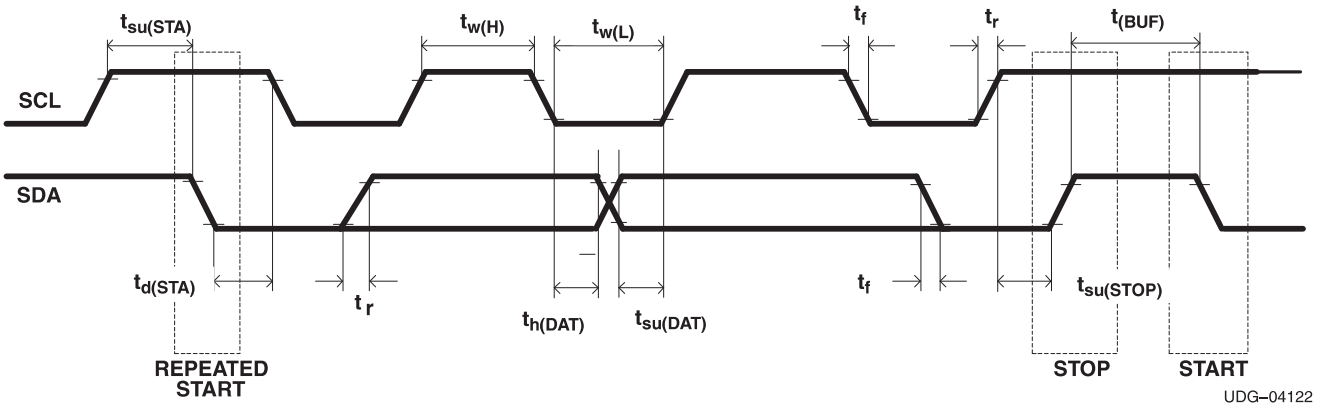

Figure 1. I²C-Compatible Interface Timing Diagrams

GENERAL DESCRIPTION

The bq27520-G4 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as time-to-empty (TTE) and state-of-charge (SOC) as well as SOC interrupt signal to the host.

Information is accessed through a series of commands, called *Standard Commands*. Further capabilities are provided by the additional *Extended Commands* set. Both sets of commands, indicated by the general format *Command( )*, are used to read and write information contained within the device control and status registers, as well as its data flash locations. Commands are sent from system to gauge using the bq27520-G4 's I^2C serial communications engine, and can be executed during application development, system manufacture, or end-equipment operation.

Cell information is stored in the device in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the bq27520-G4 's companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The key to the bq27520-G4 's high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

The device measures charge/discharge activity by monitoring the voltage across a small-value series sense resistor (5 mΩ to 20 mΩ typ.) located between the system's Vss and the battery's PACK- terminal. When a cell is attached to the device, cell impedance is learned, based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The device external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with R25 = 10.0kΩ ±1%. B25/85 = 3435K ± 1% (such as Semitec NTC 103AT). Alternatively, the bq27520-G4 can also be configured to use its internal temperature sensor or receive temperature data from the host processor. When an external thermistor is used, a 18.2k pull up resistor between BI/TOUT and TS pins is also required. The bq27520-G4 uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

To minimize power consumption, the device has different power modes: NORMAL, SLEEP+, SLEEP, HIBERNATE, and BAT INSERT CHECK. The bq27520-G4 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly.

For complete operational details, refer to *bq27520-G4 Technical Reference Manual*.

NOTE

FORMATTING CONVENTIONS IN THIS DOCUMENT:

Commands: *italics* with *parentheses* and no breaking spaces, e.g. *RemainingCapacity( ).*

NVM Data: *italics*, **bold**, and *breaking spaces*, e.g. **Design Capacity**.

Register bits and flags: brackets and *italics*, *e.g. [TDA]*

NVM Data bits: brackets, *italics* and **bold**, *e.g:* ***[LED1]***

Modes and states: ALL CAPITALS, e.g. UNSEALED mode.

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DATA COMMANDS

STANDARD DATA COMMANDS

Thebq27520-G4 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in Table 2. Because each command consists of two bytes of data, two consecutive I^2C transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional details are found in the *bq27520-G4 Technical Reference Manual*.

Table 2. Standard Commands

NAME		COMMAND CODE	UNITS	SEALED ACCESS
Control( )	CNTL	0x00 / 0x01	N/A	R/W
AtRate( )		0x02 / 0x03	mA	R/W
AtRateTimeToEmpty( )		0x04 / 0x05	Minutes	R
Temperature( )	TEMP	0x06 / 0x07	0.1 K	R/W
Voltage( )	VOLT	0x08 / 0x09	mV	R
Flags( )	FLAGS	0x0a / 0x0b	N/A	R
NominalAvailableCapacity( )	NAC	0x0c / 0x0d	mAh	R
FullAvailableCapacity( )	FAC	0x0e / 0x0f	mAh	R
RemainingCapacity( )	RM	0x10 / 0x11	mAh	R
FullChargeCapacity( )	FCC	0x12 / 0x13	mAh	R
AverageCurrent( )		0x14 / 0x15	mA	R
TimeToEmpty( )	TTE	0x16 / 0x17	Minutes	R
StandbyCurrent( )		0x18 / 0x19	mA	R
StandbyTimeToEmpty( )		0x1a / 0x1b	Minutes	R
StateOfHealth( )	SOH	0x1c / 0x1d	% / num	R
CycleCount( )		0x1e / 0x1f	num	R
StateOfCharge( )	SOC	0x20 / 0x21	%	R
InstantaneousCurrent( )		0x22 / 0x23	mA	R
InternalTemperature( )		0x28 / 0x29	0.1 K	R
ResistanceScale( )		0x2a / 0x2b		R
OperationConfiguration( )	Op Config	0x2c / 0x2d	N/A	R
DesignCapacity( )		0x2e / 0x2f	mAh	R

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Control( ): 0x00/0x01

Issuing a *Control( )* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control( )* command allows the system to control specific features of the bq27520-G4 during normal operation and additional features when the device is in different access modes, as described in Table 3. Additional details are found in the *bq27520-G4 Technical Reference Manual*.

Table 3. *Control( )* Subcommands

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of DF checksum, hibernate, IT, etc.
DEVICE_TYPE	0x0001	Yes	Reports the device type (eg: 0x0520)
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type
PREV_MACWRITE	0x0007	Yes	Returns previous *Control( )* subcommand code
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration
OCV_CMD	0x000c	Yes	Request the gauge to take a OCV measurement
BAT_INSERT	0x000d	Yes	Forces *Flags( ) [BAT_DET]* bit set when ***OpConfig B [BIE]*** = 0
BAT_REMOVE	0x000e	Yes	Forces *Flags( ) [BAT_DET]* bit clear when ***OpConfig B [BIE]*** = 0
SET_HIBERNATE	0x0011	Yes	Forces *CONTROL_STATUS [HIBERNATE]* to 1
CLEAR_HIBERNATE	0x0012	Yes	Forces *CONTROL_STATUS [HIBERNATE]* to 0
SET_SLEEP+	0x0013	Yes	Forces *CONTROL_STATUS [SNOOZE]* to 1
CLEAR_SLEEP+	0x0014	Yes	Forces *CONTROL_STATUS [SNOOZE]* to 0
DF_VERSION	0x001F	Yes	Returns the ***Data Flash Version*** code
SEALED	0x0020	No	Places the bq27520-G4 in SEALED access mode
IT_ENABLE	0x0021	No	Enables the Impedance Track™ (IT) algorithm
RESET	0x0041	No	Forces a full reset of the bq27520-G4

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FUNCTIONAL DESCRIPTION

The bq27520-G4 measures the voltage, temperature, and current to determine battery capacity and state of charge (SOC) based on the patented Impedance Track™ algorithm (Refer to Application Report SLUA450, *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* for more information). The bq27520-G4 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the battery. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

Battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When a system load is applied, the impedance of the battery is measured by comparing the open circuit voltage (OCV) obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. It is also used for the value in ***Design Capacity***. The bq27520-G4 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity( )* and *StateOfCharge( )*, specifically for the present load and temperature. *FullChargeCapacity( )* is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage( )* reaches the ***Terminate Voltage***. *NominalAvailableCapacity( )* and *FullAvailableCapacity( )* are the uncompensated (no or light load) versions of *RemainingCapacity( )* and *FullChargeCapacity( )* respectively.

The bq27520-G4 has two *Flags( )* bits and two pins to warn the host if the battery's SOC has fallen to critical levels. If *RemainingCapacity( )* falls below the first capacity threshold specified by ***SOC1 Set Threshold***, the *Flags ( ) [SOC1]* bit is set and is cleared if *RemainingCapacity( )* rises above the ***SOC1 Clear Threshold***. If enabled via ***OpConfig C [BATLSPUEN]***, the BAT_LOW pin reflects the status of the *[SOC1]* flag bit. Also, if enabled by ***OpConfig B [BL_INT]***, the SOC_INT will toggle upon a state change of the *[SOC1]* flag bit.

As *Voltage( )* falls below the ***SysDown Set Volt Threshold***, the *Flags( ) [SYSDOWN]* bit is set and SOC_INT will toggle once to provide a final warning to shut down the system. As *Voltage( )* rises above ***SysDown Clear Voltage*** the *[SYSDOWN]* bit is cleared and SOC_INT will toggle once to signal the status change.

Additional details are found in the *bq27520-G4 Technical Reference Manual*.

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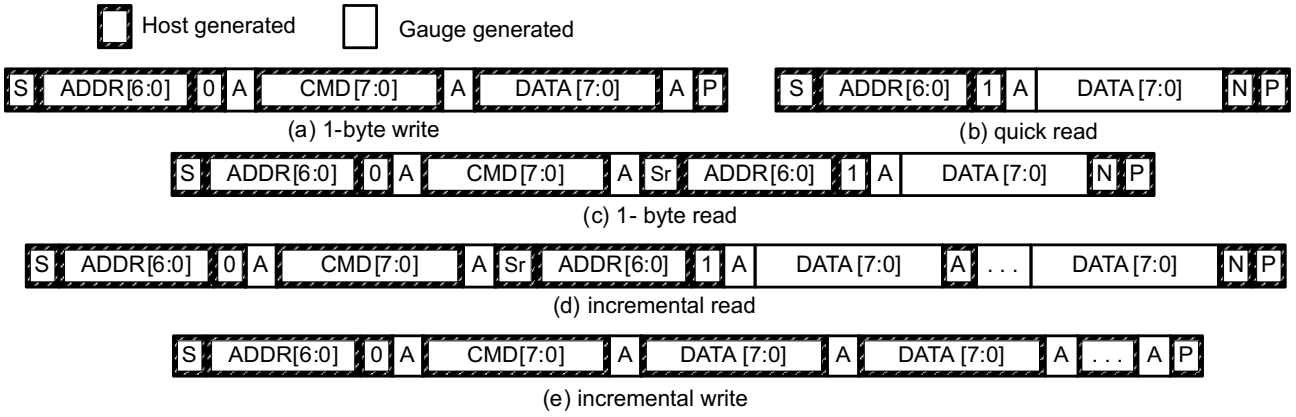
COMMUNICATIONS

I²C INTERFACE

The bq27520-G4 supports the standard I²C read, incremental read, quick read, one byte write, and incremental write functions. The 7 bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The first 8-bits of the I²C protocol will; therefore, be 0xAA or 0xAB for write or read, respectively.

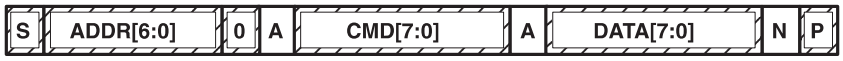


(S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The "quick read" returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, will increment whenever data is acknowledged by the bq27520-G4 or the I²C master. "Quick writes" function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data)

The following command sequences are not supported:

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x6B (NACK command):

I²C Time Out

The I²C engine will release both SDA and SCL if the I²C bus is held low for 2 seconds. If the bq27520-G4 was holding the lines, releasing them will free them for the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine will enter the low power sleep mode.

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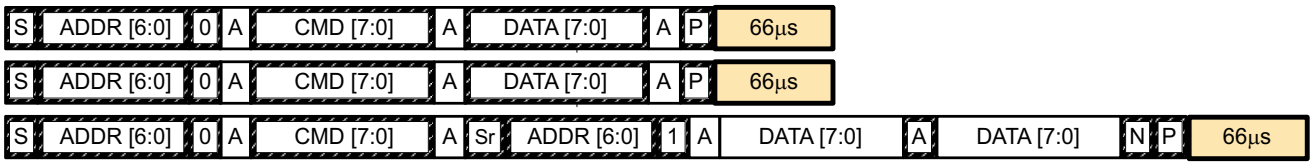
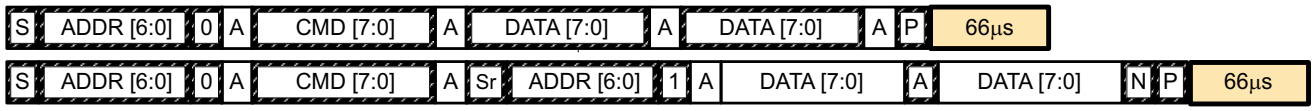
I²C Command Waiting Time

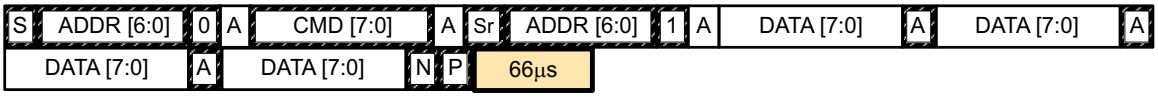
To ensure proper operation at 400 kHz, a $t_{(BUF)}$ ≥ 66 µs bus free waiting time should be inserted between all packets addressed to the bq27520-G4 . In addition, if the SCL clock frequency (f_{SCL}) is > 100 kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows the standard waiting time required between issuing the control subcommand the reading the status result. An OCV_CMD subcommand requires 1.2 seconds prior to reading the result. For read-write standard command, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host should not issue all standard commands more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time inserted between two 1-byte write packets for a subcommand and reading results
(required for 100 kHz < f_{SCL} ≤ 400 kHz)



Waiting time inserted between incremental 2-byte write packet for a subcommand and reading results
(acceptable for f_{SCL} ≤ 100 kHz)



Waiting time inserted after incremental read

I²C Clock Stretching

A clock stretch can occur during all modes of fuel gauge operation. In SLEEP and HIBERNATE modes, a short clock stretch will occur on all I²C traffic as the device must wake-up to process the packet. In the other modes (BAT INSERT CHECK , NORMAL, SLEEP+) clock stretching will only occur for packets addressed for the fuel gauge. The majority of clock stretch periods are small as the I²C interface performs normal data flow control. However, less frequent yet more significant clock stretch periods may occur as blocks of Data Flash are updated. The following table summarizes the approximate clock stretch duration for various fuel gauge operating conditions.

Gauging Mode	Operating Condition / Comment	Approximate Duration
SLEEP HIBERNATE	Clock stretch occurs at the beginning of all traffic as the device wakes up.	≤ 4 ms
BAT INSERT CHECK NORMAL SLEEP+	Clock stretch occurs within the packet for flow control. (after a start bit, ACK or first data bit)	≤ 4 ms
	Normal Ra table Data Flash updates.	24 ms
	Data Flash block writes.	72 ms
	Restored Data Flash block write after loss of power.	116 ms
	End of discharge Ra table Data Flash update.	144 ms

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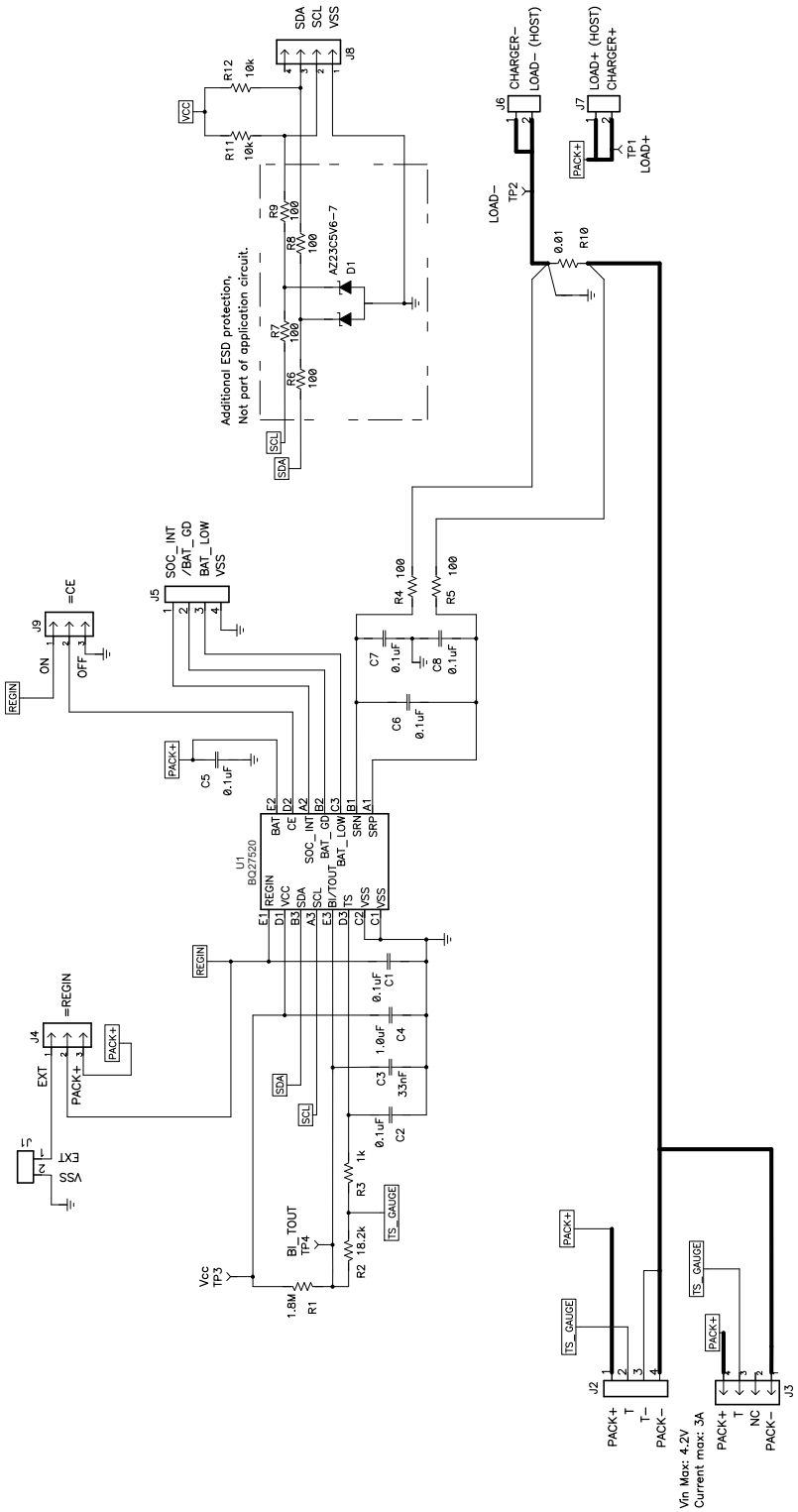
REFERENCE SCHEMATICS

SCHEMATIC



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27520YZFR-G4	ACTIVE	DSBGA	YZF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27520	Samples
BQ27520YZFT-G4	ACTIVE	DSBGA	YZF	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27520	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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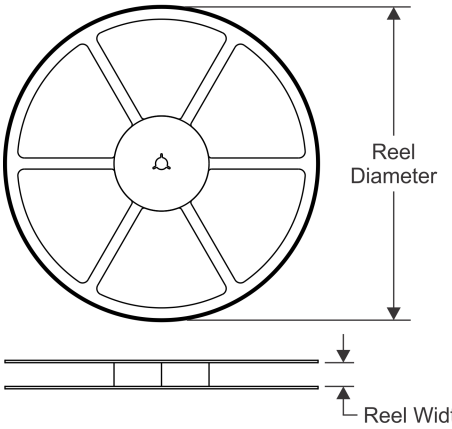
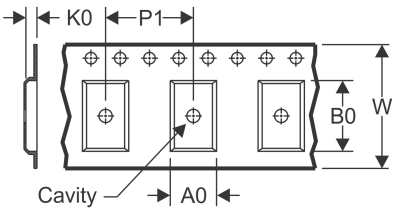
TAPE AND REEL INFORMATION

REEL DIMENSIONS

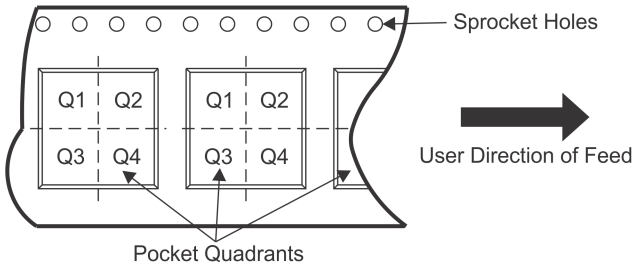


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

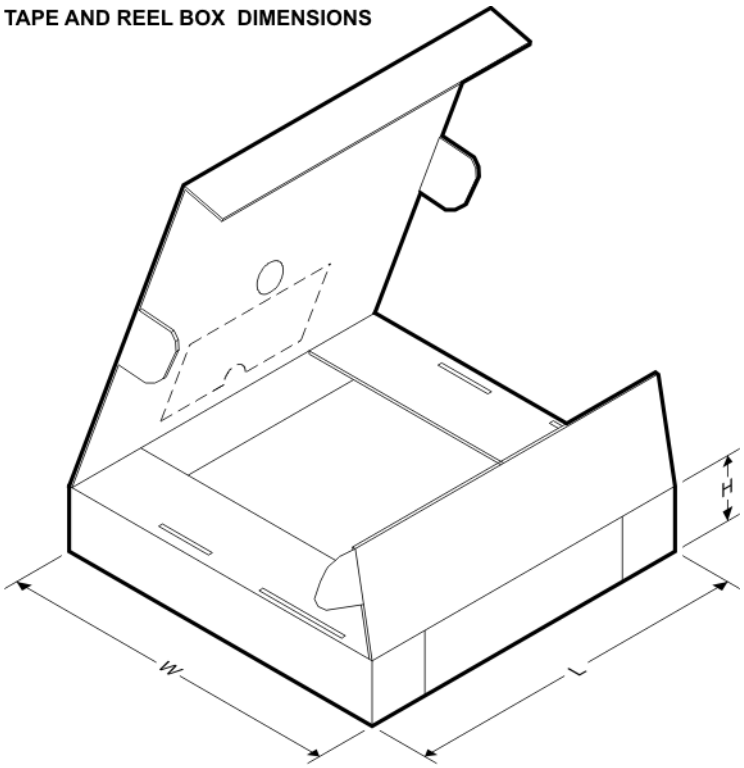
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27520YZFR-G4	DSBGA	YZF	15	3000	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1
BQ27520YZFT-G4	DSBGA	YZF	15	250	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1

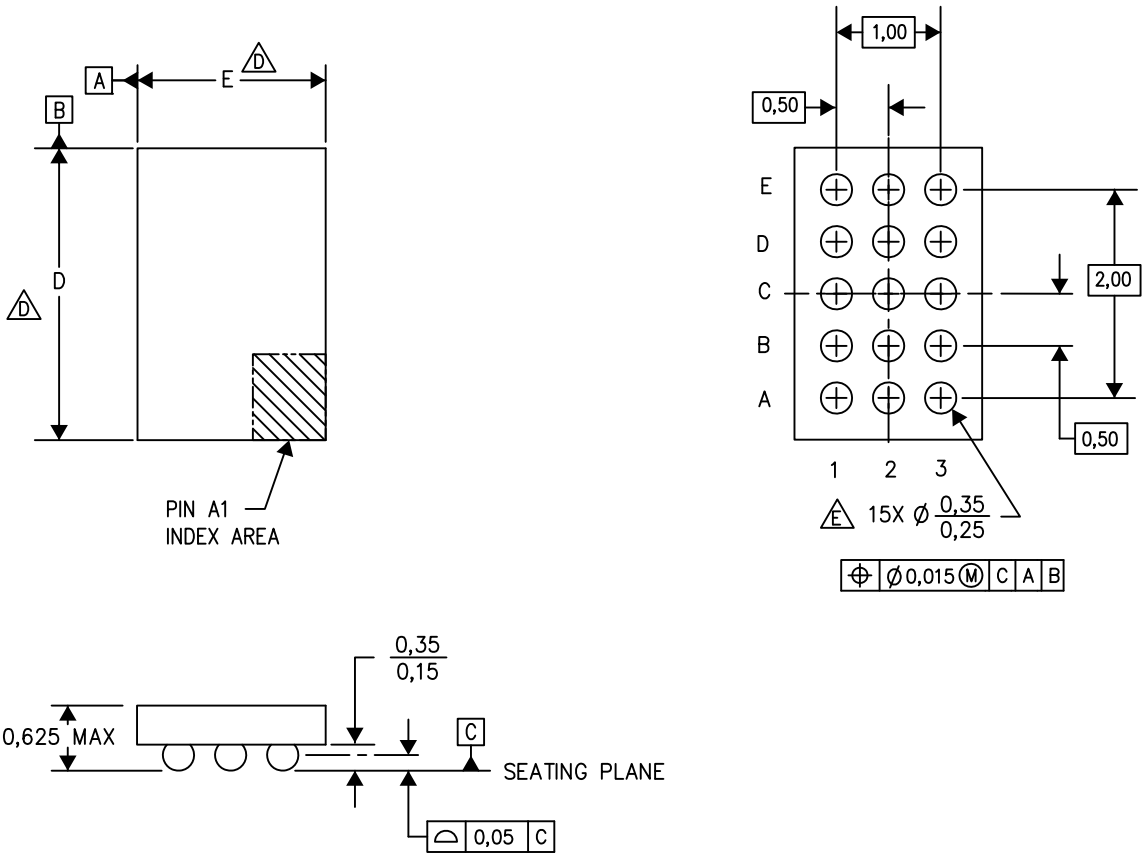
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27520YZFR-G4	DSBGA	YZF	15	3000	210.0	185.0	35.0
BQ27520YZFT-G4	DSBGA	YZF	15	250	210.0	185.0	35.0

YZF (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



D: Max = 2.64 mm, Min = 2.58 mm

E: Max = 1.986 mm, Min =1.926 mm

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
3 x 5 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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