

## Quad channel high side solid state relay

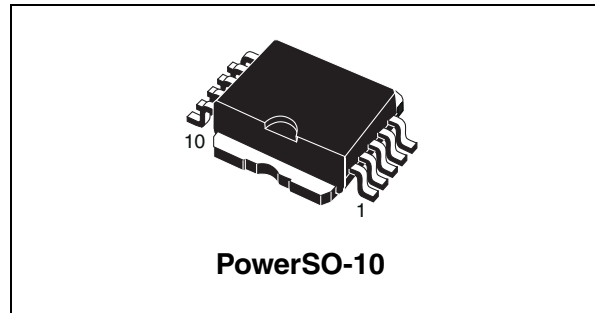
### Features

Type	R <sub>DS(on)</sub>	I <sub>OUT</sub>	V <sub>CC</sub>
VNQ660SP	50mΩ <sup>(1)</sup>	6A	36V

1. Per each channel.

- CMOS compatible inputs
- Off state open load detection
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against loss of ground and loss of V<sub>CC</sub>
- Reverse battery protection<sup>(a)</sup>

a. See [Application schematic on page 16](#)



### Description

The VNQ660SP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground.

This device has four independent channels. Built-in thermal shutdown and output current limitation protect the chip from over temperature and short circuit.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VNQ660SP	VNQ660SP13TR

# Contents

<b>1</b>	<b>Block diagram and pin description</b> .....	<b>5</b>
<b>2</b>	<b>Electrical specifications</b> .....	<b>6</b>
2.1	Absolute maximum ratings .....	6
2.2	Thermal data .....	6
2.3	Electrical characteristics .....	7
2.4	Electrical characteristics curves .....	13
<b>3</b>	<b>Application information</b> .....	<b>16</b>
3.1	GND protection network against reverse battery .....	16
3.1.1	Solution 1: a resistor in the ground line (RGND only) .....	16
3.1.2	Solution 2: a diode (D <sub>GND</sub> ) in the ground line .....	17
3.2	Load dump protection .....	17
3.3	MCU I/O protection .....	17
3.4	Maximum demagnetization energy (V <sub>CC</sub> = 13.5V) .....	18
<b>4</b>	<b>Package and PCB thermal data</b> .....	<b>19</b>
4.1	PowerSO-10 thermal data .....	19
<b>5</b>	<b>Package and packing information</b> .....	<b>22</b>
5.1	ECOPACK® packages .....	22
5.2	PowerSO-10 mechanical data .....	22
5.3	PowerSO-10 packing information .....	24
<b>6</b>	<b>Revision history</b> .....	<b>25</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Suggested connections for unused and not connected pins . . . . .	5
Table 3.	Absolute maximum ratings . . . . .	6
Table 4.	Thermal data (per island) . . . . .	6
Table 5.	Power . . . . .	7
Table 6.	Protections . . . . .	8
Table 7.	V <sub>CC</sub> - output diode . . . . .	8
Table 8.	Switching (V <sub>CC</sub> = 13V; T <sub>j</sub> = 25°C) . . . . .	9
Table 9.	Logic inputs. . . . .	9
Table 10.	Openload detection. . . . .	9
Table 11.	Truth table. . . . .	10
Table 12.	Electrical transient requirements . . . . .	11
Table 13.	Thermal parameters . . . . .	21
Table 14.	PowerSO-10 mechanical data . . . . .	23
Table 15.	Document revision history . . . . .	25

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Configuration diagram (top view) . . . . .	5
Figure 3.	Current and voltage conventions . . . . .	7
Figure 4.	Status timings . . . . .	9
Figure 5.	Switching characteristics . . . . .	10
Figure 6.	Waveforms . . . . .	12
Figure 7.	Off state output current . . . . .	13
Figure 8.	High level input current . . . . .	13
Figure 9.	Input clamp voltage . . . . .	13
Figure 10.	Turn-on voltage slope . . . . .	13
Figure 11.	Overshoot shutdown . . . . .	13
Figure 12.	Turn-off voltage slope . . . . .	13
Figure 13.	ILIM vs Tcase . . . . .	14
Figure 14.	On state resistance vs $V_{CC}$ . . . . .	14
Figure 15.	Input high level . . . . .	14
Figure 16.	Input hysteresis voltage . . . . .	14
Figure 17.	On state resistance vs Tcase . . . . .	14
Figure 18.	Input low level . . . . .	14
Figure 19.	Status leakage current . . . . .	15
Figure 20.	Status low output voltage . . . . .	15
Figure 21.	Status clamp voltage . . . . .	15
Figure 22.	Openload Off state detection threshold . . . . .	15
Figure 23.	Application schematic . . . . .	16
Figure 24.	Maximum turn-off current versus load inductance . . . . .	18
Figure 25.	PowerSO-10 PC board . . . . .	19
Figure 26.	Rthj-amb Vs PCB copper area in open box free air condition . . . . .	19
Figure 27.	Thermal impedance junction ambient single pulse . . . . .	20
Figure 28.	Thermal fitting model of a quad channel HSD in PowerSO-10 . . . . .	20
Figure 29.	PowerSO-10 package dimensions . . . . .	22
Figure 30.	PowerSO-10 suggested pad layout . . . . .	24
Figure 31.	PowerSO-10 tube shipment (no suffix) . . . . .	24
Figure 32.	SO-28 tape and reel shipment (suffix "TR") . . . . .	24

# 1 Block diagram and pin description

Figure 1. Block diagram

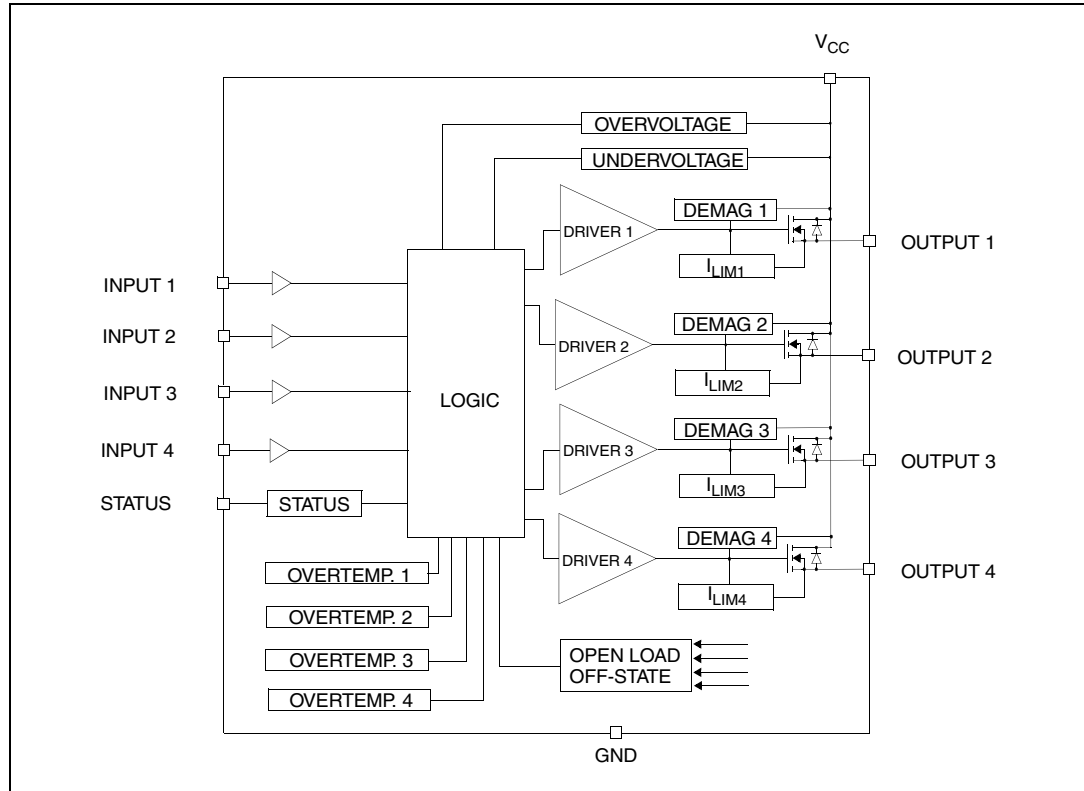


Figure 2. Configuration diagram (top view)

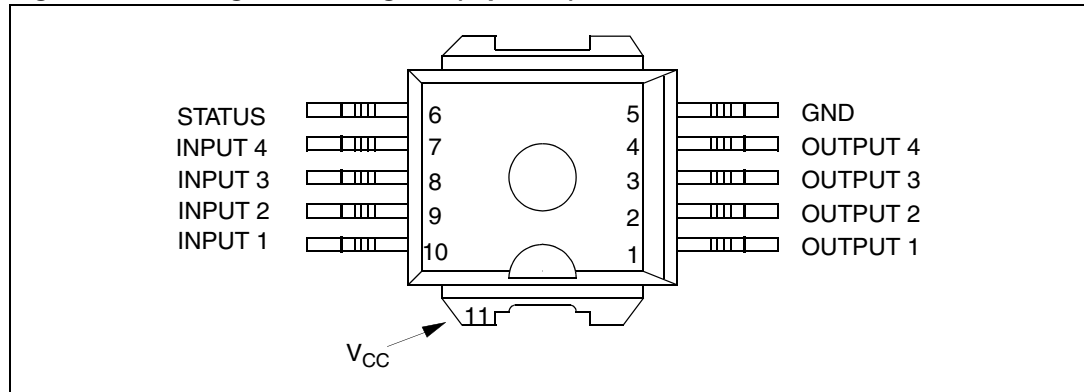


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$I_{OUT}$	DC output current, per each channel	Internally limited	A
$I_R$	Reverse DC output current, per each channel	- 15	A
$I_{IN}$	Input current	+/- 10	mA
$I_{STAT}$	Status current	+/- 10	mA
$I_{GND}$	DC ground current at $T_C \leq 25^\circ\text{C}$	-200	mA
$V_{ESD}$	Electrostatic discharge (human body model: $R=1.5\text{K}\Omega$ , $C = 100\text{pF}$ )		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- $V_{CC}$	5000	V
$E_{MAX}$	Maximum switching energy ( $L = 0.38\text{mH}$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5\text{V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_L = 14\text{A}$ )	101	mJ
$P_{tot}$	Power dissipation at $T_C = 25^\circ\text{C}$	114	W
$T_j$	Junction operating temperature	- 40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	- 65 to 150	$^\circ\text{C}$
$E_C$	Non repetitive clamping energy at $T_C = 25^\circ\text{C}$	150	mJ

### 2.2 Thermal data

**Table 4. Thermal data (per island)**

Symbol	Parameter	Value		Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1 <sup>(1)</sup>	52 <sup>(2)</sup>	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON)	51.1 <sup>(1)</sup>	33 <sup>(2)</sup>	$^\circ\text{C}/\text{W}$

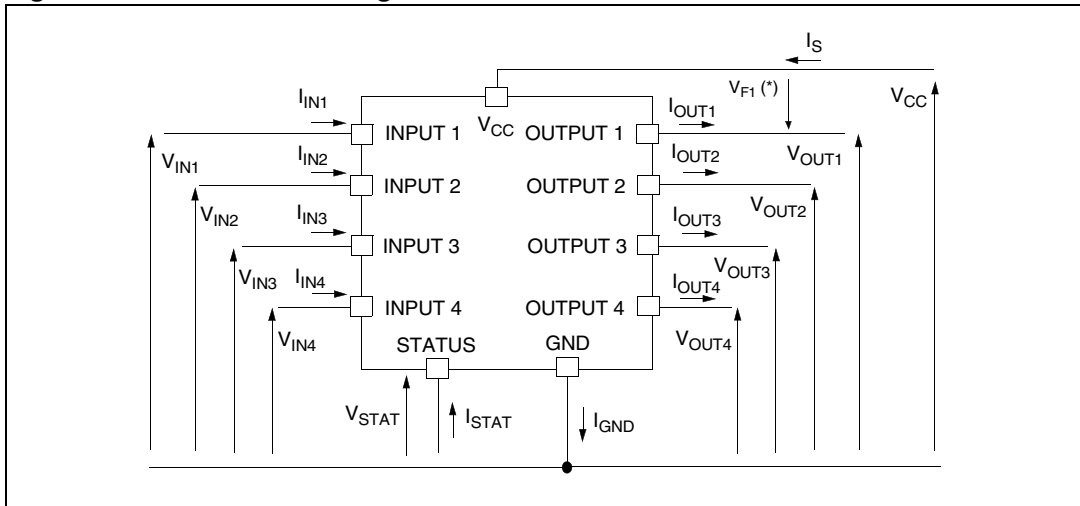
1. When mounted on a standard single-sided FR-4 board with  $1\text{cm}^2$  of Cu (at least  $35\ \mu\text{m}$  thick).

2. When mounted on a standard single-sided FR-4 board with  $6\text{cm}^2$  of Cu (at least  $35\ \mu\text{m}$  thick).

### 2.3 Electrical characteristics

Values specified in this section are for  $6V < V_{CC} < 24V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise stated.

**Figure 3. Current and voltage conventions**



Note:  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.

**Table 5. Power**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}^{(1)}$	Operating supply voltage		6	13	36	V
$V_{USD}^{(1)}$	Undervoltage shutdown		3.5	4.6	6	V
$V_{UVhyst}^{(1)}$	Undervoltage hysteresis		0.2		1	V
$V_{OV}^{(1)}$	Overvoltage shutdown		36			V
$V_{OVhyst}^{(1)}$	Overvoltage hysteresis		0.25			V
$R_{ON}$	On state resistance	$I_{OUT} = 1A; T_j = 25^{\circ}C$ $9V < V_{CC} < 18V$ $I_{OUT} = 1A; T_j = 150^{\circ}C$ $9V < V_{CC} < 18V$ $I_{OUT} = 1A; V_{CC} = 6V$		40 85	50 100 130	mΩ
$I_S^{(1)}$	Supply current	Off State; $V_{CC} = 13.5V$ ; $V_{IN} = V_{OUT} = 0V$  Off State; $V_{CC} = 13.5V$ ; $V_{IN} = V_{OUT} = 0V$ ; $T_j = 25^{\circ}C$  On State; $V_{CC} = 13V; V_{IN} = 3.25V$ ; $9V < V_{CC} < 18V$		12 12 6	40 25 12	μA μA mA

**Table 5. Power (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off1)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$	0		50	$\mu A$
$I_{L(off2)}$	Off state output current	$V_{IN} = 0V; V_{OUT} = 3.5V$	-75		0	$\mu A$
$I_{L(off3)}$	Off state output current	$V_{IN} = V_{OUT} = 0V; V_{CC} = 13V;$ $T_j = 125^\circ C$			5	$\mu A$
$I_{L(off4)}$	Off state output current	$V_{IN} = V_{OUT} = 0V; V_{CC} = 13V;$ $T_j = 25^\circ C$			3	$\mu A$

1. Per device.

**Table 6. Protections**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	170	200	$^\circ C$
$T_R$	Reset temperature		135			$^\circ C$
$T_{hyst}$	Thermal hysteresis		7	15	25	$^\circ C$
$I_{lim}$	DC short circuit current	$9V < V_{CC} < 36V$ $6V < V_{CC} < 36V$	6	10	18 18	A A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2A;$ $V_{IN} = 0V;$ $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			25	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 - 0.7	8	V V

*Note:* To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 7.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$- I_{OUT} = 1.6A; T_j = 150^\circ C$			0.6	V



**Table 8. Switching ( $V_{CC} = 13V$ ;  $T_j = 25^\circ C$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 13\Omega$ channels 1,2,3,4 (see <a href="#">Figure 5</a> )		40	70	$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 13\Omega$ channels 1,2,3,4 (see <a href="#">Figure 5</a> )		40	140	$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 13\Omega$ channels 1,2,3,4 (see <a href="#">Figure 5</a> )		See <a href="#">Figure 10</a>		$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 13\Omega$ channels 1,2,3,4 (see <a href="#">Figure 5</a> )		See <a href="#">Figure 12</a>		$V/\mu s$

**Table 9. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				1.25	V
$I_{IL}$	Input low level current	$V_{IN} = 1.25V$	1			$\mu A$
$V_{IH}$	Input high level voltage		3.25			V
$I_{IH}$	Input high level current	$V_{IN} = 3.25V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$C_{IN}$	Input capacitance				40	pF
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

**Table 10. Openload detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{SDL}$	Status delay	See <a href="#">Figure 4</a>			20	$\mu s$
$V_{OL}$	Openload voltage detection threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$t_{DOL}$	Openload detection delay at turn-off	$V_{CC} = 18V$ (see <a href="#">Figure 4</a> )			300	$\mu s$

**Figure 4. Status timings**

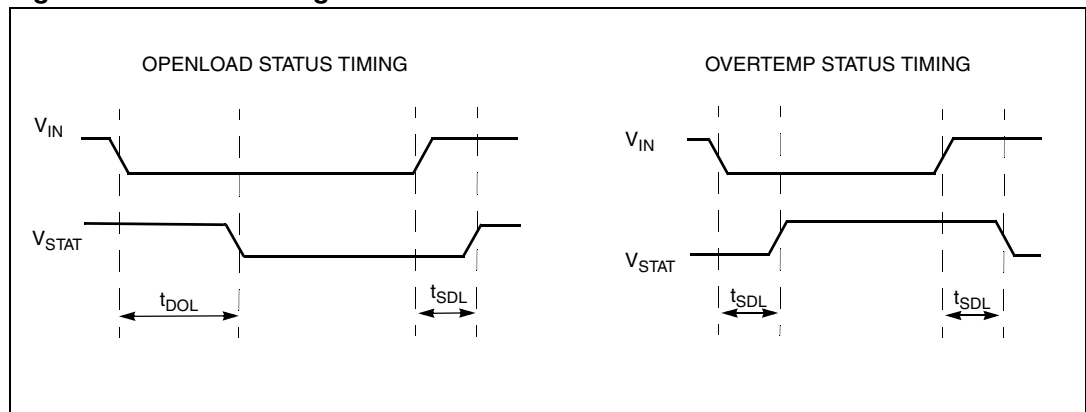


Figure 5. Switching characteristics

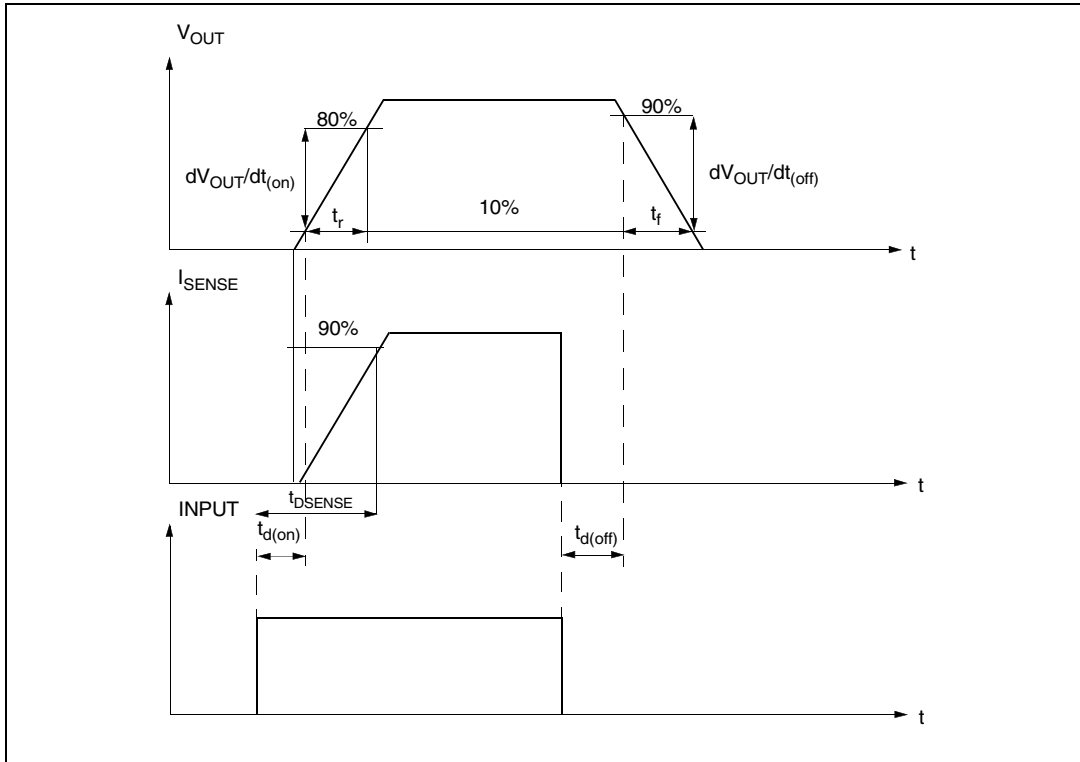


Table 11. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_J < T_{TSD})$ H $(T_J > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

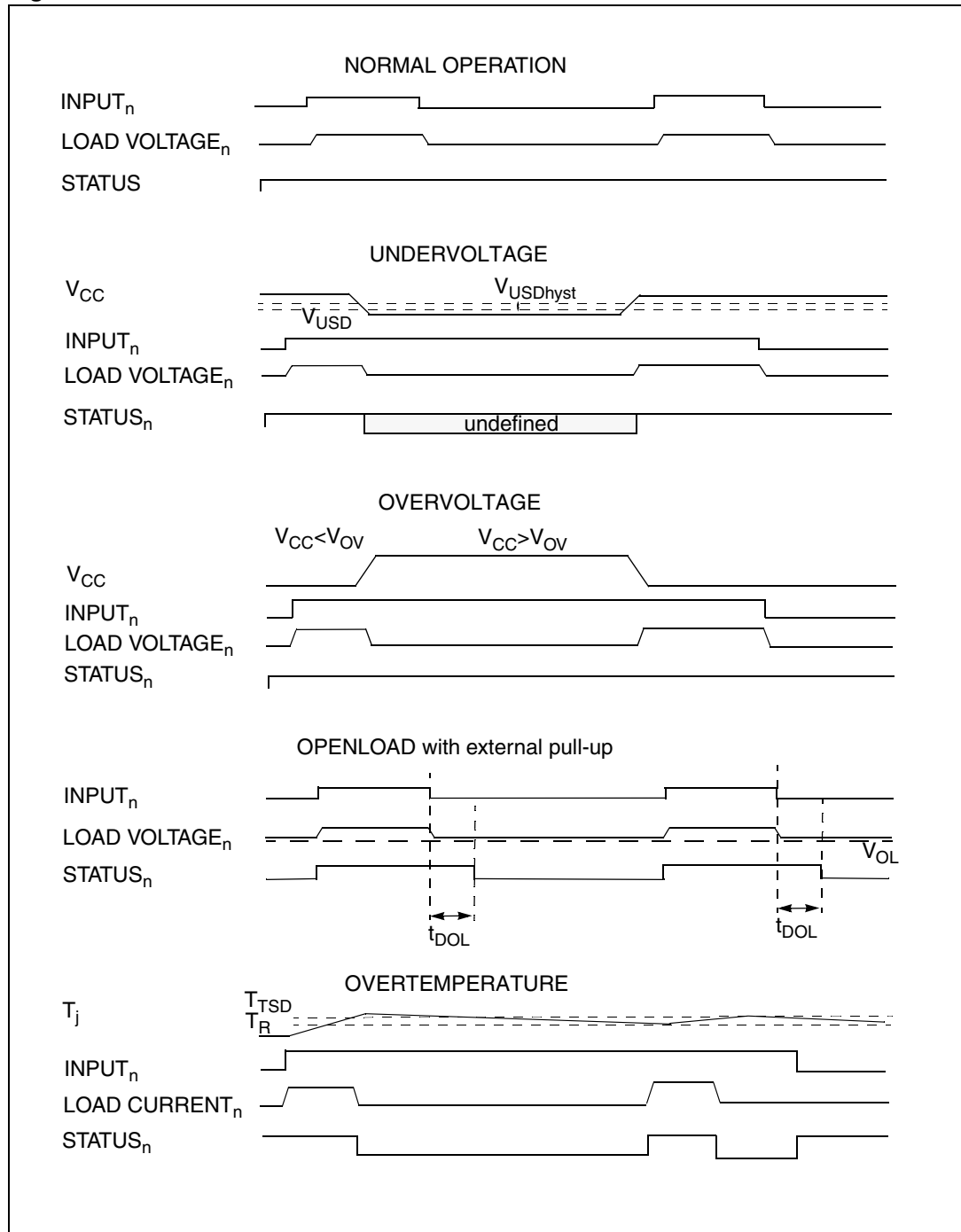
Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1μs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1μs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

ISO T/R 7637/1 Test pulse	Test level			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



## 2.4 Electrical characteristics curves

Figure 7. Off state output current

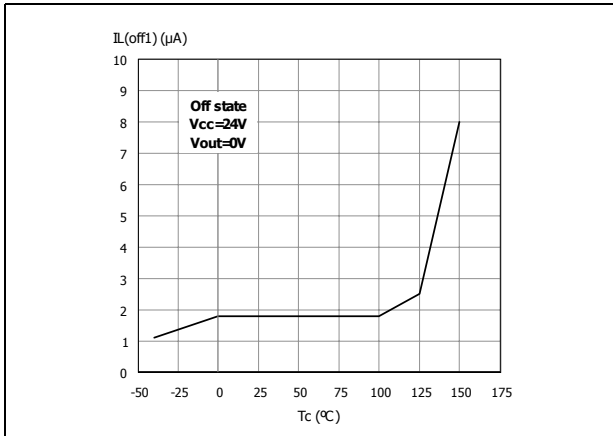


Figure 8. High level input current

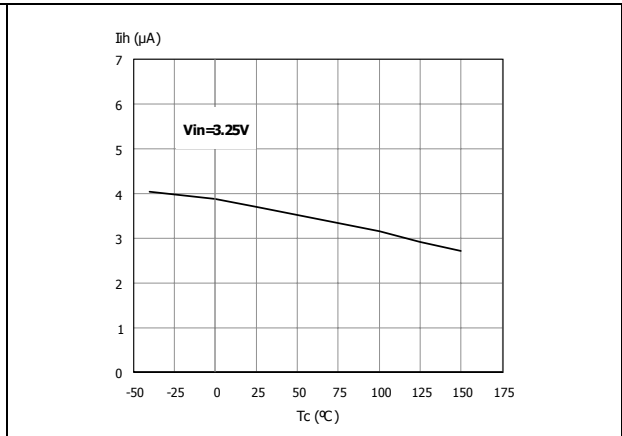


Figure 9. Input clamp voltage

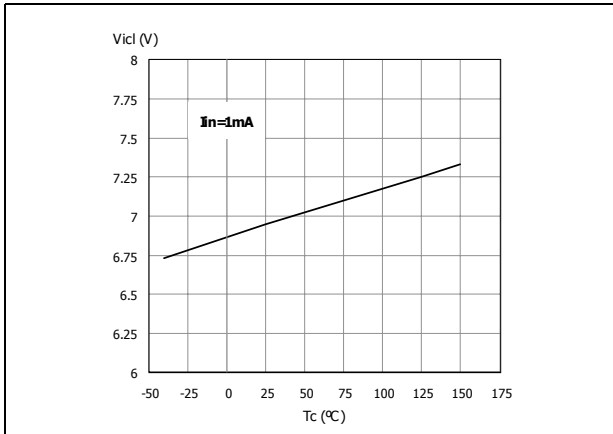


Figure 10. Turn-on voltage slope

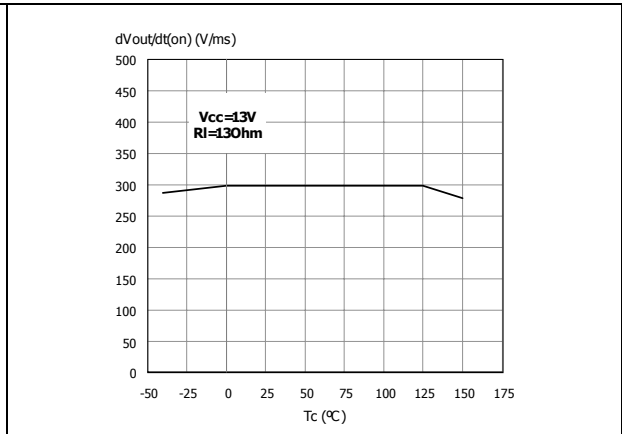


Figure 11. Overvoltage shutdown

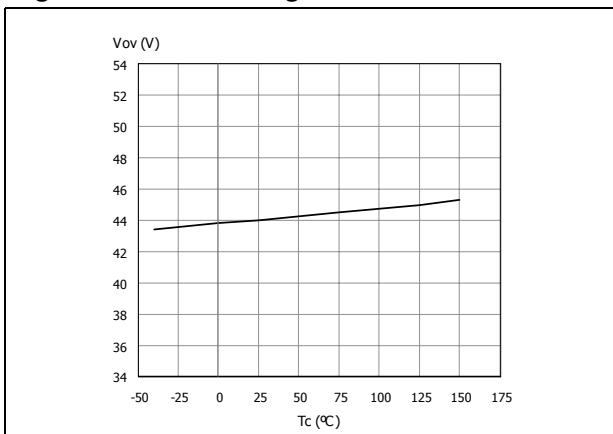


Figure 12. Turn-off voltage slope

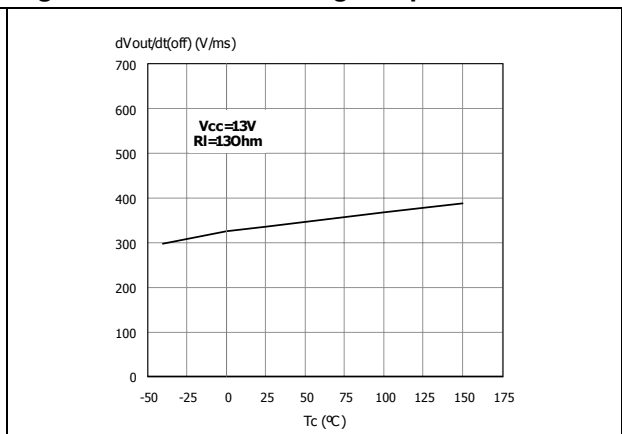


Figure 13.  $I_{LIM}$  vs  $T_{case}$

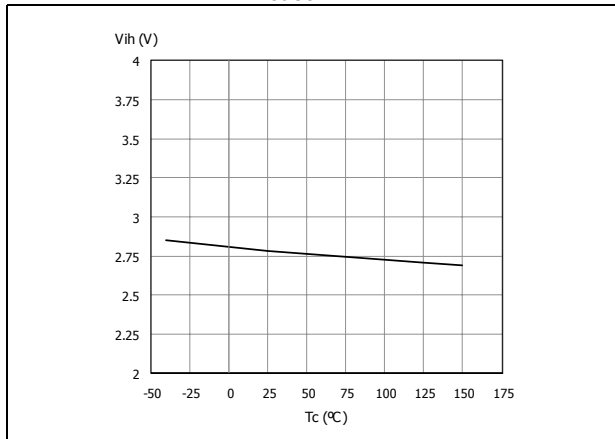


Figure 14. On state resistance vs  $V_{CC}$

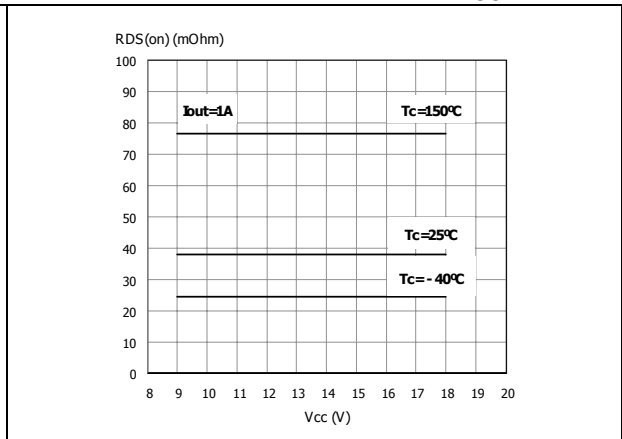


Figure 15. Input high level

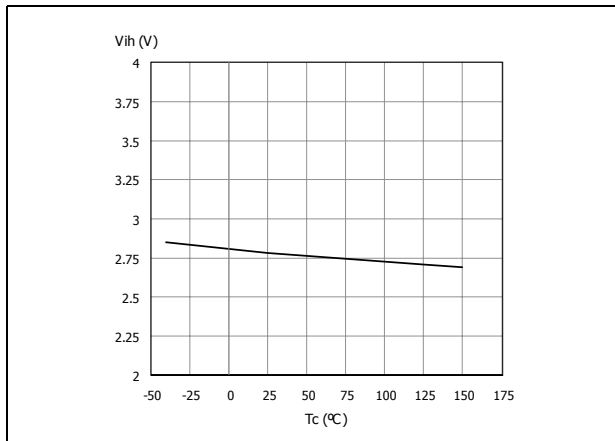


Figure 16. Input hysteresis voltage

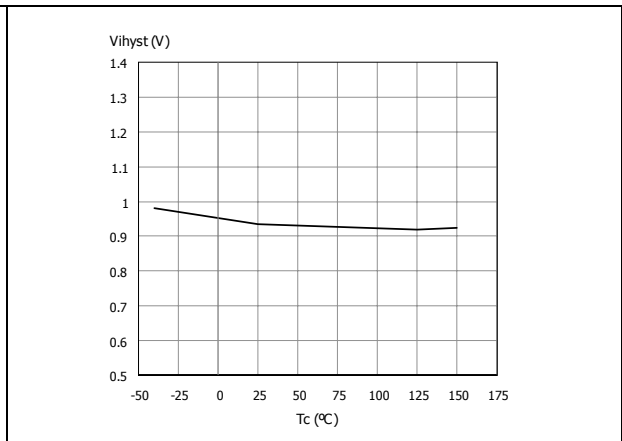


Figure 17. On state resistance vs  $T_{case}$

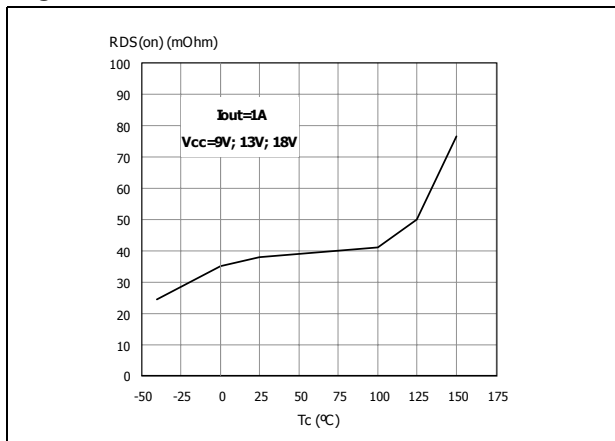


Figure 18. Input low level

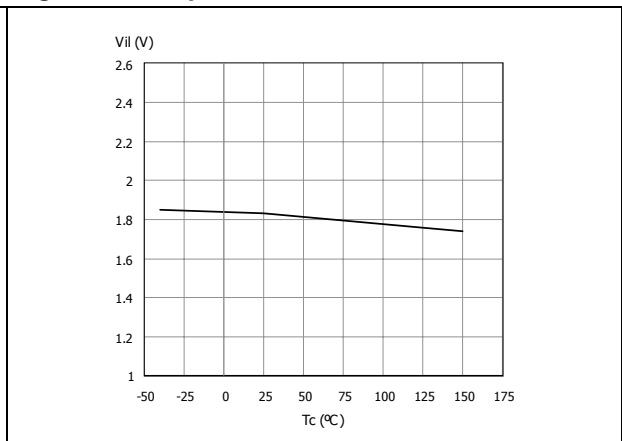


Figure 19. Status leakage current

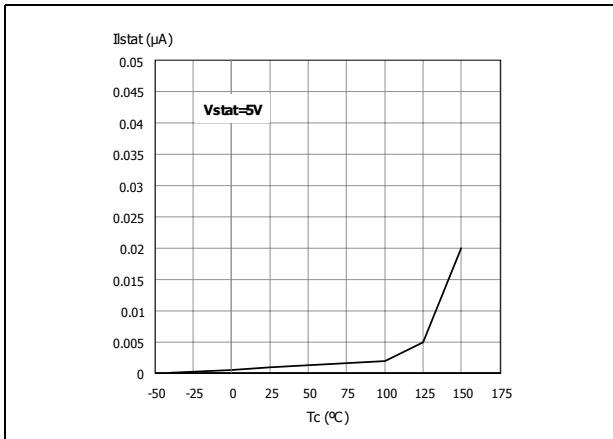


Figure 20. Status low output voltage

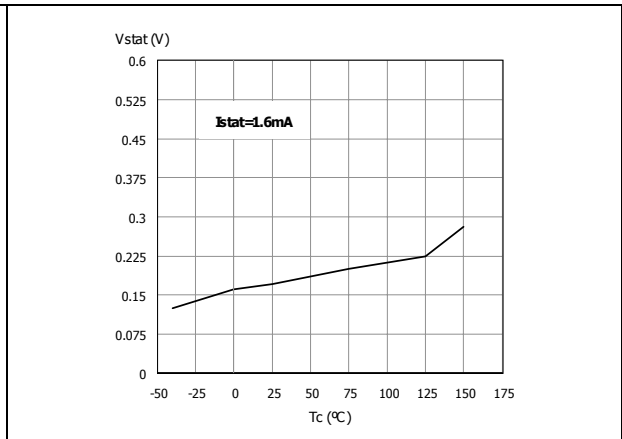


Figure 21. Status clamp voltage

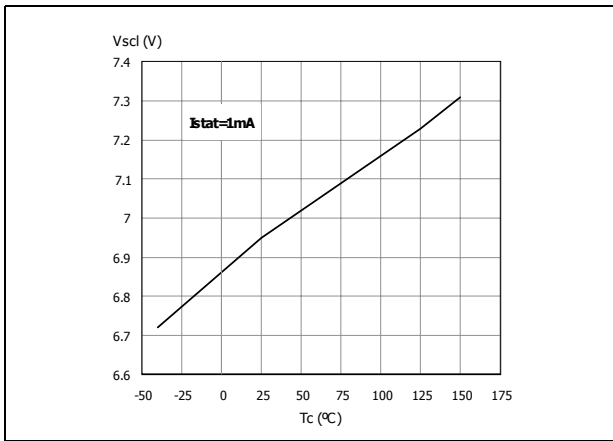
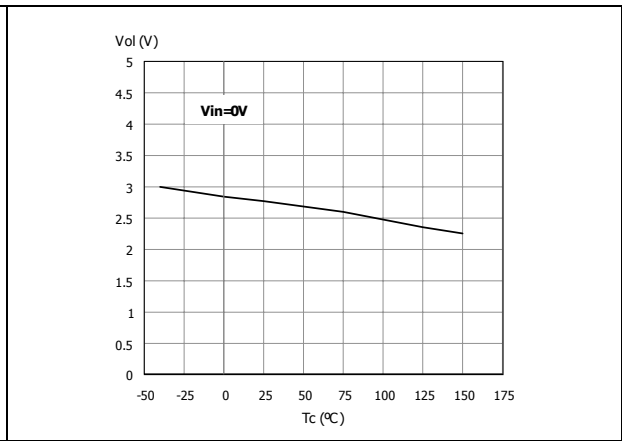
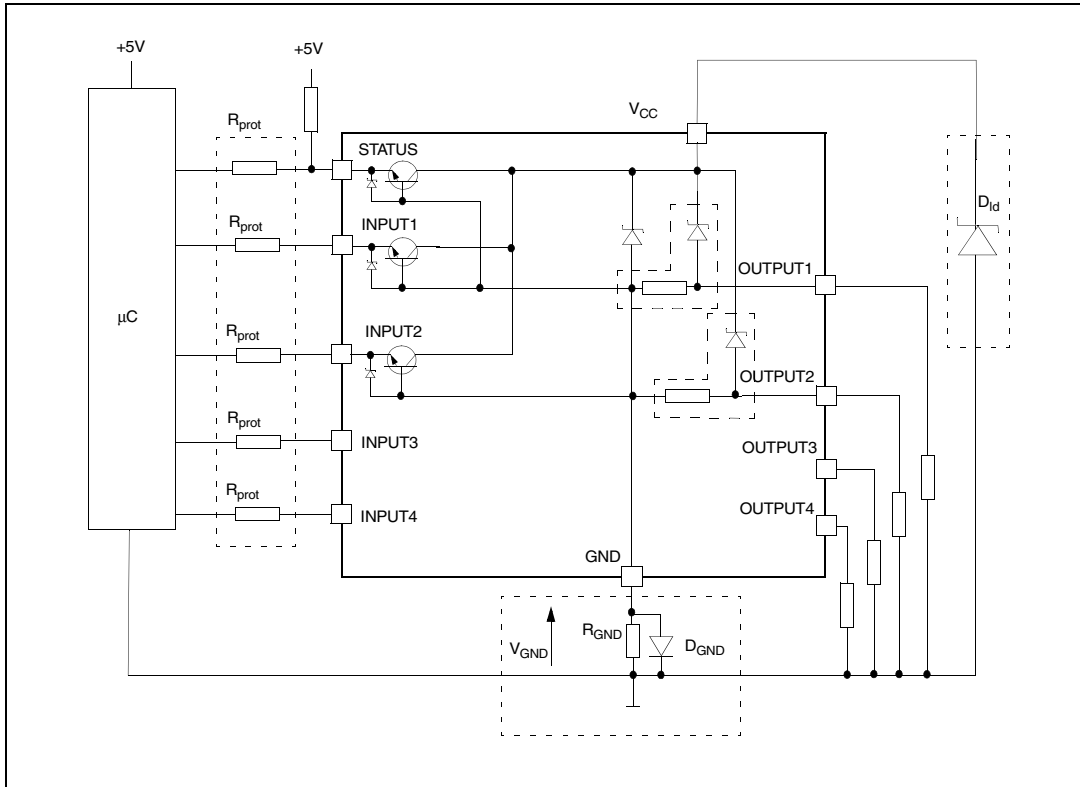


Figure 22. Openload Off state detection threshold



### 3 Application information

Figure 23. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

#### 3.1.1 Solution 1: a resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following show how to dimension the R<sub>GND</sub> resistor:

1.  $R_{GND} \leq 600mV / 2 (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$  during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$



This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(ON)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the  $R_{GND}$  will produce a shift ( $I_{S(ON)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than those shown in the ISO T/R 7637/1 table.

## 3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

### Example

For the following conditions:

$$V_{CCpeak} = -100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

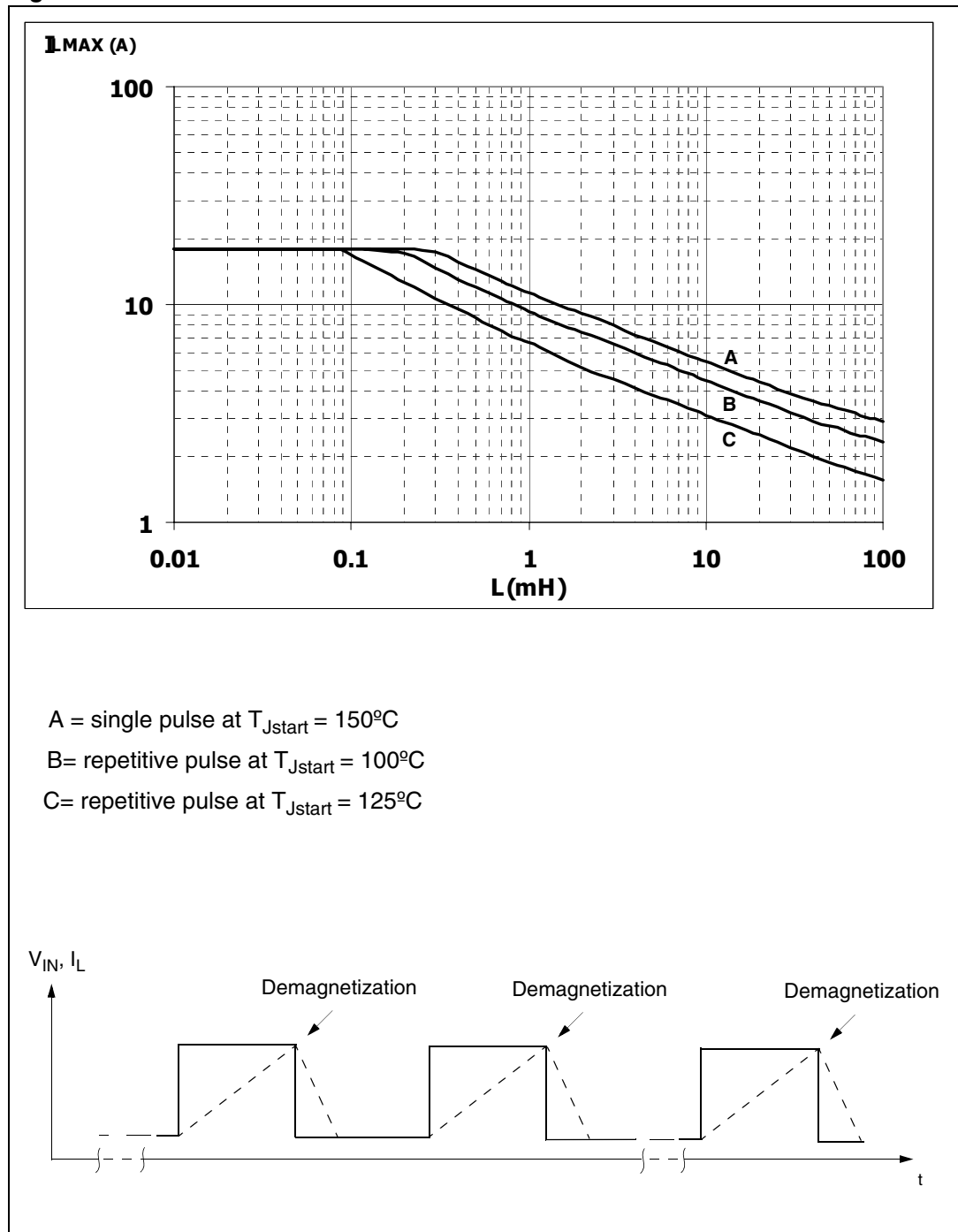
$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 24. Maximum turn-off current versus load inductance

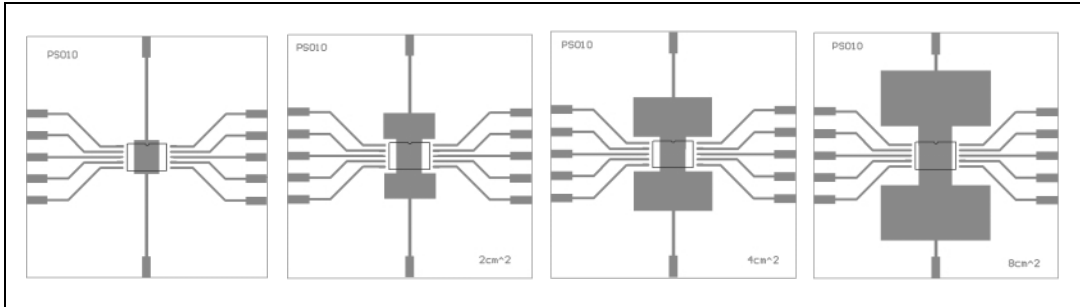


Note: Values are generated with  $R_L = 0\Omega$   
 In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

## 4 Package and PCB thermal data

### 4.1 PowerSO-10 thermal data

Figure 25. PowerSO-10 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 $\mu$ m, Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 26.  $R_{thj-amb}$  Vs PCB copper area in open box free air condition

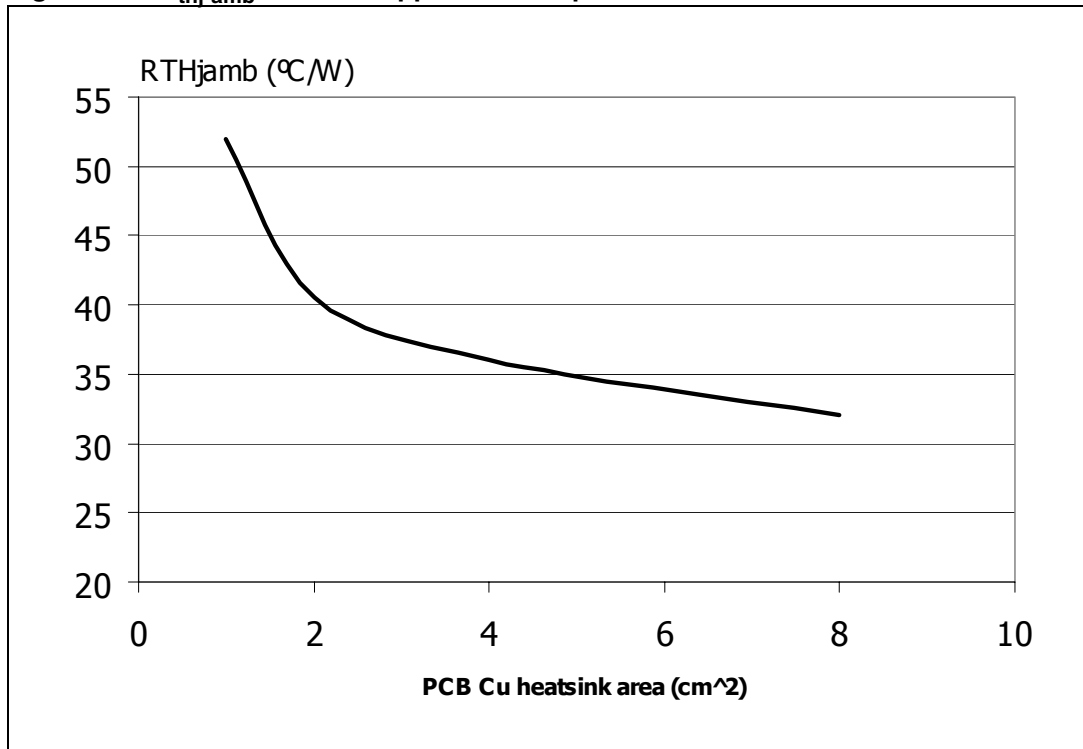
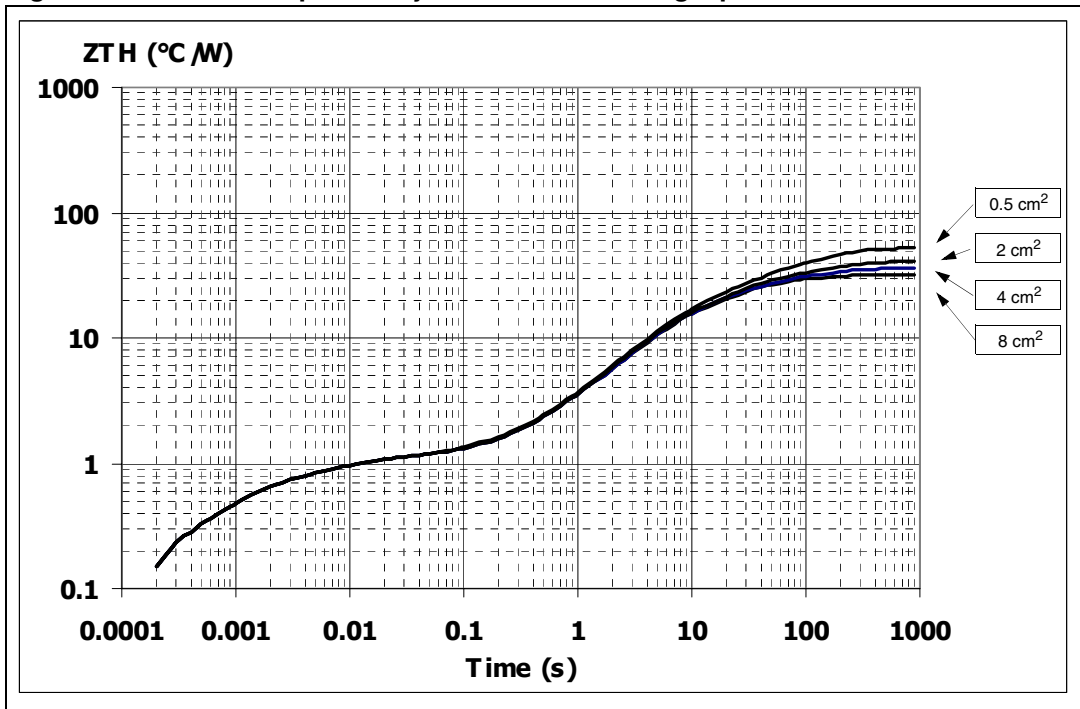


Figure 27. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p / T$

Figure 28. Thermal fitting model of a quad channel HSD in PowerSO-10

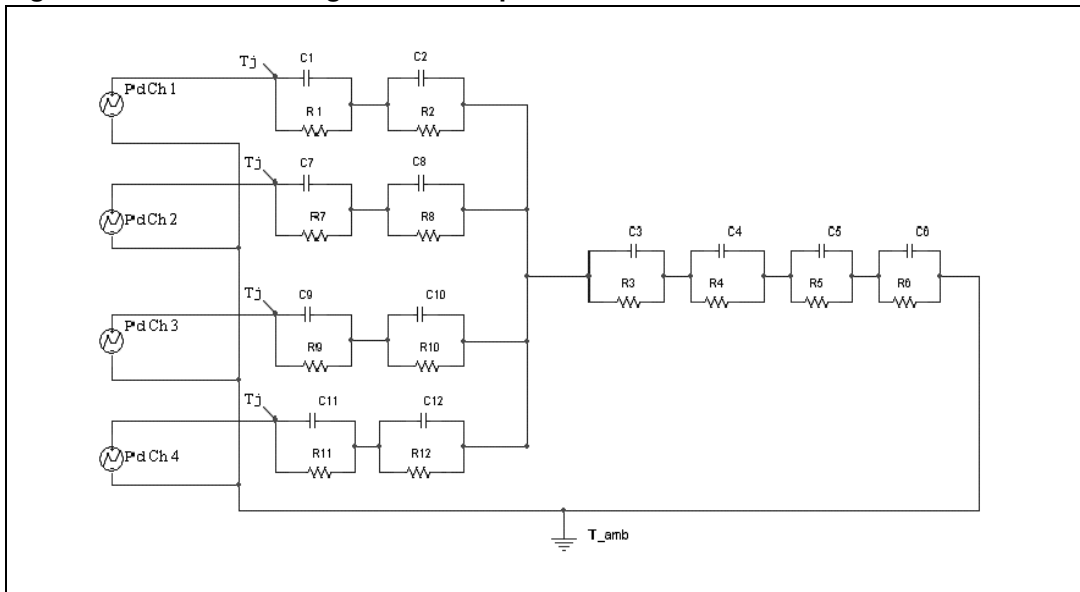


Table 13. Thermal parameters

Area / island (cm <sup>2</sup> )	0.5	2	4	8
R1 = R7 = R9 = R11 (°C/W)	0.15			
R2 = R8 = R10 = R12 (°C/W)	0.5			
R3 (°C/W)	0.4			
R4 (°C/W)	10			
R5 (°C/W)	15			
R6 (°C/W)	26	14.5	10	6
C1 = C7 = C9 = C11 (W.s/°C)	0.0006			
C2 = C8 = C10 = C12 (W.s/°C)	0.0021			
C3 (W.s/°C)	0.02			
C4 (W.s/°C)	0.5			
C5 (W.s/°C)	1.5			
C6 (W.s/°C)	5	10	14	18

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at [www.st.com](http://www.st.com).

### 5.2 PowerSO-10 mechanical data

Figure 29. PowerSO-10 package dimensions

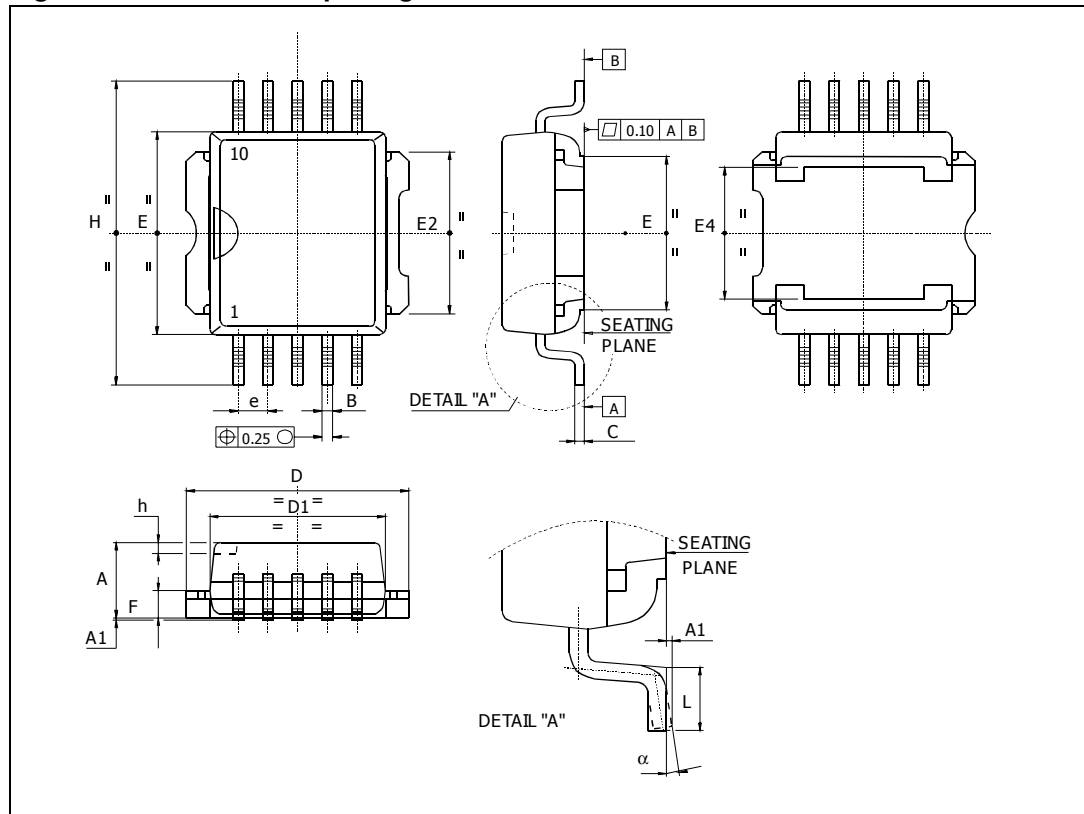


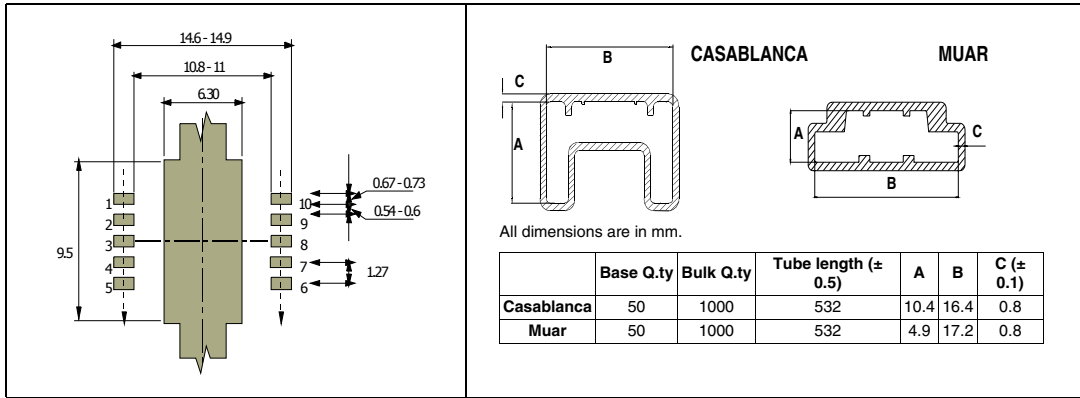
Table 14. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A <sup>(1)</sup>	3.4		3.6
A1	0		0.10
B	0.40		0.60
B <sup>(1)</sup>	0.37		0.53
C	0.35		0.55
C <sup>(1)</sup>	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 <sup>(1)</sup>	7.30		7.50
E4	5.90		6.10
E4 <sup>(1)</sup>	5.90		6.30
e		1.27	
F	1.25		1.35
F <sup>(1)</sup>	1.20		1.40
H	13.80		14.40
H <sup>(1)</sup>	13.85		14.35
h		0.50	
L	1.20		1.80
L <sup>(1)</sup>	0.80		1.10
$\alpha$	0°		8°
$\alpha$ <sup>(1)</sup>	2°		8°

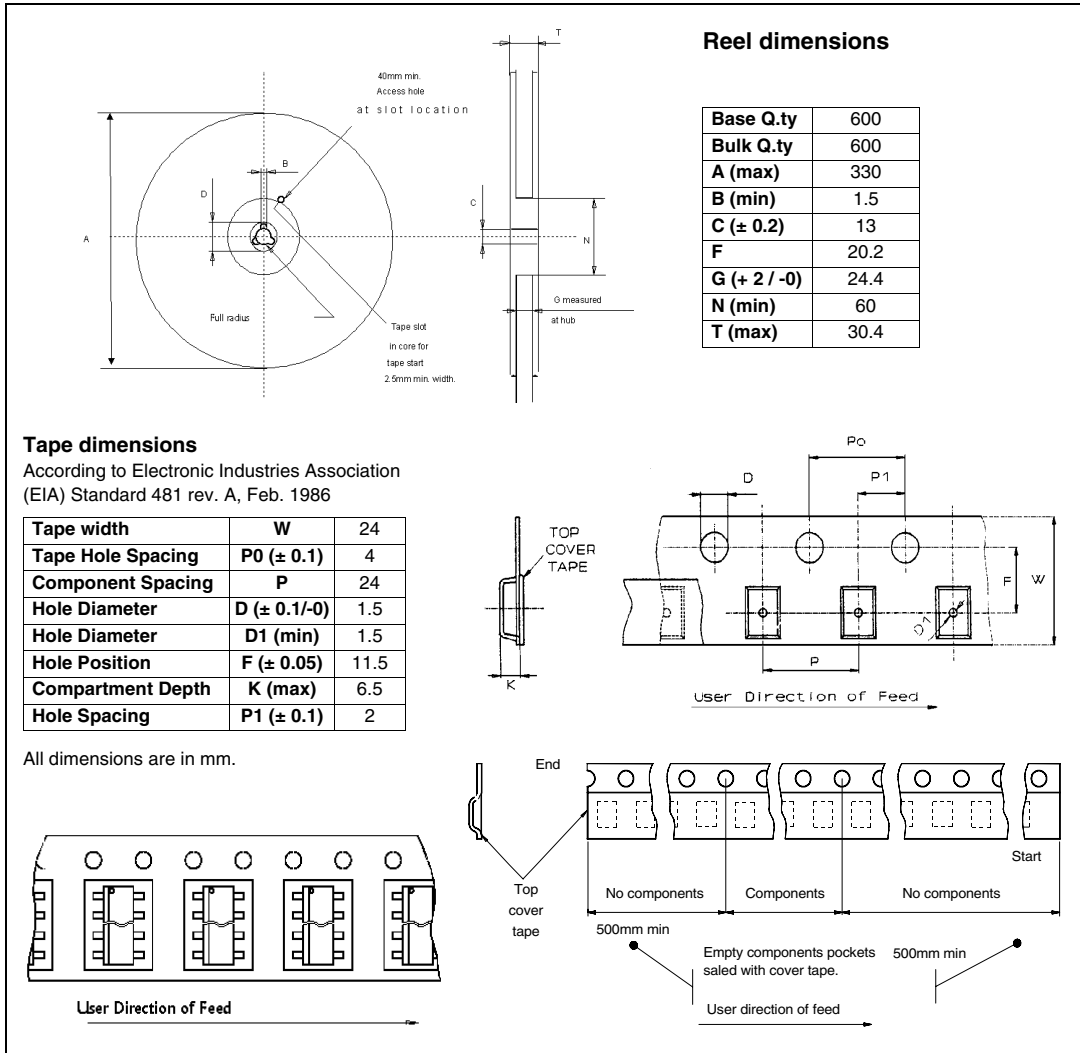
1. Muar only POA P013P.

### 5.3 PowerSO-10 packing information

**Figure 30. PowerSO-10 suggested pad layout**      **Figure 31. PowerSO-10 tube shipment (no suffix)**



**Figure 32. SO-28 tape and reel shipment (suffix "TR")**





## 6 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
22-Jun-2004	1	Initial release.
14-Jul-2004	2	New revision.
24-Jul-2004	3	Minor changes. Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and not connected pins insertion (page 3). 6 cm <sup>2</sup> Cu condition insertion in thermal data table (page 3). V <sub>CC</sub> - output diode section update (page 3). Protections note insertion (page 4) Revision history table insertion (page 18).
28-Jul-2004	4	Disclaimers Update (page 19).
03-Dec-2008	5	Document reformatted and restructured. Added contents, list of tables and figures. Added <i>ECOPACK® packages</i> information.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)