

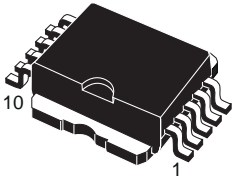


DOUBLE CHANNEL HIGH SIDE DRIVER

TYPE	R _{DS(on)}	I _{OUT}	V _{CC}
VND830SP	60 mΩ (*)	6 A (*)	36 V

(*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- LOSS OF GROUND PROTECTION
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)



PowerSO-10™

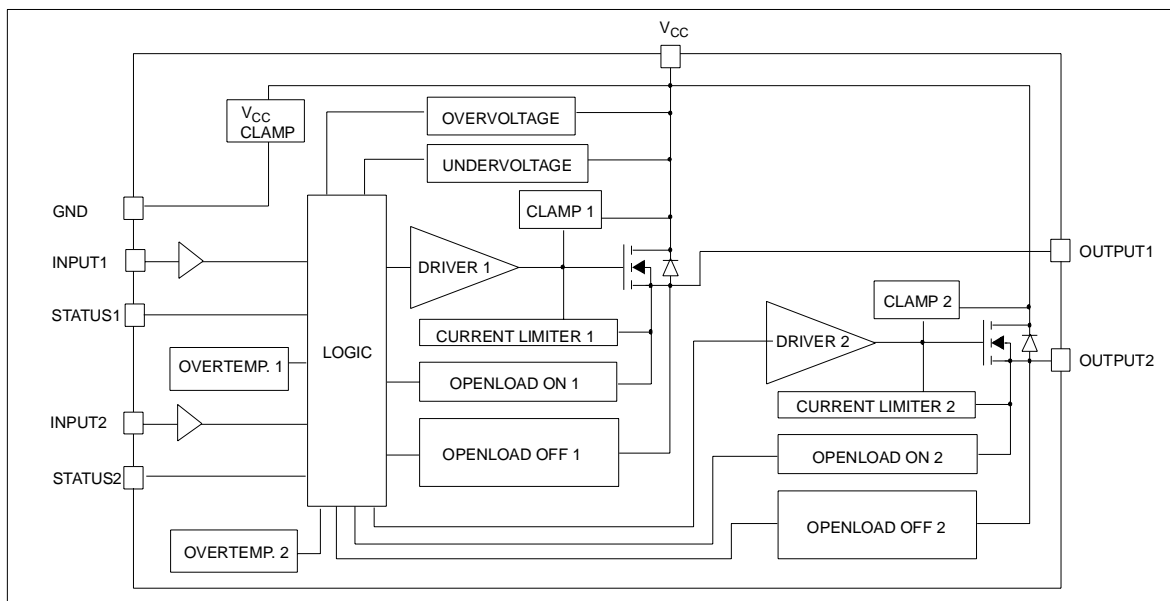
ORDER CODES		
PACKAGE	TUBE	T&R
PowerSO-10™	VND830SP	VND830SP13TR

DESCRIPTION

The VND830SP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient

compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM



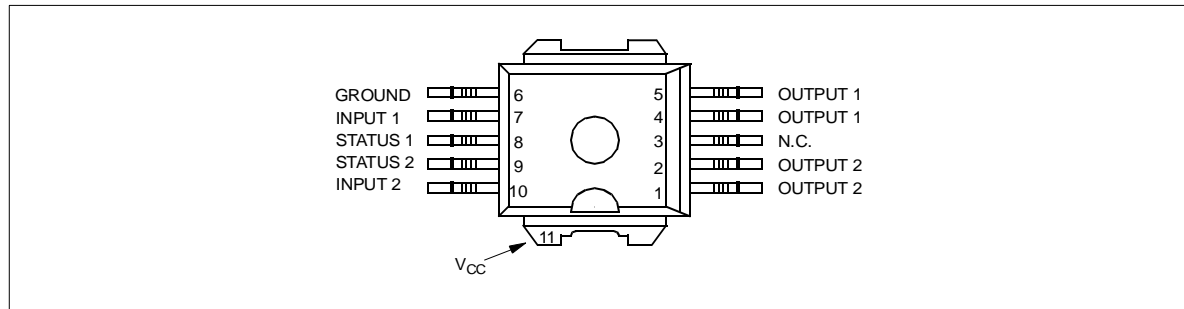
(**) See application schematic at page 8

VND830SP

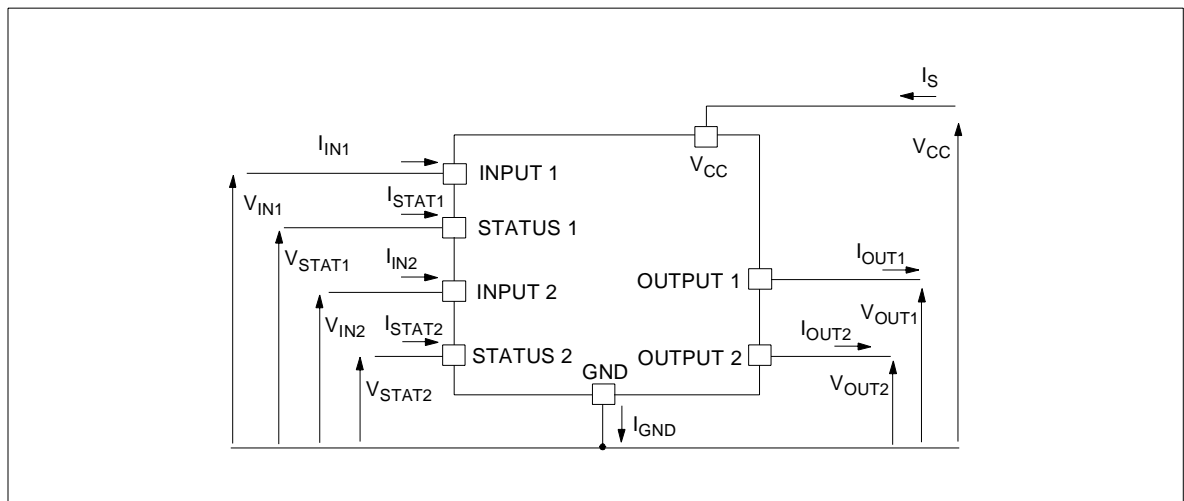
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3	V
$-I_{GND}$	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
$-I_{OUT}$	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{STAT}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5K Ω ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
E_{MAX}	Maximum Switching Energy ($L=1.8mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=9A$)	100	mJ
P_{tot}	Power Dissipation $T_C=25^\circ C$	73.5	W
T_j	Junction Operating Temperature	Internally Limited	$^\circ C$
T_C	Case Operating Temperature	- 40 to 150	$^\circ C$
T_{stg}	Storage Temperature	- 55 to 150	$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case	1.7	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	51.7 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise specified)

(Per each channel)

POWER OUTPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC} (**)	Operating Supply Voltage		5.5	13	36	V
V _{USD} (**)	Undervoltage Shut-down		3	4	5.5	V
V _{OV} (**)	Overvoltage Shut-down		36			V
R _{ON}	On State Resistance	I _{OUT} = 2A; T _j = 25°C I _{OUT} = 2A; V _{CC} > 8V			60 120	mΩ mΩ
I _S (**)	Supply Current	Off State; V _{CC} = 13V; V _{IN} = V _{OUT} = 0V Off State; V _{CC} = 13V; T _j = 25°C; V _{IN} = V _{OUT} = 0V On State; V _{CC} = 13V		12 12 5	40 25 7	µA µA mA
I _{L(off1)}	Off State Output Current	V _{IN} = V _{OUT} = 0V; V _{CC} = 36V; T _j = 125°C	0		50	µA
I _{L(off2)}	Off State Output Current	V _{IN} = 0V; V _{OUT} = 3.5V	-75		0	µA
I _{L(off3)}	Off State Output Current	V _{IN} = V _{OUT} = 0V; V _{CC} = 13V; T _j = 125°C			5	µA
I _{L(off4)}	Off State Output Current	V _{IN} = V _{OUT} = 0V; V _{CC} = 13V; T _j = 25°C			3	µA

(**) Per device

SWITCHING (V_{CC} = 13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	R _L = 6.5Ω from V _{IN} rising edge to V _{OUT} = 1.3V		30		µs
t _{d(off)}	Turn-off Delay Time	R _L = 6.5Ω from V _{IN} falling edge to V _{OUT} = 11.7V		30		µs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L = 6.5Ω from V _{OUT} = 1.3V to V _{OUT} = 10.4V		See relative diagram		V/µs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L = 6.5Ω from V _{OUT} = 11.7V to V _{OUT} = 1.3V		See relative diagram		V/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IL}	Input Low Level				1.25	V
I _{IL}	Low Level Input Current	V _{IN} = 1.25V	1			µA
V _{IH}	Input High Level		3.25			V
I _{IH}	High Level Input Current	V _{IN} = 3.25V			10	µA
V _{I(hyst)}	Input Hysteresis Voltage		0.5			V
V _{ICL}	Input Clamp Voltage	I _{IN} = 1mA I _{IN} = -1mA	6	6.8 -0.7	8	V V

VND830SP

ELECTRICAL CHARACTERISTICS (continued)

STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}= 1.6 \text{ mA}$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT}= 5\text{V}$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT}= 5\text{V}$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT}= 1\text{mA}$	6	6.8	8	V
		$I_{STAT}= -1\text{mA}$		-0.7		V

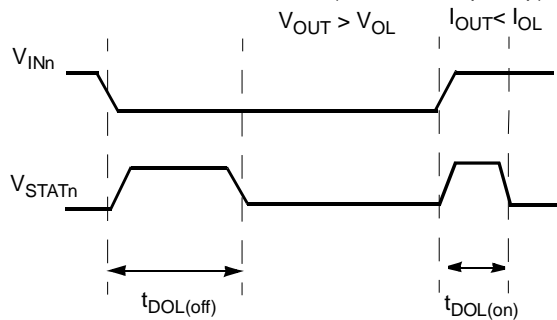
PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset Temperature		135			$^{\circ}\text{C}$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}\text{C}$
t_{SDL}	Status Delay in Overload Conditions	$T_j > T_{TSD}$			20	μs
I_{lim}	Current limitation	$V_{CC}=13\text{V}$	6	9	15	A
		$5.5\text{V} < V_{CC} < 36\text{V}$			15	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2\text{A}; L= 6\text{mH}$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

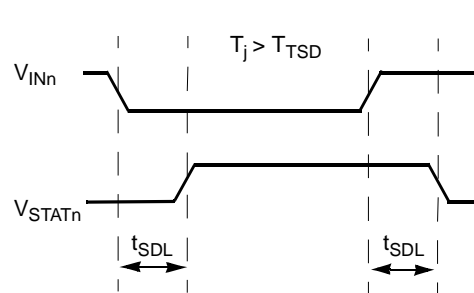
OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN}=5\text{V}$	50	100	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0\text{A}$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN}=0\text{V}$	1.5	2.5	3.5	V
$T_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

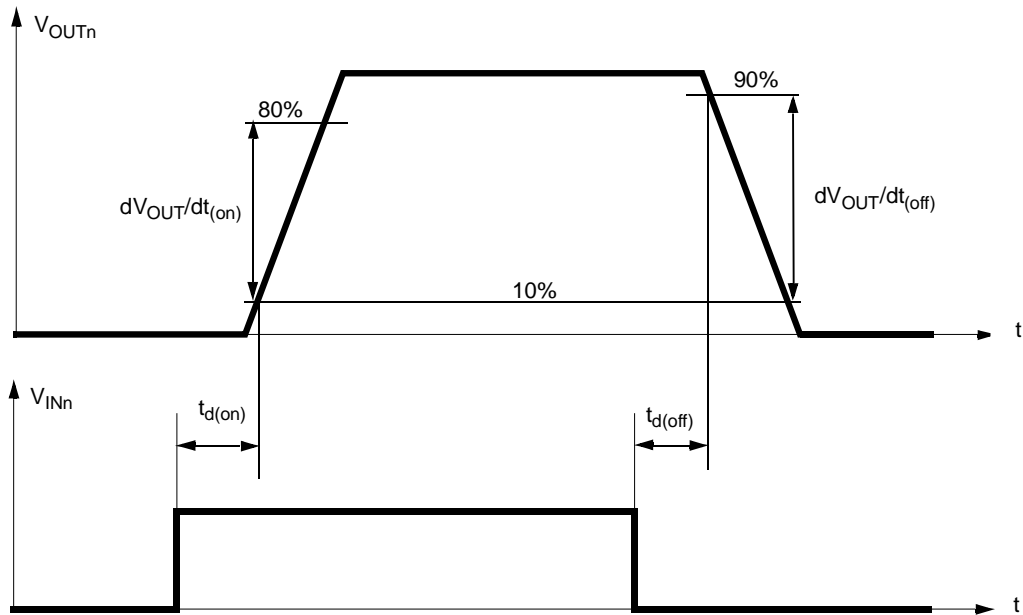
OPEN LOAD STATUS TIMING (with external pull-up)



OVER TEMP STATUS TIMING



Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage $> V_{OL}$	L	H	L
	H	H	H
Output Current $< I_{OL}$	L	L	H
	H	H	L

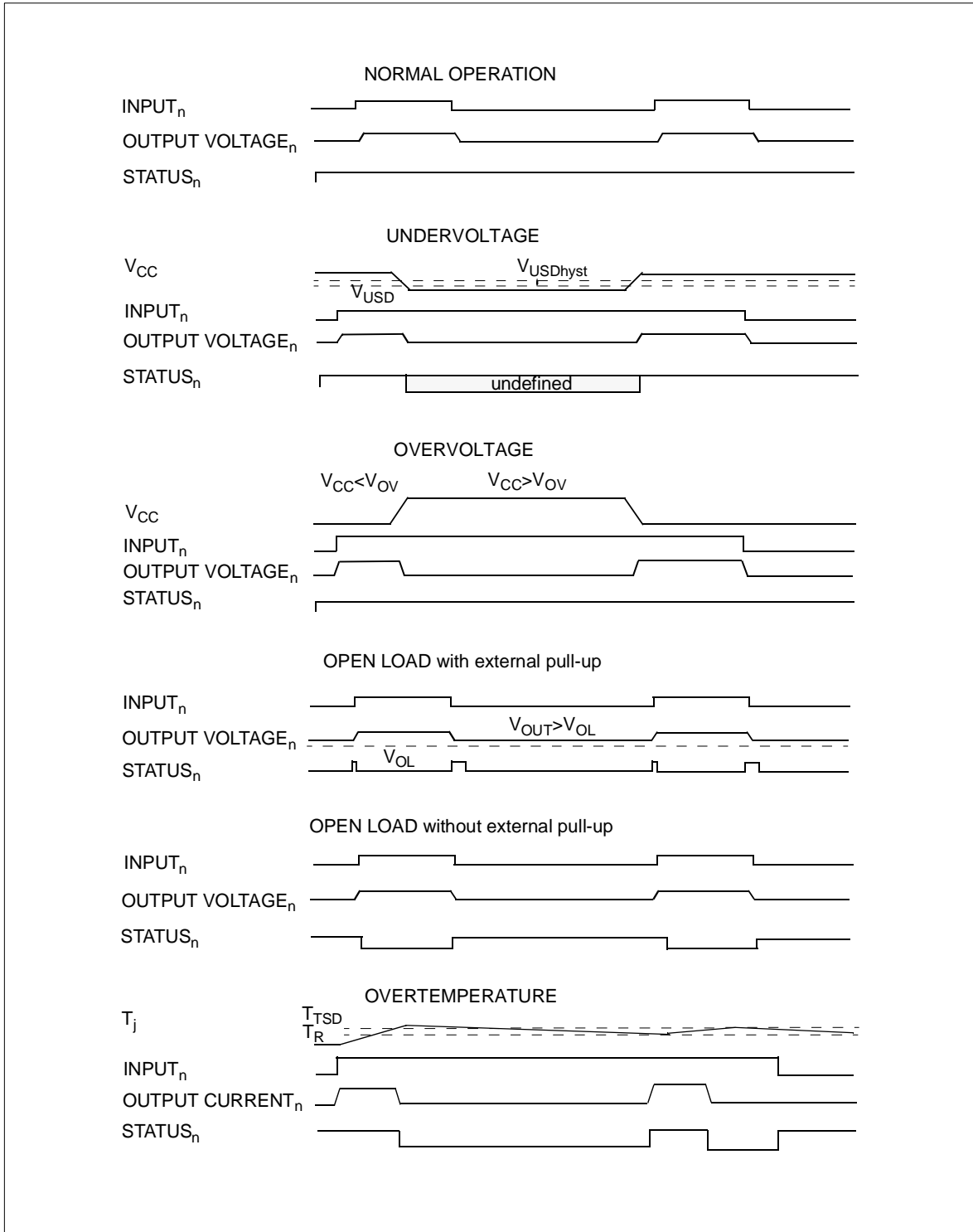
ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

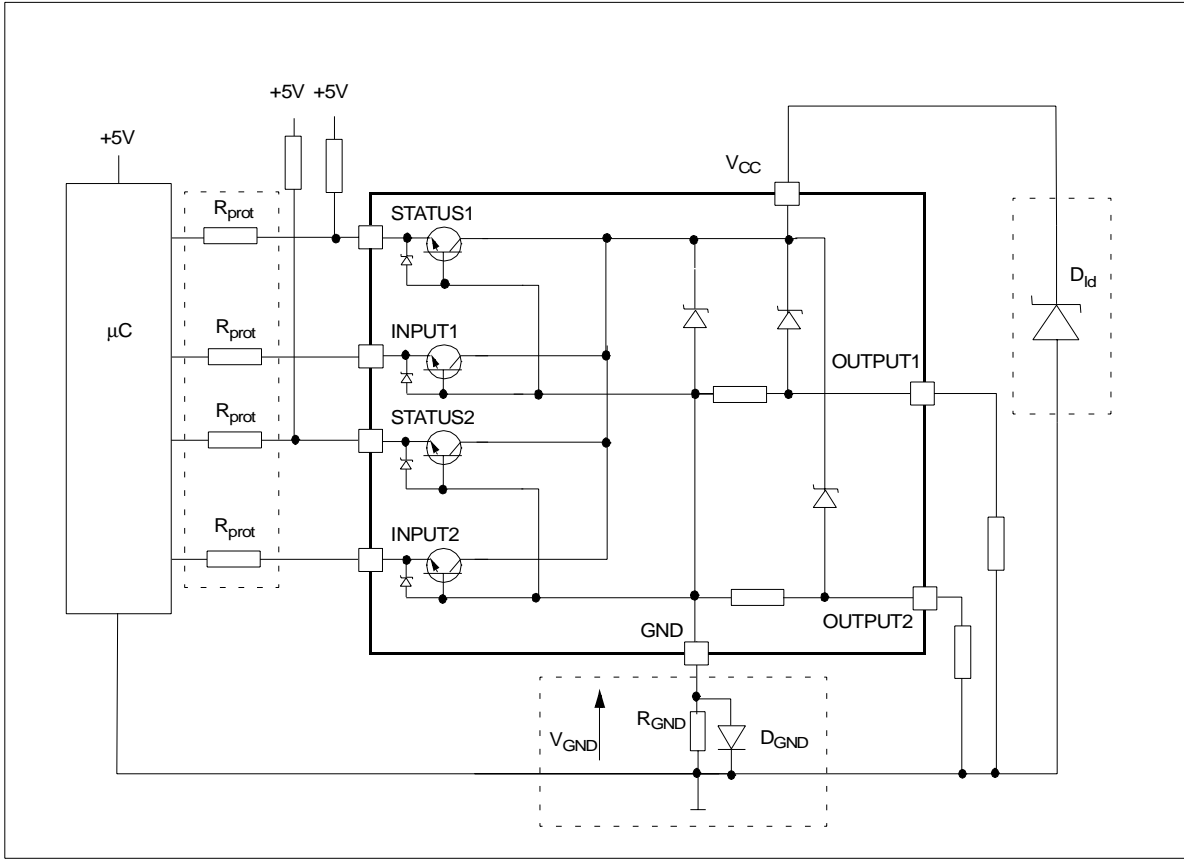
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / I_{S(ON)max}$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(ON)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(ON)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary

depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -100V and I_{latchup} ≥ 20mA; V_{OHµC} ≥ 4.5V
 5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to

supply the microprocessor.

The external resistor has to be selected according to the following requirements:

- 1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin}; this results in the following condition

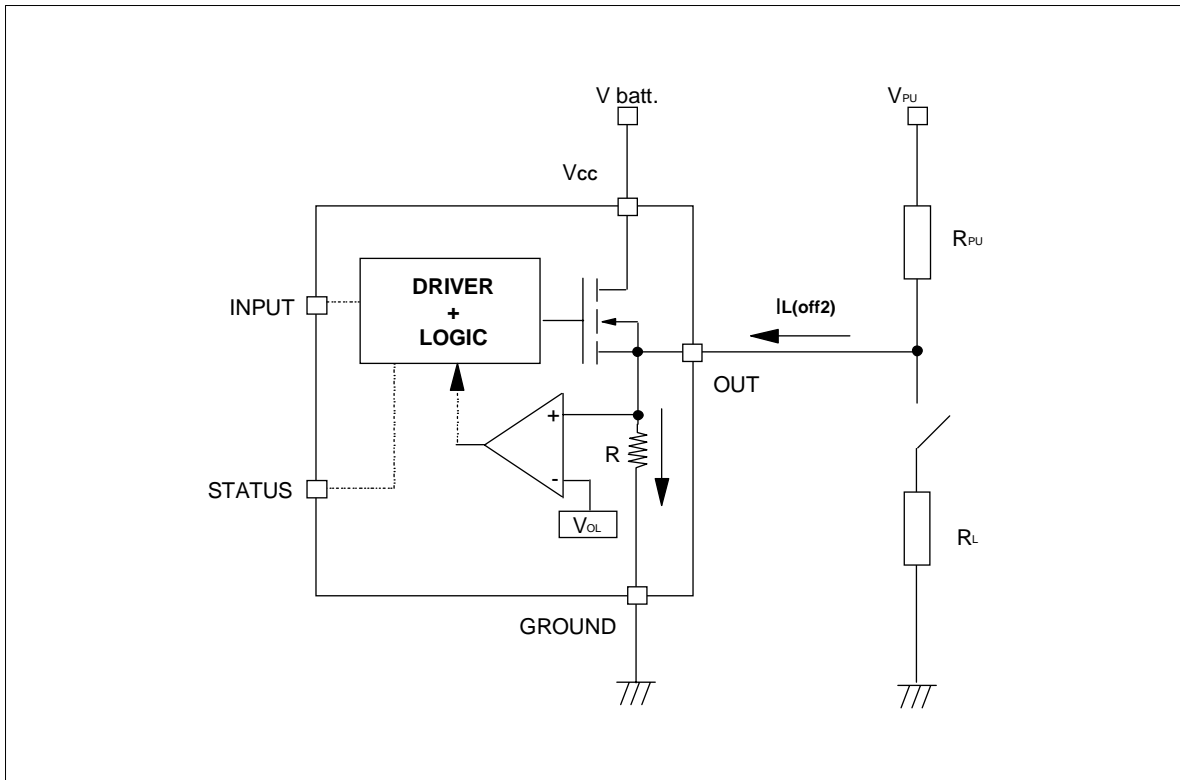
$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}.$$
- 2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition

$$R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}.$$

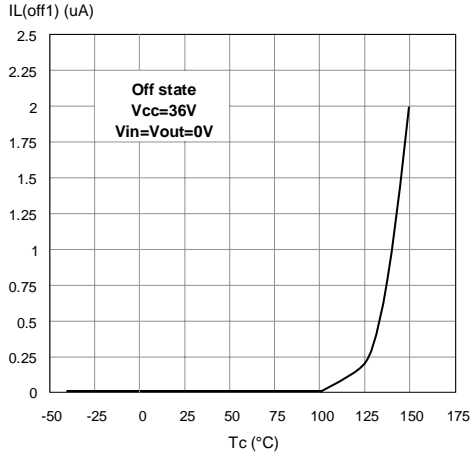
Because I_{S(OFF)} may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin}, V_{OLmax} and I_{L(off2)} are available in the Electrical Characteristics section.

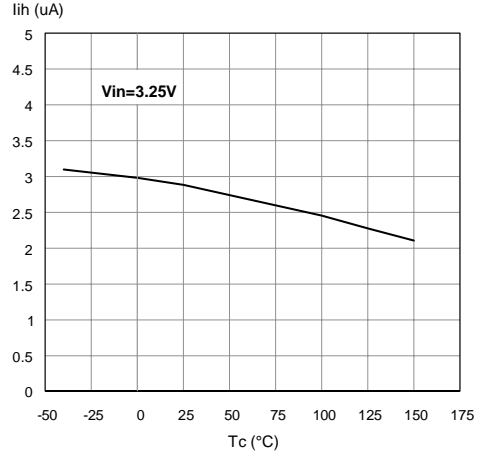
Open Load detection in off state



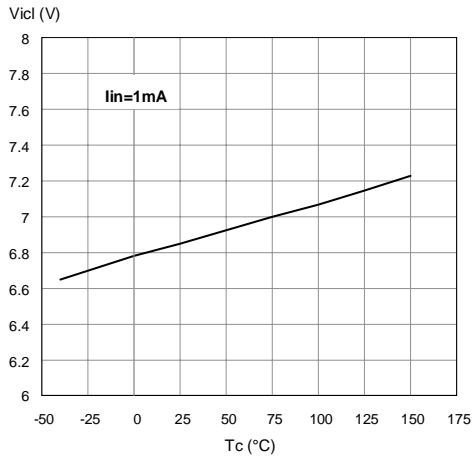
Off State Output Current



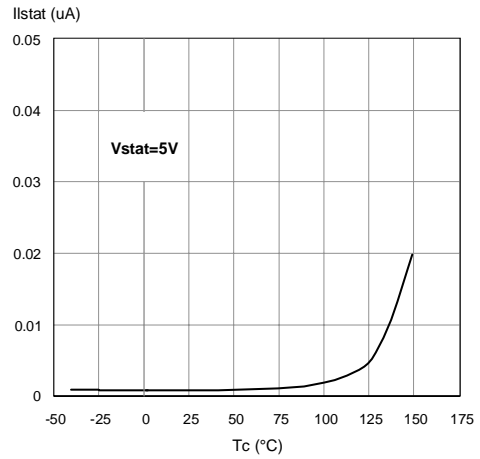
High Level Input Current



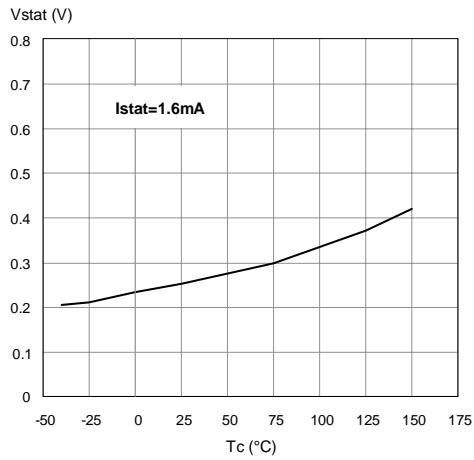
Input Clamp Voltage



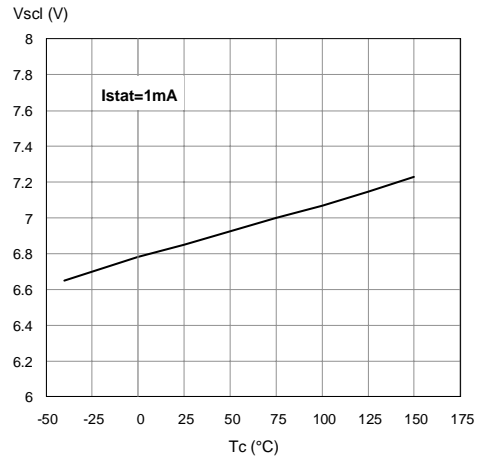
Status Leakage Current



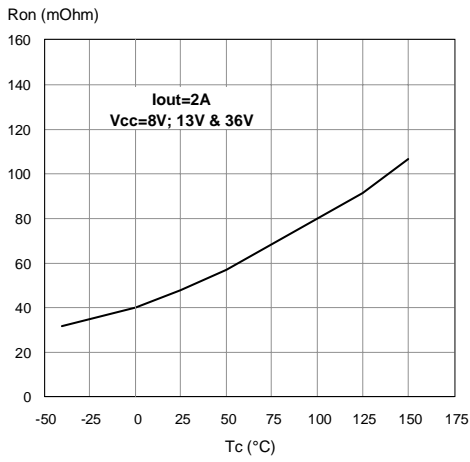
Status Low Output Voltage



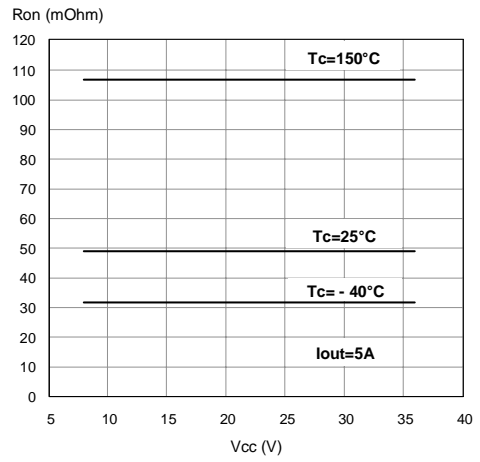
Status Clamp Voltage



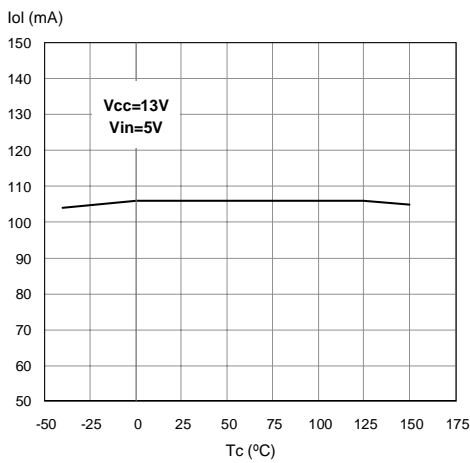
On State Resistance Vs T_{case}



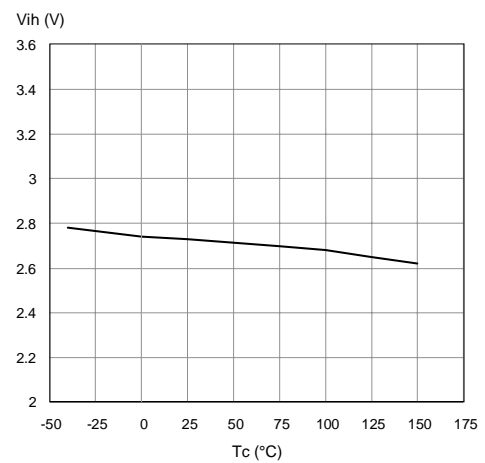
On State Resistance Vs V_{CC}



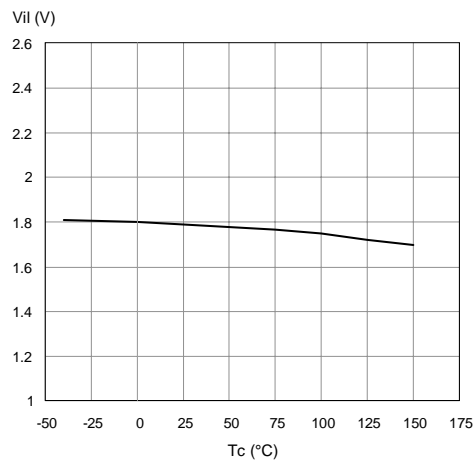
Openload On State Detection Threshold



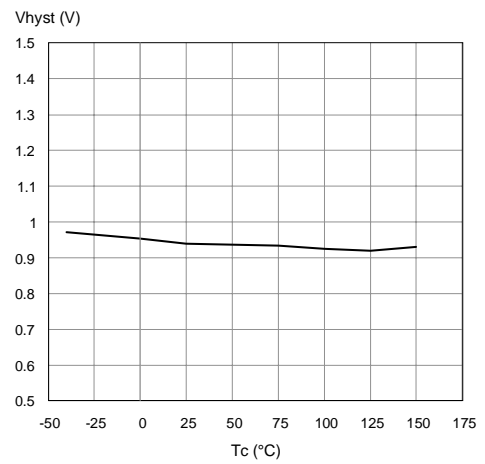
Input High Level



Input Low Level

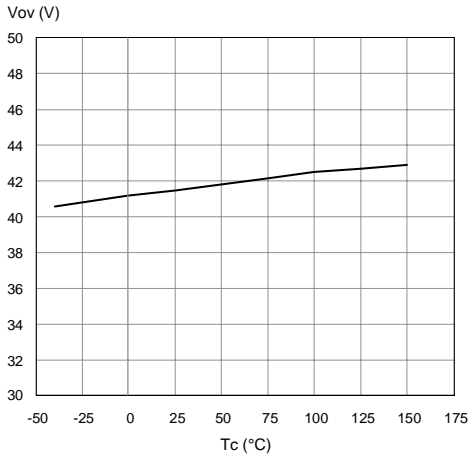


Input Hysteresis Voltage

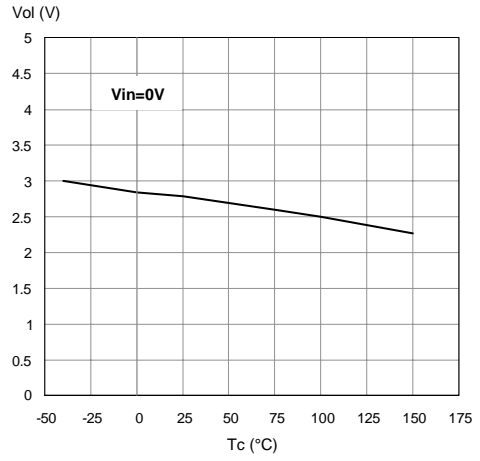


VND830SP

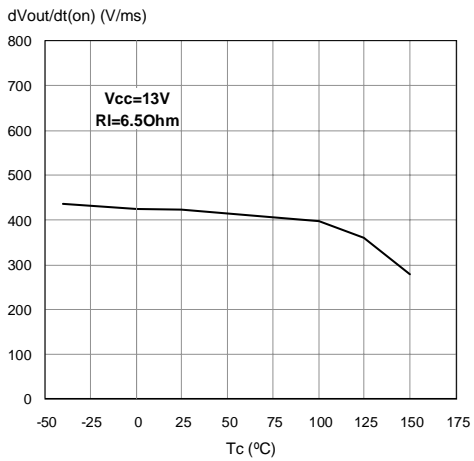
Overvoltage Shutdown



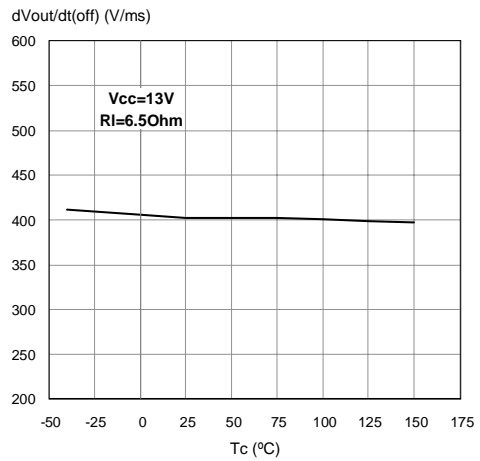
Openload Off State Voltage Detection Threshold



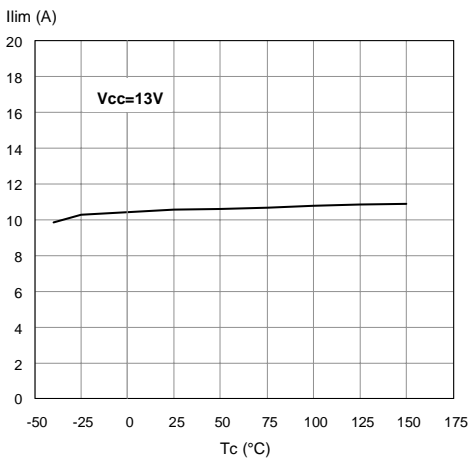
Turn-on Voltage Slope



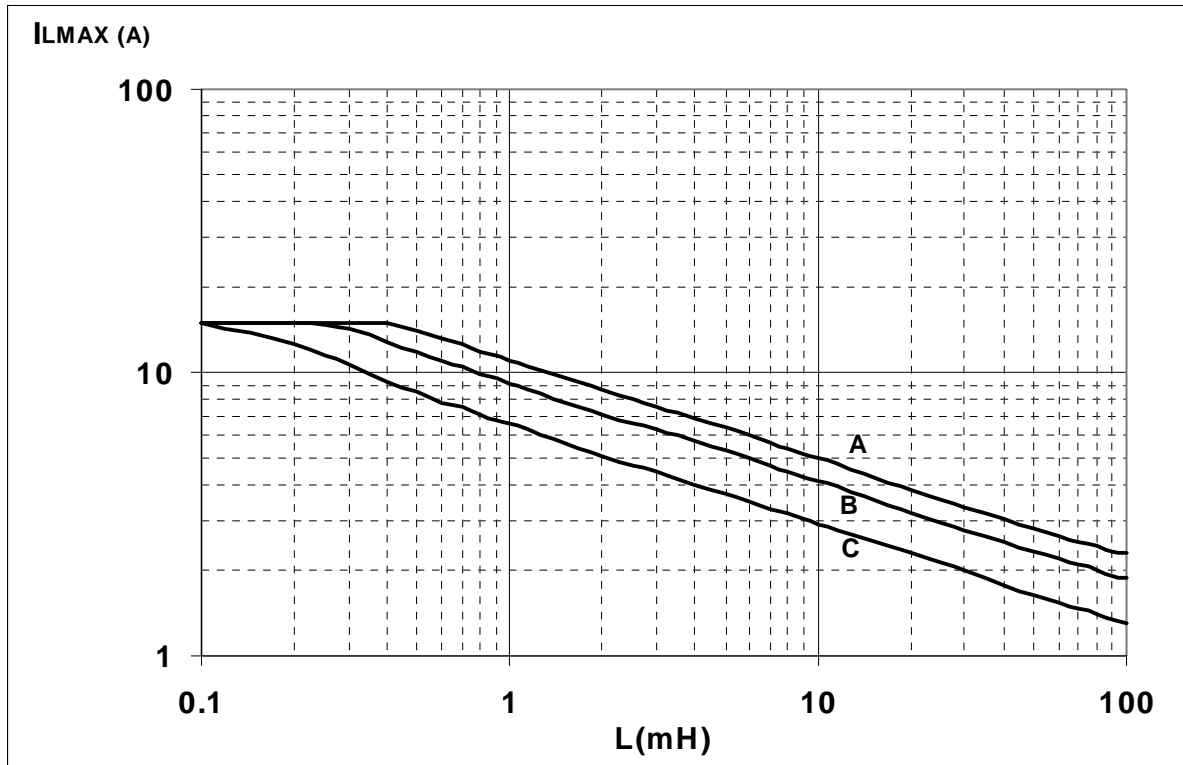
Turn-off Voltage Slope



I_{LIM} Vs T_{case}



Maximum turn off current versus load inductance



A = Single Pulse at $T_{jstart}=150^{\circ}\text{C}$

B = Repetitive pulse at $T_{jstart}=100^{\circ}\text{C}$

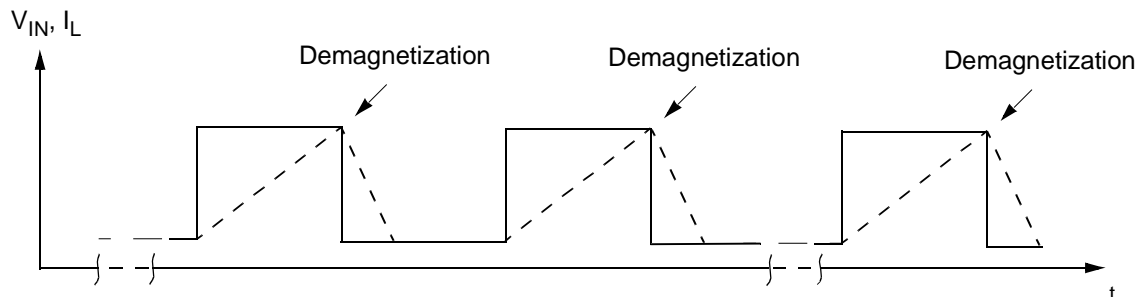
C = Repetitive Pulse at $T_{jstart}=125^{\circ}\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

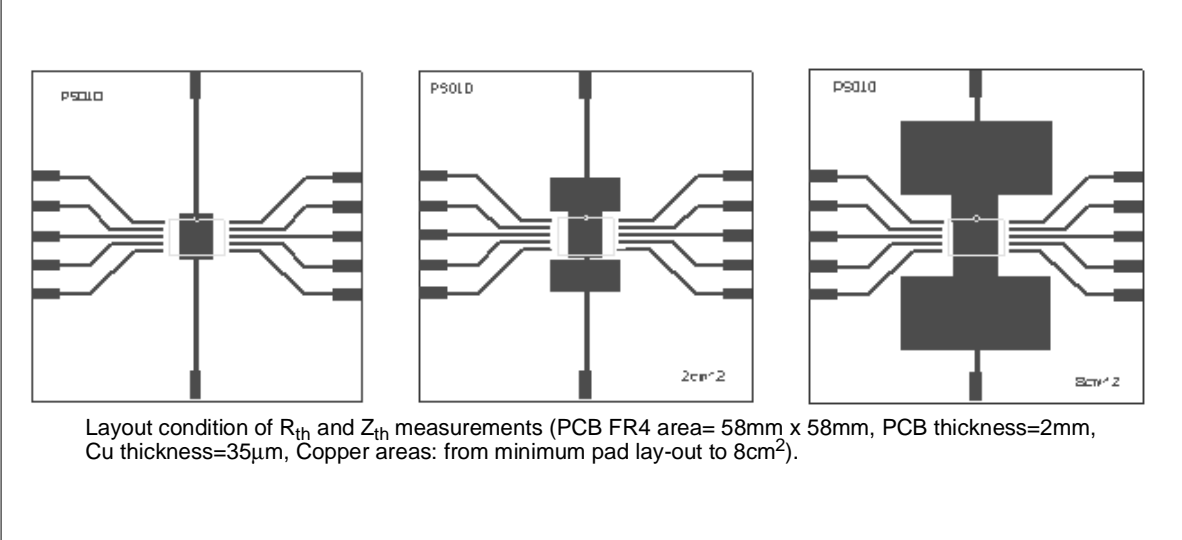
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

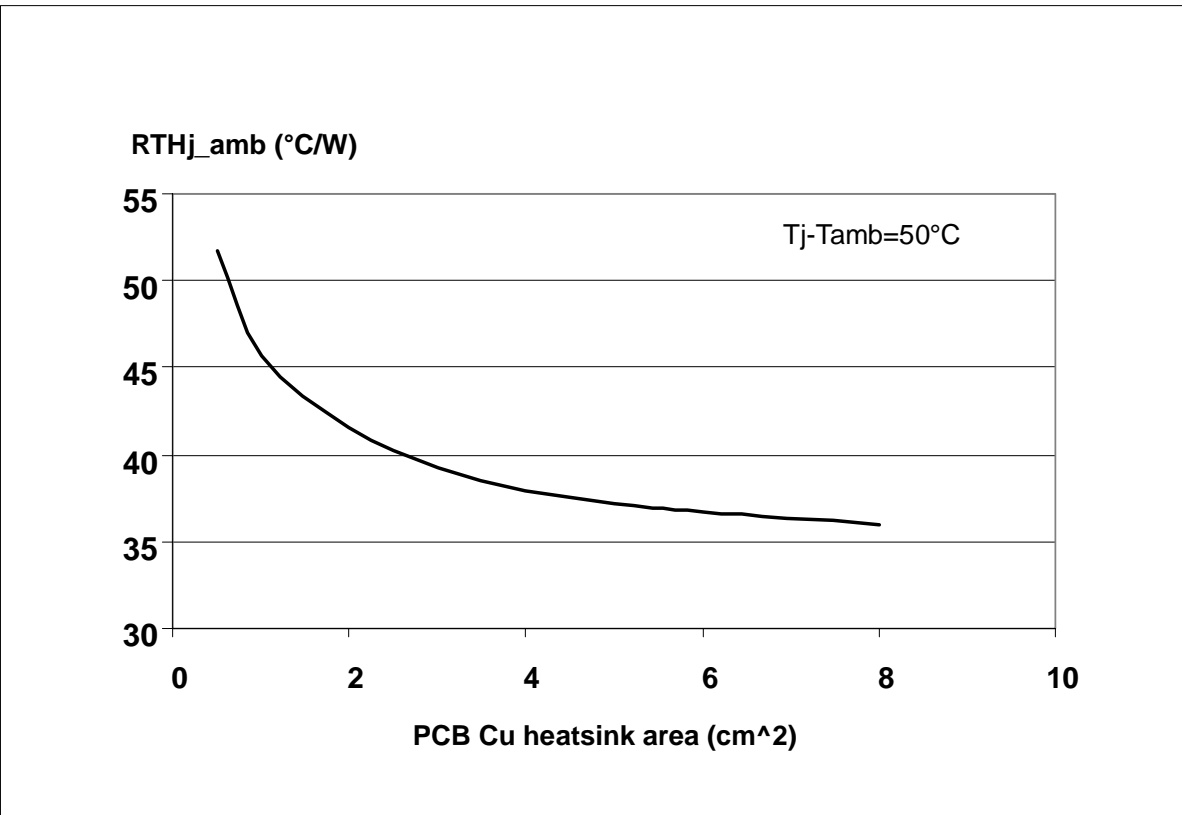


PowerSO-10™ THERMAL DATA

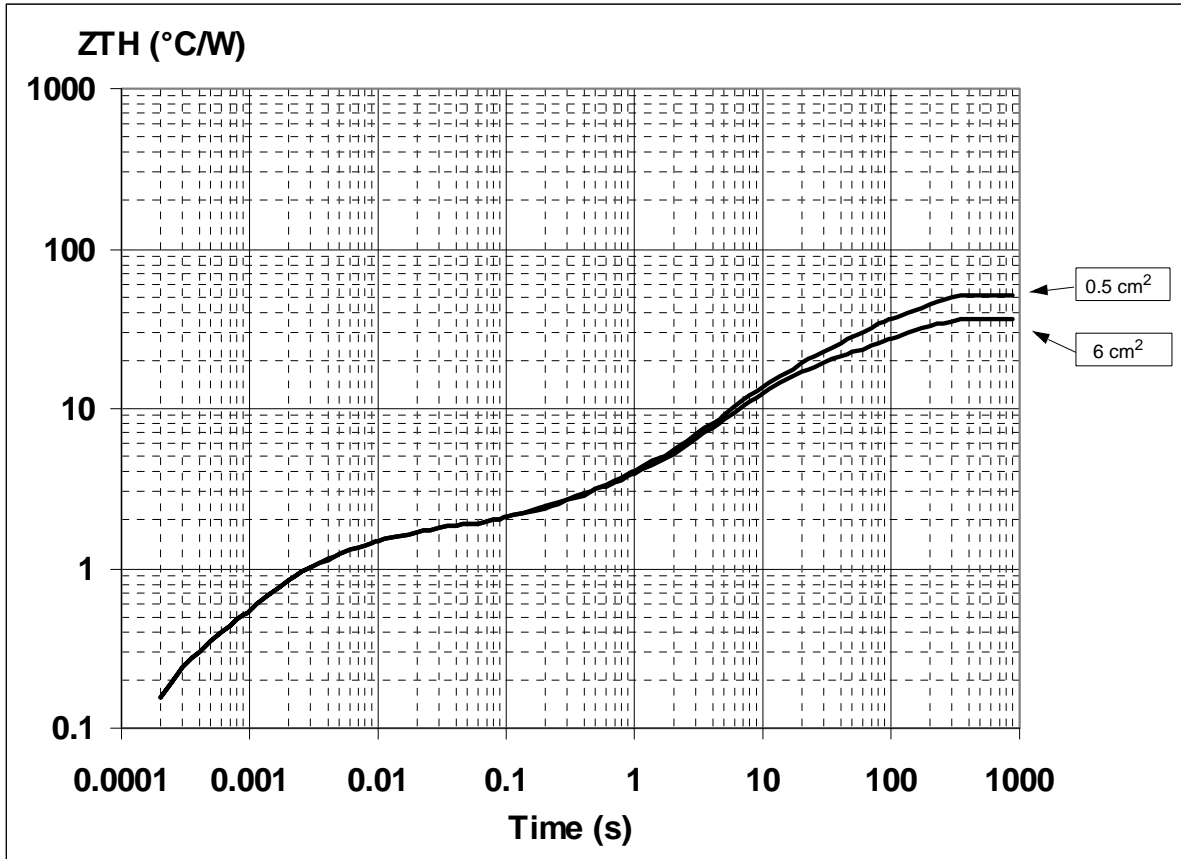
PowerSO-10™ PC Board



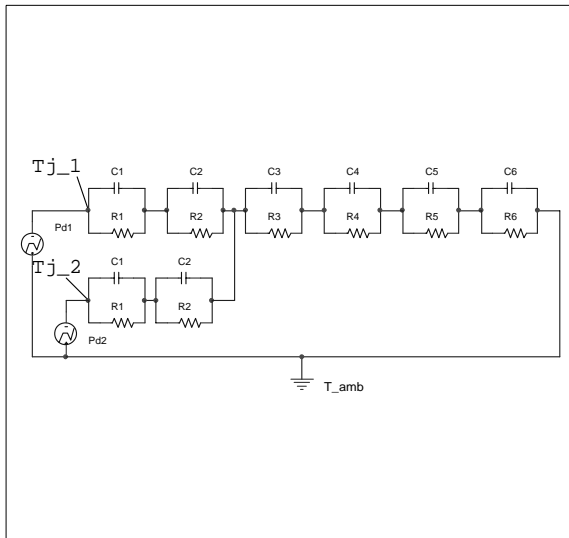
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



PowerSO-10 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

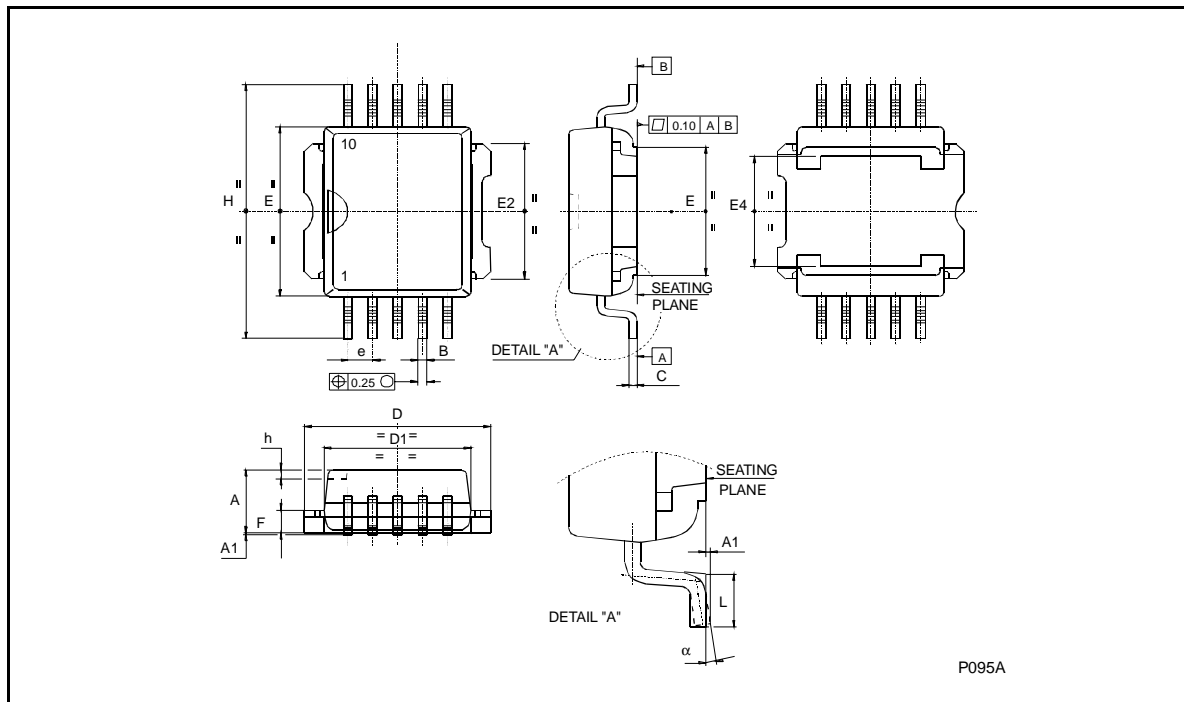
Thermal Parameter

Area/island (cm ²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.8	
R3 (°C/W)	0.7	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	
C3 (W.s/°C)	0.013	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

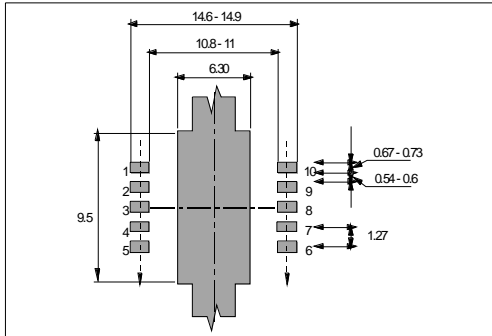
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

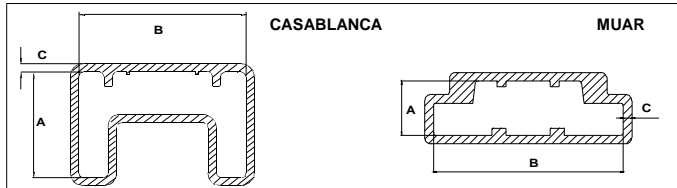
(*) Muar only POA P013P



PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (±0.5)	A	B	C (±0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")

REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	60
T (max)	30.4

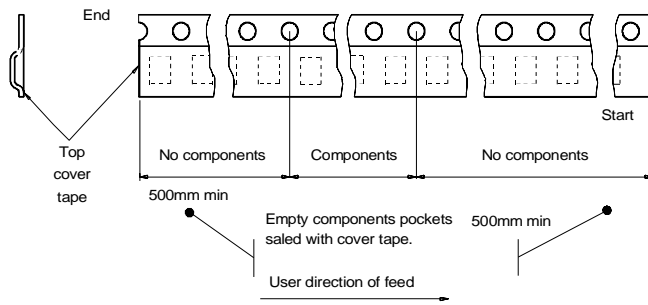
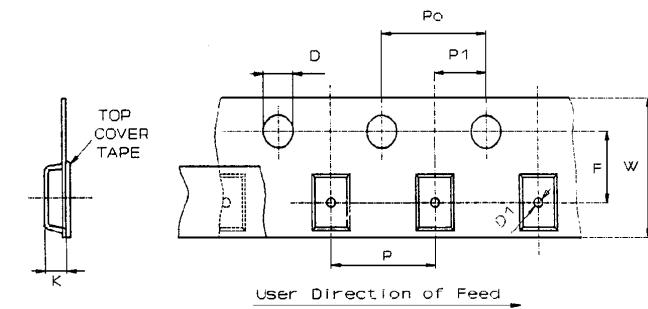
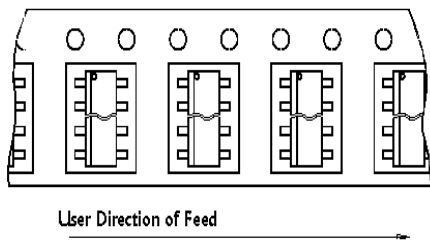
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



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