

## Double channel high-side driver with analog current sense for 24 V automotive applications

Datasheet – production data

### Features

Max transient supply voltage	$V_{CC}$	58 V
Operating voltage range	$V_{CC}$	8 to 36 V
Typ on-state resistance (per ch.)	$R_{ON}$	35 m $\Omega$
Current limitation (typ)	$I_{LIM}$	42 A
Off-state supply current	$I_S$	2 $\mu$ A

- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Fault reset standby pin (FR\_Stby)
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Off-state open load detection
  - Output short to  $V_{CC}$  detection
  - Overload and short to ground latch off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Thermal shutdown
  - Electrostatic discharge protection



### Application

All types of resistive, inductive and capacitive loads

### Description

The VND5T035AK-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature or short to  $V_{CC}$  are reported via the current sense pin.

Output current limitation protects the device in overload conditions. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pins disables all outputs and sets the device in standby mode.

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# 1 Block diagram and pin description

Figure 1. Block diagram

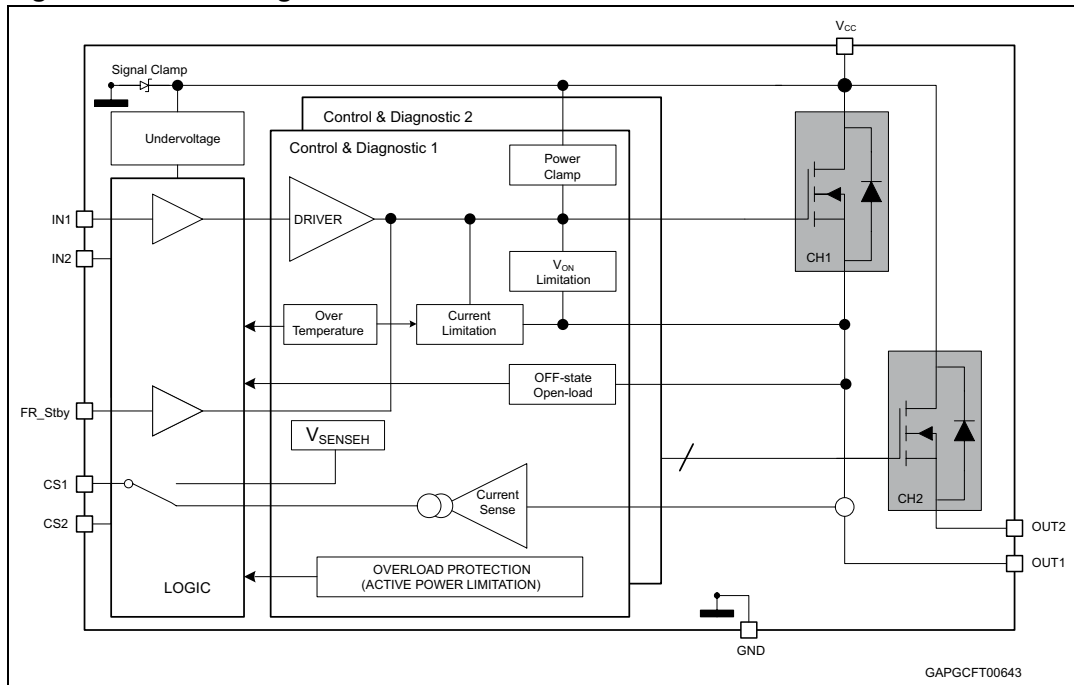


Table 1. Pin function

Name	Function
V <sub>CC</sub>	Battery connection
OUT <sub>1,2</sub>	Power outputs
GND	Ground connection
IN <sub>1,2</sub>	Voltage controlled input pins with hysteresis, CMOS compatible. They Control output switch state
CS <sub>1,2</sub>	Analog current sense pins, they deliver a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram PowerSSO-24 (top view)

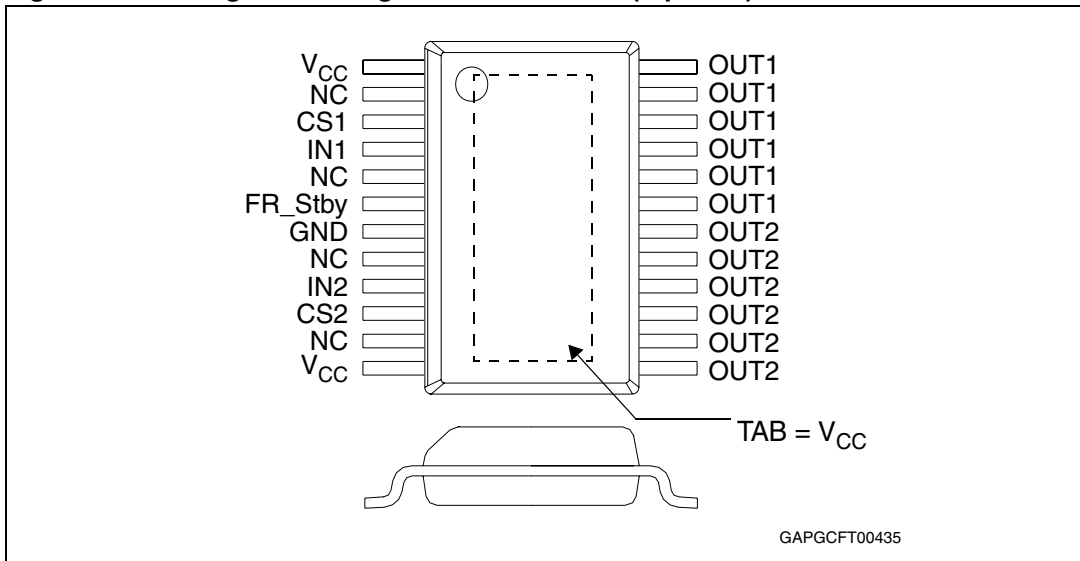


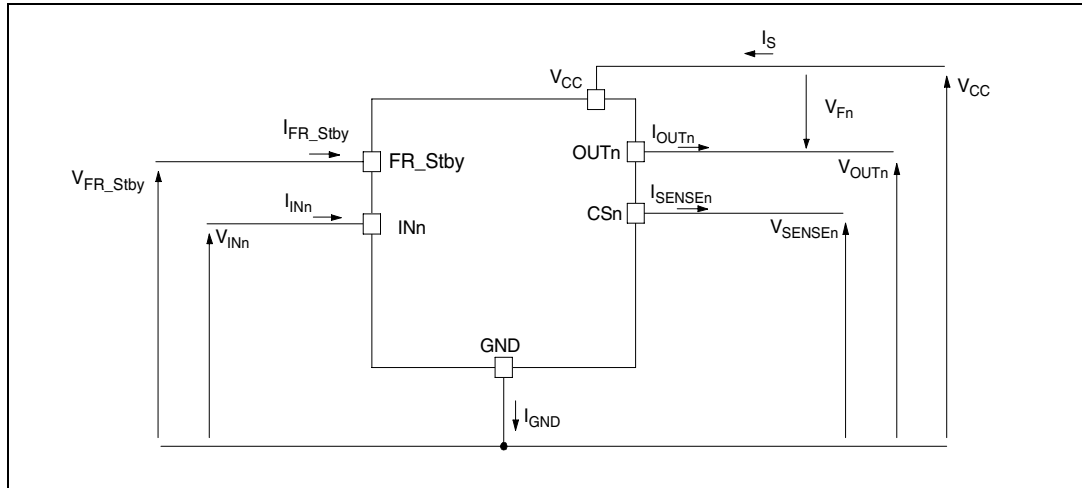
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CurrentSense	N.C.	Output	Input	FR_Stby
Floating	Not allowed	X <sup>(1)</sup>	X	X	X
To ground	Through 10 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ

1. X: do not care.

## 2 Electrical specifications

**Figure 3. Current and voltage conventions**



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	58	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	40	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{FR\_Stby}$	Fault reset standby DC input current	-1 to 1.5	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC} - 58$ to $+V_{CC}$	V
$E_{MAX}$	Maximum switching energy ( $L = 2.3$ mH; $V_{BAT} = 32$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}$ (typ))	250	mJ

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$L_{smax}$	Maximum strain inductance in short circuit condition $R_L = 300\text{ m}\Omega$ , $V_{BAT} = 32\text{ V}$ , $T_{jstart} = 150\text{ }^\circ\text{C}$ , $I_{OUT} = I_{LMHmax}$	40	$\mu\text{H}$
$V_{ESD}$	Electrostatic discharge (Human Body Model: $R = 1.5\text{ K}\Omega$ ; $C = 100\text{ pF}$ )		
	– $IN_{1,2}$	4000	V
	– $CS_{1,2}$	2000	V
	– $FR\_Stby$	4000	V
	– $OUT_{1,2}$	5000	V
	– $V_{CC}$	5000	V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	750	V
$T_j$	Junction operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (max) (with one channel ON)	2	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (max)	See <a href="#">Figure 27</a>	$^\circ\text{C/W}$



## 2.3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$ ;  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise specified.

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		8	24	36	V
$V_{USD}$	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
$R_{ON}$	On-state resistance <sup>(1)</sup>	$I_{OUT} = 3\text{ A}$ ; $T_j = 25\text{ °C}$		35		mΩ
		$I_{OUT} = 3\text{ A}$ ; $T_j = 150\text{ °C}$			70	
$V_{clamp}$	Clamp voltage	$I_S = 20\text{ mA}$	58	64	70	V
$I_S$	Supply current	Off-state; $V_{CC} = 24\text{ V}$ ; $T_j = 25\text{ °C}$ ; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 <sup>(2)</sup>	5 <sup>(2)</sup>	μA
		On-state; $V_{CC} = 24\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$		4.2	6	mA
$I_{L(off)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $T_j = 125\text{ °C}$	0		5	
$V_F$	Output - $V_{CC}$ diode voltage	$-I_{OUT} = 3\text{ A}$ ; $T_j = 150\text{ °C}$			0.7	V

1. For each channel

2. PowerMOS leakage included

**Table 6. Switching ( $V_{CC} = 24\text{ V}$ ;  $T_j = 25\text{ °C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 8\text{ Ω}$		46		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 8\text{ Ω}$		54		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 8\text{ Ω}$		0.55		V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 8\text{ Ω}$		0.46		V/μs
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 8\text{ Ω}$		1		mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 8\text{ Ω}$		0.65		mJ

**Table 7. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
$V_{FR\_Stby\_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR\_Stby\_L}$	Low level fault_reset_standby current	$V_{FR\_Stby} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{FR\_Stby\_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR\_Stby\_H}$	High level fault_reset_standby current	$V_{FR\_Stby} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{FR\_Stby(hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR\_Stby\_CL}$	Fault_reset_standby clamp voltage	$I_{FR\_Stby} = 15\text{ mA (10 ms)}$	11		15	V
		$I_{FR\_Stby} = -1\text{ mA}$		-0.7		V
$t_{reset}$	Overload latch-off reset time	See <a href="#">Figure 4</a>	2		24	$\mu\text{s}$
$t_{stby}$	Standby delay	See <a href="#">Figure 5</a>	120		1200	$\mu\text{s}$

**Figure 4. Treset definition**

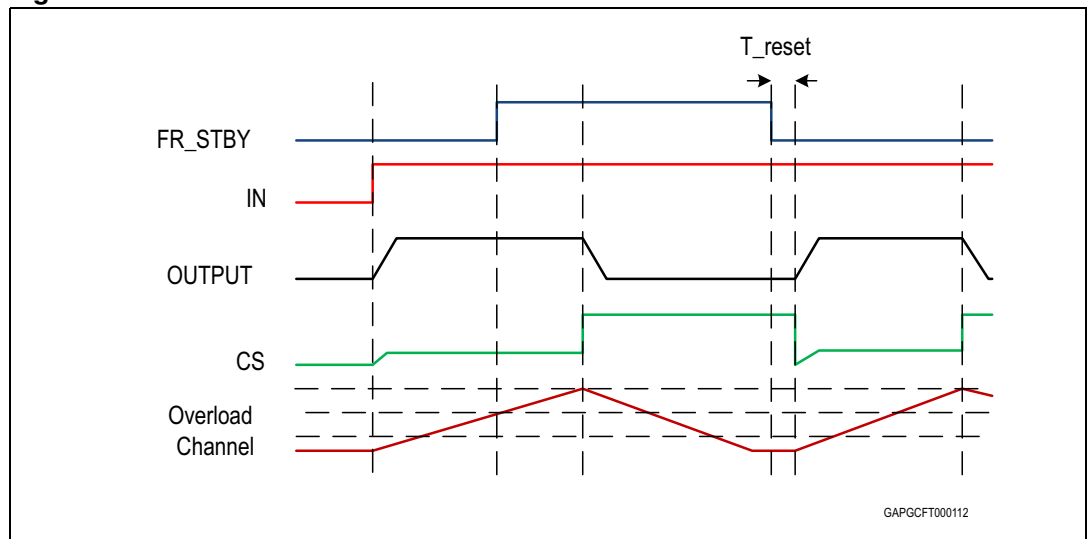


Figure 5. Tstby definition

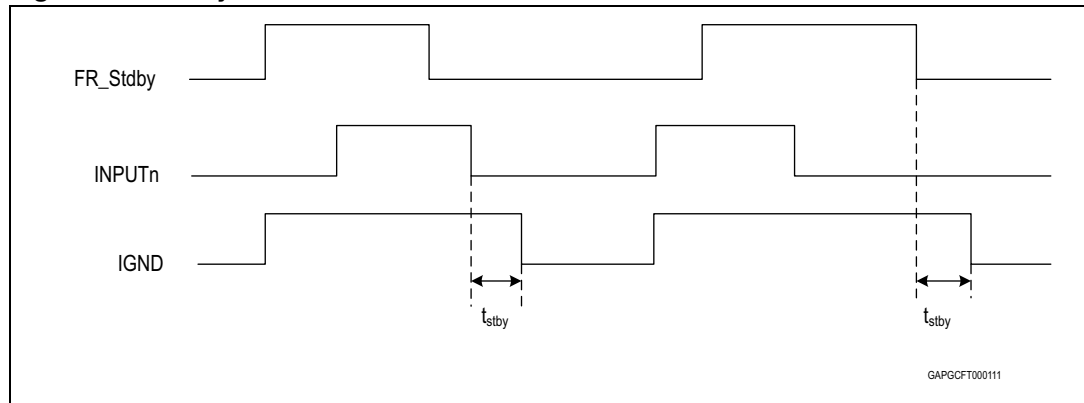


Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short circuit current	$V_{CC} = 24V$	30	42	55	A
		$5 V < V_{CC} < 36 V$			55	A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC} = 24 V; T_R < T_j < T_{TSD}$		10.5		A
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		°C
$T_{RS}$	Thermal reset of status		135			°C
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		°C
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 3 A; V_{IN} = 0; L = 6 mH$	$V_{CC} - 58$	$V_{CC} - 64$	$V_{CC} - 70$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 150 mA; T_j = -40°C...+150°C$		25		mV

Table 9. Current sense ( $8\text{ V} < V_{CC} < 36\text{ V}$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 1\text{ A}; V_{SENSE} = 2\text{ V};$ $T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$ $T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$	1952 2080	2960	4150 3840	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 1\text{ A}; V_{SENSE} = 2\text{ V};$ $T_j = -40^\circ\text{C} \text{ to } 150^\circ\text{C}$	-15		15	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 3\text{ A}; V_{SENSE} = 4\text{ V};$ $T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$ $T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$	2490 2585	2930	3440 3265	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 3\text{ A}; V_{SENSE} = 4\text{ V};$ $T_j = -40^\circ\text{C} \text{ to } 150^\circ\text{C}$	-10		+10	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 12\text{ A}; V_{SENSE} = 4\text{ V};$ $T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$ $T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$	2770 2755	2900	3125 3045	
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 12\text{ A}; V_{SENSE} = 4\text{ V};$ $T_j = -40^\circ\text{C} \text{ to } 150^\circ\text{C}$	-5		5	%
$I_{SENSE0}$	Analog sense leakage current	$I_{OUT} = 0\text{ A}; V_{SENSE} = 0\text{ V};$ $V_{IN} = 0\text{ V}; T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$	0		1	$\mu\text{A}$
		$I_{OUT} = 0\text{ A}; V_{SENSE} = 0\text{ V};$ $V_{IN} = 5\text{ V}; T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$	0		2	$\mu\text{A}$
$V_{SENSE}$	Max analog sense output voltage	$I_{OUT} = 12\text{ A}; R_{SENSE} = 3.9\text{ K}\Omega$	5			V
$V_{SENSEH}$	Analog sense output voltage in fault condition <sup>(2)</sup>	$V_{CC} = 24\text{ V}; R_{SENSE} = 3.9\text{ K}\Omega$	7.5	8.5	9.5	V
$I_{SENSEH}$	Analog sense output current in fault condition <sup>(2)</sup>	$V_{CC} = 24\text{ V}; V_{SENSE} = 5\text{ V}$	4.9	9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pins	$V_{SENSE} < 4\text{ V};$ $0.2\text{ A} < I_{OUT} < 12\text{ A};$ $I_{SENSE} = 90\% \text{ of } I_{SENSE\text{ max}};$ (see <a href="#">Figure 6</a> )		200	400	$\mu\text{s}$
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	$V_{SENSE} < 4\text{ V};$ $I_{SENSE} = 90\% \text{ of } I_{SENSE\text{ MAX}};$ $I_{OUT} = 90\% \text{ of } I_{OUT\text{ MAX}};$ $I_{OUT\text{ MAX}} = 3\text{ A}$ (see <a href="#">Figure 10</a> )			250	$\mu\text{s}$
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pins	$V_{SENSE} < 4\text{ V};$ $0.2\text{ A} < I_{OUT} < 12\text{ A};$ $I_{SENSE} = 10\% \text{ of } I_{SENSE\text{ max}};$ (see <a href="#">Figure 6</a> )		5	20	$\mu\text{s}$

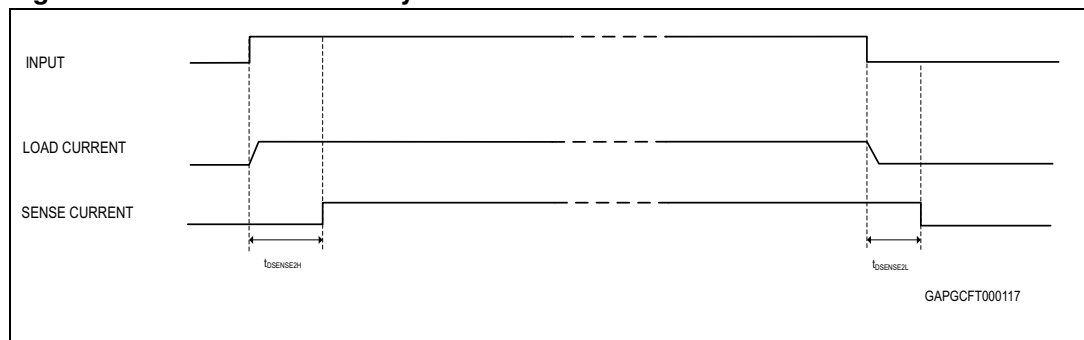
1. Parameter guaranteed by design; it is not tested.

2. Fault condition includes: power limitation, overtemperature and open load in off-state condition.

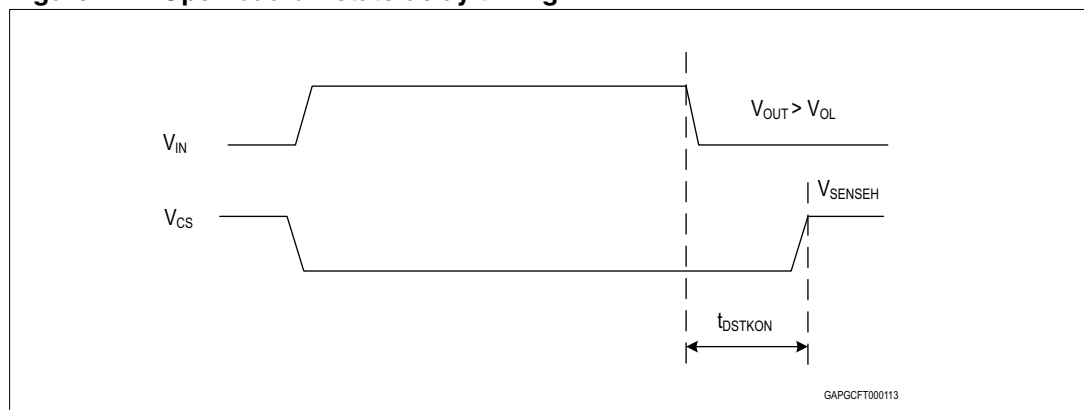
**Table 10. Openload detection ( $V_{FR\_Stby} = 5\text{ V}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OL}$	Openload off-state voltage detection threshold	$V_{IN} = 0\text{ V}; 8\text{ V} < V_{CC} < 36\text{ V}$	2		4	V
$t_{DSTKON}$	Output short circuit to $V_{CC}$ detection delay at turn off	See <a href="#">Figure 7</a>	180		1800	$\mu\text{s}$
$I_{L(off2)}$	Off-state output current at $V_{OUT} = 4\text{ V}$	$V_{IN} = 0\text{ V}; V_{SENSE} = 0\text{ V}; V_{OUT}$ rising from 0 V to 4 V	-120		0	$\mu\text{A}$
$t_{d\_vol}$	Delay response from output rising edge to $V_{SENSE}$ rising edge in openload	$V_{OUT} = 4\text{ V}; V_{IN} = 0\text{ V}; V_{SENSE} = 90\% \text{ of } V_{SENSEH}; R_{SENSE} = 3.9\text{ K}$			20	$\mu\text{s}$
$t_{DFRSTK\_ON}$	Output short circuit to $V_{CC}$ detection delay at FRSTBY activation	See <a href="#">Figure 9</a> ; $\text{Input}_{1,2} = \text{low}$			50	$\mu\text{s}$

**Figure 6. Current sense delay characteristics**

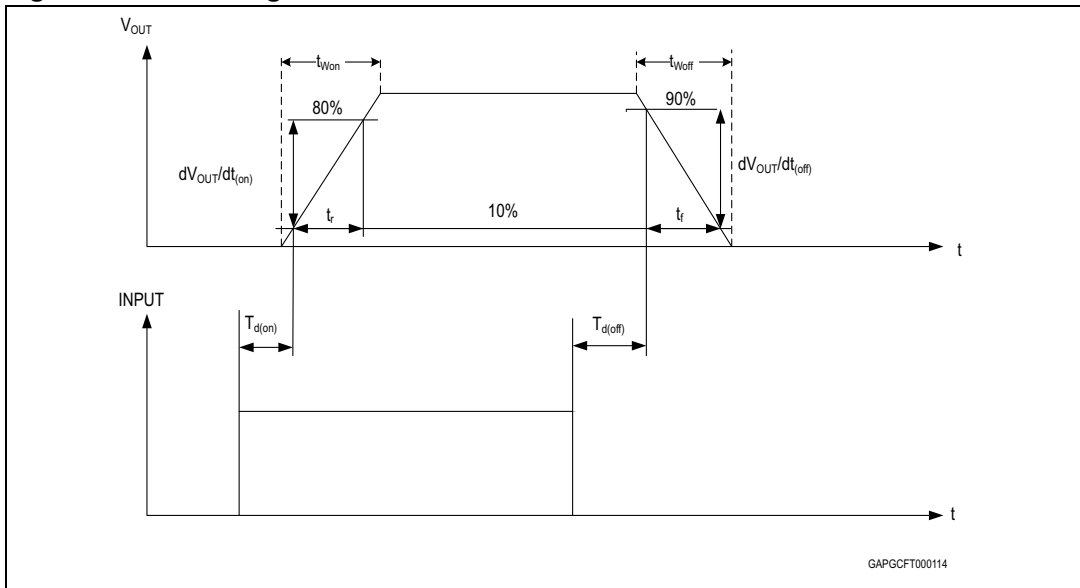


**Figure 7. Openload off-state delay timing**

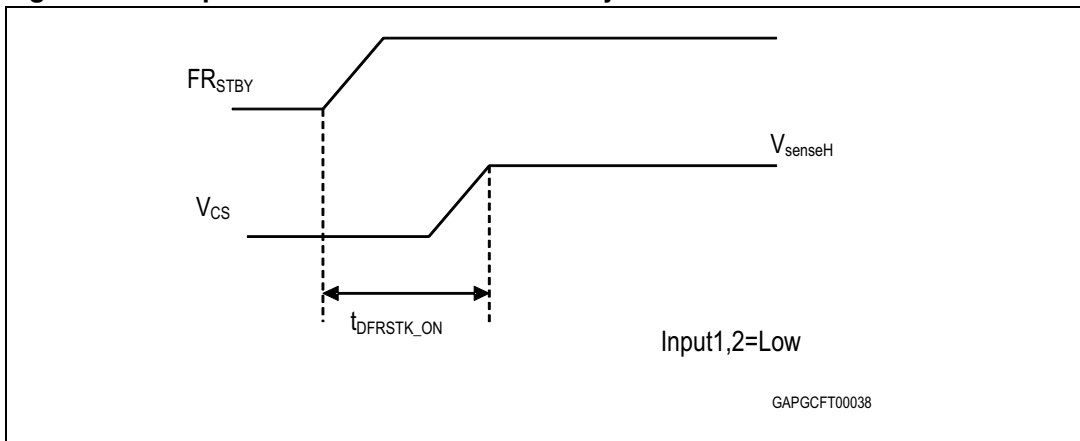


Note:  $V_{fr\_stby} = \text{high}$

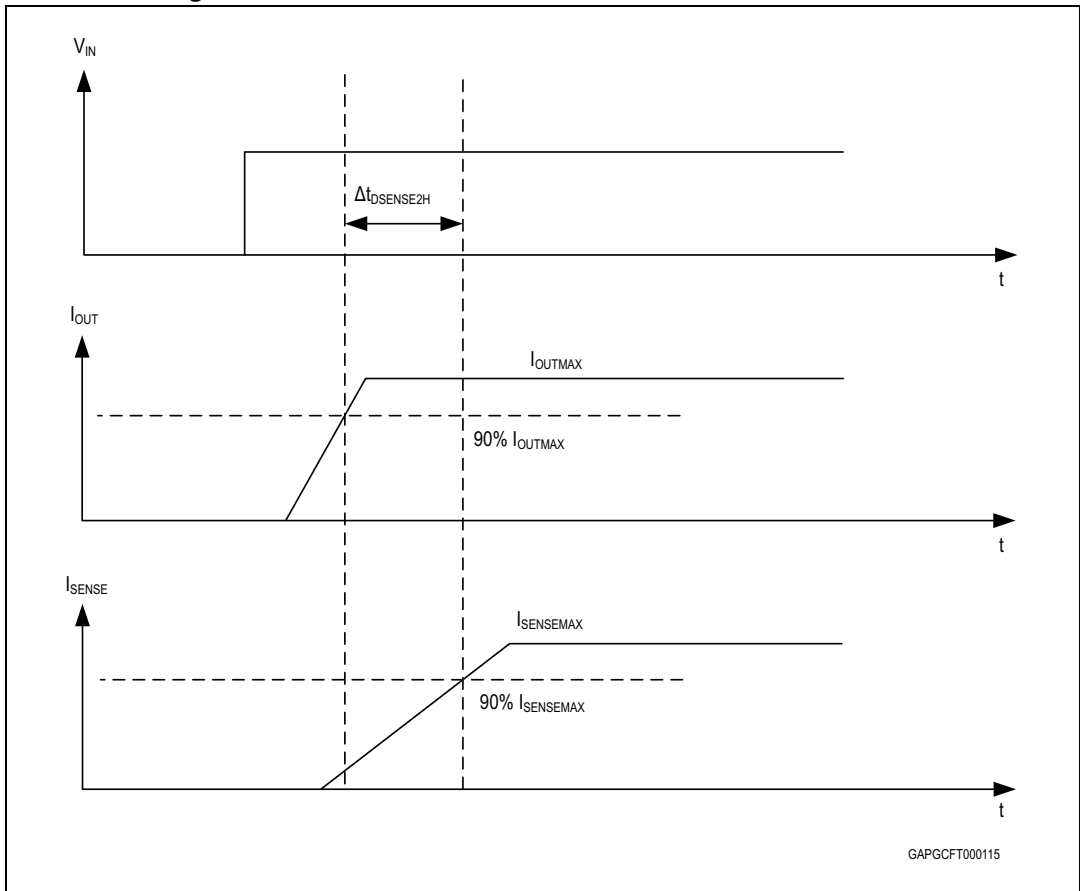
**Figure 8. Switching characteristics**



**Figure 9. Output stuck to VCC detection delay time at FRSTBY activation**



**Figure 10. Delay response time between rising edge of output current and rising edge of current sense**



**Figure 11. Output voltage drop limitation**

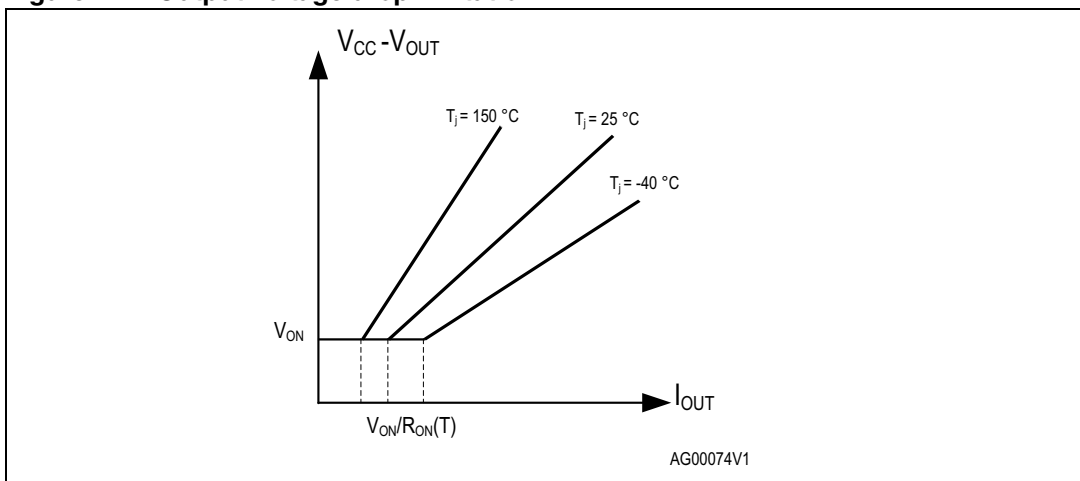


Figure 12. Device behavior in overload condition

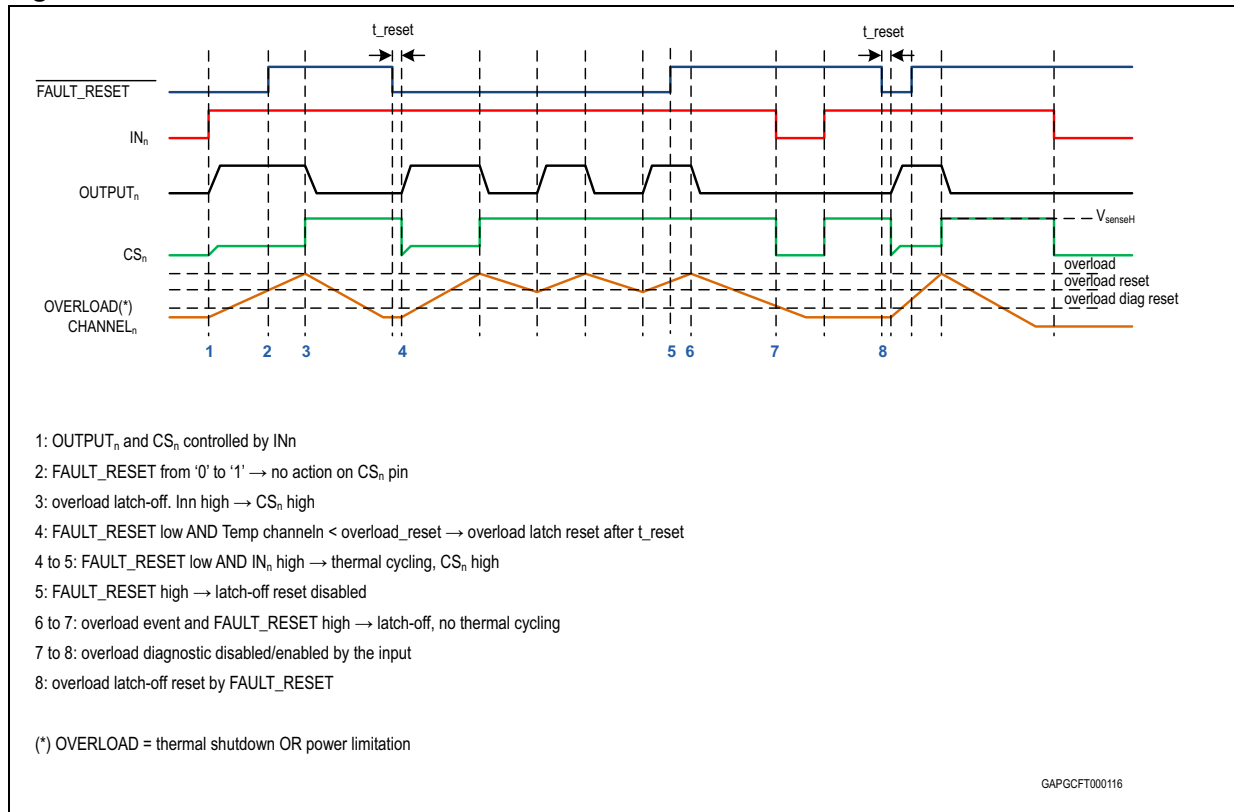


Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature / short to ground	X	L	L	0
	L	H	Cycling	V <sub>SENSEH</sub>
	H	H	Latched	V <sub>SENSEH</sub>
Undervoltage	X	X	L	0
Short to V <sub>BAT</sub>	L	L	H	0
	H X	L H	H H	V <sub>SENSEH</sub> < Nominal
Open load off-state (with pull-up)	L	L	H	0
	H X	L H	H H	V <sub>SENSEH</sub> 0
Negative output voltage clamp	X	L	Negative	0



**Table 12. Electrical transient requirements (part 1)**

ISO 7637-2: 2004(E) Test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	- 450 V	- 600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	+ 37 V	+ 50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	- 150 V	- 200 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+ 150 V	+ 200 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b <sup>(1)</sup>	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

1. Valid in case of external load dump clamp: 58 V maximum referred to ground.

**Table 13. Electrical transient requirements (part 2)<sup>(1)</sup>**

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b <sup>(2)</sup>	E	E
3b <sup>(3)</sup>	C	C
4	C	C
5b <sup>(4)</sup>	C	C

1. In order to guarantee the ISO transient classes a minimum 10KΩ protection resistors are needed on logic pins
2. Without capacitor between V<sub>CC</sub> and GND.
3. With 10 nF between V<sub>CC</sub> and GND.
4. External load dump clamp, 58 V maximum, referred to ground.

**Table 14. Electrical transient requirements (part 3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

## 2.4 Electrical characteristics curves

Figure 13. Off-state output current

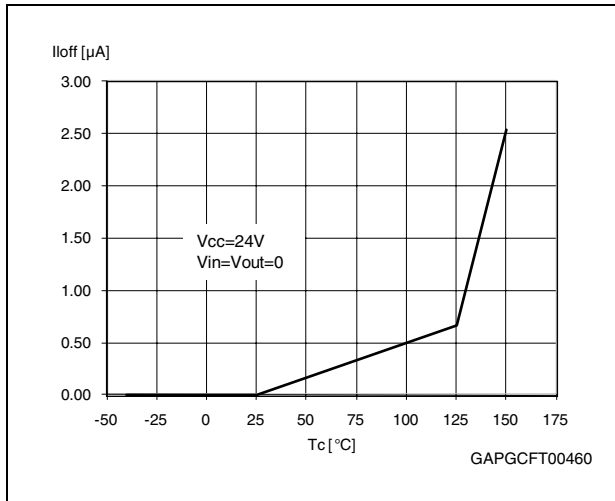


Figure 14. High-level input current

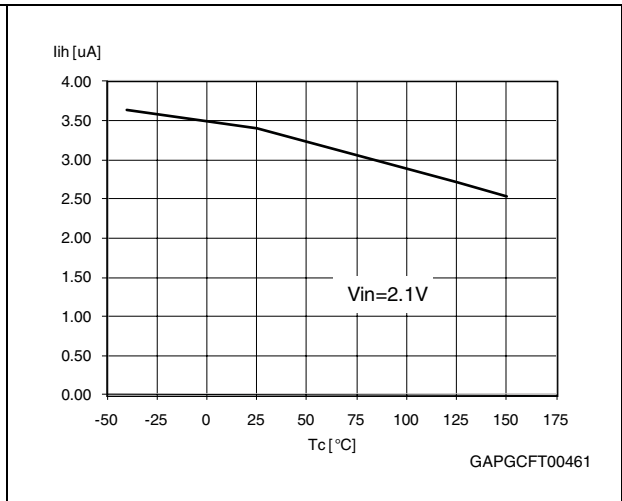


Figure 15. Input clamp voltage

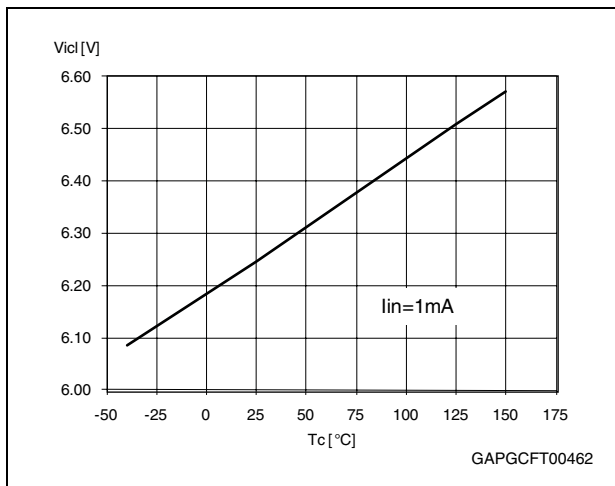


Figure 16. High-level input voltage

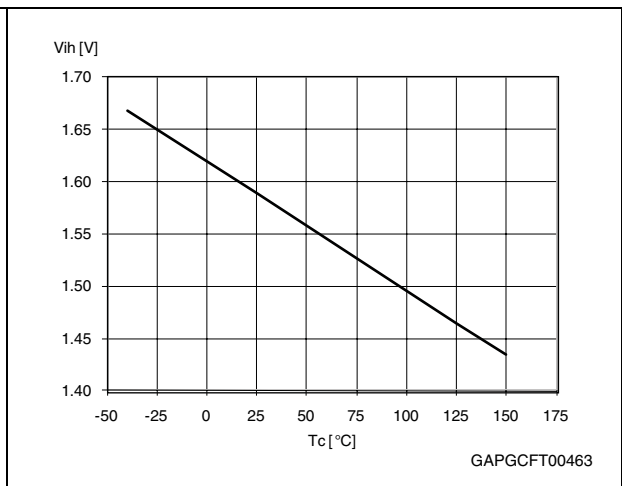


Figure 17. Low-level input voltage

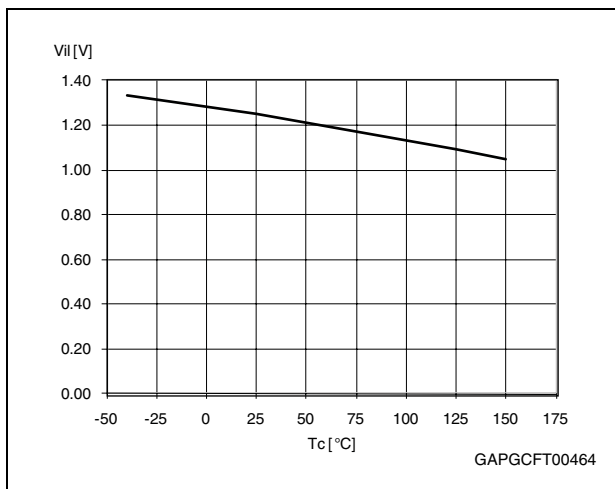


Figure 18. Input hysteresis voltage

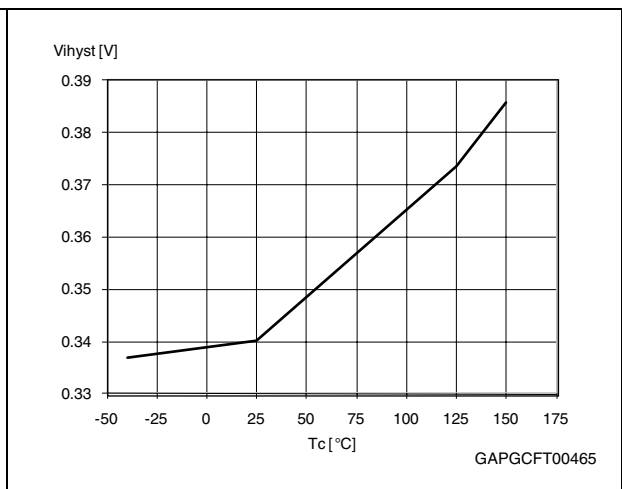


Figure 19. On-state resistance vs  $T_{case}$

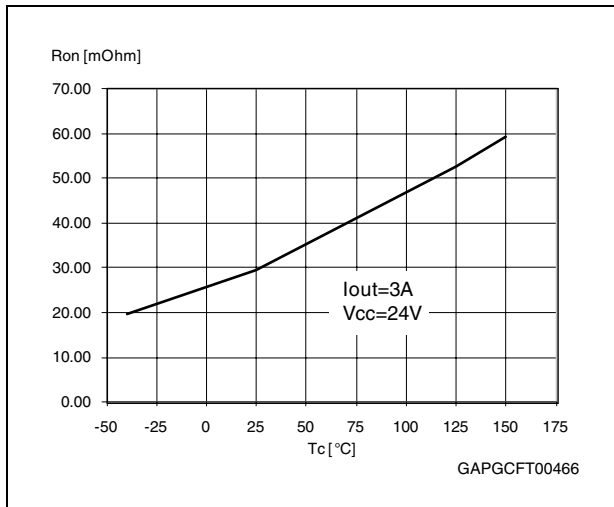


Figure 20. On-state resistance vs  $V_{CC}$

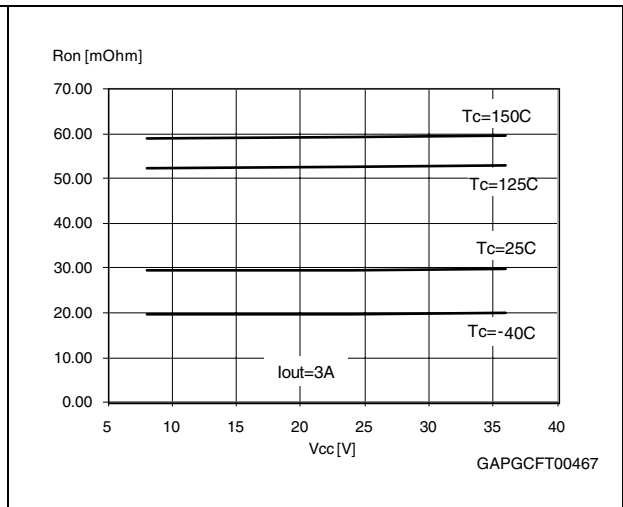


Figure 21.  $I_{LIMH}$  vs  $T_{case}$

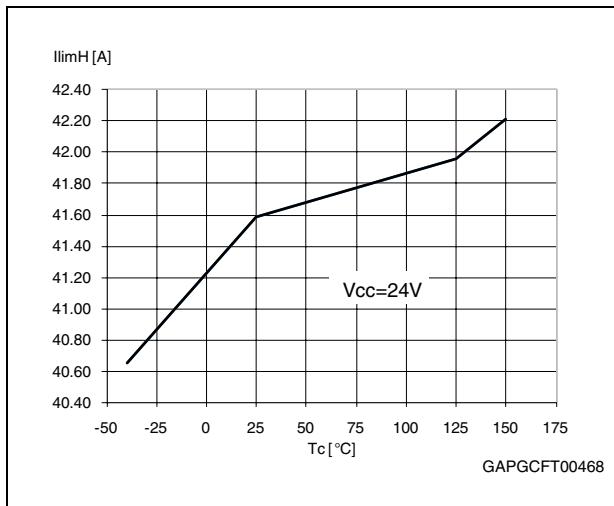


Figure 22. Turn-on voltage slope

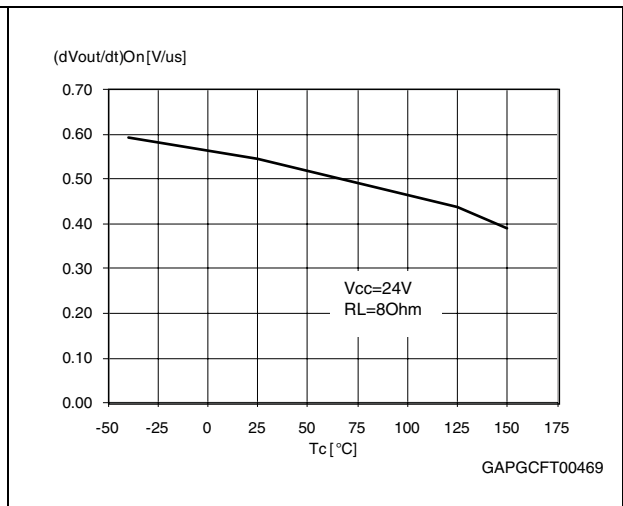
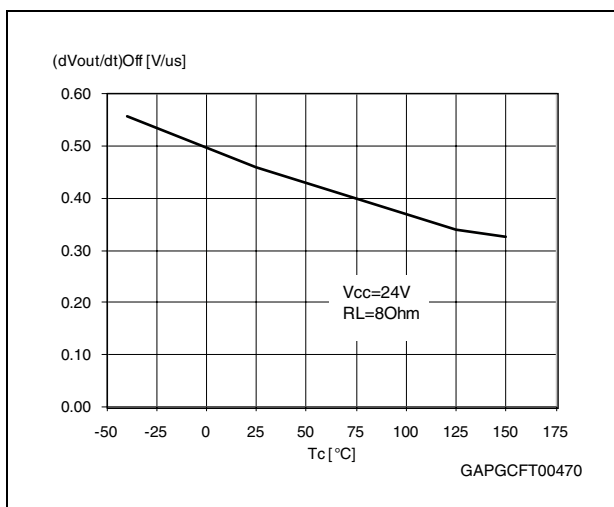


Figure 23. Turn-off voltage slope





### 3.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 4.7 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\approx 600 \text{ mV}$ ) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/2 table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transient is present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests that a resistor ( $R_{prot}$ ) have to be inserted in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

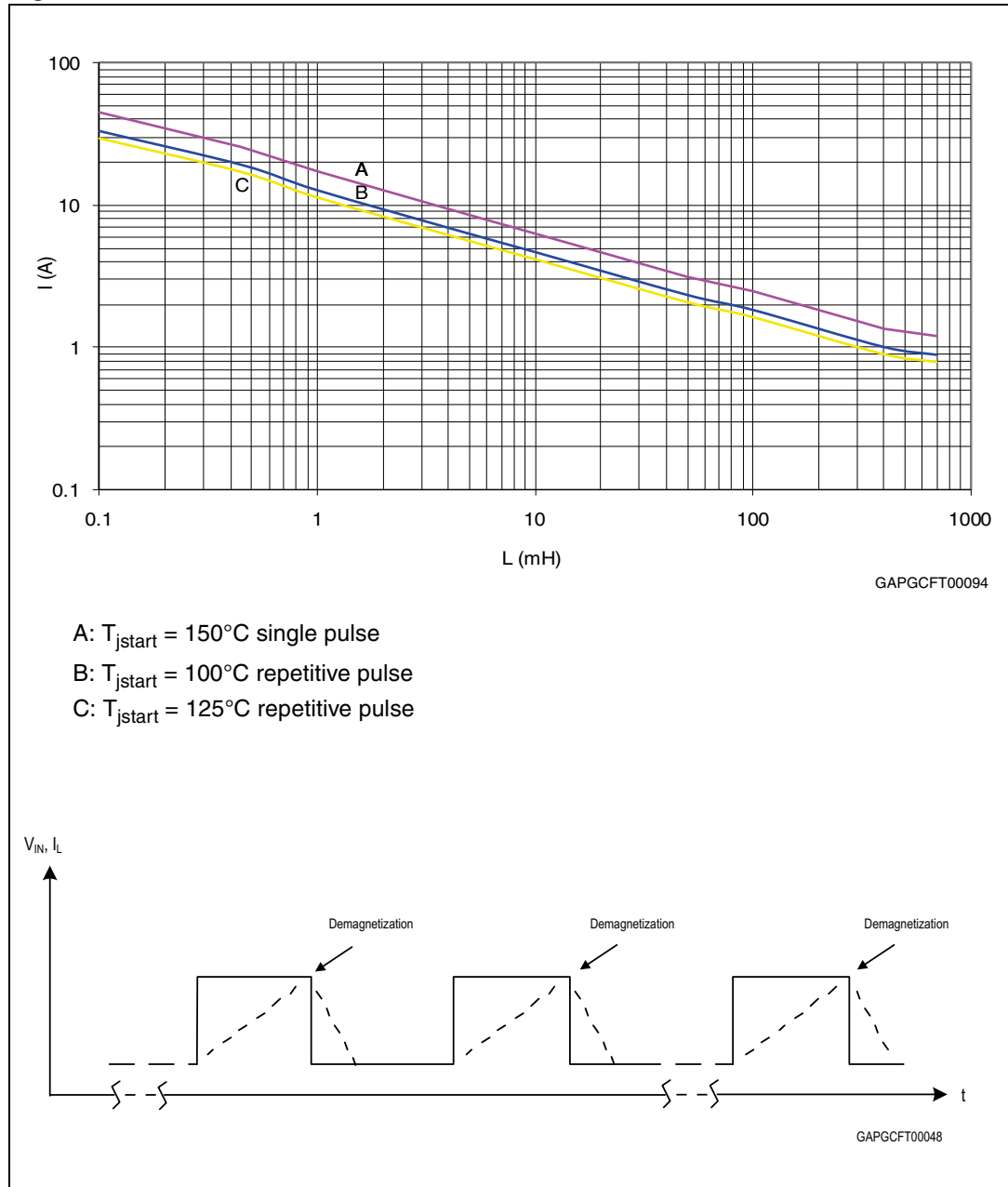
For  $V_{CCpeak} = -600 \text{ V}$  and  $I_{latchup} \geq 20 \text{ mA}$ ;  $V_{OH\mu C} \geq 4.5 \text{ V}$

$$30 \text{ k}\Omega \leq R_{prot} \leq 180 \text{ k}\Omega$$

Recommended  $R_{prot}$  value is  $60 \text{ k}\Omega$ .

### 3.4 Maximum demagnetization energy ( $V_{CC} = 24\text{ V}$ )

Figure 25. Maximum turn-off current versus inductance

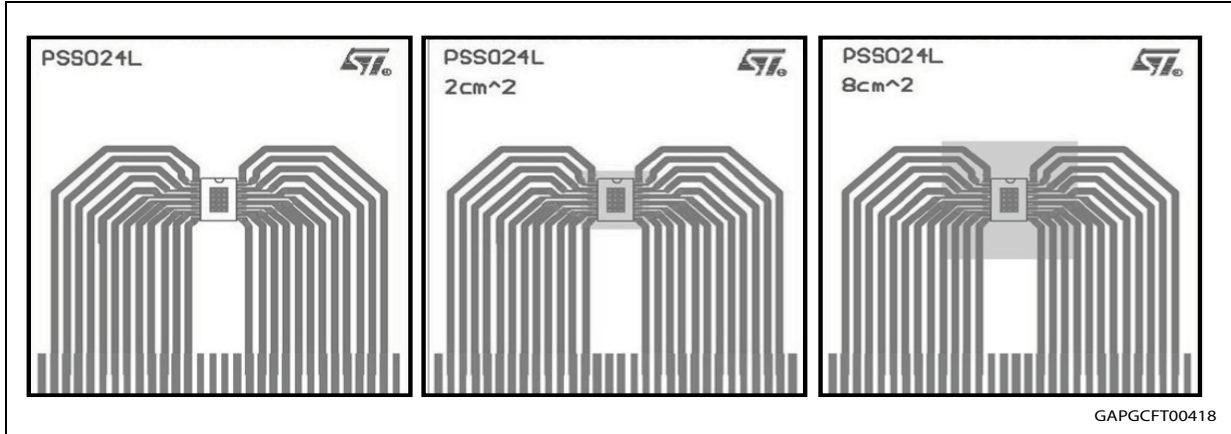


Note: Values are generated with  $R_L = 0\ \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

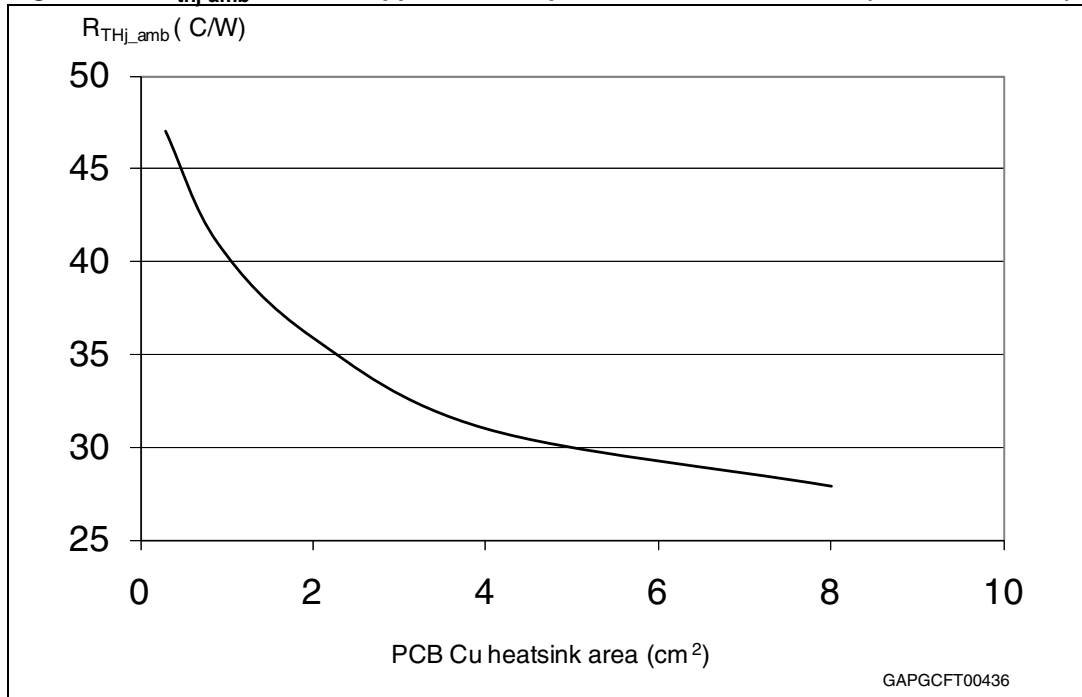
### 4.1 PowerSSO-24 thermal data

Figure 26. PowerSSO-24 PC board

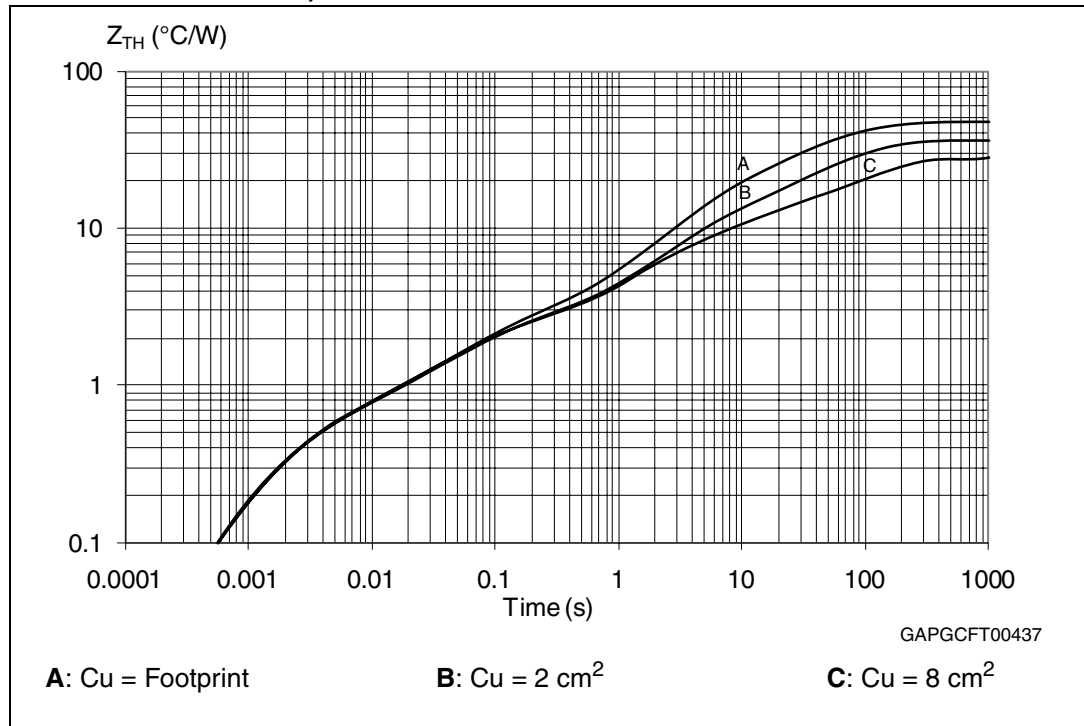


1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

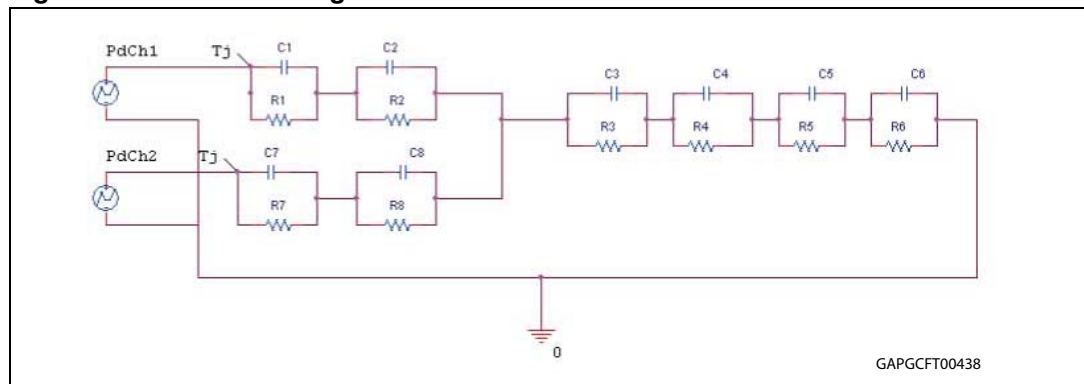
Figure 27.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel ON)



**Figure 28. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)**



**Figure 29. Thermal fitting model of a double channel HSD in PowerSSO-24**



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered



**Equation 1: Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Table 15. Thermal parameters**

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0,5	—	—
R2 (°C/W)	0.75	—	—
R3 (°C/W)	1	—	—
R4 (°C/W)	7.7	—	—
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0,5	—	—
R8 (°C/W)	0.75	—	—
C1 (W.s/°C)	0,005	—	—
C2 (W.s/°C)	0,05	—	—
C3 (W.s/°C)	0,1	—	—
C4 (W.s/°C)	0,5	—	—
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0,005	—	—
C8 (W.s/°C)	0,05	—	—

## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 PowerSSO-24 package information

Figure 30. PowerSSO-24 package dimensions

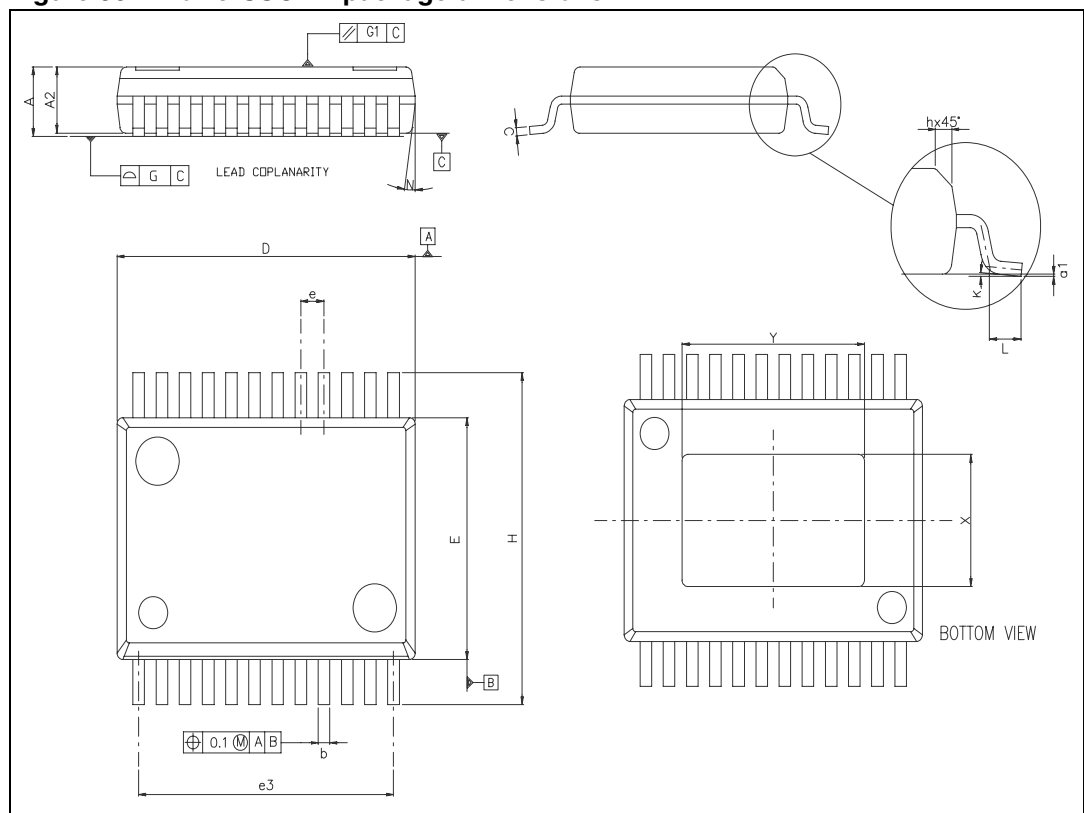


Table 16. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k		5°	
L	0.55		0.85
N			10°
X	4.1		4.7
Y	6.5		7.1

### 5.3 PowerSSO-24 packing information

Figure 31. PowerSSO-24 tube shipment (no suffix)

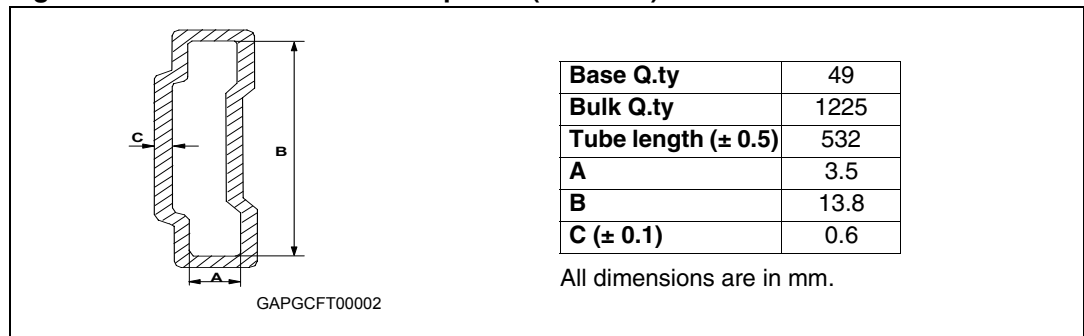
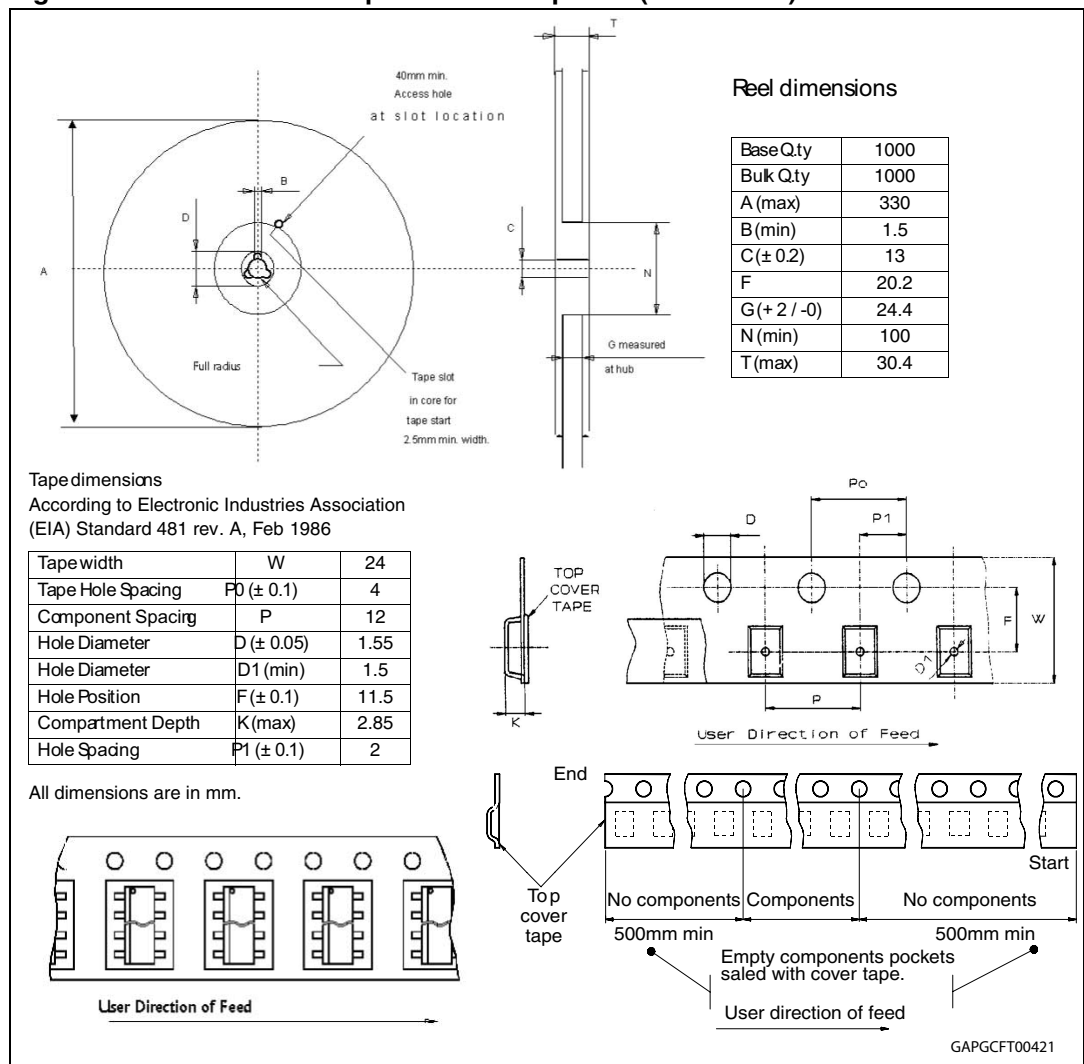


Figure 32. PowerSSO-24 tape and reel shipment (suffix "TR")



## 6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VND5T035AK-E	VND5T035AKTR-E

## 7 Revision history

**Table 18. Document revision history**

Date	Revision	Changes
21-Sep-2011	1	Initial release.
19-Oct-2011	2	Updated <a href="#">Table 2: Suggested connections for unused and not connected pins</a> Added note on <a href="#">Table 13: Electrical transient requirements (part 2)</a>
26-Oct-2011	3	Changed document status from preliminary data to definitive datasheet
13-Mar-2012	4	Updated <a href="#">Figure 13: Off-state output current</a> Updated <a href="#">Section 3.4: Maximum demagnetization energy (<math>V_{CC} = 24\text{ V}</math>)</a>

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