

SINGLE CHANNEL HIGH SIDE SOLID STATE RELAY

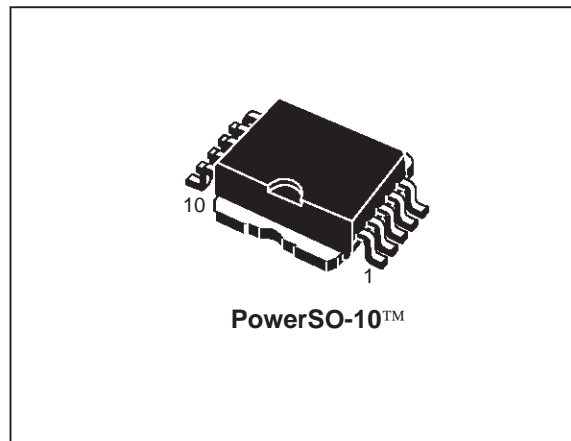
TARGET SPECIFICATION

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN610SP	10m Ω	45A	36 V

- OUTPUT CURRENT: 45 A
- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
 - LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)

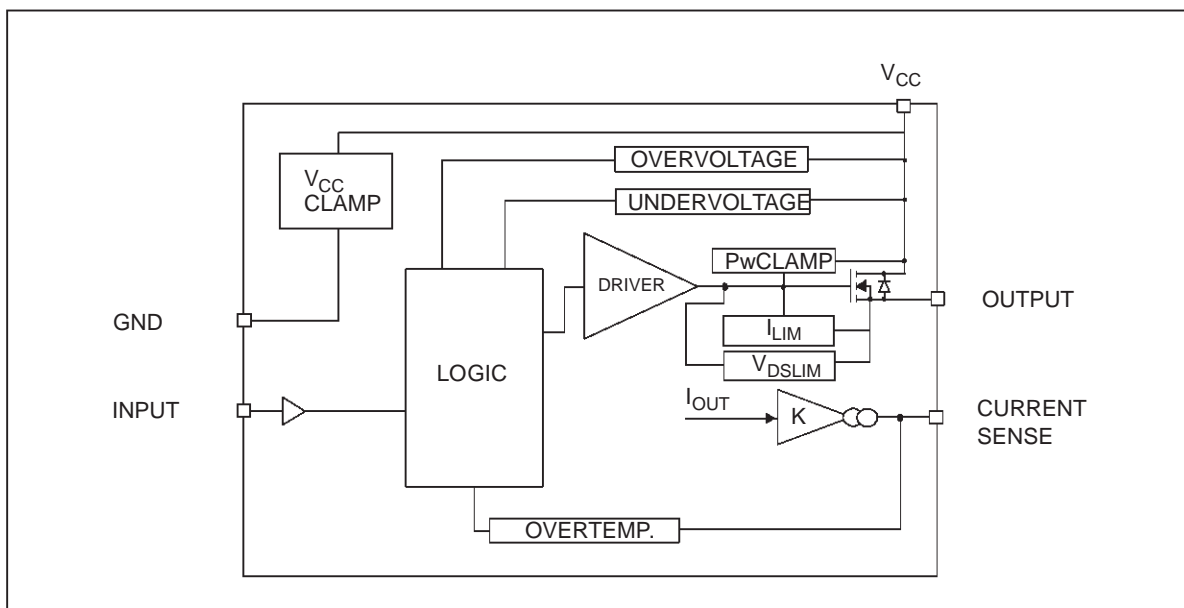
DESCRIPTION

The VN610SP is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin



voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio). Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM

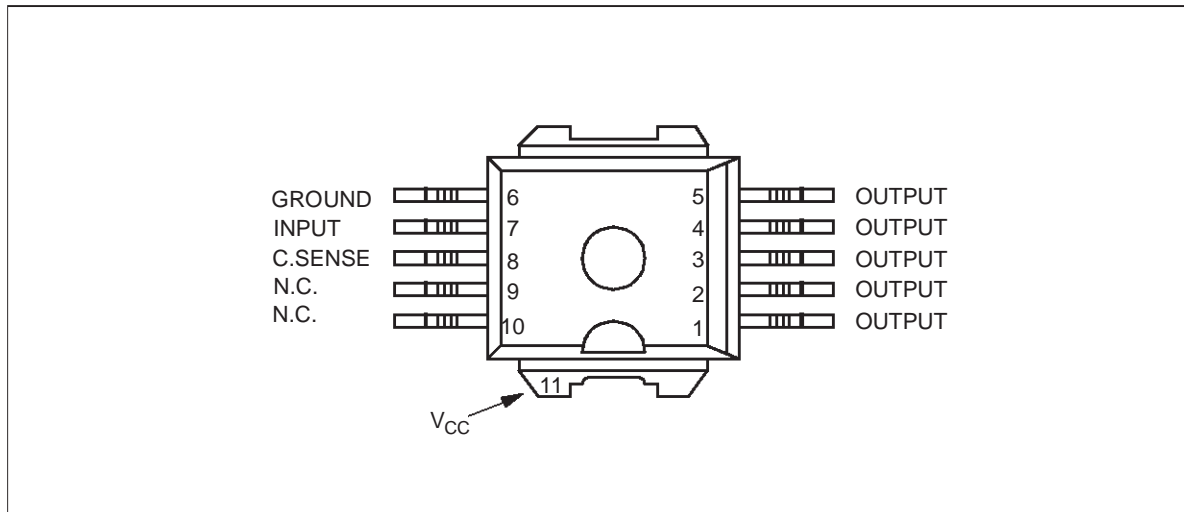


(*) See application schematic at page 8

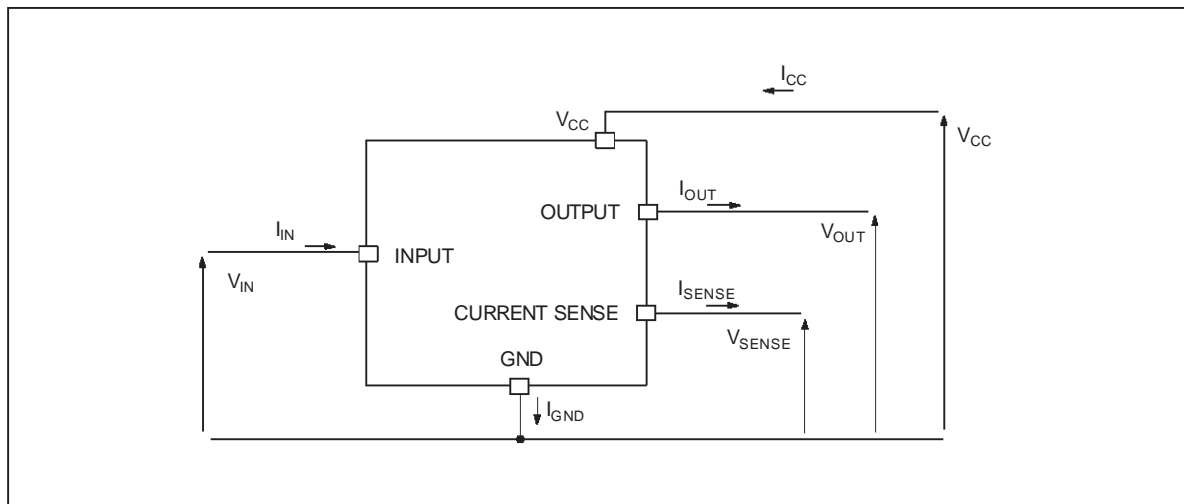
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-50	A
I_{IN}	DC input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3	V
		+15	V
V_{ESD}	Electrostatic discharge (R=1.5kΩ; C=100pF)	2000	V
P_{TOT}	Power dissipation at $T_C \leq 25^\circ C$	125	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	50	°C/W

ELECTRICAL CHARACTERISTICS (8V< V_{CC} <36V; -40°C< T_j <150°C; unless otherwise specified)
POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown	(See Note 1)	36	42	48	V
R_{ON}	On state resistance	$I_{OUT}=15A$; $T_j=25^\circ C$ $I_{OUT}=15A$; $T_j=150^\circ C$ $I_{OUT}=9A$; $V_{CC}=6V$			10 20 35	mΩ
V_{clamp}	Clamp Voltage	$I_{CC}=20\text{ mA}$ (see note 1)	41	48	55	V
I_S	Supply current	Off state; INPUT= n.c.; $V_{CC}=13V$ On state; $V_{IN}=5V$; $V_{CC}=13V$; $I_{OUT}=0A$; $R_{SENSE}=3.9K$			25 5	μA mA
$I_{L(off)}$	Off state output current	$V_{IN}=V_{OUT}=0V$	0		50	μA

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

SWITCHING ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R1=0.87\Omega$		50		μs
$t_{d(off)}$	Turn-off delay time	$R1=0.87\Omega$		50		μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R1=0.87\Omega$		0.3		V/μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R1=0.87\Omega$		0.3		V/μs
W_{ON}	Switching losses energy at turn-on	$R1=2.6\Omega$		1.0		mJ
W_{OFF}	Switching losses energy at turn-off	$R1=2.6\Omega$		0.5		mJ

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	DC Short circuit current	$V_{CC}=13V$ $5.5V < V_{CC} < 36V$	45	75	120 120	A A
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT}=2A$; $V_{IN}=0$; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
V_{ON}	Output voltage drop limitation	$I_{OUT}=1.5A$ $T_j = -40^\circ C \dots +150^\circ C$		50		mV

ELECTRICAL CHARACTERISTICS (continued)

CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See Fig.1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT}=1.5A$; $V_{SENSE}=0.5V$; $T_j = -40^{\circ}C \dots 150^{\circ}C$	3300	4400	6000	
K_2	I_{OUT}/I_{SENSE}	$I_{OUT}=15A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	4200 4400	4900 4900	6000 5750	
K_3	I_{OUT}/I_{SENSE}	$I_{OUT}=45A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	4200 4400	4900 4900	5500 5250	
V_{SENSE}	Max analog sense output voltage	$V_{CC}=5V$; $I_{OUT}=7.5A$; $R_{SENSE}=10K\Omega$	2			V
		$V_{CC} > 8V$; $I_{OUT}=15A$; $R_{SENSE}=10K\Omega$	4			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{CC}=13V$; $R_{SENSE}=3.9K\Omega$		5.5		V

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$	6.5	7.4	8.5	V
		$I_{IN}=-1mA$		-0.7		V

TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	0
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

SWITCHING CHARACTERISTICS

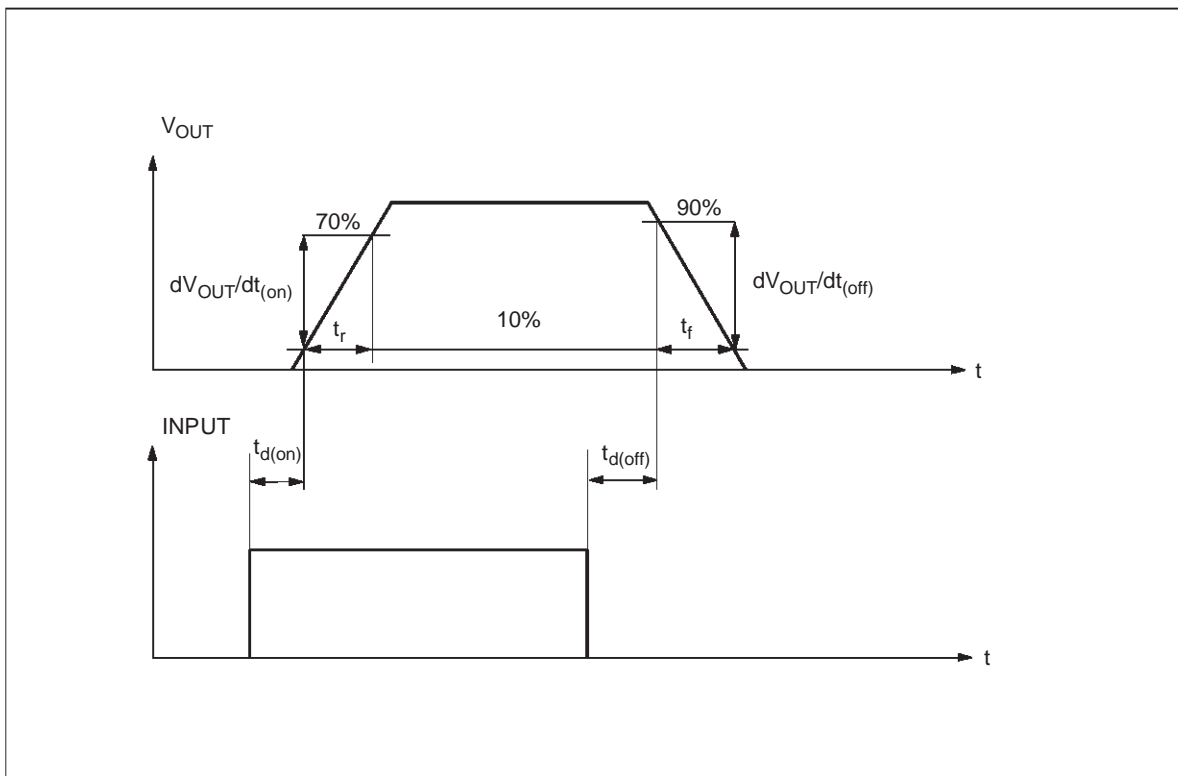


Fig 1: I_{OUT}/I_{SENSE} versus I_{OUT}

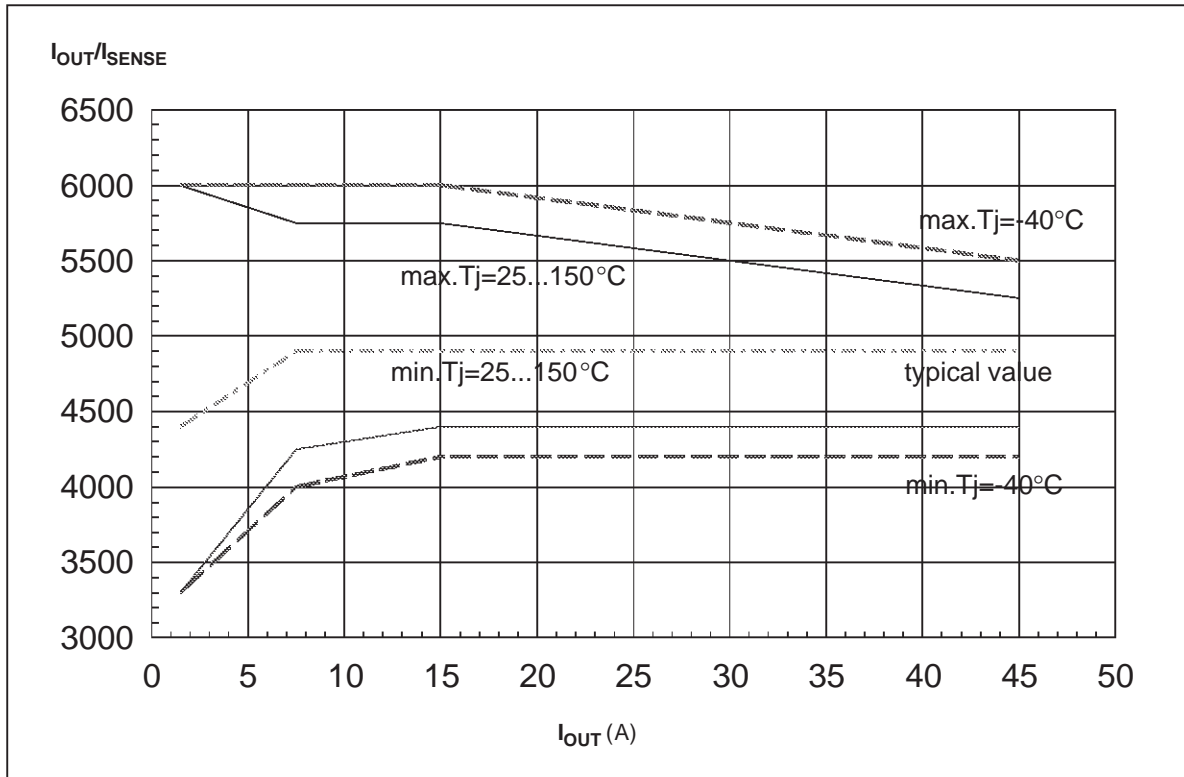
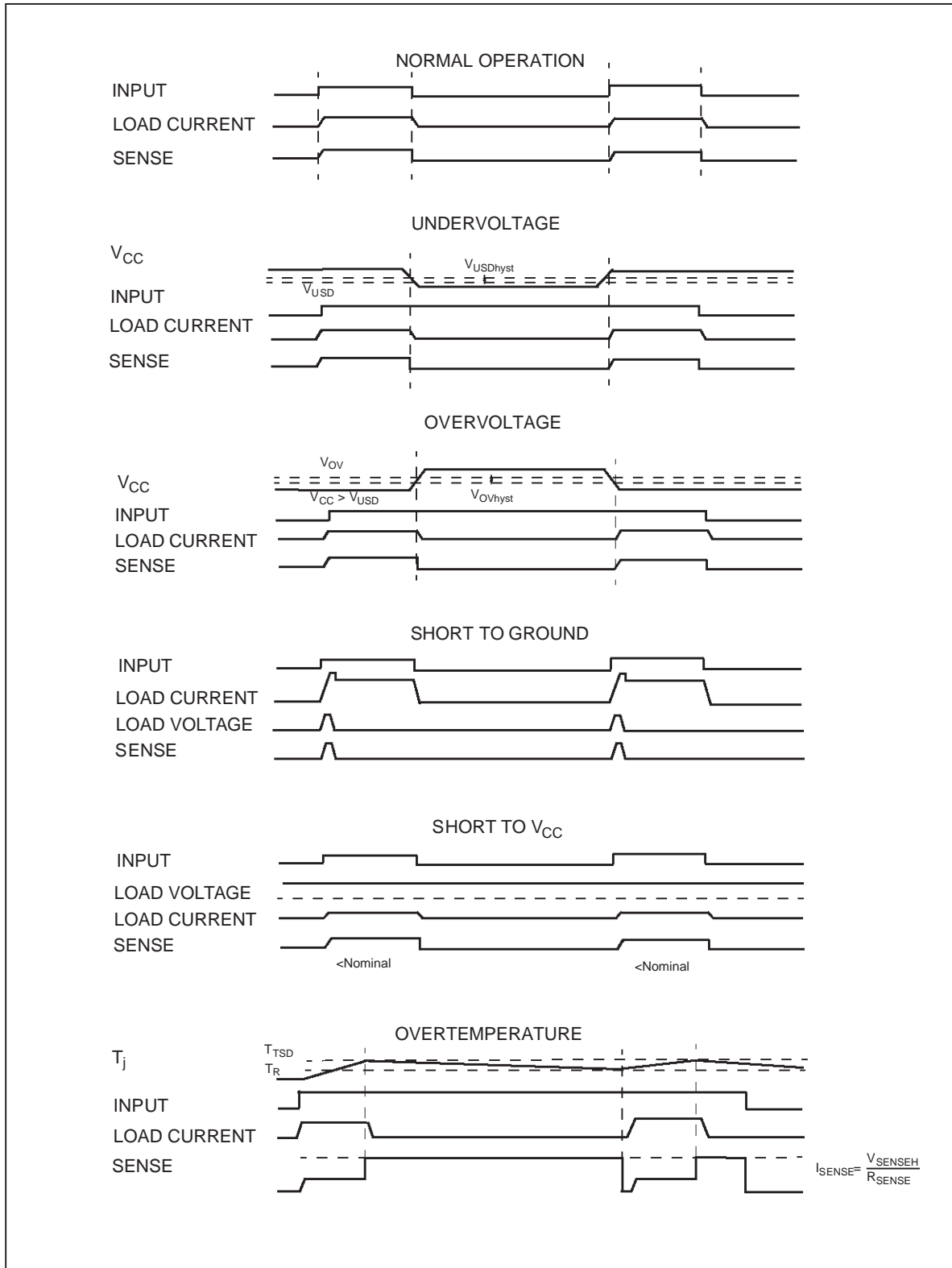
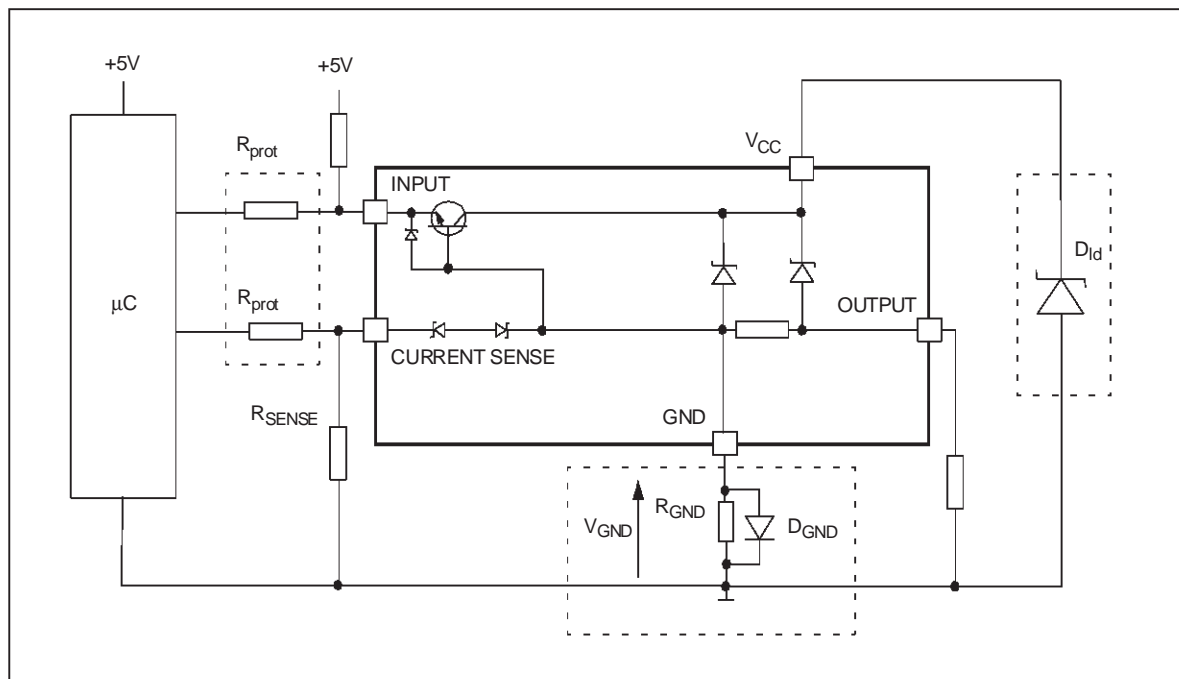


Figure1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{Id} is necessary (Transil or MOV) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

 μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 10\text{k}\Omega$.

Recommended R_{prot} value is 65k Ω .

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