Burr-Brown Products
from Texas Instruments

VCA810

SBOS275C − JUNE 2003 − REVISED OCTOBER 2004

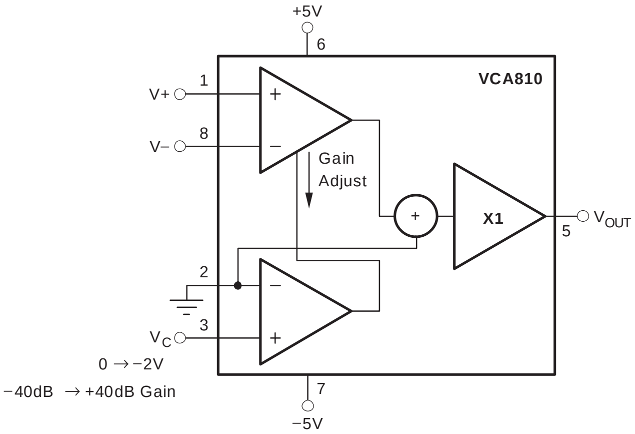
High Gain Adjust Range, Wideband, Voltage-Controlled Amplifier

FEATURES

- **HIGH GAIN ADJUST RANGE: ±40dB**
- **DIFFERENTIAL IN/SINGLE-ENDED OUT**
- **LOW INPUT NOISE VOLTAGE: 2.4nV/$\sqrt{Hz}$**
- **CONSTANT BANDWIDTH vs GAIN: 35MHz**
- **HIGH dB/V GAIN LINEARITY: ±0.3dB**
- **GAIN CONTROL BANDWIDTH: 25MHz**
- **LOW OUTPUT DC ERROR: < ±40mV**
- **HIGH OUTPUT CURRENT: ±60mA**
- **LOW SUPPLY CURRENT: 24.8mA (max for −40°C to +85°C temperature range)**

APPLICATIONS

- **OPTICAL RECEIVER TIME GAIN CONTROL**
- **SONAR SYSTEMS**
- **VOLTAGE-TUNABLE ACTIVE FILTERS**
- **LOG AMPLIFIER**
- **PULSE AMPLITUDE COMPENSATION**
- **AGC RECEIVER WITH RSSI**
- **IMPROVED REPLACEMENT FOR THE VCA610**



DESCRIPTION

The VCA810 is a DC-coupled, wideband, continuously variable, voltage-controlled gain amplifier. It provides a differential input to single-ended output conversion with a high-impedance gain control input used to vary the gain over a –40dB to +40dB range linear in dB/V.

Operating from ±5V supplies, the gain control voltage for the VCA810 will adjust the gain from –40dB at 0V input to +40dB at –2V input. Increasing the control voltage above ground will attenuate the signal path to > 80dB. Signal bandwidth and slew rate remain constant over the entire gain adjust range. This 40dB/V gain control is accurate within ±1.5dB (±0.9dB for High Grade), allowing the gain control voltage in an AGC application to be used as a Received Signal Strength Indicator (RSSI) with ±1.5dB accuracy.

Excellent common-mode rejection and common-mode input range at the two high-impedance inputs allow the VCA810 to provide a differential receiver operation with gain adjust. The output signal is referenced to ground. Zero differential input voltage gives a 0V output with a small DC offset error. Low input noise voltage ensures good output SNR at the highest gain settings.

In applications where pulse edge information is critical, and the VCA810 is being used to equalize varying channel loss, minimal change in group delay over gain setting will retain excellent pulse edge information.

An improved output stage provides adequate output current to drive the most demanding loads. While principally intended to drive analog-to-digital converters (ADCs) or 2nd-stage amplifiers, the ±60mA output current will easily drive doubly-terminated 50Ω lines or a passive post filter stage over the ±1.7V output voltage range.

VCA810 RELATED PRODUCTS

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/$\sqrt{Hz}$)	SIGNAL BANDWIDTH (MHz)
VCA811	—	80	2.4	80
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2614	45	3.6	40
—	VCA2616	45	3.3	40
—	VCA2618	45	5.5	30

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ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Analysis Section
Differential Input Voltage	±V_S
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D	−40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+150°C
ESD Rating (Human Body Model)	2000V
(Charge Device Model)	1500V
(Machine Model)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

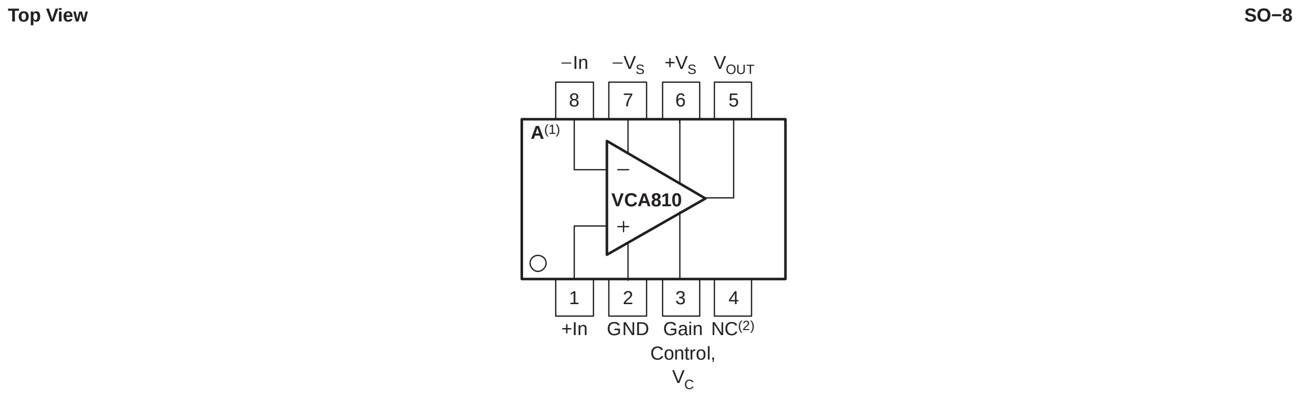
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA810ID	SO−8	D	−40°C to +85°C	VCA810	VCA810ID	Rails, 100
					VCA810IDR	Tape and Reel, 2500
VCA810AID	SO−8	D	−40°C to +85°C	VCA810A[2]	VCA810AID	Rails, 100
					VCA810AIDR	Tape and Reel, 2500

(1) For the most current specification and package information, see the Package Option Addendum located at the end of this data sheet.
(2) The ***A*** indicating high grade will appear opposite the pin 1 marking indicator.

PIN CONFIGURATION



NOTES: (1) High Grade Indicator. (2) NC = Not Connected.

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C**.

R_L = 500Ω, and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

PARAMETER	CONDITIONS	VCA810ID						TEST LEVELS(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	+0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	$-2V \le V_C \le 0$	35	30	29	29	MHz	min	B
Large-Signal Bandwidth	$V_O = 2V_{PP}$, $-2 \le V_C \le -1$	35	30	29	29	MHz	min	B
Frequency Response Peaking	$V_O < 500mV_{PP}$, $-2 \le V_C \le 0$	0.1	0.5	0.5	0.5	dB	min	B
Slew Rate	V_O = 3.5V Step, $-2 \le V_C \le -1$, 10%−90%	350	300	300	295	V/µs	min	B
Settling Time to 0.1%	V_O = 1V Step, $-2 \le V_C \le -1$	30	40	41	41	ns	min	B
Rise-and-Fall Time	V_O = 1V Step, $-2 \le V_C \le -1$	10	12	12.1	12.1	ns	min	B
Group Delay	G=0dB, V_C=−1V, f = 5MHz, $V_O = 500mV_{PP}$	6.2				ns	typ	C
Group Delay Variation	$V_O < 500mV_{PP}$, $-2 \le V_C \le 0$, f = 5MHz	3.5				ns	typ	C
Harmonic Distortion								
2nd-Harmonic	$V_O = 1V_{PP}$, f = 1MHz, V_C = −1V, G = 0dB	−71	−51	−50	−49	dBc	min	B
3rd-Harmonic	$V_O = 1V_{PP}$, f = 1MHz, V_C = −1V, G = 0dB	−35	−34	−32	−29	dBc	min	B
Input Voltage Noise	V_C = −2V	2.4	2.8	3.4	3.5	$nV/\sqrt{Hz}$	max	B
Input Current Noise	$-2V \le V_C \le 0V$	1.4	1.8	2.0	2.1	$pA/\sqrt{Hz}$	max	B
Fully Attenuated Feedthrough	f ≤ 1MHz, V_C > +200mV	−80	−70			dB	max	B
Overdrive Recovery	V_{IN} = 2V to 0V, V_C = −2V, G = 40dB	100	150			ns	min	B
DC PERFORMANCE	Single-Ended or Differential Input							
Output Offset Voltage(4) (both inputs grounded)	$-2V \le V_C \le 0V$	±4	**±22**	±30	±32	mV	max	A
Output Offset Voltage Drift				±125	±125	V/°C	max	B
Input Offset Voltage(4)	Both Inputs Grounded	±0.1	**±0.25**	±0.30	±0.35	mV	max	A
Input Offset Voltage Drift				±1	±1.2	µV/°C	max	B
Input Bias Current	$-2V \le V_C \le 0V$	−6	**−10**	−12	−14	µA	max	A
Input Bias Current Drift				±25	±30	nA/°C	max	B
Input Offset Current	$-2V \le V_C \le 0V$	±100	**±600**	±700	±800	nA	max	A
Input Offset Current Drift				±1.4	±2.2	nA/°C	max	B
INPUT								
Common-Mode Input Range		±2.4	**±2.3**	±2.3	±2.2	V	min	A
Common-Mode Rejection Ratio	V_{CM} = 0.5V, V_C = −2V, Input Referred	95	**85**	83	80	dB	min	A
Input Impedance	V_{CM} = 0V, Single-Ended	1 || 1				MΩ||pF	typ	C
	V_{CM} = 0V, Differential	>10||<2				kΩ||pF	typ	C
Differential Input Range(5)	V_C = 0V, V_{CM} = 0V	3				V_{PP}	typ	C
OUTPUT								
Voltage Output Swing	V_C = −2V, $R_L \ge 500\Omega$	±1.8	**±1.7**	±1.4	±1.3	V	min	A
	V_C = −2V, $R_L = 100\Omega$	±1.7	**±1.6**	±1.3	±1.2	V	min	A
Output Current	V_O = 0V	±60	**±40**	±35	±32	mA	min	A
Output Short-Circuit Current	V_O = 0V	±120				mA	typ	C
Output Impedance	V_O = 0V, f < 100kHz	0.2				Ω	typ	C
GAIN CONTROL (V_C, Pin 3)	Single-Ended or Differential Input							
Specified Gain Range	$\Delta V_C/\Delta dB$ = 25mV/dB	±40				dB	typ	C
Maximum Control Voltage	G = −40dB	0				V	typ	C
Minimum Control Voltage	G = +40dB	−2				V	typ	C
Gain Accuracy	$-1.8V \le V_C \le -0.2V$	±0.4	**±1.5**	±2.5	±3.5	dB	max	A
	$V_C < -1.8V$, $V_C > -0.2V$	±0.5	**±2.2**	±3.7	±4.7	dB	max	A
Gain Drift	$-1.8V \le V_C \le -0.2V$			±0.02	±0.03	dB/°C	max	B
	$V_C < -1.8V$, $V_C > -0.2V$			±0.03	±0.04	dB/°C	max	B
Gain Control Slope		−40				dB/V	typ	C
Gain Control Linearity(6)	$-1.8V \le V_C \le 0V$	±0.3	**±1**	±1.1	±1.2	dB	max	A
	$V_C < -1.8V$	±0.7	**±1.6**	±2.5	±3.2	dB	max	A
Gain Control Bandwidth		25	20	19	19	MHz	min	B

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Total output offset is: *Output Offset Voltage* ± *Input Offset Voltage* x Gain.
(5) Maximum input at minimum gain for < 1dB gain compression.
(6) Maximum deviation from best line fit.
(7) Magnitude.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C**.

R_L = 500Ω, and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

PARAMETER	CONDITIONS	VCA810ID						TEST LEVELS(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	+0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/MAX	
Gain Control Slew Rate	80dB Gain Step	900				dB/ns	typ	C
Gain Settling Time	1%, 80dB Step	0.8				µs	typ	C
Input Bias Current	V_C = −1V	−1.5	**−3.5**	−4.5	−8	µA	max	A
Gain + Power-Supply Rejection Ratio	V_C = −2V, G = +40dB, $+V_S$ = 5V ±0.5V	0.5	**1.5**	1.8	2	dB/V	max	A
Gain − Power-Supply Rejection Ratio	V_C = −2V, G = +40dB, $-V_S$ = 5V ±0.5V	0.7	**1.5**	1.8	2	dB/V	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage			**±4**	±4	±4	V	min	A
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Positive Supply Quiescent Current								
Maximum Quiescent Current	$+V_S$ = +5V, G = −40dB	10	**12.5**	12.6	12.7	mA	min	A
Minimum Quiescent Current	$+V_S$ = +5V, G = −40dB	10	**7.5**	7.2	7.1	mA	max	A
Maximum Quiescent Current	$+V_S$ = +5V, G = +40dB	18	**20.5**	22	22.3	mA	min	A
Minimum Quiescent Current	$+V_S$ = +5V, G = +40dB	18	**15.5**	14.5	13.5	mA	max	A
Negative Supply Quiescent Current(7)								
Maximum Quiescent Current	$-V_S$ = −5V, G = −40dB	12	**14.5**	14.6	14.7	mA	max	A
Minimum Quiescent Current	$-V_S$ = −5V, G = −40dB	12	**9.5**	9.4	9.3	mA	min	A
Maximum Quiescent Current	$-V_S$ = −5V, G = +40dB	20	**22.5**	24.5	24.8	mA	max	A
Minimum Quiescent Current	$-V_S$ = −5V, G = +40dB	20	**17.5**	16.5	16	mA	min	A
Positive Power-Supply Rejection Ratio	Input Referred, V_C = −2V	90	**75**	75	73	dB	min	A
Negative Power-Supply Rejection Ratio	Input Referred, V_C = −2V	85	**70**	70	68	dB	min	A
THERMAL CHARACTERISTICS								
Specification Operating Range: ID Package		−40 to +85				°C	typ	C
Thermal Resistance	Junction-to-Ambient							
D SO−8		125				°C/W	typ	C

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(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Total output offset is: *Output Offset Voltage* ± *Input Offset Voltage* x Gain.

(5) Maximum input at minimum gain for < 1dB gain compression.

(6) Maximum deviation from best line fit.

(7) Magnitude.

HIGH GRADE DC SPECIFICATIONS: V_S = ±5V (VCA810AID)

Boldface limits are tested at **+25°C**.

R_L = 500Ω, and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

PARAMETER	CONDITIONS	VCA810AID						TEST LEVELS(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	+0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/MAX	
DC PERFORMANCE	Single-Ended or Differential Input							
Output Offset Voltage	$-2V < V_C < 0$	±4	**±14**	±24	±26	mV	max	A
Input Offset Voltage		±0.1	**±0.2**	±0.25	±0.3	mV	max	A
Input Offset Current		±100	**±500**	±600	±700	mA	max	A
GAIN CONTROL (V_C, Pin 3)	Single-Ended or Differential Input							
Gain Accuracy	$-1.8V \leq V_C \leq -0.2V$	±0.4	**±0.9**	±1.9	±2.9	dB	max	A
	$V_C < -1.8V$, $V_C > -0.2V$	±0.5	**±1.5**	±3.0	±4.0	dB	max	A
Gain Control Linearity(4)	$-1.8V \leq V_C \leq 0V$	±0.3	**±0.6**	±0.7	±0.8	dB	max	A
	$V_C < -1.8V$	±0.7	**±1.1**	±1.9	±2.7	dB	max	A

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(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Maximum deviation from best line fit.

(5) Magnitude.

HIGH GRADE DC SPECIFICATIONS: V_S = ±5V (VCA810AID) (continued)

Boldface limits are tested at **+25°C**.

R_L = 500Ω, and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

		VCA810AID						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(1)	+0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVELS(3)
POWER SUPPLY								
Positive Supply Quiescent Current								
Maximum Quiescent Current	$+V_S$ = +5V, G = −40dB	10	**11.5**	11.6	11.7	mA	min	A
Minimum Quiescent Current	$+V_S$ = +5V, G = −40dB	10	**8.5**	8.2	8.1	mA	max	A
Maximum Quiescent Current	$+V_S$ = +5V, G = +40dB	18	**19.5**	21	21.3	mA	min	A
Minimum Quiescent Current	$+V_S$ = +5V, G = +40dB	18	**16.5**	15.5	14.5	mA	max	A
Negative Supply Quiescent Current(5)								
Maximum Quiescent Current	$−V_S$ = −5V, G = −40dB	12	**14**	14.1	14.2	mA	min	A
Minimum Quiescent Current	$−V_S$ = −5V, G = −40dB	12	**10**	9.9	9.8	mA	max	A
Maximum Quiescent Current	$−V_S$ = −5V, G = +40dB	20	**22**	24	24.3	mA	min	A
Minimum Quiescent Current	$−V_S$ = −5V, G = +40dB	20	**18**	17	16.5	mA	max	A

(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

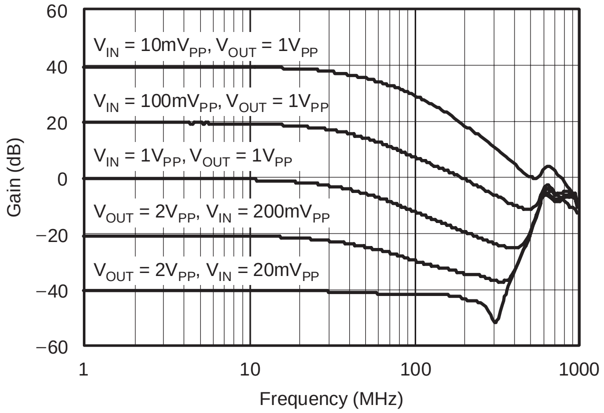
(4) Maximum deviation from best line fit.

(5) Magnitude.

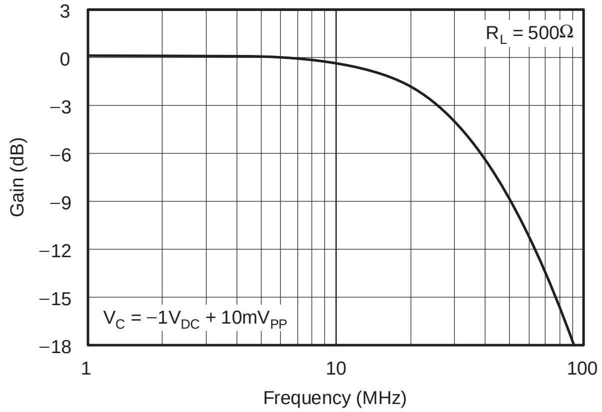
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_L = 500\Omega$ and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

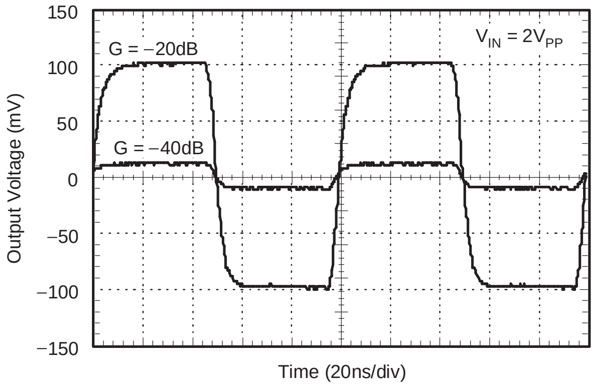
SMALL−SIGNAL FREQUENCY RESPONSE



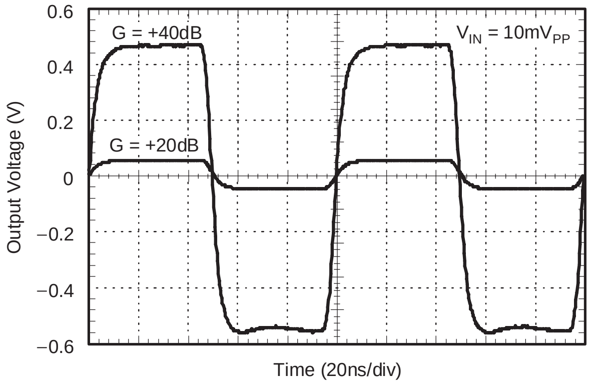
GAIN CONTROL FREQUENCY RESPONSE



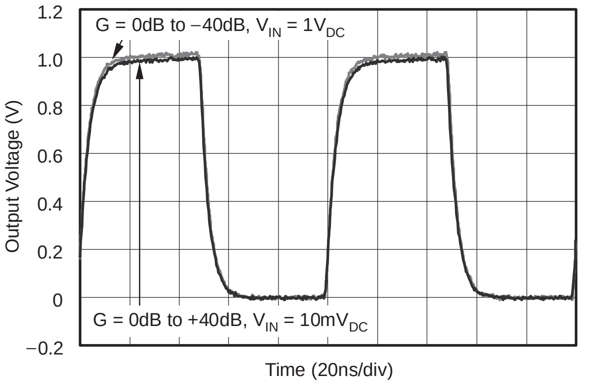
ATTENUATED PULSE RESPONSE



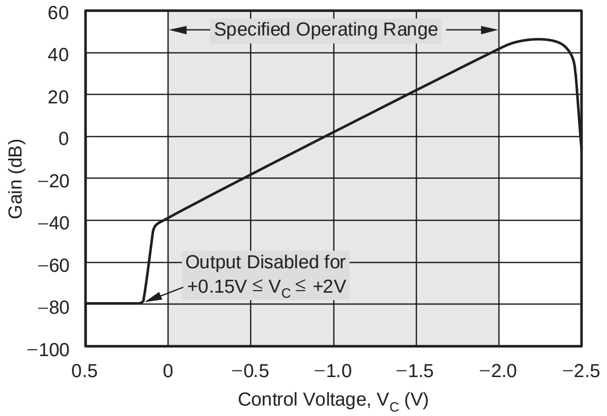
HIGH GAIN PULSE RESPONSE



GAIN CONTROL PULSE RESPONSE

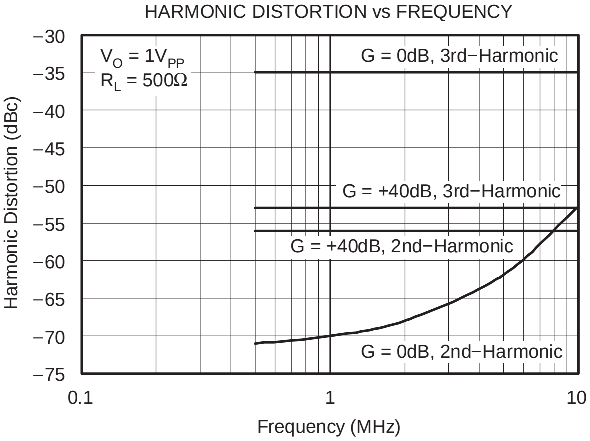


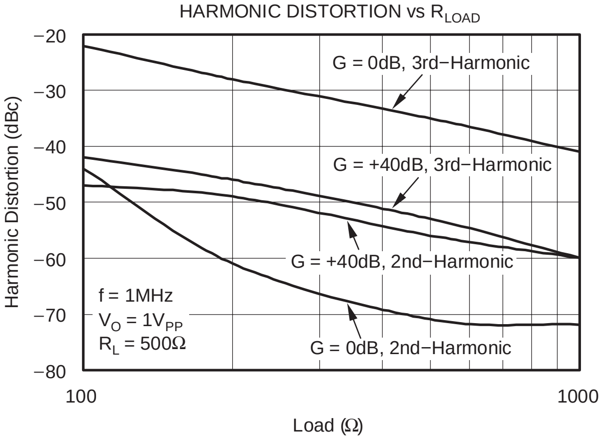
GAIN vs CONTROL VOLTAGE

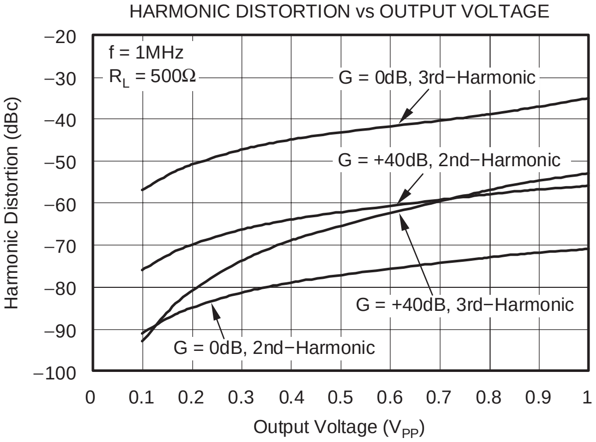


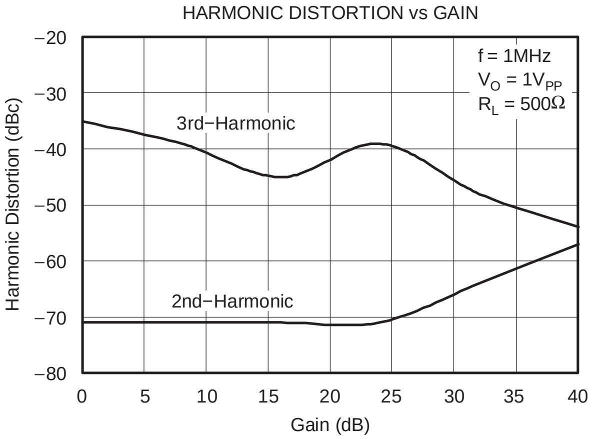
TYPICAL CHARACTERISTICS: V_S = ±5V continued

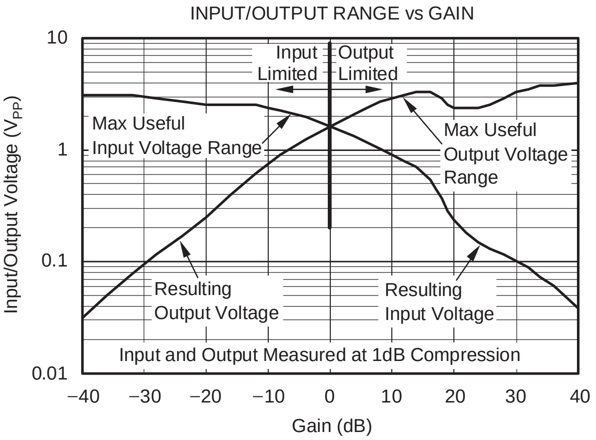
R_L = 500Ω and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

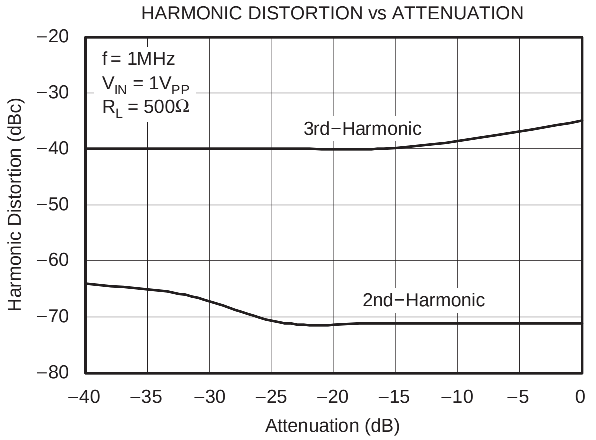








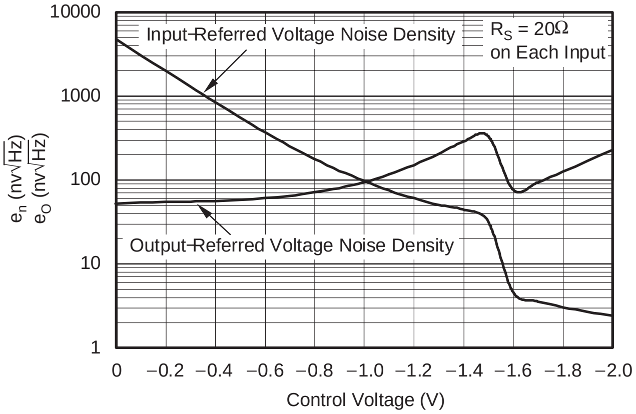




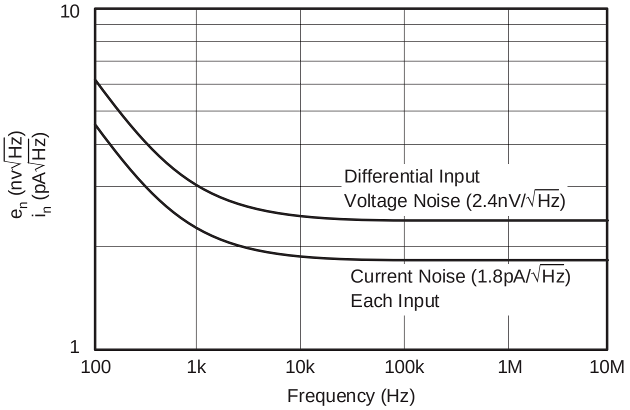
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ continued

$R_L = 500\Omega$ and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

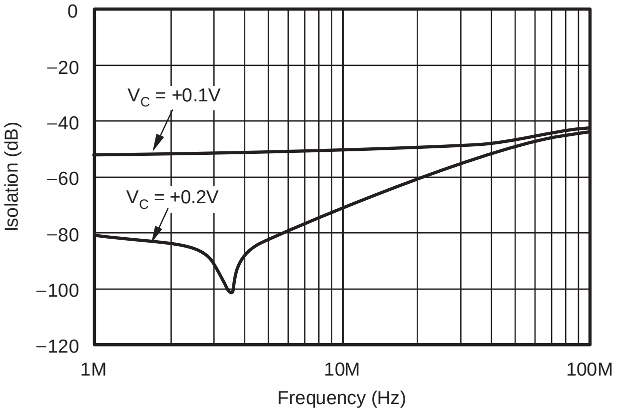
NOISE DENSITY vs CONTROL VOLTAGE



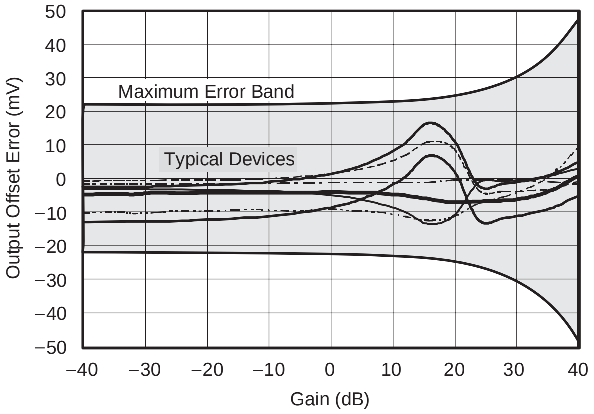
INPUT VOLTAGE AND CURRENT NOISE



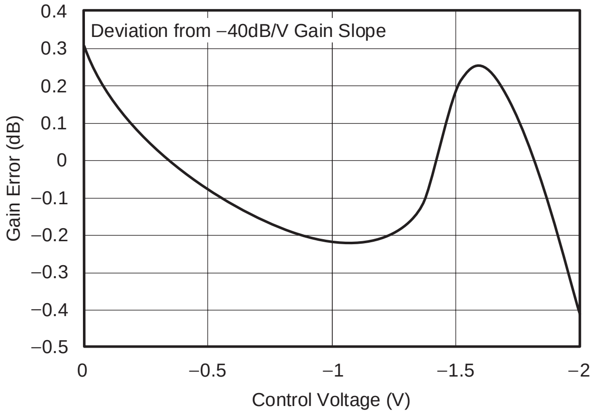
FULLY ATTENUATED ISOLATION
vs FREQUENCY



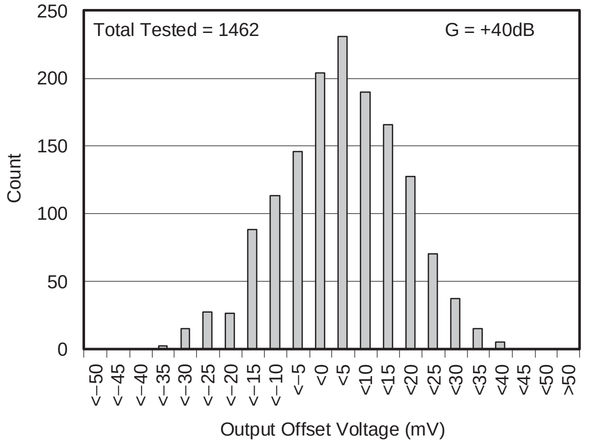
OUTPUT OFFSET VOLTAGE
TOTAL ERROR BAND vs GAIN



TYPICAL GAIN ERROR PLOT

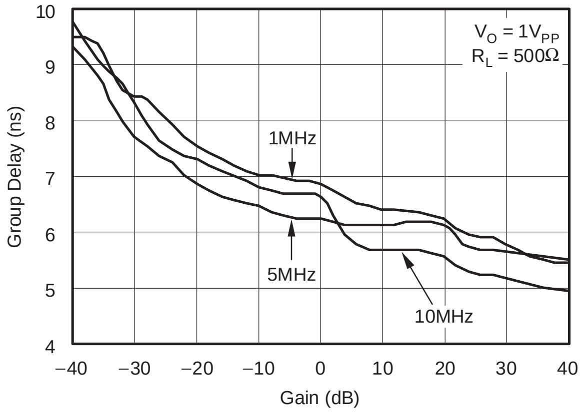


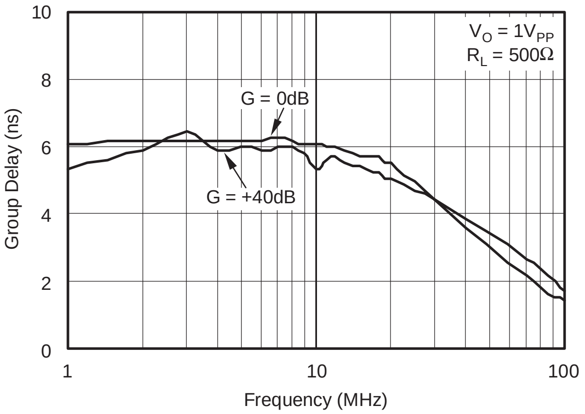
OUTPUT OFFSET VOLTAGE DISTRIBUTION

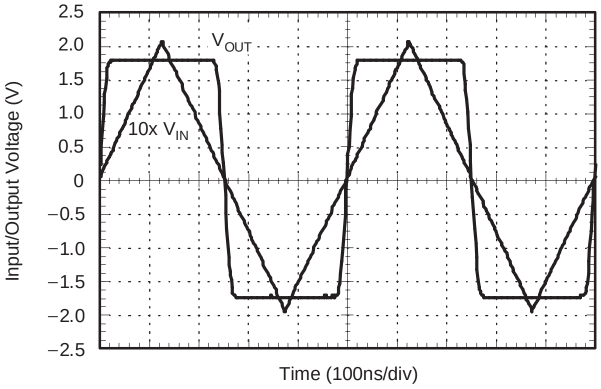


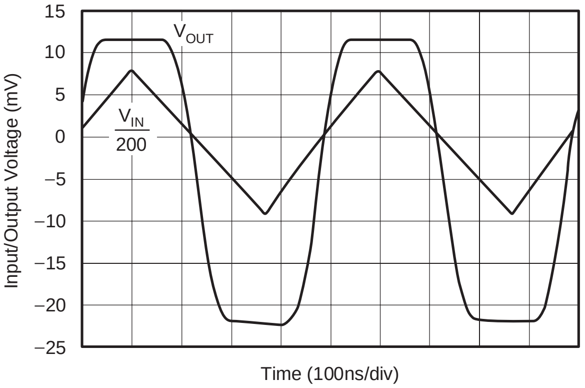
TYPICAL CHARACTERISTICS: V_S = ±5V continued

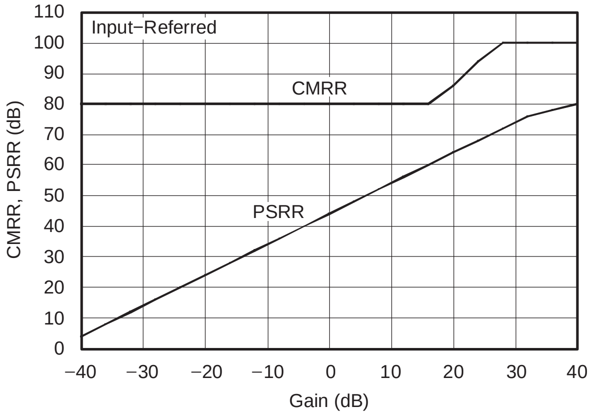
R_L = 500Ω and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

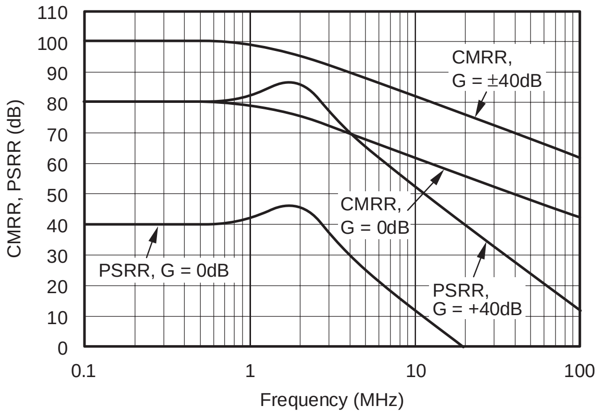

GROUP DELAY vs GAIN


GROUP DELAY vs FREQUENCY


OVERDRIVE RECOVERY AT MAXIMUM GAIN

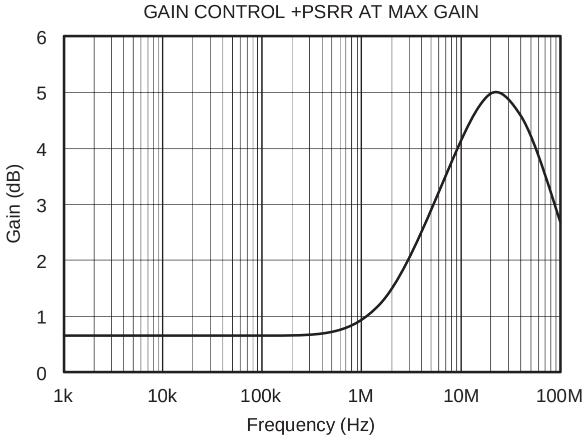

OVERDRIVE RECOVERY AT MAXIMUM ATTENUATION

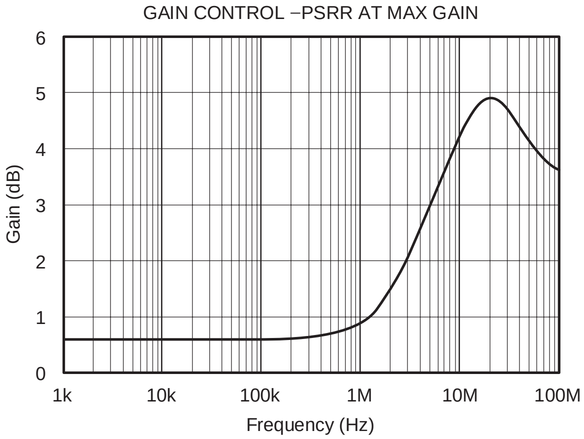

COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs GAIN

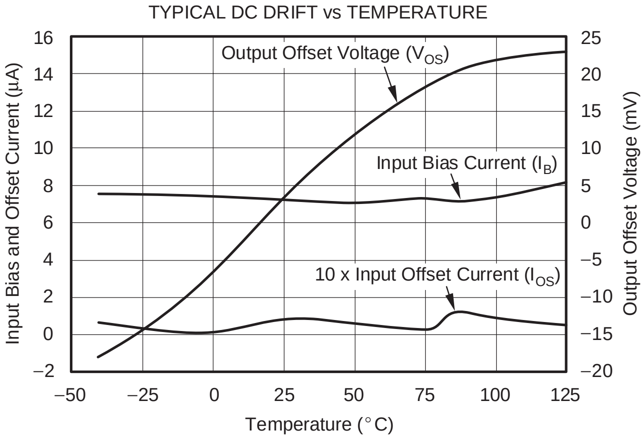

COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs FREQUENCY

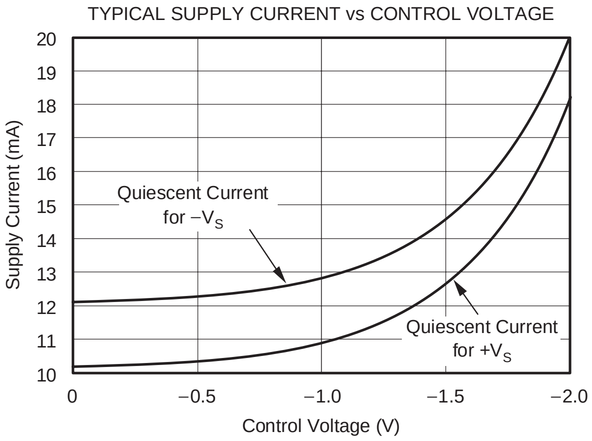
TYPICAL CHARACTERISTICS: V_S = ±5V continued

R_L = 500Ω and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.









APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION

The VCA810 is a high gain adjust range, wideband, voltage amplifier with a voltage-controlled gain, as shown in Figure 1. The circuit's basic voltage amplifier responds to the control of an internal gain-control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting flexible input impedance matching. To preserve termination options, no internal circuitry connects to the input bases of this differential stage. For this reason, the user must provide DC paths for the input base currents from a signal source, either through a grounded termination resistor or by a direct connection to ground. The differential input stage also permits rejection of common-mode signals. At its output, the voltage amplifier presents a low impedance, simplifying impedance matching. An open-loop design produces wide bandwidth at all gain settings. A ground-referenced differential to single-ended conversion at the output retains the low output offset voltage.

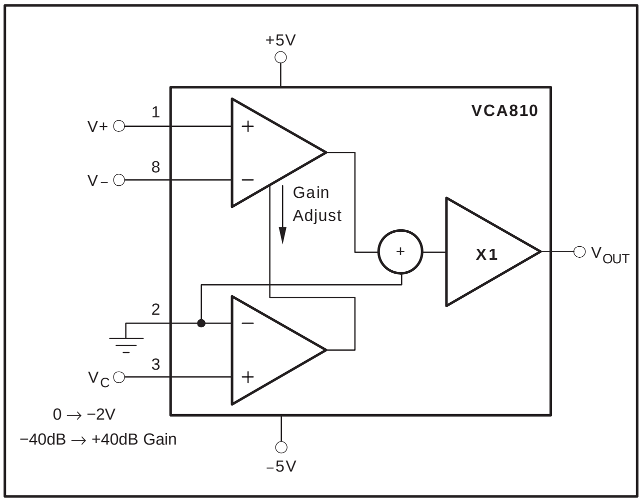


Figure 1. Block Diagram of the VCA810

A gain control voltage, V_C, controls the amplifier gain magnitude through a high-speed control circuit. Gain polarity can be either inverting or non-inverting, depending upon the amplifier input driven by the input signal. The gain control circuit presents the high-input impedance of a non-inverting op amp connection. The control voltage pin is referred to ground as shown in Figure 1. The control voltage V_C varies the amplifier gain according to the exponential relationship $G_{(V/V)} = 10^{-2(V_C+1)}$.

This translates to the log gain relationship $G_{(dB)} = -40 \cdot (V_C + 1)$ dB. Thus, $G_{(dB)}$ varies linearly over the specified −40dB to +40dB range as V_C varies from 0V to −2V. Optionally, making V_C slightly positive (≥ +0.15V) effectively disables the amplifier, giving > 80dB of signal path attenuation at low frequencies.

Internally, the gain-control circuit varies the amplifier gain by varying the transconductance, g_m, of a bipolar transistor using the transistor bias current. Varying the bias currents of differential stages varies g_m to control the voltage gain of the VCA810. A g_m-based gain adjust normally suffers poor thermal stability. The VCA810 includes circuitry to minimize this effect.

VCA810 OPERATION

Figure 2 shows the circuit configuration used as the basis of the Electrical Characteristics and Typical Characteristics. Voltage swings reported in the specifications are taken directly at the input and output pins. For test purposes, the input impedance is set to 50Ω with a resistance to ground. A 25Ω resistance (R_T) is included on the V− input to get bias current cancellation. Proper supply bypassing is shown in Figure 2, and consists of two capacitors on each supply pin: one large electrolytic capacitor (2.2μF to 6.8μF), effective at lower frequencies, and one small ceramic capacitor (0.1μF) for high frequency decoupling. For more information on decoupling, refer to the *Board Layout* section.

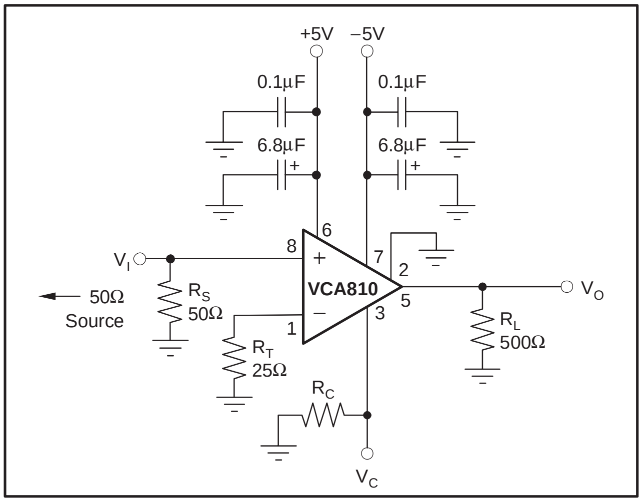


Figure 2. Variable Gain, Specification and Test Circuit

Notice that both inverting and non-inverting inputs are connected to ground with a resistor (R_S and R_T). Matching the DC source impedance looking out of each input will minimize input offset voltage error.

RANGE FINDING TGC AMPLIFIER

The block diagram in Figure 3 illustrates the fundamental configuration common to pulse-echo range finding systems. A photodiode preamp provides an initial gain stage to the photodiode.

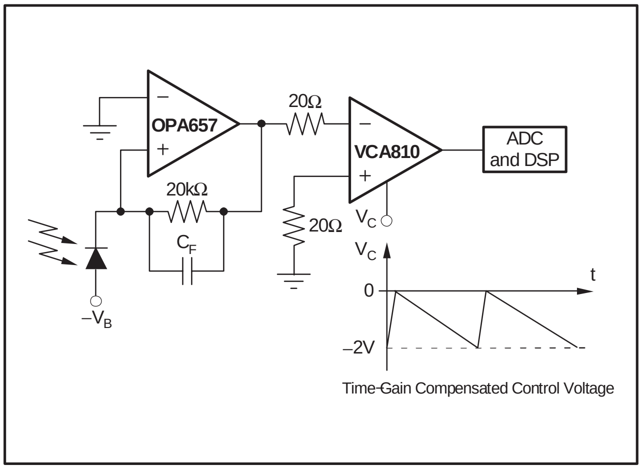


Figure 3. Typical Range Finding Application

The control voltage V_C varies the amplifier gain for a basic signal-processing requirement: compensation for distance attenuation effects, sometimes called Time-Gain Compensation (TGC). Time-gain compensation increases the amplifier gain as the signal moves through the air to compensate for signal attenuation. For this purpose, a ramp signal applied to the VCA810 gain control input linearly increases the dB gain of the VCA810 with time.

WIDE-RANGE AGC AMPLIFIER

The voltage-controlled gain feature of the VCA810 makes this amplifier ideal for precision AGC applications with control ranges as large as 60dB. The AGC circuit of Figure 4 adds an op amp and diode for amplitude detection, a hold capacitor to store the control voltage and resistors R_1 through R_3 that determine attack and release times. Resistor R_4 and capacitor C_C phase compensate the AGC feedback loop. The op amp compares the positive peaks of output V_O with a DC reference voltage, V_R. Whenever a V_O peak exceeds V_R, the OPA820 output swings positive, forward-biasing the diode and charging the holding capacitor. This charge drives the capacitor voltage in a positive direction, reducing the amplifier gain. R_3 and the C_H largely determine the attack time of this AGC correction.

Between gain corrections, resistor R_1 charges the capacitor in a negative direction, increasing the amplifier gain. R_1, R_2, and C_H determine the release time of this action. Resistor R_2 forms a voltage divider with R_1, limiting the maximum negative voltage developed on C_H. This limit prevents input overload of the VCA810 gain control circuit.

Figure 5 shows the AGC response for the values shown in Figure 4.

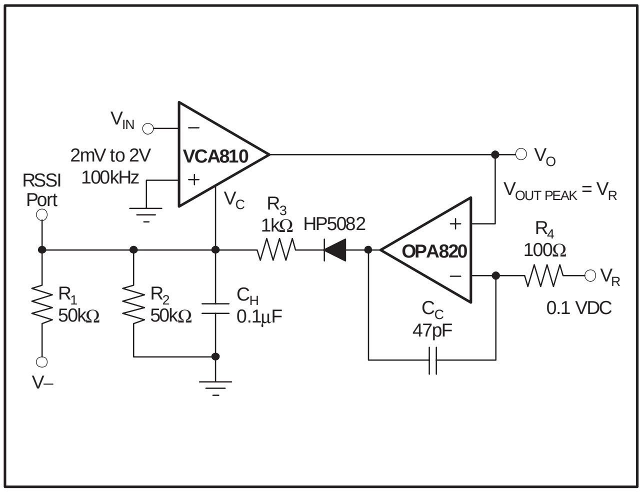


Figure 4. 60dB Input Range AGC

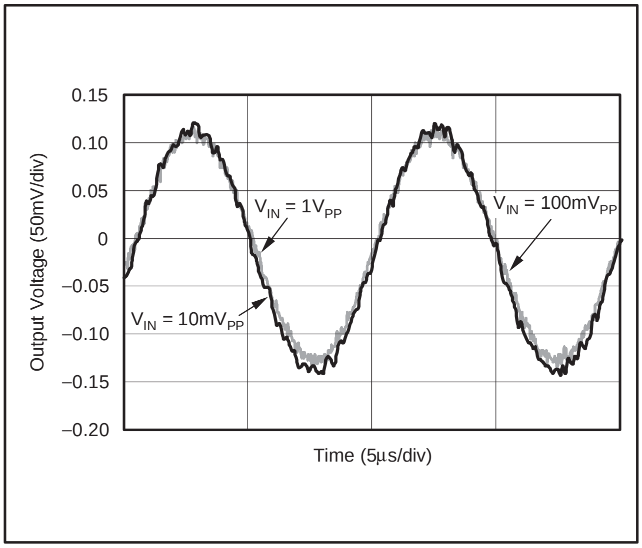


Figure 5. AGC Output Voltage for 100kHz Sinewave at $10mV_{PP}$, $100mV_{PP}$ and $1V_{PP}$

STABILIZED WEIN-BRIDGE OSCILLATOR

Adding Wein-bridge feedback to the above AGC amplifier produces an amplitude-stabilized oscillator. As Figure 6 shows, this alternative requires the addition of just two resistors (R_{W1}, R_{W2}) and two capacitors (C_{W1}, C_{W2}).

Connecting the feedback network to the amplifier non-inverting input introduces positive feedback to induce oscillation. The feedback factor displays a frequency dependence due to the changing impedances of the C_W capacitors. As frequency increases, the decreasing impedance of the C_{W2} capacitor increases the feedback factor. Simultaneously, the decreasing impedance of the C_{W1} decreases this factor. Analysis shows that the maximum factor occurs at $f_W = \frac{1}{2\pi \cdot R_W \cdot C_W}$ Hz, making this the frequency most conducive to oscillation. At this frequency, the impedance magnitude of C_W equals R_W, and inspection of the circuit shows that this condition produces a feedback factor of 1/3. Thus, self-sustaining oscillation requires a gain of three through the amplifier. The AGC circuitry establishes this gain level. Following initial circuit turn-on, R_1 begins charging C_H negative, increasing the amplifier gain from its minimum. When this gain reaches three, oscillation begins at f_W; the continued charging effect of R_1 makes the oscillation amplitude grow. This growth continues until that amplitude reaches a peak value equal to V_R. Then, the AGC circuit counteracts the R_1 effect, controlling the peak amplitude at V_R by holding the amplifier gain at a level of three. Making V_R an AC signal, rather than a DC reference, produces amplitude modulation of the oscillator output.

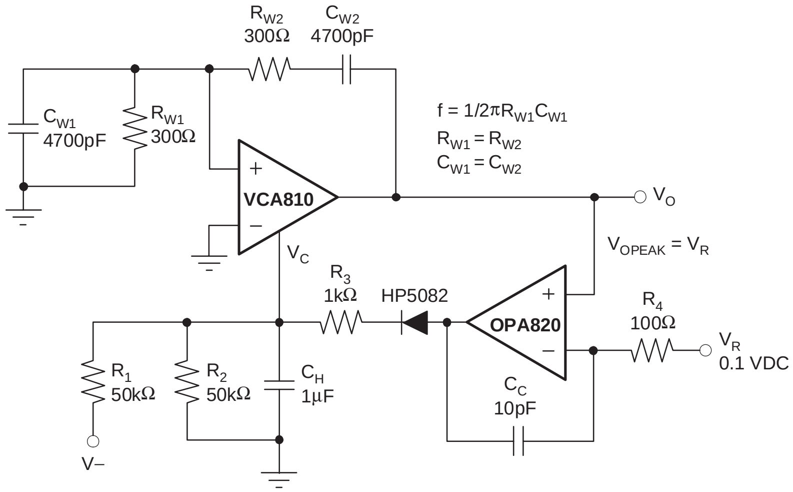


Figure 6. Amplitude-Stabilized Oscillator

LOW DRIFT WIDEBAND LOG AMP

The VCA810 can be used to provide a 2.5MHz (–3dB) log amp with low offset voltage and low gain drift. The exponential gain-control characteristic of the VCA810 permits simple generation of a temperature-compensated logarithmic response. Enclosing the exponential function in an op-amp feedback path inverts this function, producing the log response. Figure 7 shows the practical implementation of this technique. A DC reference voltage, V_R, sets the VCA810 inverting input voltage. This configuration makes the amplifier output voltage $V_{OA} = -GV_R$, where $G = 10^{-2(V_C+1)}$.

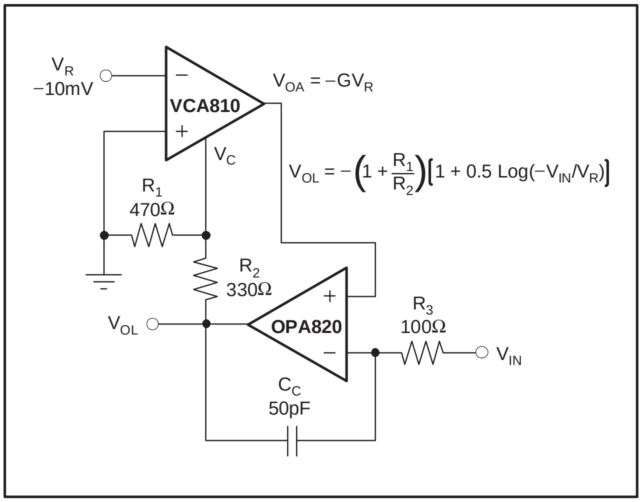


Figure 7. Temperature Compensated Log Response

A second input voltage also influences V_{OA} through control of gain G. The feedback op amp forces V_{OA} to equal the input voltage V_{IN} connected at the op amp inverting input. Any difference between these two signals drops across R_3, producing a feedback current that charges C_C. The resulting change in V_{OL} adjusts the gain of the VCA810 to change V_{OA}.

At equilibrium:

$$V_{OA} = V_{IN} = -V_R \cdot 10^{-2(V_C+1)} \qquad (1)$$

The op amp forces this equality by supplying the gain control voltage, $V_C = \dfrac{R_1 \cdot V_{OL}}{R_1 + R_2}$.

Combining the last two expressions and solving for V_{OL} yields the circuit's logarithmic response:

$$V_{OL} = -\left(1 + \frac{R_2}{R_1}\right) \cdot \left[1 + 0.5 \cdot \log\left(-\frac{V_{IN}}{V_R}\right)\right] \qquad (2)$$

An examination of this result illustrates several circuit characteristics. First, the argument of the log term, $-V_{IN}/V_R$, reveals an option and a constraint. In Figure 7, V_R represents a DC reference voltage. Optionally, making this voltage a second signal produces log-ratio operation. Either way, the log term's argument constrains the polarities of V_R and V_{IN}. These two voltages must be of opposite polarities to ensure a positive argument. This polarity combination results when V_R connects to the inverting input of the VCA810. Alternately, switching V_R to the amplifier non-inverting input removes the minus sign of the log term argument. Then, both voltages must be of the same polarity in order to produce a positive argument. In either case, the positive polarity requirement of the argument restricts V_{IN} to a unipolar range. Figure 8 illustrates these constraints.

The above V_{OL} expression reflects a circuit gain introduced by the presence of R_1 and R_2. This feature adds a convenient scaling control to the circuit. However, a practical matter sets a minimum level for this gain. The voltage divider formed by R_1 and R_2 attenuates the voltage supplied to the V_C terminal by the op amp. This attenuation must be great enough to prevent any possibility of an overload voltage at the V_C terminal. Such an overload saturates the VCA810 gain-control circuitry, reducing the amplifier's gain. For the feedback connection of Figure 7, this overload condition permits a circuit latch. To prevent this, choose R_1 and R_2 to ensure that the op amp cannot possibly deliver a more negative input than −2.5V to the V_C terminal.

Figure 8 exhibits three zones of operation described below:

Zone I: $V_C > 0V$. The VCA810 is operating in full attenuation (−80dB). The non-inverting input of the OPA820 will see ~0V. V_{OL} is going to be the integration of the input signal.

Zone II: $-2V < V_C < 0V$. The VCA810 is in its normal operating mode, creating the log relationship in Equation (2).

Zone III: $V_C < -2V$. The VCA810 control pin is out of range, and some measure should be taken so that it does not exceed –2.5V. A limiting action could be achieved by using a voltage limiting amplifier.

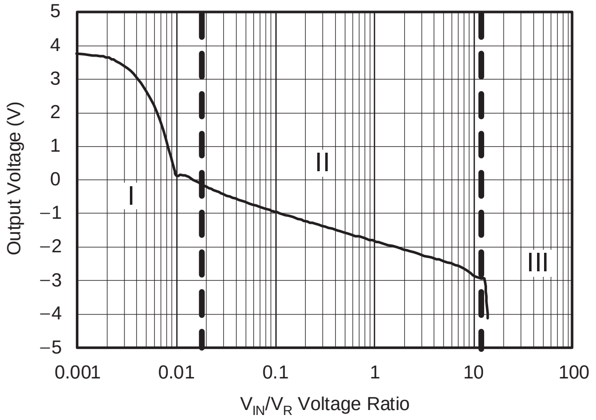


Figure 8. Test Result for LOG Amp for $V_R = -100mV$

LOW DRIFT, WIDEBAND EXPONENTIAL AMP

A common use of the log amp above involves signal companding. The inverse function, signal expanding, requires an exponential transfer function. The VCA810 produces this latter response directly, as shown in Figure 9. DC reference V_R again sets the amplifier input voltage, and the input signal V_{IN} now drives the gain control point. Resistors R_1 and R_2 attenuate this drive to prevent overloading the gain control input. Setting these resistors at the same values as in the preceding log amp produces an exponential amplifier with the inverse function of the log amp.

Testing the circuit given in Figure 9 gives the exponential response shown in Figure 10.

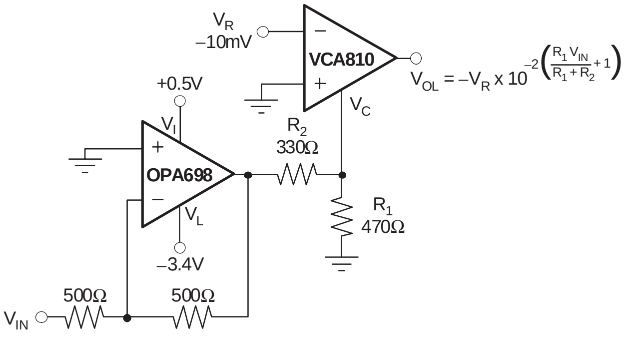


Figure 9. Exponential Amplifier

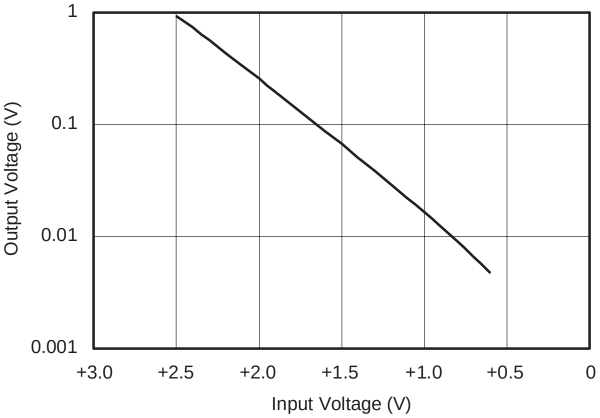


Figure 10. Exponential Amplifier Response

VOLTAGE-CONTROLLED LOW-PASS FILTER

In the circuit of Figure 11, the VCA810 serves as the variable-gain element of a voltage-controlled low-pass filter. This section discusses how this implementation expands the circuit voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit response pole responds to control voltage V_C according to the relationship in Equation (3):

$$f_P = \frac{G}{2\pi \cdot R_2 C} \tag{3}$$

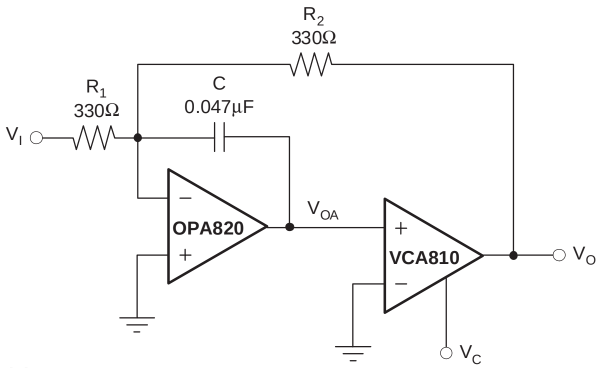
where $G = 10^{-2(V_C + 1)}$.

With the components shown, the circuit provides a linear variation of the low-pass cutoff from 300Hz to 1MHz.

The response control results from amplification of the feedback voltage applied to R_2. First consider the case where the VCA810 produces G = 1. Then, the circuit performs as if this amplifier were replaced by a short circuit. Visually doing so leaves a simple voltage amplifier with a feedback resistor bypassed by a capacitor. This basic circuit produces a response pole at $f_P = \frac{G}{2\pi \cdot R_2 C}$.

For G > 1, the circuit applies a greater voltage to R_2, increasing the feedback current this resistor supplies to the summing junction of the OPA820. The increased feedback current produces the same result as if R_2 had been decreased in value in the basic circuit described above. Decreasing the effective R_2 resistance moves the circuit pole to a higher frequency, producing the $f_P = \frac{G}{2\pi \cdot R_2C}$ response control.

Finite loop gain and a signal-swing limitation set performance boundaries for the circuit. Both limitations occur when the VCA810 attenuates, rather than amplifies, the feedback signal. These two limitations reduce the circuit's utility at the lower extreme of the VCA810 gain range. For $-1 \le V_C \le 0$, this amplifier produces attenuating gains in the range from 0dB to −40dB. This range directly reduces the net gain in the circuit's feedback loop, increasing gain error effects. Additionally, this attenuation transfers an output swing limitation from the OPA820 output to the overall circuit's output. Note that OPA820 output voltage, V_{OA}, relates to V_O through the expression, $V_O = G \cdot V_{OA}$. Thus, a G < 1 limits the maximum V_O swing to a value less than the maximum V_{OA} swing.



$$\frac{V_O}{V_I} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + s\frac{R_2C_2}{G}}$$

$$f_P = \frac{G}{2\pi R_2C}$$

$$G = 10^{-2(V_C+1)}$$

Figure 11. Tunable Low-Pass Filter

Figure 12 shows the low-pass frequency for different control voltages.

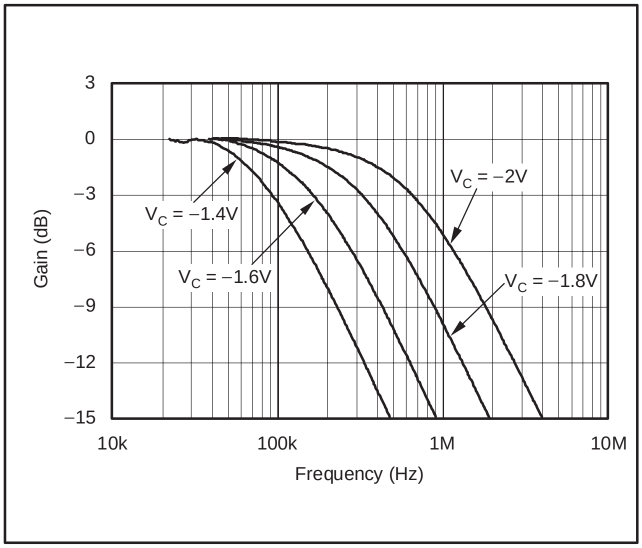


Figure 12. Voltage-Controlled Low-Pass Filter Frequency Response

TUNABLE EQUALIZER

A circuit analogous to the above low-pass filter produces a voltage-controlled equalizer response. The gain control provided by the VCA810 of Figure 13 varies this circuit response zero from 1Hz to 10kHz, according to the relationship of Equation (4):

$$f_Z \approx \frac{G}{2\pi \cdot GR_1C} \qquad (4)$$

where $G = 10^{-2(V_C+1)}$.

To visualize the circuit's operation, consider a circuit condition and an approximation that permit replacing the VCA810 and R_3 with short circuits. First, consider the case where the VCA810 produces G = 1. Replacing this amplifier with a short circuit leaves the operation unchanged. In this shorted state, the circuit is simply a voltage amplifier with an R-C bypass around R_1. The resistance of this bypass, R_3, serves only to phase-compensate the circuit, and practical factors make $R_3 \ll R_1$. Neglecting R_3 for the moment, the circuit becomes just a voltage amplifier with a capacitive bypass of R_1. This circuit produces a response zero at $f_Z = \frac{1}{2\pi \cdot R_1C}$.

Adding the VCA810 as shown in Figure 13 permits amplification of the signal applied to capacitor C, and produces voltage control of the frequency f_Z. Amplified signal voltage on C increases the signal current conducted by the capacitor to the op amp feedback network. The result is the same as if C had been increased in value to GC. Replacing C with this effective capacitance value produces the circuit control expression $f_Z = \frac{1}{2\pi \cdot R_1 GC}$.

Another factor limits the high-frequency performance of the resulting high-pass filter: the finite bandwidth of the op amp. This limits the frequency duration of the equalizer response. Limitations such as bandwidth and stability are clearly shown in Figure 14.

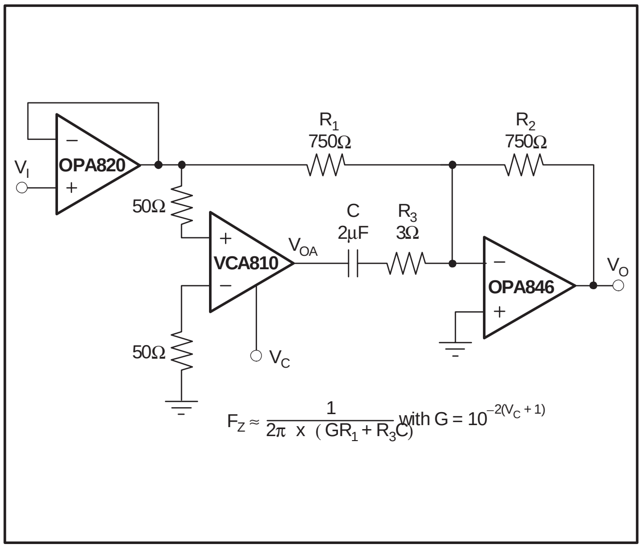


Figure 13. Tunable Equalizer

Other limitations of this circuit are stability versus VCA810 gain and input signal level for the circuit. Figure 14 also illustrates these two factors. As the VCA810 gain increases, the crossover slope between the A_{OL} curve of the OPA846 and noise gain will be greater than 20dB/decade, rendering the circuit unstable. The signal level for high gain of the VCA810 will meet two limitations: the output voltage swings of both the VCA810 and the OPA846. The expression $V_{OA} = GV_I$ relates these two voltages. Thus, an output voltage limit V_{OAL} constrains the input voltage to $V_I \le V_{OAL}/G$.

With the components shown, BW = 50kHz. This bandwidth provides an integrator response duration of four decades of frequency for f_Z = 1Hz, dropping to one decade for f_Z = 10kHz.

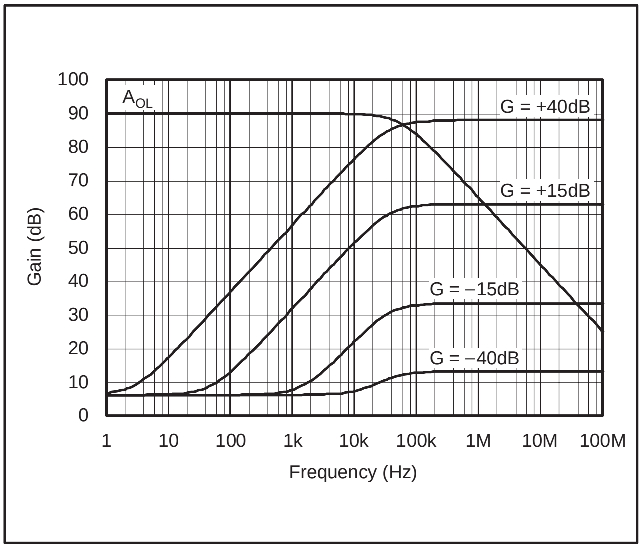


Figure 14. Amplifier Noise Gain and A_{OL} for Different Gain

VOLTAGE-CONTROLLED BAND-PASS FILTER

The variable gain of the VCA810 also provides voltage control over the center frequency of a band-pass filter. As shown in Figure 15, this filter follows from the state-variable configuration with the VCA810 replacing the inverter common to that configuration. Variation of the VCA810 gain moves the filter's center frequency through a 100:1 range following the relationship of Equation (5):

$$f_O = \frac{10^{-(V_C+1)}}{2\pi \cdot RC} \tag{5}$$

As before, variable gain controls a circuit time constant to vary the filter response. The gain of the VCA810 amplifies or attenuates the signal driving the lower integrator of the circuit. This amplification alters the effective resistance of the integrator time constant, producing the response of Equation (6):

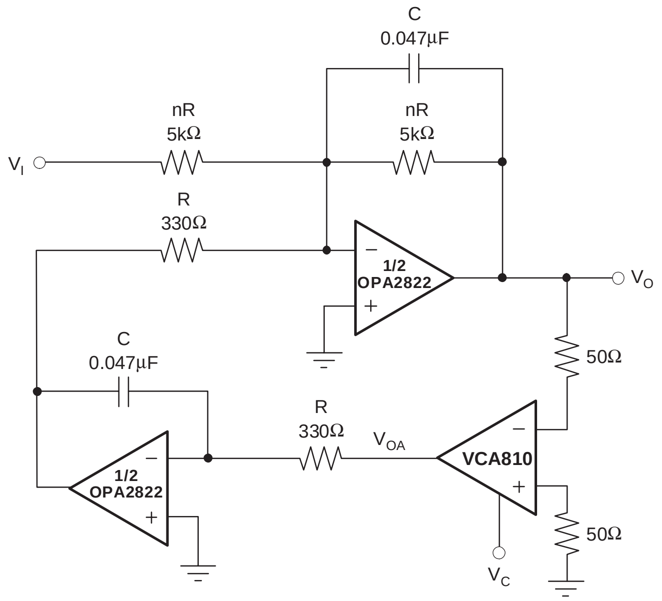
$$\frac{V_O}{V_I} = \frac{-\frac{s}{nRC}}{s^2 + \frac{s}{nRC} + \frac{G}{R^2C^2}} \tag{6}$$

Evaluation of this response equation reveals a passband gain of A_O = –1, a bandwidth of BW = 1/2nRC, and a selectivity of $Q = n \cdot 10^{-(V_C+1)}$. Note that variation of control voltage V_C alters Q but not bandwidth.

The gain provided by the VCA810 restricts the output swing of the filter. Output signal V_O must be constrained to a level that does not drive the VCA810 output, V_{OA}, into its saturation limit. Note that these two outputs have voltage swings related by $V_{OA} = GV_O$. Thus, a swing limit V_{OAL} imposes a circuit output limit of $V_{OL} \leq V_{OAL}/G$.

Figure 16 shows the frequency response for two different gain conditions of the schematic shown in Figure 15.

In particular, notice the center frequency shift and the selectivity of Q changing as the gain is increased.



$$\frac{V_O}{V_I} = \frac{-\frac{s}{nRC}}{s^2 + \frac{s}{nRC} + \frac{G}{R^2C^2}}$$

$$f_O = \frac{10^{-(V_C+1)}}{2\pi RC}$$

$$BW = \frac{1}{2\pi RC}$$

$$Q = n \cdot 10^{-(V_C+1)}$$

$$A_O = -1$$

Figure 15. Tunable Band-Pass Filter

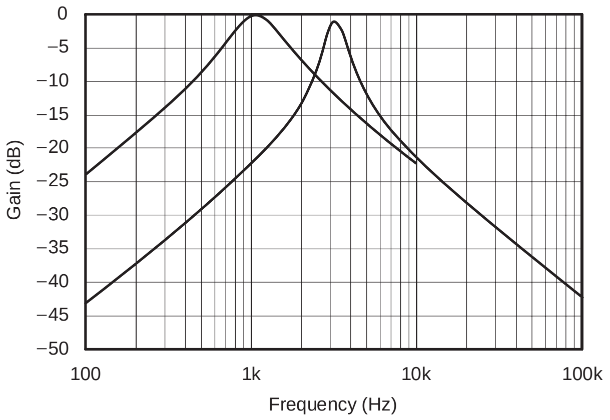


Figure 16. Tunable Band-Pass Filter Response

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A PC board is available to assist in the initial evaluation of circuit performance using the VCA810. This evaluation board (EVM) is available free, as an unpopulated PC board delivered with descriptive documentation. The summary information for this board is shown in Table 1 below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
VCA810ID	SO−8	DEM-VCA81xD	SBOU025

Table 1. EVM Ordering Information

Go to the TI web site (www.ti.com) to request evaluation boards through the VCA810 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA810 is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small signal AC performance, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

OPERATING SUGGESTIONS

INPUT/OUTPUT RANGE

The VCA810's 80dB gain range allows the user to handle an exceptionally wide range of input signal levels. If the input and output voltage range specifications are exceeded, however, signal distortion and amplifier overdrive will occur. The VCA810 maximum input and output voltage range is best illustrated in the Typical Characteristics plot, *Input/Output Range vs Gain*. This chart plots input and output voltages versus gain in dB.

The maximum input voltage range is the largest at full attenuation (−40dB) and decrease as the gain increases. Similarly, the maximum useful output voltage range increases as the input decreases. We can distinguish three overloading issues as a result of the operating mode: high attenuation, mid-range gain-attenuation, and high gain.

From –40dB to –10dB, gain overdriving the input stage is the only method to overdrive the VCA810. Preventing this type of overdrive is achieved by limiting the input voltage range.

From –10dB to +40dB, overdriving can be prevented by limiting the output voltage range. There are two limiting mechanisms operating in this situation. From –10dB to +10dB, an internal stage is the limiting factor; from +10dB to +40dB, the output stage is the limiting factor.

Output overdriving occurs when either the maximum output voltage swing or output current is exceeded. The VCA810 high output current of ±60mA insures that virtually all output overdrives will be limited by voltage swing rather than by current limiting. Table 2 summarizes these overdrive conditions.

GAIN RANGE	LIMITING MECHANISM	TO PREVENT, OPERATE DEVICE WITHIN:
$-40dB < G < -10dB$	Input Stage Overdrive	Input Voltage Range
$-10dB < G < +10dB$	Internal Stage Overdrive	Output Voltage Range
$+5dB < G < +40dB$	Output Stage Overdrive	Output Voltage Range

Table 2. Output Signal Compression

OVERDRIVE RECOVERY

As shown in the Typical Characteristics plot, *Input/Output Range vs Gain*, the onset of overdrive occurs whenever the actual output begins to deviate from the ideal expected output. If possible, the user should operate the VCA810 within the linear regions shown in order to minimize signal distortion and overdrive delay time. However, instances of amplifier overdrive are quite common in Automatic Gain Control (AGC) circuits, which involve the application of variable gain to input signals of varying levels. The VCA810 design incorporates circuitry that allows it to recover from most overdrive conditions in 200ns or less. Overdrive recovery time is defined as the time required for the output to return from overdrive to linear operation, following the removal of either an input or gain-control overdrive signal. The overdrive plots for maximum gain and maximum attenuation are shown in the Typical Characteristics plots.

OUTPUT OFFSET ERROR

Several elements contribute to the output offset voltage error; among them are the input offset voltage, the output offset voltage, the input bias current and the input offset current. To simplify the following analysis, the output offset voltage error is dependent only on the output-offset voltage of the VCA810 and the input offset voltage. The output offset error can then be expressed as Equation (7):

$$V_{OS} = V_{OSO} + 10^{\left(\frac{G_{dB}}{20}\right)} \cdot V_{IOS} \tag{7}$$

with:

- V_{OS}: Output Offset Error
- V_{OSO}: Output Offset Voltage
- G_{dB}: VCA810 Gain in dB
- V_{IOS}: Input Offset Voltage

This is shown in Figure 17.

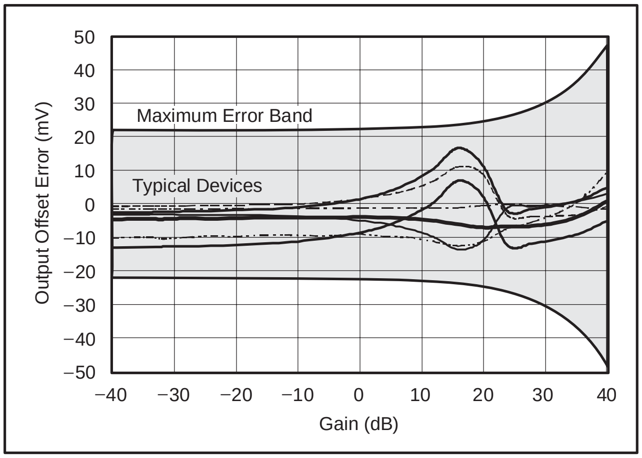


Figure 17. Output Offset Error vs. Gain

The histogram *Output Offset Voltage at Maximum Gain* in the Typical Characteristics curves shows the distribution for the output offset voltage at maximum gain.

OFFSET ADJUSTMENT

Where desired, the offset of the VCA810 can be removed as shown in Figure 18. This circuit simply presents a DC voltage to one of the amplifier inputs to counteract the offset error voltage. For best offset performance, the trim adjustment should be made with the amplifier set at the maximum gain of the intended application. The offset voltage of the VCA810 varies with gain as shown in Figure 17, limiting the complete offset cancellation to one selected gain. Selecting the maximum gain optimizes offset performance for higher gains where high amplification of the offset effects produces the greatest output offset. Two features minimize the offset control circuit noise contribution to the amplifier input circuit. First, making the resistance of R_2 a low value minimizes the noise directly introduced by the control circuit. This approach reduces both the thermal noise of the resistor and the noise produced by the resistor with the amplifier input noise current. A second noise reduction results from capacitive bypass of the potentiometer output. This reduction filters out power-supply noise that would otherwise couple to the amplifier input.

This filtering action diminishes as the wiper position approaches either end of the potentiometer, but practical conditions prevent such settings. Over its full adjustment range, the offset control circuit produces a ±5mV input offset correction for the values shown. However, the VCA810 only requires one tenth of this range for offset correction, assuring that the potentiometer wiper will always be near the potentiometer center. With this setting, the resistance seen at the wiper remains high, which stabilizes the filtering function.

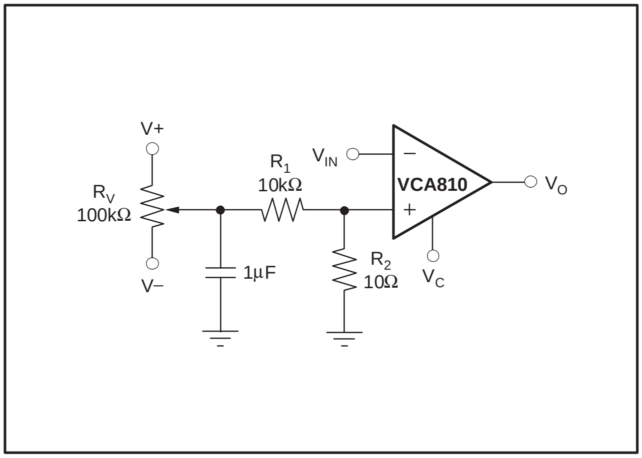


Figure 18. Optional Offset Adjustment

GAIN CONTROL

The VCA810 gain is controlled by means of a unipolar negative voltage applied between ground and the gain control input, pin 3. If use of the output disable feature is required, a ground-referenced bipolar voltage is needed. Output disable occurs for +0.15V ≤ V_C ≤ +2V, and produces > 80dB of attenuation. The control voltage should be limited to +2V in disable mode, and –2.5V in gain mode in order to prevent saturation of internal circuitry. The VCA810 gain-control input has a –3dB bandwidth of 25MHz and varies with frequency, as shown in the Typical Characteristic curves. This wide bandwidth, although useful for many applications, can allow high-frequency noise to modulate the gain control input. In practice, this can be easily avoided by filtering the control input, as shown in Figure 19. R_P should be no greater than 100Ω so as not to introduce gain errors by interacting with the gain control input bias current of 6μA.

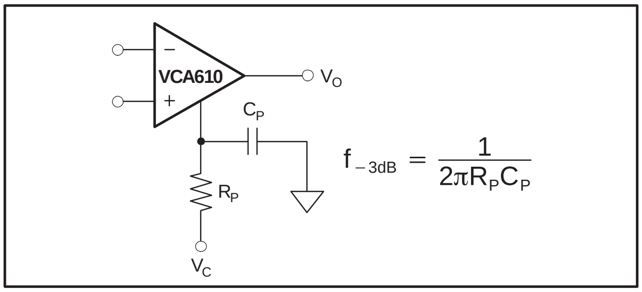


Figure 19. Control Line Filtering

GAIN CONTROL AND TEEPLE POINT

When the VCA810 controlled voltage reaches −1.5V, also referred to as the Teeple point, the signal path undergoes major changes. From 0V to the Teeple point, the gain is controlled by one bank of amplifiers: a low-gain VCA. As the Teeple point is passed, the signal path is switched to a higher gain VCA. This gain-stage switching can be seen most clearly in the *Noise Density vs Control Voltage* Typical Characteristics curve. The output-referred voltage noise density increases proportionally to the control voltage and reaches a maximum value at the Teeple point. As the gain increases and the internal stages switch, the output-referred voltage noise density drops suddenly and restarts its proportional increase with the gain.

NOISE PERFORMANCE

The VCA810 offers $2.4\text{nV}/\sqrt{\text{Hz}}$ input-referred voltage noise and $1.8\ \text{pA}/\sqrt{\text{Hz}}$ input-referred current noise at a gain of +40dB. The input-referred voltage noise, and the input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 20 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either $\text{nV}/\sqrt{\text{Hz}}$ or $\text{pA}/\sqrt{\text{Hz}}$.

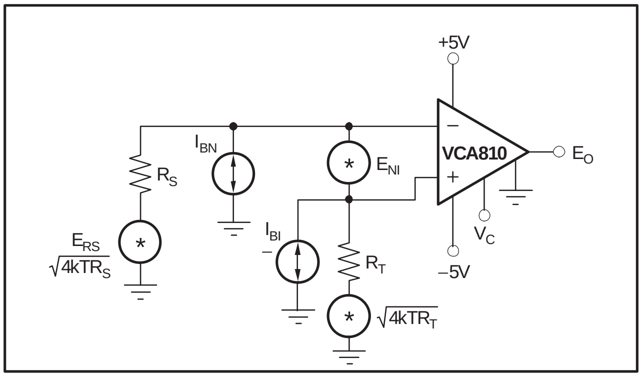


Figure 20. VCA810 Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation (8) shows the general form for the output noise voltage using the terms shown in Figure 20.

$$E_O = G_{(V/V)} \cdot \sqrt{E^2_{NI} + \left(I_{BI} \cdot R_T\right)^2 + \left(I_{BN} \cdot R_S\right)^2 + 4kT\left(R_S + R_T\right)} \tag{8}$$

Dividing this expression by the gain will give the equivalent input-referred spot-noise voltage at the non-inverting input as shown by Equation (9).

$$E_N = \sqrt{E^2_{NI} + \left(I_{BI} \cdot R_T\right)^2 + \left(I_{BN} \cdot R_S\right)^2 + 4kT\left(R_S + R_T\right)} \tag{9}$$

Evaluating these two equations for the VCA810 circuit and component values shown in Figure 2 (maximizing gain) will give a total output spot-noise voltage of $272.3\text{nV}\sqrt{\text{Hz}}$ and a total equivalent input-referred spot-noise voltage of $2.72\text{nV}\sqrt{\text{Hz}}$. This total input-referred spot-noise voltage is higher than the $2.4\text{nV}\sqrt{\text{Hz}}$ specification for the VCA810 alone. This reflects the noise added to the output by the input current noise times the input resistance R_S and R_T. Keeping input impedance low is required to maintain low total equivalent input-referred spot-noise voltage.

THERMAL ANALYSIS

The VCA810 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_J = T_A + P_D \cdot \theta_{JA}$.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using an VCA810ID (SO-8 package) in the circuit of Figure 2 operating at maximum gain and at the maximum specified ambient temperature of +85°C.

$P_D = 10V(24.8mA) + 5^2/(4 \bullet 500\Omega) = 260.5mW$

Maximum $T_J = +85°C + (0.260W \bullet 125°C/W) = 117.6°C$

This maximum operating junction temperature is well below most system level targets. Most applications will be lower since an absolute worst-case output stage power was assumed in this calculation of $V_{CC}/2$ which is beyond the output voltage range for the VCA810.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the VCA810 requires careful attention to board layout parasitic and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. This includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the non-inverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (> 25Ω) with the input pin connected to ground to help decouple package parasitic.

b) Minimize the distance (< 0.25”) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the VCA810. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or non-inverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them.

e) Socketing a high-speed part like the VCA810 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA810 onto the board.

INPUT AND ESD PROTECTION

The VCA810 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table.

All pins on the VCA810 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply, as shown in Figure 21. These diodes will begin to conduct when the pin voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long-term reliability, however, diode current should be externally limited to 10mA whenever possible.

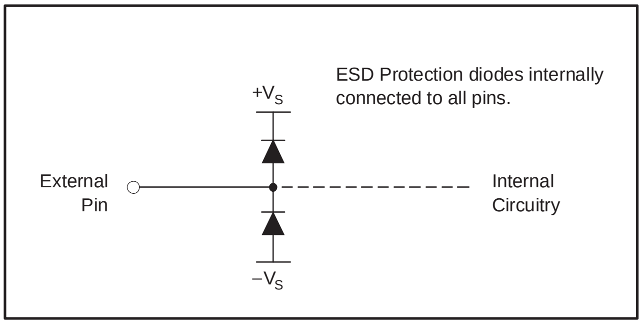


Figure 21. Internal ESD Protection

PACKAGE OPTION ADDENDUM

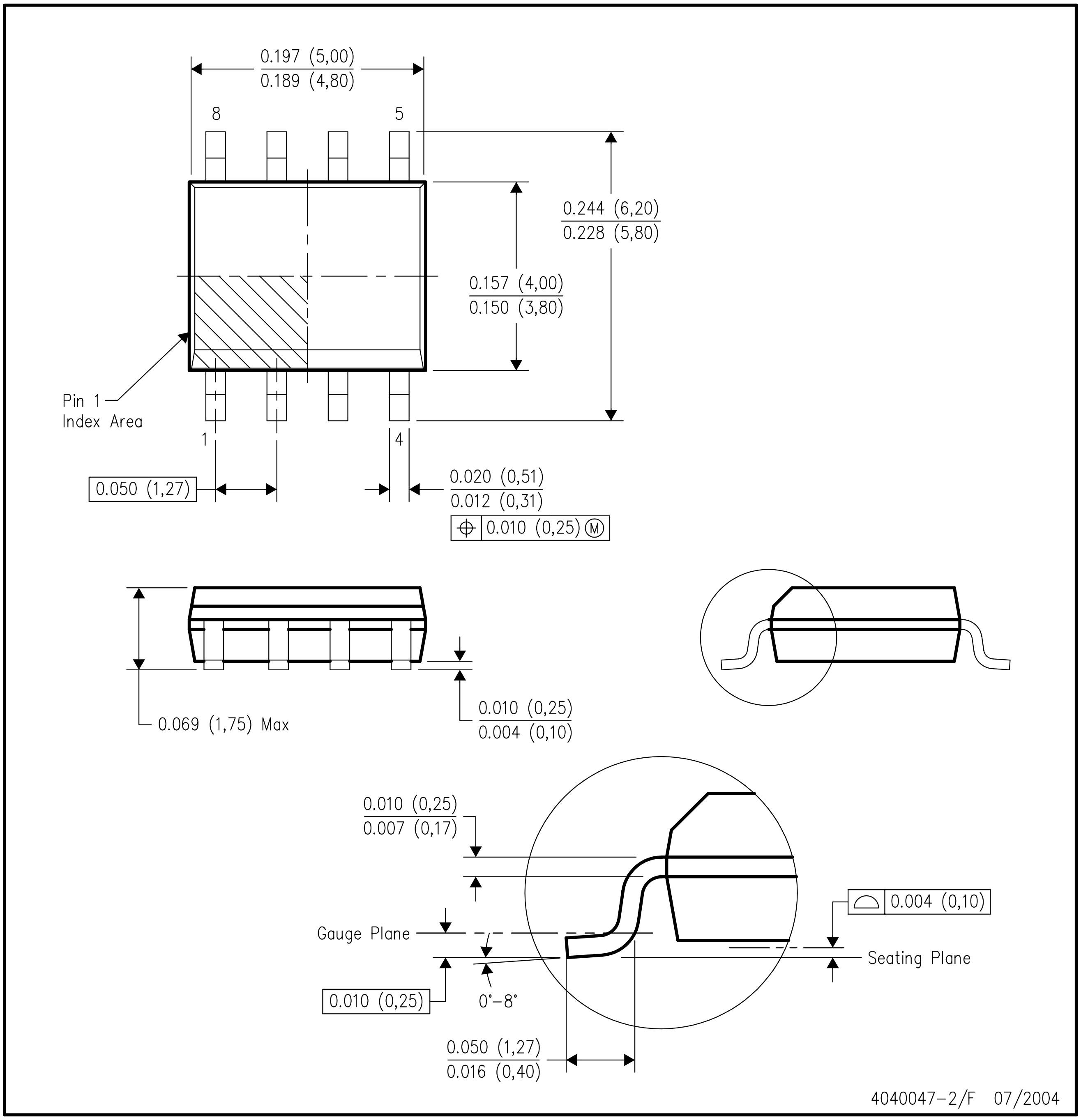
25-Oct-2004

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
VCA810AID	ACTIVE	SOIC	D	8	100
VCA810AIDR	ACTIVE	SOIC	D	8	2500
VCA810ID	ACTIVE	SOIC	D	8	100
VCA810IDR	ACTIVE	SOIC	D	8	2500

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.

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