UCC28780 Adaptive ZVS Active-Clamp Flyback Controller

1 Features

- Efficiency Performance Exceeds DoE Level VI and EU CoC V5 Tier-2 External Power Supply Standards
- Optimized for High Switching Frequency Up to 1 MHz
- Configurable with External Si or GaN FETs
- Capable of Both Full and Partial Zero Voltage Switching (ZVS) Over all Tolerances
- Adaptive Burst Control for Light-Load Efficiency with Low Output Ripple and No Audible Noise
- Secondary-Side Regulation Allows for Dynamically Scalable Output Voltage
- Internal Soft Start
- Brownout Detection without Direct Line Sensing
- Accurate Programmable Over Power Protection (OPP) to Support Peak Power Operation
- Fault Protections: Internal Over Temperature, Output Over-Voltage, Over Current, Short Circuit, and Pin Fault
- NTC Resistor Interface with External Enable

2 Applications

- High Density Adapter and Charger
- USB Power Delivery Chargers
- AC-to-DC or DC-to-DC Auxiliary Power Supply

3 Description

UCC28780 is a high-frequency active-clamp flyback controller that enables high density AC-to-DC power supplies that comply with stringent global efficiency standards. User programmable advanced control law features allow performance to be optimized for both Silicon (Si) and Gallium Nitride (GaN) power FETs. Direct operation with combination driver and GaN FET devices is further enhanced with logic level gate signals and enable outputs.

Zero voltage switching (ZVS) is achieved over wide operating range with advanced auto-tuning technique, adaptive dead time optimization, and variable switching frequency control law. Along with multimode control that changes the operation based on input and output conditions, UCC28780 enables high efficiency without the risk of audible noise. With a variable switching frequency of up to 1 MHz and accurate programmable over power protection, which provides consistent thermal design power across wide line range, passive components can be further reduced and enable high power density.

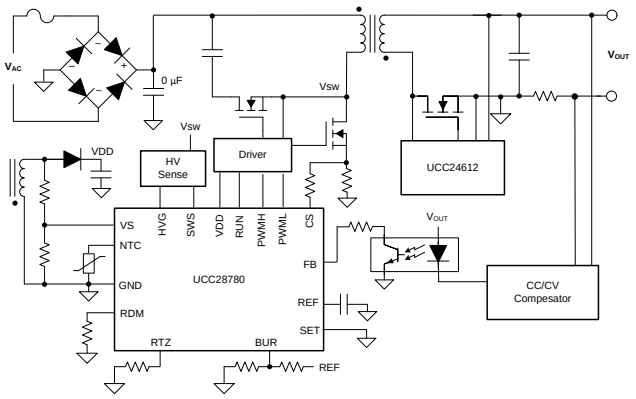
UCC28780 works with VDS sensing synchronous rectifier controllers, such as UCC24612, to achieve higher conversion efficiency and more compact designs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28780	SOIC-16	10.33 mm × 7.50 mm
	VQFN-16	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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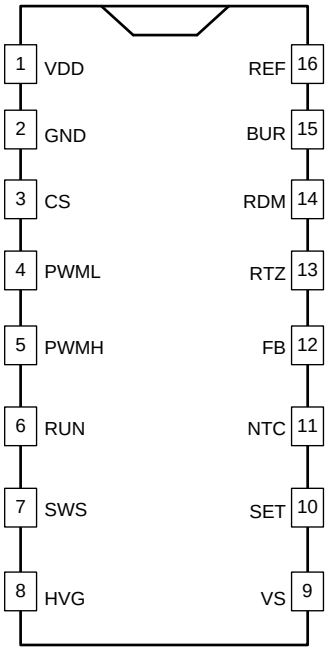
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

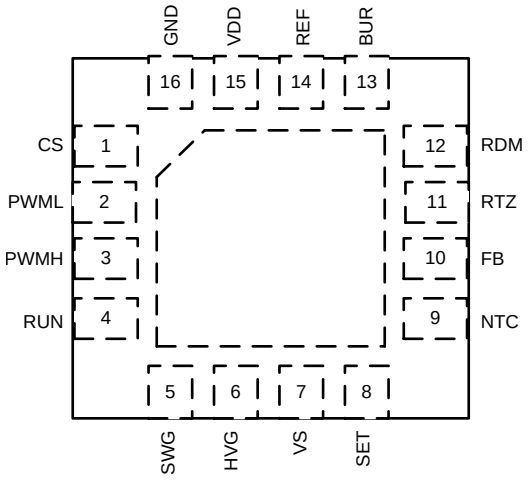
DATE	REVISION	NOTES
October, 2017	*	Advance Information release.

5 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



RTE Package
16-Pin VQFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC	QFN		
BUR	15	13	I	This pin is used to program the burst level of the converter for light load. A resistive divider between REF and GND is used to set a voltage at this pin to determine the peak current control level when the converter enters the adaptive burst mode.

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Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	SOIC	QFN		
CS	3	1	I	This is the current sense input pin. This pin couples, through a line compensation resistor, to a current sense resistor for the low-side primary switch and is used to sense and control the peak primary current each switching cycle. There is a small current that is sourced from this pin during operation, this current is proportional to the converter's input voltage and is derived from the VS pin input signal.
FB	12	10	I	The feedback signal to close the converter's regulation loop is coupled to this pin. This pin presents a ~4V output that is designed to have 0 µA to 68 µA current pulled out of it to move the converter from full-power to zero power operation.
GND	2	16	P	Ground return for all controller signals
HVG	8	6	O	The high voltage gate pin is used to bias the gate of an external depletion MOSFET in high voltage sensing circuit.
NTC	11	9	I	This is an interface to an externa NTC (negative temperature coefficient) resistor for remote temperature sensing. Pulling this pin low shuts down PWM action and initiates a fault response.
PWMH	5	3	O	The PWMH pin is a logic output used to control an external level shift and gate drive function for the high-side clamp switch on the primary of the active clamp flyback power stage.
PWML	4	2	O	The PWML pin is a logic output used to control a gate drive function to the low-side primary switch of the active clamp flyback power stage.
RDM	14	12	I	A resistor to ground on this pin programs a synthesized demagnetization time used to control the high-side switch on-time for zero voltage switching of the converter's switch-node. The controller applies a voltage on this pin that will vary with the supply output voltage derived from the VS pin signal.
REF	16	14	O	5V reference output that requires a well-placed ceramic bypass capacitor to ground. This reference can supply a limited external load current and is used to power internal circuits.
RTZ	13	11	I	A resistor to ground on this pin programs a nominal transition to zero delay following the turn-off of the high-side clamp switch. This delay is used to control the turn-on edge of the low-side switch.
RUN	6	4	O	This output pin is high when the controller is in a run state. During start-up and wait states this output is low. When high, it can be used to enable external circuits such as gate drivers for the power stage. These is a preset delay, $t_{D(RUN-PWML)}$, of about 2.2 µs that delays the initiation of switching after this pin has gone high.
SET	10	8	I	This pin is coupled either to GND or REF to set the zero voltage threshold at the SWS input pin. When SET pin is tied to GND, the threshold at SWS pin is set at its low level of 4 V. When SET pin is tied to REF pin, the zero crossing threshold is set at 9 V. This setting also selects the current sense leading edge blanking time (t_{CSLEB}), the PWML-to-PWMH dead-time ($t_{D(PWML-H)}$), the Min. PWML on time ($t_{on(min)}$) in low power mode, and the Max. PWML on time for detecting CS pin fault (t_{CSF}).
SWS	7	5	I	This switch-node sensing input is used to monitor the switch node voltage as it nears zero volts in normal operation. During start-up, this pin is coupled to VDD to allow the high voltage sensing network to provide start-up current from the converter's high voltage input.
VDD	1	15	P	Supply input to the controller. A good ceramic capacitor placed in close proximity to this pin and GND is required.
VS	9	7	I	This voltage sensing input pin is coupled via a resistor divider to the auxiliary winding of the converter's transformer. The pin and the associated external resistors are used to monitor the output and input voltages of the converter as well as the end of demagnetization period each power cycle.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VDD		38	V
	SWS	–6	38	
	VDD-SWS		38	
	CS	–0.3	3.6	
	NTC	–0.3	7	
	FB	–0.3	7	
	VS (Continuous)	–0.75	7	
	VS (Transient, 100ns Max.)	–1	7	
	RTZ	–0.3	7	
	BUR	–0.3	7	
	SET	–0.3	7	
	RDM	–0.3	7	
Output Voltage	REF	–0.3	7	V
	HVG	–0.3	25	
	PWML, PWMH, RUN	–0.3	7	
Source Current (Continuous)	REF		5	mA
	HVG		Self-limiting	
	VS (Continuous)		2	
	VS (Transient, 100ns Max.)		2.5	
	FB		1	
	PWML, PWMH, RUN		1	
	RTZ		Self-limiting	
	RDM		Self-limiting	
Sink Current(Continuous)	PWML, PWMH, RUN		–1	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	11.5		34	V
C_{REF}	REF bypass capacitor	0.1			µF
C_{HVG}	HVG bypass capacitor	2.2			nF
C_{SWS}	SWS damping capacitor		22		pF
T_J	Operating Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		D SOIC 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information

THERMAL METRIC(1)		RTE- + PAD QFN 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, I_{HVG} = 25 µA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT CURRENT						
$I_{RUN(STOP)}$	Supply current, run	No switching		2.2		mA
$I_{RUN(SW)}$	Supply current, run	Switching, I_{VSL} = 0 µA		2.5		mA
I_{WAIT}	Supply current, wait	I_{FB} = -85 µA		400		µA
I_{START}	Supply current, start	V_{VDD} = $V_{VDD(ON)}$ – 100 mV, V_{VS} = 0 V		45		µA
I_{FAULT}	Supply current, fault	Fault state		210		µA
UNDER-VOLTAGE LOCKOUT (UVLO)						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} increasing		17.5		V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} decreasing	9.6	10.0	10.5	V
$V_{VDD(PCT)}$	Offset to power cycle for long output voltage overshoot	Offset above $V_{VDD(OFF)}$, I_{FB} = -85 µA		1		V
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSL} = -1.25 mA, voltage below ground		250		mV
V_{ZCD}	Zero-crossing detection (ZCD) level	V_{VS} decreasing		30		mV
t_{ZC}	Zero-crossing timeout delay			2.2		µs
$t_{D(ZCD)}$	Propagation delay from ZCD high to PWML high	V_{VS} step from 4 V to -0.1 V		15		ns
I_{VSB}	Input bias current	V_{VS} = 4 V		0		µA
CS INPUT						
$V_{CST(max)}$	Maximum CS threshold voltage	V_{CS} increasing		800		mV
$V_{CST(min)}$	Minimum CS threshold voltage	V_{CS} decreasing, I_{FB} = -85 µA		150		mV
t_{CSLEB}	Leading-edge blanking time	V_{SET} = 5 V, V_{CS} = 1 V		200		ns
		V_{SET} = 0 V, V_{CS} = 1 V		130		
$t_{D(CS)}$	Propagation delay of CS comparator high to PWML low	V_{CS} step from 0 V to 1 V		15		ns
K_{LC}	Line-compensation current ratio	I_{VSL} = -1.25 mA, I_{VSL} / current out of CS pin		25		A/A
RUN, PWML, PWMH						
V_{PWMLH} V_{PWMHH} V_{RUNH}	PWM pins high level, and RUN pin high level	$I_{PWML(H)}$ = -1 mA, I_{RUN}= -1 mA		4.75		V
V_{PWMLL} V_{PWMHL} V_{RUNL}	PWM pins low level, and RUN pin low level	$I_{PWML(H)}$ = +1 mA, I_{RUN} = +1 mA		0.25		V
t_{RISE}	Turn-on rise time, 10% to 90%	C_{LOAD} = 10 pF		10		ns
t_{FALL}	Turn-off fall time, 90% to 10%	C_{LOAD} = 10 pF		10		ns
$t_{D(RUN-PWML)}$	Delay from RUN high to PWML high		1.8		5.4	µs
$t_{D(PWML-H)}$	Dead time between PWML low and PWMH high	V_{SET} = 0 V	30	40	50	ns
$t_{D(VS-PWMH)}$	Dead time between VS high and PWMH high	V_{SET} = 5 V		50		ns
$t_{ON(MIN)}$	Minimum on time of PWML in low power mode	V_{SET} = 5 V, I_{FB} = -85 µA, V_{CS} = 1 V		100		ns
		V_{SET} = 0 V, I_{FB} = -85 µA, V_{CS} = 1 V		65		ns

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Electrical Characteristics (continued)

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 μA, I_{HVG} = 25 μA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVP}	Over-voltage threshold	V_{VS} increasing		4.6		V
V_{OCP}	Over-current threshold	V_{CS} increasing		1.2		
$V_{CST(OPP)}$	Overpower threshold on CS pin	I_{VSL} = 0 μA		600		mV
		I_{VSL} = -333 μA		537		
		I_{VSL} = -666 μA		453		
		I_{VSL} = -1.25 mA		425		
K_{OPP}	OPP threshold voltage ratio	$V_{CST(OPP)}$ ratio between I_{VSL} = 0 μA and I_{VSL} = -1.25 mA		1.41		V/V
t_{OPP}	OPP fault timer	I_{FB} = 0 A		160		ms
$I_{VSL(RUN)}$	VS line-sense run current	Current out of VS pin increasing		353		μA
$I_{VSL(STOP)}$	VS line-sense stop current	Current out of VS pin decreasing		320		
K_{VSL}	VS line-sense ratio	$I_{VSL(STOP)}$ / $I_{VSL(RUN)}$		0.9		A/A
t_{BO}	Brown-out detection delay time	I_{VSL} < $I_{VSL(STOP)}$		60		ms
$R_{RDM(TH)}$	R_{RDM} threshold for CS pin fault			55		kΩ
t_{CSF0}	Max. PWML on time for detecting CS pin fault	R_{RDM} < $R_{RDM(TH)}$ for V_{SET} = 0 V		1		μs
t_{CSF1}	Max. PWML on time for detecting CS pin fault	V_{SET} = 5 V		2		μs
t_{FDR}	Fault reset delay timer	OCP, OPP, OVP, SCP, or CS pin fault		1.5		s
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature	125	160		°C
NTC INPUT						
R_{NTCTH}	NTC shut-down resistance	R_{NTC} decreasing		10.0		kΩ
R_{NTCR}	NTC recovery resistance	R_{NTC} increasing		22.5		kΩ
I_{NTC}	NTC pull-up current, out of pin	R_{NTC} = 12 kΩ		100		μA
BUR INPUT AND LOW POWER MODE						
$K_{BUR-CST}$	Ratio from V_{BUR} to V_{CST}	V_{CST} between $V_{CST(OPP1)}$ and 0.7 V		4		V/V
$f_{BR(UP)}$	Upper threshold of burst rate frequency			34		kHz
$f_{BR(LR)}$	Lower threshold of burst rate frequency		21	25	29	kHz
f_{LPM}	Burst rate frequency in low power mode		21	25	29	kHz
RTZ INPUT						
$t_{Z(MAX)}$	Maximum programmable dead time from PWMH low to PWML high	R_{RTZ} = 200 kΩ, I_{VSL} = -1 mA, V_{SET} = 5 V		490		ns
$t_{Z(MIN)}$	Minimum programmable dead time from PWMH low to PWML high	R_{RTZ} = 56 kΩ, I_{VSL} = -1 mA, V_{SET} = 0 V		70		ns
t_Z	Dead time from PWMH low to PWML high	I_{VSL} = -200 μA	158	175	193	ns
		I_{VSL} = -450 μA		150		ns
		I_{VSL} = -733 μA	109	125	139	ns
K_{TZ}	T_Z compensation ratio	T_Z ratio between I_{VSL} = -200 μA and I_{VSL} = -733 μA		1.4		V/V

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Electrical Characteristics (continued)

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, I_{HVG} = 25 µA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SWS INPUT						
$V_{TH(SWS)}$	SWS zero voltage threshold	V_{SET} = 5 V		9		V
		V_{SET} = 0 V		4		V
$t_{D(SWS-PWML)}$	Time between SWS low to PWML high	V_{SWS} step from 5 V to 0 V		10		ns
FB INPUT						
$I_{FB(SBP)}$	Maximum control FB current	I_{FB} increasing		68	95	µA
$V_{FB(REG)}$	Regulated FB voltage level	I_{FB} = 0 A		4		V
R_{FB}	FB input resistance			5		kΩ
REF OUTPUT						
V_{REF}	REF voltage level	I_{REF} = 0 A	4.9	5	5.1	V
$I_{S(REF)}$	Short current of REF pin	Short REF pin		9		mA
$V_{R(LINE)}$	Line regulation of V_{REF}	V_{VDD} = 12 V to 35 V		0		mV
$V_{R(LOAD)}$	Load regulation of V_{REF}	I_{REF} = 0 mA to 1 mA, change in V_{REF}		0		mV
HVG OUTPUT						
V_{HVG}	HVG voltage level	I_{HVG}= +/-200 µA	9.8	11	12	V
$I_{SE(HVG)}$	HVG max sink current during startup	V_{HVG} = 13 V		80		µA
$I_{S(HVG)}$	Short current of HVG pin	Short HVG pin		0.6		mA
$V_{HR(LINE)}$	Line regulation of V_{HVG}	V_{VDD} =12 V to 35 V		0		mV
RDM INPUT						
$t_{DM(max)}$	Maximum PWMH width with maximum tuning			6.76		µs
$t_{DM(min)}$	Minimum PWMH width with minimum tuning			3.52		µs

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7 Detailed Description

7.1 Overview

The UCC28780 is a transition-mode (TM) active clamp flyback (ACF) controller, equipped with advanced control schemes optimizing for Silicon and GaN power FETs and driving high- frequency applications up to 1 MHz to enable significant size reduction of passive components for higher power density and higher average efficiency. The ZVS control of UCC28780 is capable of auto-tuning the on-time of a high-side clamp switch (Q_H) by using a unique lossless ZVS sensing network connected between the switch-node voltage (V_{sw}) and SWS pin. The ACF controller is designed to adaptively lock onto targeted full ZVS or partial ZVS conditions for the low-side main switch (Q_L) with minimum circulating energy over wide operating conditions. Auto-tuning eliminates the risk of losing ZVS due to component tolerance, input/output voltage changes, and temperature variations, since the Q_H on-time is corrected cycle-by-cycle.

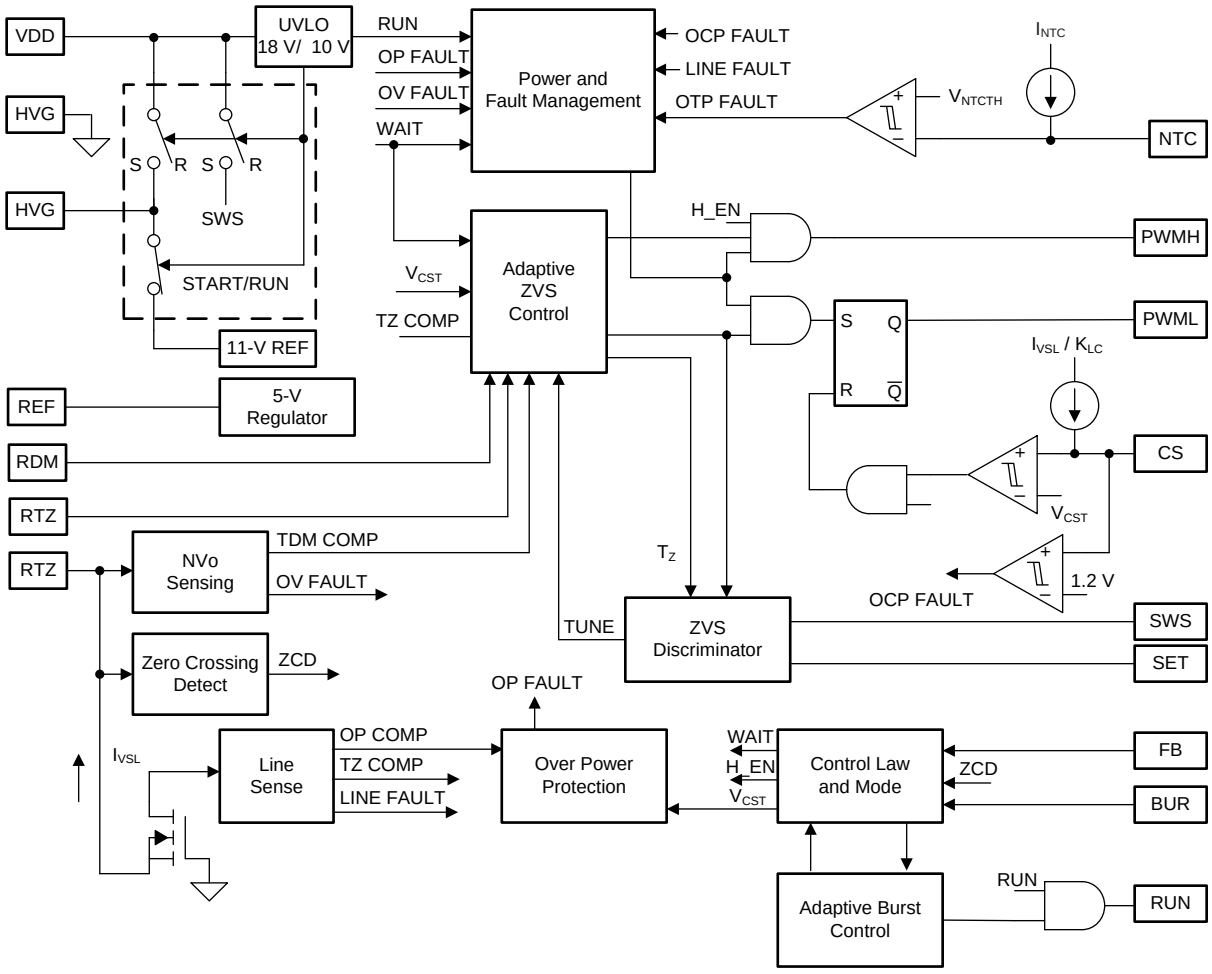
Dead times between PWML (controls Q_L) and PWMH (controls Q_H) are optimally adjusted to help minimize the circulating energy required for ZVS. Therefore, the overall system efficiency can be significantly improved and more consistent efficiency can be obtained in mass production of the soft-switching topology. The programming features of the RTZ, RDM, BUR, and SET pins provides rich flexibility to optimize the power stage efficiency across a range of output power and operating frequency levels.

The unique burst mode control of the UCC28780 maximizes the light load efficiency of the ACF power stage, while avoiding the concerns of conventional burst operation - such as output ripple and audible noise. Moreover, as the output load reduces, the burst control provides an enable signal though the RUN pin to dynamically manage the static current of the half-bridge driver and also adaptively disables the on-time of Q_H. These functions can be used to manage the quiescent power needed by the half-bridge driver, further improving the converter's light-load efficiency and reducing its standby power.

Instead of using a conventional high-voltage resistor, the UCC28780 starts up its VDD supply voltage with an external high-voltage depletion MOSFET between the SWS pin and V_{sw}, Fast starting is achieved with low standby power overhead. Moreover, the HVG pin controls the gate of the depletion FET to also allow this MOSFET to serve a second purpose of lossless ZVS sensing. This arrangement reduces the controller cost and avoids additional sensing devices.

The UCC28780 also integrates a robust set of protection features tailored to maximize the reliability of the ACF power components and of the controller itself. These features include internal soft start, brown in/out, output over-voltage, output over-power, and system over-temperature, switch over-current, output short-circuit protection, and pin open/short.

7.2 Functional Block Diagram



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7.3 Detailed Pin Description

7.3.1 BUR Pin (Programmable Burst Mode)

This pin is used to program where the controller enters adaptive burst mode (ABM) based on output loading. Internal peak current limit threshold (V_{CST}) varies with output loading before entering into ABM, and is clamped to a programmable threshold ($V_{CST(BUR)}$) in ABM. Setting an appropriate $V_{CST(BUR)}$, through the voltage at the BUR pin, allows the anchoring of the onset of ABM to a desired load condition ($i_{o(BUR)}$) - helping to maintain good light load efficiency. It is found that $i_{o(BUR)}$ around 50% to 60% load is a a reasonable starting point for both silicon and GaN-based ACF designs. The gain between the voltage on BUR pin and V_{CST} in ABM is a constant gain of $K_{BUR-CST}$, so setting $V_{CST(BUR)}$ just requires properly selecting the resistor divider on the BUR pin formed by R_{BUR1} and R_{BUR2}. Another consideration in selecting the two resistors is the standby power, since they creates a continuous load on the 5-V regulator output at the REF pin. Voltages between 0.7 V and 2.4 V are in the linear range to allow the BUR pin to properly control V_{CST} in ABM. If BUR-pin voltage (V_{BUR}) is less than 0.7 V, $V_{CST(BUR)}$ is set at 0.7 V / $K_{BUR-CST}$. If V_{BUR} is higher than 2.4 V, $V_{CST(BUR)}$ stays at 2.4 V / $K_{BUR-CST}$. A high-quality ceramic-bypass capacitor (C_{BUR}) to GND helps decoupling switching noise, with 100pF maximum recommended.

$$R_{BUR2} = \frac{R_{BUR1} K_{BUR-CST} V_{CST(BUR)}}{V_{REF} - K_{BUR-CST} V_{CST(BUR)}} = \frac{R_{BUR1} \times 4V_{CST(BUR)}}{5V - 4V_{CST(BUR)}} \quad (1)$$

7.3.2 FB Pin (Feedback Pin)

The FB pin connects to the collector of an analog optocoupler output transistor through an external current-limit resistor (R_{FB}). Depending on the operating mode, the controller uses different content of the collector current flowing out of the FB pin (i_{FB}) to regulate the output voltage. For the operating modes based on peak current control, i_{FB} is converted into an internal peak current threshold (V_{CST}) to modulate the amplitude of the current sense signal on the CS pin. For example, when V_o is lower than the regulation level set by the shunt regulator, the “current level” of i_{FB} moves to lower value, so V_{CST} goes up to deliver more power to output load.

As the burst control takes over the output voltage regulation, where V_{CST} is clamped to $V_{CST(BUR)}$, the “current ripple” of i_{FB} is used to modulate burst off time, as shown in Figure 1. Specifically, after a group of pulses stop bursting, the output load current starts to discharge the output capacitor, which makes V_o start to decay. With a recommended loop compensation, this results in a corresponding in-phase i_{FB} current ripple. When the decaying i_{FB} intersects with an internal reference current (i_{ref}), the ripple regulator generates a new set of grouped burst pulses to deliver more power, which makes V_o and i_{FB} ripple move upward.

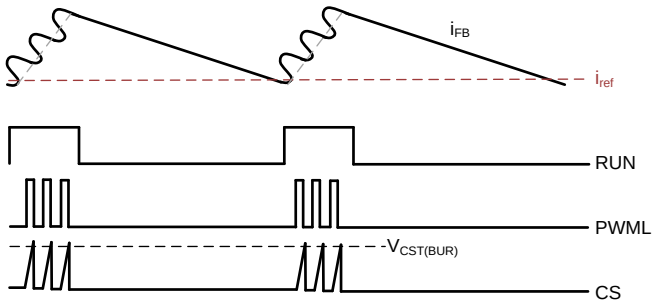

Figure 1. Concept of Burst Control in UCC28780

The nature of ripple-based control in burst mode requires additional care on the noise level of i_{FB} to improve the consistency of burst off-time between burst cycles. A high-quality ceramic-bypass capacitor between FB pin and REF pin (C_{FB}) is required for decoupling i_{FB} noise, a minimum of 100 pF is recommended. There is an internal resistor of 5 kΩ connected to the FB pin that, in conjunction with C_{FB} forms an effective low-pass filter. On the other hand, too strong low-pass filtering with too large C_{FB} can attenuate the i_{FB} ripple creating slope distortion of the intersection point between i_{FB} and i_{REF}, which can cause inconsistent burst off-times, even though V_o stays in regulation and the i_{FB} noise is low.

ADVANCE INFORMATION

Detailed Pin Description (continued)

7.3.3 VDD Pin (Device Bias Supply)

The VDD rail is the primary bias for the internal 5-V bias regulator, internal 11-V regulator, bandgap reference, and parts of the undervoltage lock-out (UVLO) circuit. V_{VDD} during startup is ramped by the depletion MOSFET (Q_s) connected to the SWS pin. V_{VDD} during normal operation is powered by the auxiliary winding (N_A) of the ACF transformer. As shown in the block diagram, the UVLO circuit connected to the VDD pin controls three power-path switches among VDD, HVG, and SWS pins, in order to allow Q_s able to perform both V_{VDD} startup and V_{sw} sensing in ZVS control. The UVLO circuit provides a turn-on threshold of $V_{VDD(on)}$ at 17.5 V and turn-off threshold of $V_{VDD(off)}$ at 10 V, so it is can accommodate lower values of VDD capacitor (C_{VDD}) and supporting low power-on delays. A high, 38-V, maximum operating level on V_{VDD} alleviates concerns with leakage energy charging of C_{VDD} and gives added flexibility when a varying output voltage must be supported. For details of the startup sequencing one can refer to the device function section of this datasheet.

As V_{VDD} reaches $V_{VDD(on)}$, Q_s is disconnected from the VDD pin, the C_{VDD} size has to be sufficient to hold V_{VDD} higher than $V_{VDD(off)}$ until the auxiliary winding voltage is high enough to take over bias power delivery during V_o soft start. Therefore, the calculation of minimum capacitance ($C_{VDD(min)}$) needs to consider the discharging effect from both the sink current of the UCC28780 during switching in its run state ($i_{RUN(sw)}$) and the average sink current of driver (i_{Dr}) throughout the longest time of V_o soft start ($t_{ss(max)}$).

$$C_{DD(\min)} = \frac{(i_{RUN(SW)} + i_{Dr})t_{SS(\max)}}{V_{VDD(on)} - V_{VDD(off)}} \tag{2}$$

$t_{ss(max)}$ estimation should consider the averaged soft-start current ($i_{sec(SS)}$) on the secondary side of ACF, the constant-current output load ($i_{o(SS)}$), maximum output capacitance ($C_{o(max)}$), and a 1ms time-out potentially been triggered in the startup sequence.

$$t_{ss(\max)} = \frac{C_{o(\max)}V_o}{i_{\sec(SS)} - i_{o(SS)}} + 1ms \tag{3}$$

During V_o soft start, V_{CST} reaches to a maximum current threshold on the CS pin ($V_{CST(max)}$) , so $i_{sec(SS)}$ at minimum voltage of input bulk capacitor ($V_{bulk(min)}$) can be approximated as:

$$i_{\sec(ss)} = \frac{N_{PS}V_{CST(\max)}}{2R_{CS}} \frac{V_{bulk(\min)}}{V_{bulk(\min)} + N_{PS}(V_o + V_f)} \tag{4}$$

Where R_{CS} is the current sense resistor, N_{PS} is primary-to-secondary turns ratio, and V_f is the forward voltage drop of secondary rectifier.

ADVANCE INFORMATION

Detailed Pin Description (continued)

7.3.4 REF Pin (Internal 5-V Bias)

The internal 5-V regulator of the controller is connected to this pin, which requires a high-quality ceramic-bypass capacitor (C_{REF}) to GND for decoupling switching noise and lowering the voltage droop as the controller transitions from wait state to run state. The minimum C_{REF} value is 0.1 μF and X7R capacitor is recommended. The maximum sourcing current is self-limited and it is capable of delivering approximately 9 mA to external circuits. 5-V bias is available only when the under-voltage lock-out (UVLO) circuit enables the operation of UCC28780. The details of the startup sequencing is covered in the device function modes of this datasheet.

7.3.5 HVG and SWS Pins

The HVG pin provides a voltage-controlled signal for the depletion mode MOSFET's (Q_s) gate voltage, enabling Q_s to serve both V_{VDD} startup and lossless ZVS sensing on V_{sw}. During V_{VDD} startup, the UVLO circuit connects SWS and HVG pins with a power-path switch which shorts the gate-to-source of Q_s. During this condition a separate power-path switch is closed between SWS an VDD pins. In this configuration Q_s behaves like a current source to charge the VDD capacitor (C_{VDD}). After V_{VDD} reaches $V_{VDD(on)}$, the two power-path switches open the connections between SWS and HVG pins and between VDD and SWS pins correspondingly. At this point, a third power-path switch connects an internal 11-V regulator to the HVG pin. As Q_s gate is fixed at 11 V and the drain-pin voltage of Q_s becomes higher than the sum of Q_s threshold voltage ($V_{th(Qs)}$) and the 11-V gate voltage, the source-pin voltage of Q_s can no longer follow the drain-pin voltage change, so this gate control method makes Q_s act as a high-voltage blocking device with the drain pin connected to the high-voltage switch node (V_{sw}). When the ACF is switching, V_{sw} can be lower than 11 V, so the body diode of Q_s forces the source-pin voltage to follow V_{sw}, becoming a replica of the V_{sw} waveform at the lower voltage level. The limited window for monitoring V_{sw} waveform suffices for ZVS control of the UCC28780. The internal 11-V regulator requires a high quality ceramic bypass capacitor (C_{HVG}) between the HVG pin and GND for noise filtering and providing compensation to the regulator circuitry. The minimum C_{HVG} value is 2.2 nF and a X7R capacitor is recommended. The controller will enter into fault state if the HVG pin is open or shorted to GND during V_{VDD}start-up, and if V_{HVG} overshoot is higher than 14 V in run state. Besides, the regulator output current is self-limiting as HVG pin is shorted.

Detailed Pin Description (continued)

7.3.6 RTZ Pin (Sets Delay for Transition Time to Zero)

The dead time between PWMH falling edge and PWML rising edge (t_Z) serves as the discharge time for V_{sw} transiting from its high level down to the target ZVS point. Since the optimal t_Z varies with V_{bulk}, the internal dead-time optimizer automatically extends t_Z as V_{bulk} is less than highest voltage of input bulk capacitor ($V_{bulk(max)}$), so the circulating energy for ZVS can be further reduced, obtaining higher efficiency at low line versus a fixed dead time over a wide line range. The R_{RTZ} resistor programs the minimum t_Z ($t_{Z(min)}$) at $V_{bulk(max)}$. The following equation can be used to set the initial value of this resistor based on the sum of the propagation delay of high-side driver ($t_{d(Dr)}$) and the resonant transition time of V_{sw} falling edge, which is a function of the lumped switch-node capacitance (C_{sw}) and magnetizing inductance (L_m).

$$R_{RTZ} = K_{TZ} \times t_{Z(\min)} = K_{TZ} \times (t_{d(Dr)} + 0.56 \times \pi \sqrt{L_m C_{sw}}) \quad (5)$$

$$K_{TZ} = 11.2 \times 10^{11} / 1F, \; V_{SET} = 0 \; V \quad (6)$$

$$K_{TZ} = 5.6 \times 10^{11} / 1F, \; V_{SET} = 5 \; V \quad (7)$$

7.3.7 RDM Pin (Sets synthesized De-Magnetization Time for ZVS Tuning)

The R_{RDM} resistor provides the power stage information to the t_{DM} optimizer for auto-tuning the on-time of PWMH to achieve ZVS within a given t_z discharge time. The following equation calculates the initial resistance, based on the knowledge of the primary magnetizing inductance (L_m), auxiliary-to-primary turns ratio (N_A/N_S), the values of the resistor divider (R_{VS1}, R_{VS2}) from the auxiliary winding to the VS pin, and the current sense resistor (R_{CS}). Among those parameters, L_m contributes the most variation due to its typically wider tolerance. The optimizer is equipped with wide enough on-time tuning range of PWMH to cover tolerance errors. Therefore, just typical values are enough for the selection calculation.

$$R_{RDM} = \frac{K_{DM} \times L_m \times \left(\frac{N_A}{N_P}\right) \times R_{VS2}}{R_{CS} \times (R_{VS1} + R_{VS2})} = \frac{5 \times 10^9 \times L_m \times \left(\frac{N_A}{N_P}\right) \times R_{VS2}}{1F \times R_{CS} \times (R_{VS1} + R_{VS2})} \quad (8)$$

7.3.8 RUN Pin (Half-bridge Driver Enable Pin)

The RUN pin is a logic level output signal to enable the half-bridge driver of the ACF. It generates a 5-V logic output when the driver should be active, and pulls down less than 0.5 V when the driver should not be active. During burst mode operation, the RUN pin serves as a power management function to dynamically reduce the static current of the driver so light-load efficiency can be further improved and standby power can be minimized. In addition, there is a minimum 2.2-µs delay time between RUN going high to PWML going high, that is intended to provide an appropriate wake-up time for UCC28780 and the half-bridge driver to transition from a wait state to a run state.

ADVANCE INFORMATION

7.4 Device Functional Modes

7.4.1 Adaptive ZVS Control with Auto-Tuning

Figure 2 shows the simplified block diagram explaining the concept of the ZVS control on UCC28780. A high voltage sensing network provides the replica of the switch node voltage waveform (V_{sw}) with a limited "visible" voltage range that SWS pin can handle. Then, the ZVS discriminator identifies the ZVS condition and determines the adjustment direction for the on-time of PWMH (t_{DM}) by detecting if V_{sw} reaches a predetermined ZVS threshold, $V_{th(sws)}$, or not within a certain timeout of t_Z, where t_Z is the targeted zero voltage transition time of V_{sw} controlled by the PWMH-to-PWML dead time optimizer. In Figure 2, V_{sw} of the current switching cycle has not reached $V_{th(sws)}$ yet, the ZVS discriminator sends a TUNE signal to increase t_{DM} a bit for the next cycle, such that the negative magnetizing current ($i_{m(-)}$), can increase incrementally to bring V_{sw} downward a bit deeper. Then, after few switching cycles, the t_{DM} optimizer settles and makes ACF lock into ZVS operation. In steady state, t_{DM} moves within the least significant bit (LSB) of the ZVS tuning loop, and the minor change of t_{DM} of each cycle is too small to significantly move the ZVS condition away from desired operating point. Figure 3 demos how fast the ZVS control can lock into ZVS. Before the ZVS loop is settled, UCC28780 starts at a valley switching condition as t_{DM} is not long enough to creates sufficient $i_{m(-)}$. Within 15 switching cycles, the ZVS tuning loop settles and begins toggling t_{DM} with an LSB.

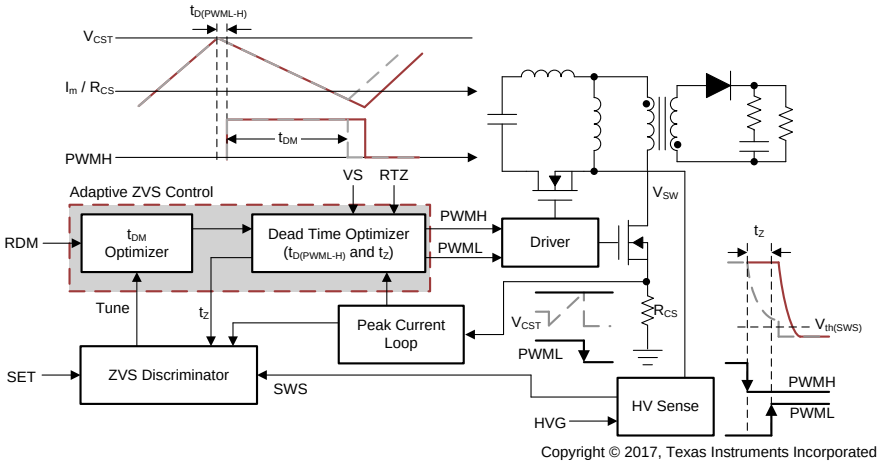

Figure 2. Concept of Adaptive ZVS Control in UCC28780 (Patent Pending)

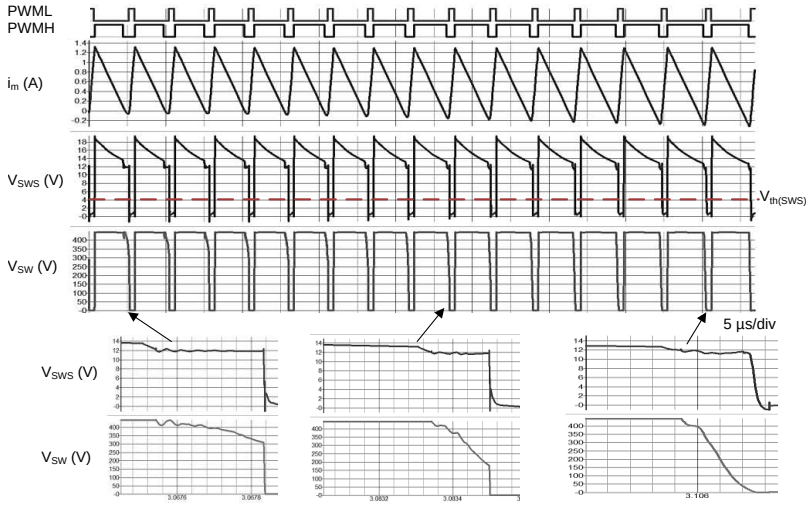

Figure 3. Demo of the Auto-Tuning Process (Patent Pending)

Device Functional Modes (continued)

7.4.2 Dead Time Optimization

The dead time optimizer in Figure 2 controls the two dead times: the dead time between PWMH falling edge and PWML rising edge (t_Z), and the dead time between PWML falling edge and PWMH rising edge ($t_{D(PWML-H)}$).

Adaptive control law for t_Z of UCC28780 utilizes the line-feedforward technique to extend t_Z as V_{bulk} reduces, as shown in Figure 4. The VS pin senses V_{bulk} through the auxiliary winding voltage as Q_L turns on, which generates a line-sensing current (i_{VSL}) out of VS pin flowing through the upper resistor of voltage divider on VS pin (R_{VS1}). Minimum t_Z ($t_{Z(min)}$) is set at highest $V_{bulk(max)}$ through the RTZ pin. After i_{VSL} current is lower than a threshold current of 666 µA, t_Z starts to linearly increase and the maximum t_Z extension is 140% higher than $t_{Z(min)}$.

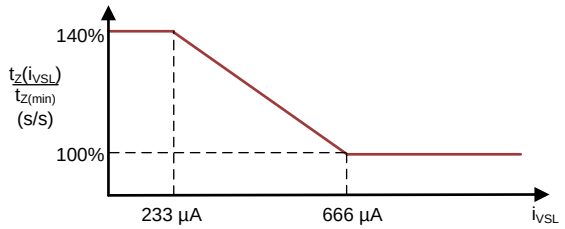

Figure 4. t_Z Control of UCC28780 (Patent Pending)

The control law for $t_{D(PWML-H)}$ of UCC28780 is programmable based on the SET pin. At V_{SET} = 0 V, a fixed delay around 40 ns is used to fit a GaN-based ACF with a fast dV/dt on V_{sw} rising edge. With V_{SET} = 5 V, dead time optimization is enabled to intelligently avoid the nonlinear junction capacitance effect of silicon MOSFET on the asymmetrical dV/dt of V_{sw} rising edge. Basically, the high capacitance region of the C_{oss} curve for the silicon low-side FET creates a shallow ramping on V_{sw} after PWML turns off. When C_{oss} of Q_L moves to the low capacitance region with V_{sw} increasing, V_{sw} starts to ramp up very quickly. The asymmetrical slope varies with different peak magnetizing currents as output load changes, so the issue of using a fixed dead time is the potential risk of hard switching on the high-side clamp switch (Q_H) if the timing is not long enough. UCC28780 utilizes the zero crossing detect (ZCD) signal on auxiliary winding voltage to identify if V_{sw} overcomes the shallow ramping or not, and then generates a 40-ns delay before asserting PWMH. This feature allows cycle-by-cycle dead time adjustment to avoid the risk of hard switching of Q_H, while providing fast enough turn-on timing for Q_H to minimize the body diode conduction time.

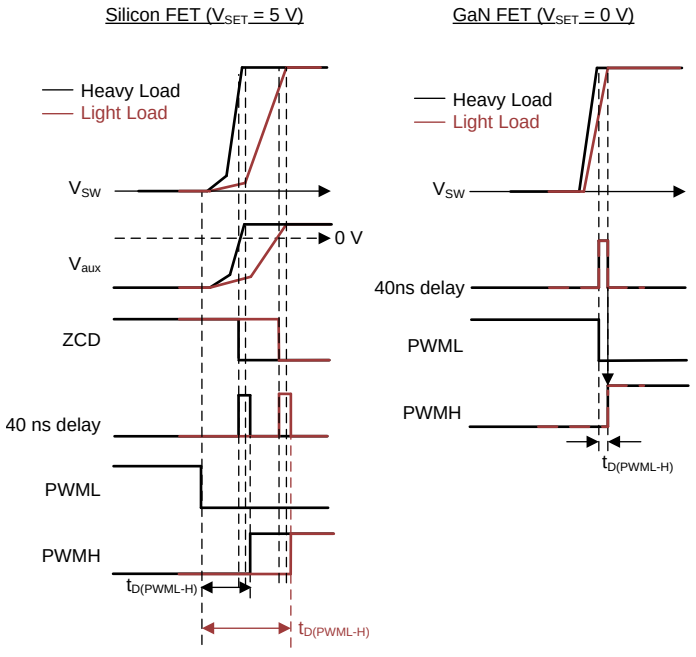

Figure 5. $t_{D(PWML-H)}$ Control of UCC28780 Optimized for GaN and Silicon FETs (Patent Pending)

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Device Functional Modes (continued)

7.4.3 Control Law across Wide Load Range

UCC28780 contains four modes of light load operation summarized in Table 1. Starting from heavier load, the AAM mode forces PWML and PWMH in complementary switching with ZVS tuning enabled. ABM mode generates a group of PWML and PWMH pulses as a burst packet, and adjusts the burst off time to regulate the output voltage. At the same time, the burst frequency variation is confined above 20kHz by adjusting the number of PWML and PWMH pulses per packet. In LPM and SBP modes, PWMH and ZVS tuning loop are disabled, so each switching cycle operates in valley switching.

Table 1. Functional Modes

	MODE	OPERATION	PWMH	ZVS
AAM	Adaptive Amplitude Modulation	Complementary ACF	Enable	YES
ABM	Adaptive Burst Mode	Variable f_{BUR} > 20 kHz, complementary ACF	Enable	YES
LPM	Low Power Mode	Fix f_{BUR} ≈ 25 kHz, valley switching	Disable	No
SBP	StandBy Power	Variable f_{BUR} < 25 kHz, valley switching	Disable	No

Figure 6 addresses the critical parameter changes among the four operating modes, where V_{CST} is the peak current threshold compared with the current-sense signal from CS pin, f_{sw} is the switching frequency of PWML, f_{BUR} is the burst frequency, and N_{sw} is the pulse number of PWML per burst packet. The following section explains the detail operation of each mode.

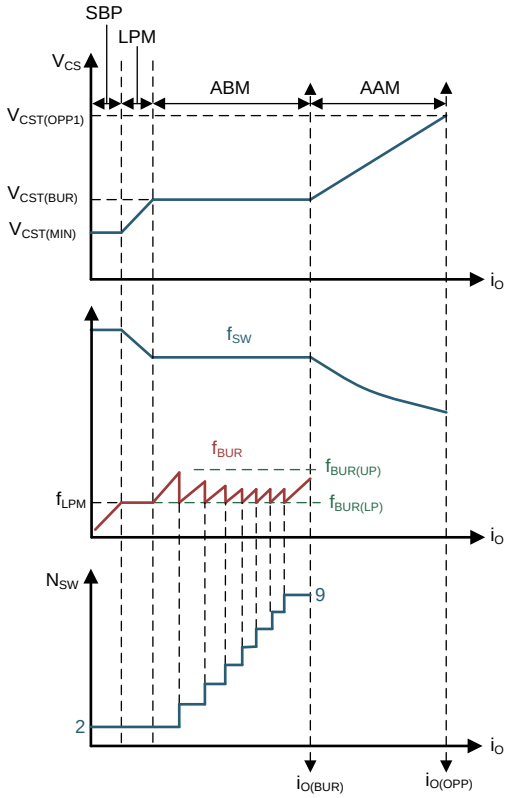

Figure 6. Control Law Over Wide Load Range (Patent Pending)

7.4.4 Adaptive Amplitude Modulation (AAM)

The switching pattern in AAM forces PWML and PWMH in a complementary fashion, as shown in Figure 7. As the load current reduces, the negative magnetizing current ($i_{m(-)}$) stays the same, while the positive magnetizing current ($i_{m(+)}$) reduces by the internal peak current loop to regulate output voltage. $i_{m(+)}$ generates a current-feedback signal on CS pin (V_{CS}) through a current-sense resistor in series with low-side switch, and a peak current threshold (V_{CST}) in the current loop controls the peak current variation. Due to the nature of transition mode (TM) operation, lowering the peak current results in higher f_{sw} operation. On the other hand, as load current increases, V_{CS} increases. When the load current increases to an over-power condition ($i_{o(OPP)}$) where V_{CS} correspondingly reaches an OPP threshold of peak current loop ($V_{CST(OPP)}$), OPP fault response can be triggered. Furthermore, the RUN signal stays high in AAM, so the half-bridge driver remains active.

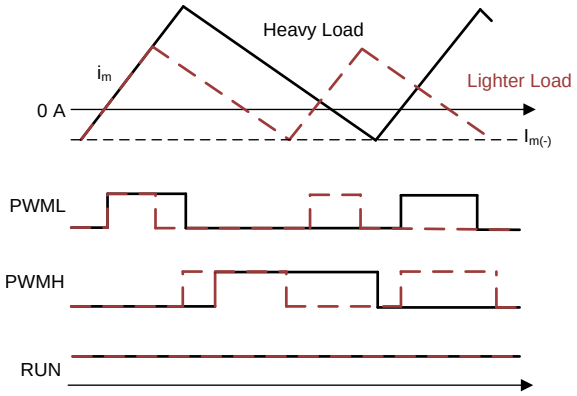

Figure 7. PWM Pattern in AAM

7.4.5 Adaptive Burst Mode (ABM)

As the load current reduces to $i_{o(BUR)}$ where V_{CS} reaches to a $V_{CST(BUR)}$ threshold, ABM starts and V_{CS} is clamped, so the magnetizing current and f_{sw} of each pulse are fixed for a given input voltage level. $V_{CST(BUR)}$ is programmed by the BUR pin voltage (V_{BUR}) with a ratio of $K_{CST-BUR}$. The PWM pattern of ABM is shown in Figure 8. When RUN goes high, a delay time between RUN and PWML ($t_{D(RUN-PWML)}$) is given to allows both the half-bridge driver and the UCC28780 to wake up from a wait state to a run state. PWML is set as the first pulse to build up the bootstrap voltage of high side driver before PWMH start switching. The first PWML pulse turns on Q_L close to a valley voltage level by sensing the condition of zero crossing detection (ZCD) on auxiliary winding voltage. The following switching cycles operate in a ZVS condition, since PWMH is enabled. As the number of PWML pulses (N_{sw}) in the burst packet reaches its target value, the RUN pin pulls low after the ZCD of the last switching cycle is detected, and forces the half-bridge driver and UCC28780 into a wait state, reducing quiescent current of both devices. In this mode, the minimum off time of the RUN signal is 2.2 µs and the minimum on time of PWML is limited to the leading-edge blanking time (t_{CSLEB}) of the peak current loop. However, more grouped pulses means more risk on higher output ripple and higher audible noise. The following equation estimates how burst frequency (f_{BUR}) varies with output load and other parameters.

$$f_{BUR} = \frac{i_o}{i_{o(BUR)}} \frac{f_{sw}}{N_{sw}} \quad (9)$$

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As $i_o < i_{o(BUR)}$, f_{BUR} can become lower than the audible noise range if N_{sw} is fixed, so the concept of ABM is to modulate N_{sw} to ensure that f_{BUR} stays above 20 kHz by monitoring f_{BUR} every burst period. As i_o reduces, f_{BUR} becomes lower and may reach a predetermined low-level frequency threshold ($f_{BUR(LR)}$), at this point N_{sw} for both PWML and PWMH are reduced by one pulse pushing f_{BUR} above $f_{BUR(LR)}$. At the same time, the burst frequency ripple on the output voltage reduces as N_{sw} drops with the load reduction. On the other hand, as i_o increases, f_{BUR} will become higher and may reach a predetermined high-level frequency threshold ($f_{BUR(UP)}$), so N_{sw} increases by one pulse to push f_{BUR} back below $f_{BUR(UP)}$. By maximizing the number of pulses per burst packet, governed by ripple and audible noise, this algorithm maximizes the number of cycles that will achieve ZVS and improving ACF efficiency. As i_o moves below the boundary between AAM and ABM, the maximum N_{sw} is nine and the minimum is two. As i_o is close to the boundary between AAM and ABM, the maximum N_{sw} can be higher than nine, to provide a smooth mode transition.

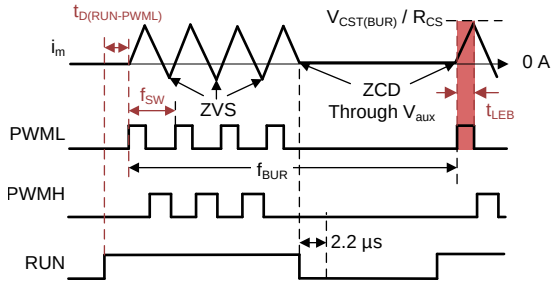

Figure 8. PWM Pattern in ABM (Patent Pending)

7.4.6 Low Power Mode (LPM)

As N_{sw} drops to two in ABM and two burst periods result in a burst frequency less than $f_{BUR(LR)}$, UCC28780 enters into LPM mode and disables PWMH. The purpose of LPM is to provide a soft peak current transition between $V_{CST(BUR)}$ and $V_{CST(min)}$. LPM fixes N_{sw} at two and f_{BUR} equal to f_{LPM} = 25 kHz. In LPM mode, V_{CST} is controlled to regulate the output voltage. At the start of each burst packet, after RUN pulls high, $t_{D(RUN-PWML)}$ is used to wake up both half-bridge driver and UCC28780. With PWMH is disabled, the two PWML pulses turn on Q_L close to valley switching by sensing ZCD. At the ZCD following second PWML pulse of a burst cycle, the RUN pin goes low and the UCC28780 enters its low-power wait state. In LPM mode, the minimum on time of PWML can be further reduced to a $t_{on(min)}$, to allow the peak current to be reduced beyond the level limited by t_{CSLEB} of peak current loop. With this feature, before f_{BUR} starts to fall below f_{LPM} and enters into audible noise range of SBP mode, the peak current is low enough to limit the magnitude of any audible excitation.

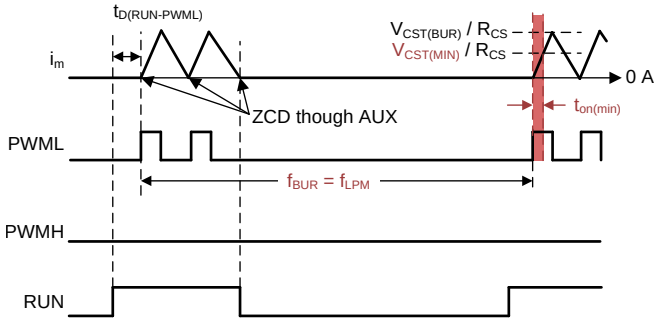

Figure 9. PWM Pattern in LPM

7.4.7 Standby Power Mode (SBP)

As V_{CST} drops to $V_{CST(min)}$, UCC28780 enters into SBP mode and PWMH continues to stay disabled. The purpose of SBP is to lower f_{BUR} in order to minimize standby power. SBP fixes N_{sw} at two and V_{CST} to $V_{CST(min)}$, while the burst off time is adjusted to regulate the output voltage. As f_{BUR} is well below f_{LPM}, the switching-related loss can be minimized. In addition, lowering f_{BUR} forces both the half-bridge driver and the UCC28780 to remain in wait states longer to minimize the static loss. The equivalent static current of the UCC28780 in SBP can be represented as

$$i_{VDD(SBP)} = (i_{RUN} - i_{Wait})(\frac{2}{f_{sw(SBP)}} + t_{D(RUN-PWML)})\, f_{BUR} + i_{Wait} \quad (10)$$

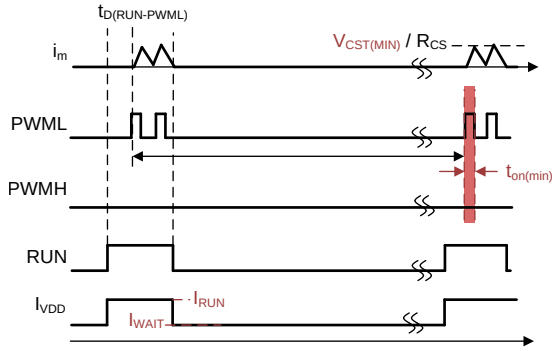

Figure 10. PWM Pattern in SBP

7.4.8 Startup Sequence

Figure 11 shows the simplified block diagram, and Figure 12 addresses the startup sequence. The detailed description on the startup waveforms is :

1. Time internal A: The two internal power-path switches connect SWS, VDD, and HVG pins together, so the depletion FET (Q_s) starts to source a charge current (i_{sws}) from V_{sw} to the VDD capacitor (C_{VDD}). Before V_{VDD} reaches to around 0.55 V, i_{sws} is limited to around tens of μA by an internal current-limiting resistor in series with one power path switch to prevent potential damage if C_{VDD} or VDD pin is shorted.
2. Time internal B: After V_{VDD} rises above 0.55 V, the internal current-limiting resistor is switched to a smaller resistance, so i_{SWS} is increased to around hundreds of μA. Then, the rising slope of V_{VDD} becomes sharper. The voltage difference between SWS and HVG pins is close to the threshold voltage of Q_s ($V_{th(Qs)}$).
3. Time internal C: As V_{VDD} reaches $V_{VDD(on)}$ of 17.5 V, one of the two power-path switches turns off to disconnect source pin of Q_s from C_{VDD}, and the other turns off gate-to-source connection of Q_s. Then, the 5V regulator connected to REF pin starts to charge up the reference capacitor (C_{REF}) to 5 V. Moreover, another power-path switch connects a current-limited 11-V regulator to the HVG pin. The voltage on the HVG pin capacitor (C_{HVG}) starts to discharge to the 11-V regulation.
4. Time internal D: Once V_{HVG} is settled to 11 V, RUN goes high and UCC28780 enters in run state with i_{VDD} = i_{RUN}.
5. Time internal E: There is a 2.2-μs delay from RUN going high to PWML starting switch to wake up half-bridge driver and UCC28780 first.
6. Time internal F: This is the soft increment region of peak magnetizing current. The first purpose is to limit the supply current if output is failed short at the beginning of V_o soft-start. The second purpose is to push the switching frequency higher than the audible noise range during repetitive startup situations. At the beginning of V_o soft-start, the peak current is limited by two V_{CST} thresholds. The first threshold $V_{CST(SM1)}$ is 0.25 V and the following second threshold $V_{CST(SM2)}$ is 0.6 V. The peak current threshold changes from $V_{CST(SM1)}$ to $V_{CST(SM2)}$ as the VS pin voltage exceeds 0.28 V. Also, when V_{CST} = $V_{CST(SM1)}$, PWMH is disabled, and the first three PWML pulses are forced to stay at this current level. Finally, in case of the inability to build up V_o with $V_{CST(SM1)}$ at beginning due to excessively large output capacitor and/or constant-current output load, there is an internal time-out of 1ms to force V_{CST} switched to $V_{CST(SM2)}$.
7. Time internal G: As VS-pin voltage rises above 0.66 V, V_{CST} is allowed to reach $V_{CST(max)}$ of 0.8 V, so the V_o rising slope becomes sharper. As PWML is on, i_{VDD} is higher than i_{RUN}, because the 5-V regulator between VDD and REF pins provides the line-sensing current pulse (i_{VSL}) on VS pin to sense V_{bulk} condition.

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8. Time internal H: V_o and V_{CST} settle, and the auxiliary winding takes over the VDD supply

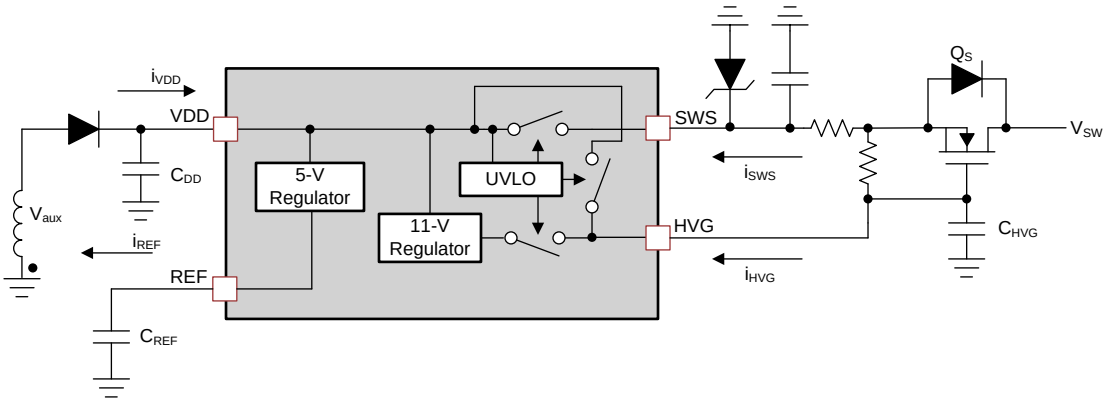

Figure 11. Functional Startup Block Diagram (Patent Pending)

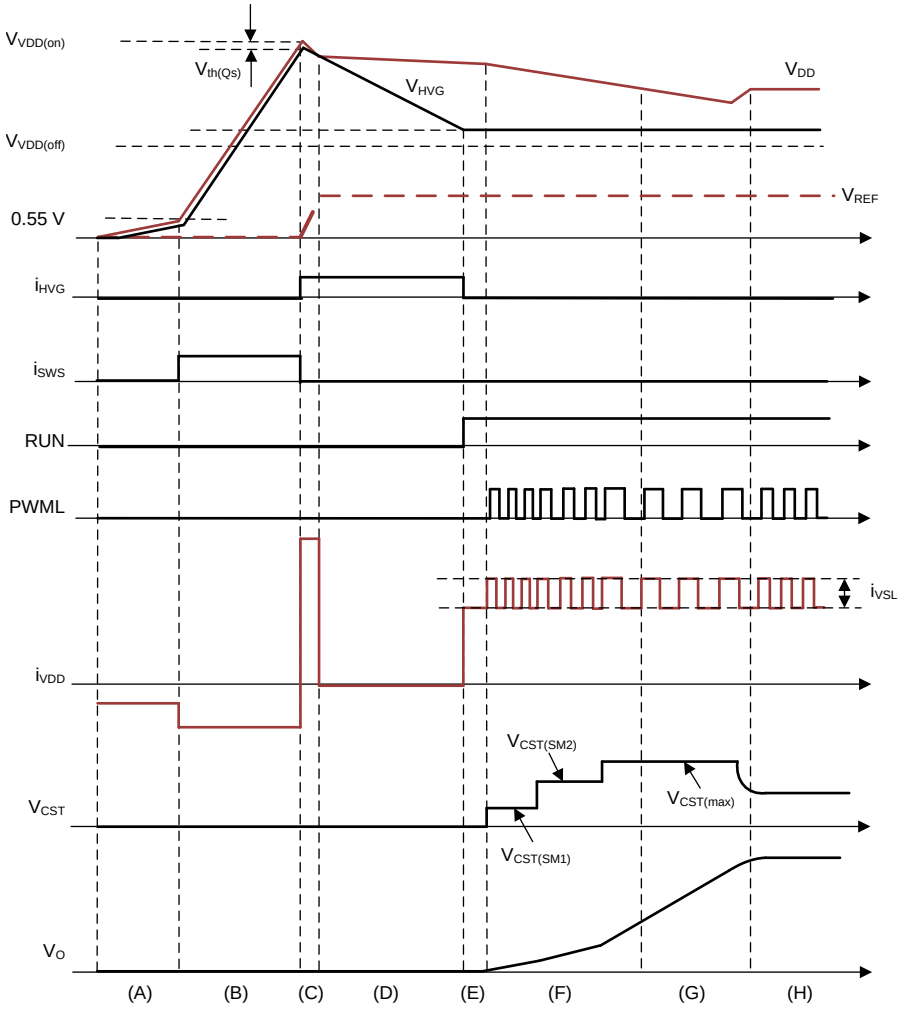

Figure 12. Startup Timing Waveforms

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7.4.9 System Fault Protection

The UCC28780 provides extensive fault protection. The protection features are summarized in Table 2.

Table 2. System Fault Protection

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
VDD UVLO	VDD voltage	$V_{VDD(off)} \le V_{VDD} \le V_{VDD(on)}$	none	UVLO Reset
Over power protection (OPP)	CS voltage	$V_{CST(OPP)} \le V_{CST} \le V_{CST(max)}$	t_{OPP} (160 ms)	t_{FDR} restart (1.5s)
Peak current limit (PCL)	CS voltage	$V_{CST} \le V_{CST(max)}$		
Over current protection (OCP)	CS voltage	$V_{CS} \ge V_{OCP}$	3 PWML pulses	t_{FDR} restart
Short circuit protection (SCP)	CS, VS, and VDD voltages	(1) $V_{VDD} = V_{VDD(off)}$ & $V_{CST} \ge V_{CST(OPP)}$ (2) $V_{VDD} = V_{VDD(off)}$ & $V_{VS} \le 0.6$ V	$\le t_{OPP}$	t_{FDR} restart
Over voltage protection (OVP)	VS voltage	$V_{VS} \ge V_{OVP}$	3 PWML pulses	t_{FDR} restart
Brown-in detection	VS current	$I_{VSL} < I_{VSL(RUN)}$	3 PWML pulses	UVLO reset
Brown-out detection	VS current	$I_{VSL} < I_{VSL(STOP)}$	t_{BO} (60ms)	UVLO reset
Over temperature protection (OTP)	NTC voltage	$R_{NTC} \le R_{NTCTH}$	3 PWML pulses	UVLO reset until $R_{NTC} \ge R_{NTCR}$

7.4.9.1 Brown-In and Brown-Out

The VS pin senses the voltage of the auxiliary winding during the on-time of PWML to detect an under-voltage condition of the input AC line. When the bulk voltage (V_{bulk}) is too low, the UCC28780 will stop switching and no V_o restart attempt is made until the AC input line voltage is back into normal range. As Q_L turns on with PWML, the auxiliary winding voltage (V_{aux}) is equal to V_{bulk} divided by primary-to-auxiliary turns ratio (N_{PA}) of the transformer, which is N_P/N_A, and V_{aux} creates a line-sensing current (i_{VSL}) out of the VS pin flowing through the upper resistor of the voltage divider on VS pin (R_{VS1}). With i_{VSL} proportional to V_{bulk}, it can be used to compare against two under-voltage thresholds, $i_{VSL(RUN)}$ and $i_{VSL(STOP)}$.

The target brown-in AC voltage ($V_{ac(BI)}$) can be programmed by the proper selection of R_{VS1}. For every UVLO cycle of VDD, there are at least three initial test pulses from PWML to check i_{VSL}. If $i_{VSL} < i_{VSL(run)}$ for three consecutive PWML pulses, the controller stops switching, the RUN pin goes low, and a new UVLO start cycle is initiated after V_{VDD} reaches $V_{VDD(off)}$. On the other hand, if $i_{VSL} > i_{VSL(RUN)}$ is qualified, V_o soft start sequence will be initiated.

$$R_{VS1} = \frac{V_{ac(BI)}\sqrt{2}}{N_{PA} \times i_{VSL(RUN)}} = \frac{N_A}{N_P}\frac{V_{ac(BI)}\sqrt{2}}{353\mu A} \tag{11}$$

The brown-out AC voltage ($V_{ac(BO)}$) is set internally by 90% of $V_{ac(BI)}$, which provides enough hysteresis to compensate for possible sensing errors though the auxiliary winding. A 60-ms timer is used to bypass the effect of line ripple content on the i_{VSL} sensing. Only when the $i_{VSL} < i_{VSL(STOP)}$ condition lasts longer than 60 ms, i.e. typically three line cycles of 50 Hz, the brown-out fault will be triggered. The fault is reset after V_{VDD} reaches $V_{DD(off)}$. Figure 13 shows an example the timing sequence of brown-in and brown-out protections.

$$V_{ac(BO)} = \frac{i_{VSL(STOP)}}{i_{VSL(RUN)}} V_{ac(BI)} = 0.9 \times V_{ac(BI)} \tag{12}$$

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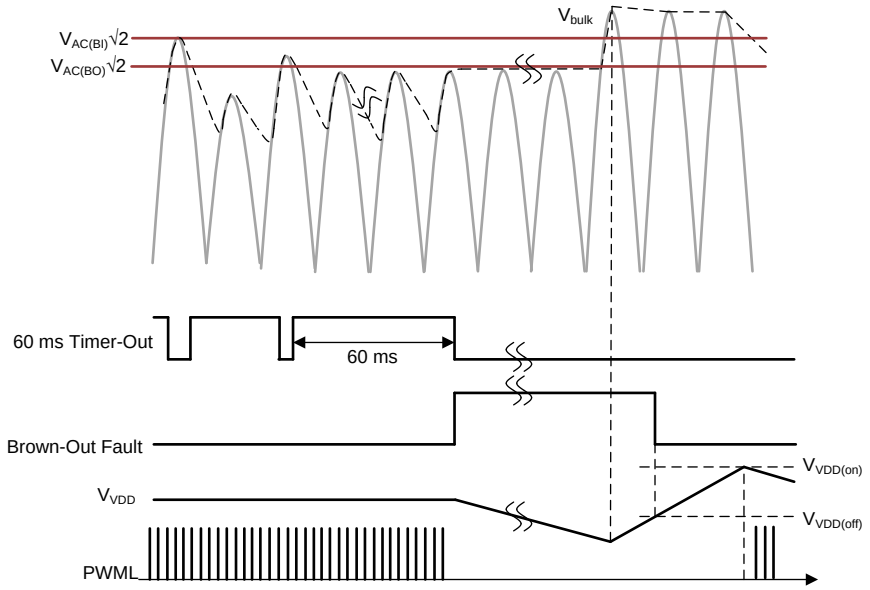

Figure 13. Timing Diagram of Brown In/Out

7.4.9.2 Output Over Voltage Protection

VS pin also senses the voltage of auxiliary winding to respond to an over-voltage condition of V_o. The UCC28780 will stop switching when V_o is too high. Following the output over-voltage detection, there is a 1.5-s fault recovery time (t_{FDR}) before any V_o restart attempt is made. As Q_L turns off, the settled V_{aux} is equal to (V_o+V_f) x N_{AS}, where N_{AS} is the auxiliary-to-secondary turns ratio of the transformer, N_A/N_S. The V_S pin senses V_{aux} though the R_{VS1} and R_{VS2} divider, so the pin voltage (V_{VS}), proportional to V_o, is compared with an internal OVP threshold (V_{OVP}). If V_{VS} > V_{OVP} is qualified for three consecutive PWML pulses, the controller stops switching, brings RUN low, and initiates a 1.5-s time out. During this time, only the UVLO-cycle of VDD is active, there are no test PWML pulses at all. After the time out is completed and V_{DD} reaches the next $V_{DD(off)}$, a normal start sequence begins. The calculation of R_{VS2} is

$$R_{VS2} = \frac{R_{VS1} \times V_{OVP}}{N_{AS} \times (V_{O(OVP)} + V_f) - V_{OVP}} = \frac{R_{VS1} \times 4.6V}{(N_A / N_S)(V_{O(OVP)} + V_f) - 4.6V} \quad (13)$$

The long time out helps to protect the power stage components from the large current stress during every V_o restart. Conceptually, if there is a large voltage difference between the clamp capacitor voltage (V_{clamp}) and the reflected voltage, N_{PS}x(V_o+V_f), a large balance current can flow through the clamp switch (Q_H) and secondary rectifier, as the first PWMH pulse turns on Q_H. The 1.5-s time allows V_{clamp} to drop to a safe lower voltage level through a bleeding resistor (R_{bleed}) in parallel with C_{clamp}. A large R_{bleed} can be used with the long time out, so there is no significant adverse effect on standby power. For example, to discharge V_{clamp} to 10% of the normal level in 1.5 s, only 3 mW of additional standby power is added with R_{bleed} = 2.8 MΩ and C_{clamp} = 220 nF. Figure 14 illustrates the timing sequence as V_{clamp} is discharged to a residual voltage ($V_{residual}$) in 1.5 s.

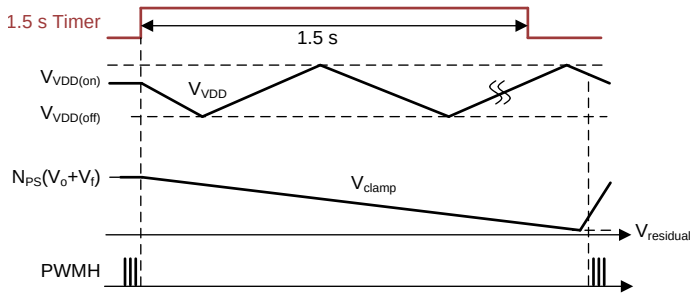

Figure 14. Timing Diagram of C_{clamp} Discharging During 1.5-s Recovery Time

7.4.9.3 Over Temperature Protection with NTC

The UCC28780 uses an external NTC resistor tied to the NTC pin to program a thermal shutdown temperature near the hotspot of the ACF. The NTC shutdown threshold of 1 V with an internal 100-μA current source results in a 10-kΩ thermistor shutdown threshold. As the NTC resistance stays lower than 10 kΩ for more than three consecutive PWML pulses, an OTP fault event is triggered, and the 1-V threshold is increased to 2.25 V. Since the NTC resistance has to increase above 22.5 kΩ to reset the OTP fault, this threshold change provides a safe temperature hysteresis to help the hot-spot temperature cool down before a V_o restart, reducing the thermal stress to the ACF components. This pin can also be used as an electrical shutdown function by shorting this pin with a control switch to GND. With the pin shorted, V_{VDD} performs UVLO cycling, and there is at least three consecutive PWML pulses generated to check the state. The NTC pin can be left floating or tied to the REF pin if not used.

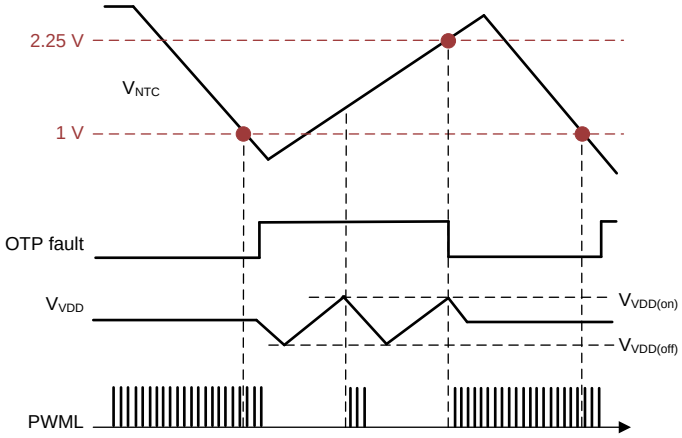

Figure 15. Timing Diagram of OTP with NTC

7.4.9.4 Programmable Over-Power Protection

The over-power protection (OPP) enables the ACF to operate in an over-power condition for a limited amount of time, so the UCC28780 can support a power stage design with peak power requirements, which might be needed in a notebook or printer adapter. As shown in Figure 16, when V_{CST} is higher than the threshold voltage of the OPP curve, a 160-ms timer is running. If V_{CST} remains higher than the OPP threshold continuously for 160 ms, the long 1.5-s timer starts and the controller stays in fault state without switching. This long recovery time reduces the average current during sustained over-power event. The system benefits includes a reduction in the thermal stress of high density adapters, protecting the USB cable, and helping to meet the Limited Power Source (LPS) requirement in IEC60950 standard.

The OPP function uses i_{VSL} as a line feedforward signal to vary the threshold level depending on V_{bulk}, in order to stabilize the OPP trigger point over a wide line range. The UCC28780 allows programing of the OPP curve by adding a line-compensation offset voltage on the CS pin through a resistor (R_{OPP}) connected between CS pin and current-sense resistor (R_{CS}). An internal current source flowing out of CS pin creates the offset voltage on R_{opp}. This current level is equal to i_{VSL} divided by a constant gain of K_{LC}. As R_{OPP} increases, the OPP trigger point becomes lower at high line, so lower peak magnetizing current is allowed to run continuously.

The highest threshold of OPP curve ($V_{CST(OPP1)}$) of 0.6 V helps to determine R_{CS} value at $V_{bulk(min)}$.

$$R_{CS} = \frac{V_{CST(OPP1)}}{\frac{P_{o(OPP)}}{V_{bulk(\min)}\eta}\frac{2}{D_{\max}} - \frac{V_{bulk(\min)}t_{d(CST)}}{L_m}} \quad (14)$$

where $P_{o(OPP)}$ is the output power triggers OPP, and $t_{d(CST)}$ is the sum of all delays in peak current loop which contributes additional peak current overshoot. $t_{d(CST)}$ consists of propagation delay of low-side driver, current sense filter delay (R_{OPP} x C_{CS}), internal CS comparator delay ($t_{D(CS)}$), and nonlinear capacitance delay of Q_L. After R_{CS} is determined, R_{OPP} can be adjusted to keep similar OPP point at highest line. Note that setting OPP trigger point too far away from the full power may introduce more challenge on thermal-design power, since ACF runs continuously with more power as long as the corresponding peak current is slightly less than OPP threshold.

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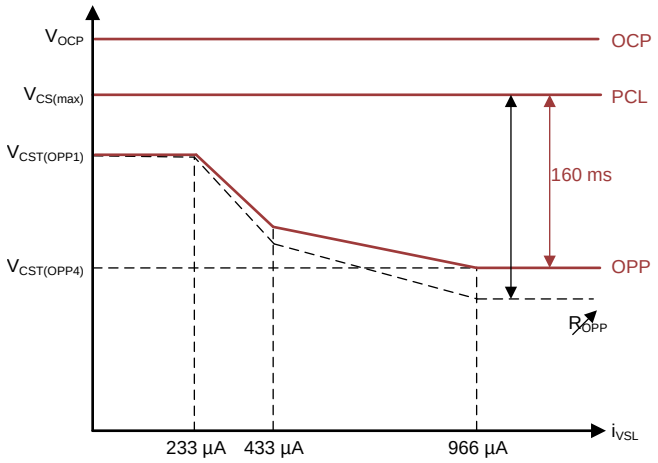

Figure 16. CS-Pin Related Faults

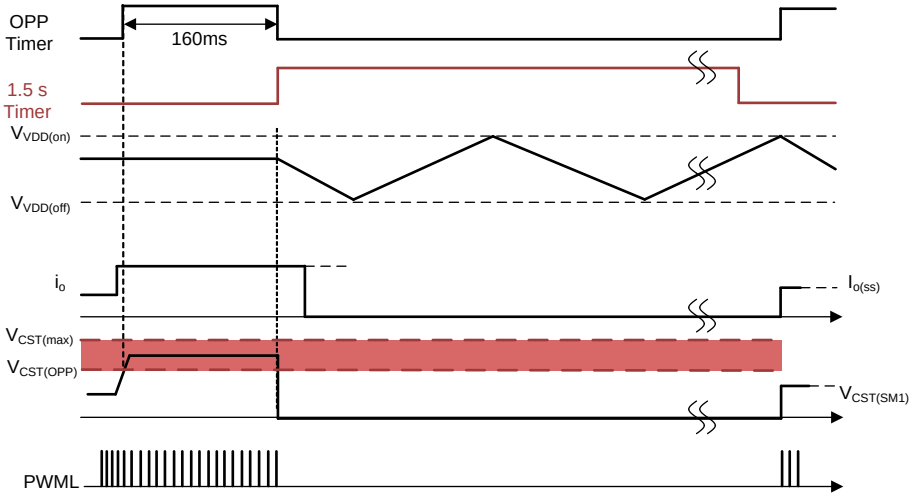

Figure 17. Timing Diagram of OPP

7.4.9.5 Peak Current Limit

The peak current threshold of the OPP curve is used to initiate the 160-ms timer, while the peak current limit (PCL) determines the highest controllable peak current of the peak current loop, $V_{CST(max)}$ = 0.8 V. In another words, this feature provides the highest "short duration" peak power ($P_{o(max)}$) that the ACF can reach. For example, to supply a highest peak power of 150%, R_{CS} should be chosen to ensure that the peak current at 150% load and $V_{bulk(min)}$ must not be above $V_{CST(max)}$. Then, the threshold of the OPP power ($P_{o(opp)}$) can be programmed to around 112% to support 150% peak power design, based on the following equation. Additionally, before V_o reaches steady state during a V_o soft-start, the highest V_{CST} can also reach to $V_{CST(max)}$. The transformer must have enough design margin separating its maximum flux density from the saturation limit of the core material under the peak current level in PCL.

$$P_{o(OPP)} = \frac{V_{CST(OPP1)}}{V_{CST(max)}} P_{o(max)} = \frac{0.6V}{0.8V} P_{o(max)} \quad (15)$$

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7.4.9.6 Short-Circuit Protection

When an output short-circuit is applied, the peak current will reach the PCL limit and trigger the 160-ms OPP fault timer. During this event, the VDD power supply will be lost due to the auxiliary winding voltage being close to 0 V. Without additional short-circuit detection, if V_{VDD} reaches $V_{VDD(off)}$ before the 160-ms timeout, then the 1.5-s recovery time for the OPP fault cannot be triggered but only a UVLO recycle is performed. To remedy this scenario, as V_{VDD} reaches $V_{VDD(off)}$, UCC28780 checks two additional parameters to identify the short circuit event, and will initiate the 1.5-s recovery without waiting for 160 ms to expire. Specifically, when V_{VDD} reaches $V_{VDD(off)}$, if either V_{CST} is greater than the OPP threshold or the VS pin voltage is less than 0.6 V, the long recovery delay will be initiated. With this additional layer of intelligence, the average load current during continual short circuit event can be greatly reduced, and thus the thermal stress on the power supply.

7.4.9.7 Over Current Protection

The UCC28780 operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.15 V to 0.8 V. If the CS-pin voltage exceeds the 1.2-V over-current level, any time after the internal leading edge blanking time (t_{CSLEB}) and before the end of the transformer demagnetization, for three consecutive PWML cycles, the device stop switching, RUN pin goes low, and 1.5-s recovery time is initiated. Silimilar to OVP, OPP, and SCP, only the UVLO-cycle of VDD is active, there are no test PWML pulses at all. After the 1.5-s time out is completed and V_{DD} reaches the next $V_{DD(off)}$, a normal start sequence begins.

7.4.9.8 Thermal Shutdown

The internal over-temperature shutdown threshold is higher than 125°C. If the junction temperature of the device reaches this threshold, the device initiates a UVLO reset and re-start fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats. This internal protection is not suitable to substitute for the NTC for hotspot temperature protection. The NTC thermistor can provide more accurate temperature sensing with less compromise on PCB layout.

7.4.9.9 Pin Open/Short Protection

As summarized in the following table, UCC28780 strengthens the protections of several critical pins under open and short conditions, such as CS, HVG, RDM and RTZ pins.

Table 3. Protections for Open and Short of Critical Pins

PROTECTION	SENSING	CONDITION	DELAY TO ACTION	ACTION
CS pin short	PWML on-time @ first PWML pulse only	> 2 µs (SET = 5 V)	none	UVLO reset
		> 2 µs (SET = 0 V, R_{RDM} ≥ 55 kΩ)		
		> 1 µs (SET = 0V, R_{RDM} < 55 kΩ)		
CS pin open	CS voltage	V_{CS} > 1.2 V	3 PWML pulses	t_{FDR} restart (1.5 s)
HVG pin open	HVG voltage @ $UVLO_{ON}$	V_{HVG} < or =12 V in less than 10 µs after V_{VDD} reaches $V_{VDD(on)}$	none	UVLO reset
HVG pin high	HVG voltage	V_{HVG} > 14 V	none	UVLO reset
RDM pin short	RDM current @ $UVLO_{ON}$	V_{RDM} = 0 V, self-limited i_{RDM}	none	UVLO reset
RDM pin open	RDM current @ $UVLO_{ON}$	RDM = Open	none	UVLO reset
RTZ pin short	RDM current @ $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited i_{RTZ}	none	UVLO reset
RTZ pin open	RDM current @ $UVLO_{ON}$	RTZ = Open	none	UVLO reset

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Typical application of a high-frequency active-clamp AC-to-DC flyback converter that enables high density AC-to-DC power supply design that complies with stringent global efficiency standards with both Silicon (Si) and Gallium Nitride (GaN) power FETs.

8.2 Typical Application Circuit for GaN FET

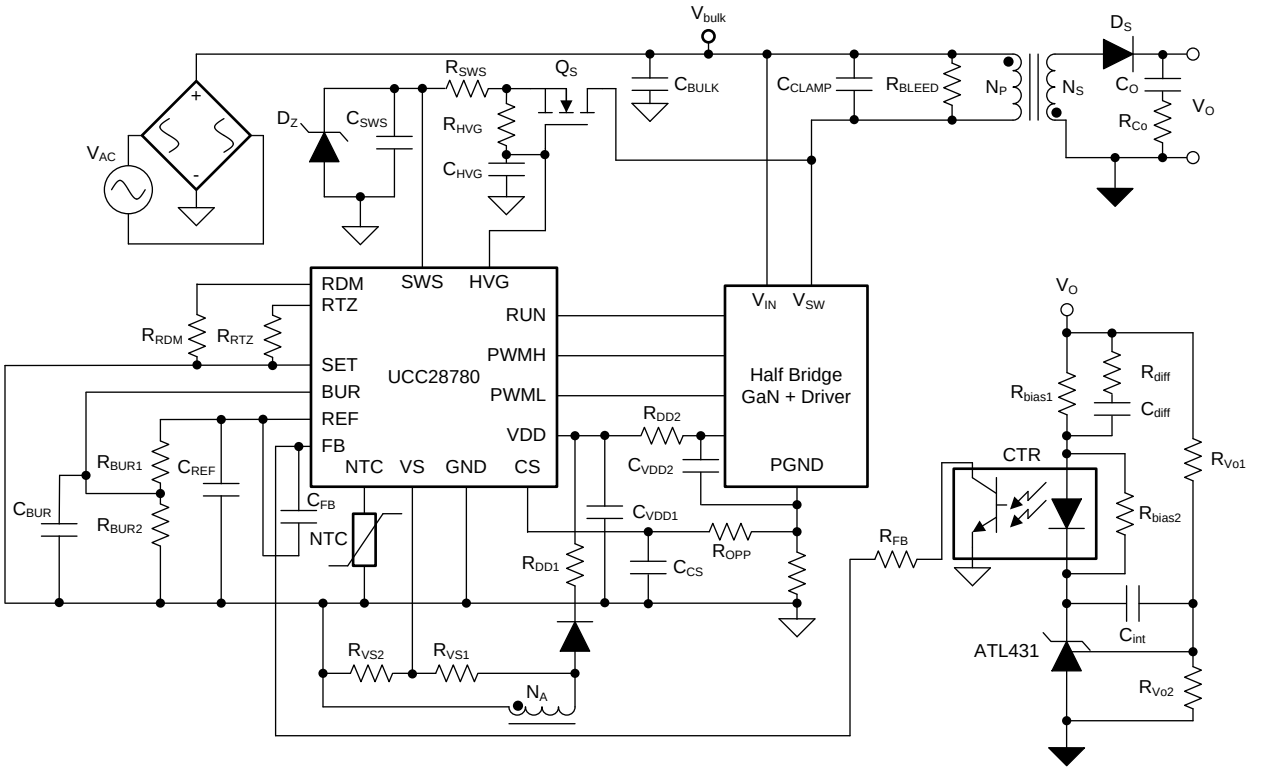

Figure 18. Typical Application Circuit for GaN FET

Typical Application Circuit for GaN FET (continued)

8.2.1 Design Requirements

Table 4. UCC28780 Electrical Performance Specifications for GaN FET

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input line voltage (RMS)		85	115/230	265	V
f_{LINE}	Input line frequency		47	50/60	63	Hz
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = nom, I_{OUT} = nom	19.6	20	20.4	V
V_{OUT_pp}	Output ripple voltage	V_{IN} = 115 V RMS, I_{OUT} = nom		260		mVpp
		V_{IN} = 230 V RMS, I_{OUT} = nom		180		
I_{OUT}	Output current	V_{IN} = min to max		2.25		A
P_{OUT_opp}	Over-power protection power limit	V_{IN} = min to max		48		W
t_{OPP}	Over-power protection duration	V_{IN} = min to max, P_{OUT} = P_{OUT_opp}		150		ms
SYSTEMS CHARACTERISTICS						
η	Full-load efficiency	V_{IN} = 115 V / 230 V RMS, I_{OUT} = 2.25A		94%		
η	4-point average efficiency	V_{IN} = 115 V / 230 V RMS, I_{OUT} = 25%, 50%, 75% and 100% nom		93.5%		
η	10% Efficiency	V_{IN} = 115 V / 230 V RMS, I_{OUT} = 10% nom		88%		
T_{AMB}	Ambient operating temperature range	V_{IN} = min to max, I_{OUT} = min to max		25		°C
D_{PWR}	Power Density	Board Dimensions 2.320 x 1.320 x 0.681 in^3		21.5		W / $(in)^3$

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8.2.2 Detailed Design Procedure

8.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

In an offline application, the input bulk capacitor (C_{bulk}) should be sized for the minimum input AC line voltage ($V_{AC(min)}$) and minimum voltage of input bulk capacitor ($V_{bulk(min)}$). If 85 Vac is the lowest normal AC line, 75 Vac is recommended as $V_{AC(min)}$ with UCC28780.

$$C_{bulk(\min)} = \frac{\frac{P_o}{\eta} \times [0.5 + \frac{1}{\pi} \times \arcsin(\frac{V_{bulk(\min)}}{\sqrt{2} \times V_{AC(\min)}})]}{(2 \times V_{AC(\min)}{}^2 - V_{bulk(\min)}{}^2) \times f_{Line}} \quad (16)$$

8.2.2.2 Transformer Calculations

8.2.2.2.1 Primary -to -Secondary Turns ratio (N_{PS})

(1) Maximum N_{PS} ($N_{PS(max)}$) is limited by the maximum derated drain-to-source voltage of Q_L ($V_{DS\_QL(max)}$). In the expression below, ΔV_{clamp} is the voltage above the reflected output voltage. It can be either the ripple voltage of C_{clamp} in AAM mode, or the voltage over-charge of C_{clamp} by the L_k energy as Q_H is disabled in LPM mode. $V_{O(max)}$ is the maximum output voltage, and V_f is the forward voltage drop of secondary rectifier.

$$N_{PS(\max)} = \frac{V_{DS\_QL(\max)} - V_{bulk(\max)} - \Delta V_{clamp}}{V_o + V_f} \quad (17)$$

(2) Minimum N_{PS} ($N_{PS(min)}$) is limited by the maximum derated drain-to-source voltage of the secondary rectifier ($V_{DS\_SR(max)}$). In the expression for $N_{PS(min)}$, ΔV_{spike} should account for any additional voltage spike higher than $V_{bulk(max)}/N_{PS}$ that occurs when Q_H is active and turns off at non zero current situation in AAM mode.

$$N_{PS(\min)} = \frac{V_{bulk(\max)}}{V_{DS\_SR(\max)} - V_o - \Delta V_{spike}} \quad (18)$$

(3) Since the high-frequency transformer is a core-loss limited design instead of saturation-limited design, the minimum duty cycle (D_{min}) at $V_{bulk(max)}$ is more important. Lower D_{min} increases core loss at $V_{bulk(max)}$, so this constraint creates another limitation on $N_{PS(min)}$.

$$D_{\min} = \frac{N_{PS(\min)}(V_o + V_f)}{V_{bulk(\max)} + N_{PS(\min)}(V_o + V_f)} \quad (19)$$

(4) The winding loss distribution between the primary and secondary side of transformer is the final consideration. As N_{PS} increases, primary RMS current reduces, while secondary RMS current increases.

8.2.2.2.2 Primary Magnetizing Inductance (L_m)

After N_{PS} is chosen, L_m can be determined based on minimum switching frequency ($f_{sw(min)}$) at $V_{bulk(min)}$, maximum duty cycle (D_{max}), and output power at full load current ($P_{o(FL)}$). The selection of minimum switching frequency ($f_{sw(min)}$) has to consider the impact on full-load efficiency and EMI filter design.

$$L_m = \frac{D_{\max}{}^2 V_{bulk(\min)}{}^2 \eta}{2 f_{sw(\min)} P_{o(FL)}} \quad (20)$$

$$D_{\max} = \frac{N_{PS}(V_o + V_f)}{V_{bulk(\min)} + N_{PS}(V_o + V_f)} \quad (21)$$

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8.2.2.2.3 Flux Density Design

The turn number on the primary side of the transformer (N_P) is determined by two design considerations:

(1) The maximum flux density (B_{max}) must be kept below the saturation limit (B_{sat}) of the magnetic core under the highest peak magnetizing current ($i_{m+(max)}$) condition. When i_{FB} = 0 A, such as V_o soft-start or step-up load transient, the peak magnetizing current will reach to its highest level ($i_{m+(max)}$), since $V_{CST} = V_{CST(max)}$. $i_{m+(max)}$ can be calculated based on the output power triggering an OPP fault ($P_{o(OPP)}$) with $V_{CST} = V_{CST(OPP1)}$ at $V_{bulk(min)}$. After N_P is chosen, N_S can be calculated through N_{PS}.

$$B_{\max} = \frac{L_m i_{m+(\max)}}{N_P A_e} < B_{sat} \tag{22}$$

$$i_{m+(\max)} = \frac{2P_{o(OPP)}}{D_{\max} V_{bulk(\min)} \eta} \frac{V_{CST(\max)}}{V_{CST(OPP1)}} \tag{23}$$

(2) The AC flux density (ΔB) affects the core loss of a transformer. For transition-mode ACF, the core loss at high line is usually highest, since the switching frequency is highest and duty cycle is smallest for a given load condition. The following equation is the ΔB calculation including the negative current contribution, used to put into the Steinmetz's equation for more accurate core loss estimation.

$$\Delta B = \frac{L_m (i_{m+} - i_{m-})}{N_P A_e} \tag{24}$$

$$i_{m+} = \sqrt{\frac{2P_{o(FL)}}{\eta L_m f_{sw}} + i_{m-}^{\,2}} \quad , \quad i_{m-} = -\sqrt{\frac{C_{sw}}{L_m}} V_{bulk} \tag{25}$$

8.2.2.2.4 Auxiliary-to -Secondary Turns Ratio (N_{AS})

1. V_{VDD} needs to be lower than the maximum derating voltage of VDD pin ($V_{VDD(max)}$) at maximum output voltage ($V_{o(max)}$).

$$N_{AS(\max)} = \frac{N_{A(\max)}}{N_S} = \frac{V_{VDD(\max)}}{V_{o(\max)} + V_f} \tag{26}$$

2. V_{VDD} needs to be higher than the turnoff voltage ($V_{VDD(off)}$) at the minimum sustained output voltage ($V_{o(min)}$).

$$N_{AS(\min)} = \frac{N_{A(\min)}}{N_S} = \frac{V_{VDD(off)}}{V_{o(\min)} + V_f} \tag{27}$$

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8.2.2.3 Clamp Capacitor Calculations

The design tradeoff between conduction loss reduction and turn-off switching loss of Q_H needs to be considered. Higher C_{clamp} results in less RMS current flowing through the transformer windings and switching devices, so the conduction loss can be reduced. However, a higher C_{clamp} design results in Q_H turning off before the clamp current returns to 0A. The condition of non zero current switching (ZCS) will increase the turn-off switching loss of Q_H. This will be aggravated if the turn-off speed of Q_H is not fast enough. Therefore, C_{clamp} needs to be fine tuned based on the loss attribution.

When silicon FET is used as Q_H, higher C_{clamp} is preferred, because of the two reasons: (1) the nonlinear C_{oss} of Q_H helps to reduce the turn-off loss under non ZCS turn-off condition, (2) turning off at high di/dt condition introduces additional circulating energy from leakage inductance (L_k) to help the reduction of negative magnetizing current. If the resonance between L_k and C_{clamp} is designed to be completed by the time Q_H is turned off, the clamp current should reach to 0 A around three quarters of the resonant period. The following equation can be used to design C_{clamp} for obtaining ZCS at $V_{bulk(min)}$ and full load. Notice that this design will result in non-ZCS condition at $V_{bulk(max)}$, since the switching frequency at $V_{bulk(max)}$ is higher in transition-mode operation. A Low-ESR clamp capacitor is recommended to minimize the conduction loss. If a ceramic capacitor is used as the low-ESR capacitor, the DC bias effect on the capacitance reduction needs to be considered.

$$C_{clamp(\max)} = \frac{1}{L_k}\left[\frac{2L_m i_{m+(FL)}}{3\pi N_{PS}(V_o + V_f)}\right]^2 \tag{28}$$

When GaN FET is used as Q_H, there is still a chance to use higher C_{clamp} design to reduce RMS current without sacrificing the turn-off switching loss too much, by taking the advantage of current dipping effect with a silicon-FET synchronous rectifier (SR). After Q_L turns off, the smaller primary junction capacitance from GaN FET and the higher reflected junction capacitance from silicon SR create a mismatch of the voltage ramping speed between primary and secondary windings of the ACF transformer. This effect makes the initial value of resonance current flowing through the primary winding and Q_H not starting from the peak magnetizing current but a lot lower level instead. Since lower peak clamp current results in smaller negative peak clamp current, the turn-off switching loss can be reduced under non-ZCS condition at high line.

ADVANCE INFORMATION

8.2.2.4 Bleeding Resistor Calculations

A large R_{bleed} is used to discharge clamp capacitor voltage to a residual voltage ($V_{residual}$) during the 1.5-s fault delay recovery time (t_{FDR}). After the converter recovers from the fault mode, lower $V_{residual}$ reduces the maximum short current ($i_{short(max)}$) flowing through the switching devices within their respective safe operating areas, even if the output voltage is shorted. $i_{short(max)}$ can be determined by calculating target $V_{residual}$ based on the de-rated maximum pulse current of Q_H or the SR current reflected to the primary side, depending on which is lower.

$$R_{bleed} = \frac{t_{FDR}}{C_{clamp} \ln(\frac{NV_o + \Delta V}{V_{residual}})} \quad (29)$$

$$V_{residual} \approx i_{short(\max)} \sqrt{\frac{L_k}{C_{clamp}}} \quad (30)$$

8.2.2.5 Output Capacitor Calculations

The output capacitor (C_o) is often determined by the transient-response requirement from the no-load condition. For a target output voltage undershoot (ΔV_o) with the load step-up transient of ΔI_o, the minimum C_o ($C_{o(min)}$) can be expressed as

$$C_{o(\min)} = \frac{\Delta I_o t_{RESP}}{\Delta V_o} \quad (31)$$

where t_{RESP} is the time delay from the moment ΔI_o is applied to the moment when i_{FB} falls below 1 μA.

Secondly, the maximum ESR of output capacitor ($R_{Co(max)}$) is often limited by the maximum output peak-to-peak voltage ripple ($V_{o(pk-pk)}$), where the worst-case output ripple is considered at full load and $V_{bulk(min)}$. If the high-frequency switching ripple at output is mainly dominated by the ESR ripple, a sinusoidal approximation of the secondary current waveform of the ACF is made to calculate the ESR requirement, based on target output ripple specification.

$$R_{Co(\max)} = \frac{2 \times (1 - D_{\max} - f_{sw(\min)} \pi \sqrt{L_m C_{sw}}) \times V_{o(pk-pk)}}{\pi \times I_{o(FL)}} \quad (32)$$

ADVANCE INFORMATION

8.2.2.6 Calculation of ZVS Sensing Network

There are four components in the application circuit to help the depletion MOSFET (Q_s) perform ZVS sensing safely, C_{SWS}, R_{SWS}, D_Z, and R_{HVG}. Design considerations and selection guidelines for the values of these components are given here.

At the rising edge of switch node, the fast dV/dt coupling though the drain-to-source capacitance of Q_s ($C_{oss(Qs)}$) generates a charge current flowing into the capacitive loading of the Q_s source pin. The result is a voltage overshoot on both the SWS pin and across the gate-to-source of Q_s ($V_{GS(Qs)}$). The SWS pin, with an absolute maximum voltage of 38 V, can handle higher voltage stress than $V_{GS(Qs)}$. Therefore, a capacitor between the SWS pin and GND (C_{SWS}) should be selected properly to prevent the voltage overshoot from damaging the Q_s gate. Since $C_{oss(Qs)}$ and C_{SWS} form a voltage divider, the minimum C_{SWS} ($C_{SWS(min)}$) can be derived as

$$C_{SWS(\min)} = \frac{C_{oss(Qs)}[V_{bulk(\max)} + N_{PS}(V_o + V_f)]}{V_{HVG} + V_{GS\_\max(Qs)}} - C_{Dz} \tag{33}$$

where $V_{GS\_max(Qs)}$ is the de-rated maximum gate-to-source voltage of Q_s, V_{HVG} is the steady-state voltage level of 11 V, and C_{Dz} is the parasitic capacitance of TVS diode (D_z) on the SWS pin.

Without resistive damping, both the charge current on the rising edge of V_{sw} and the discharge current on the falling edge of V_{sw} are oscillatory with the parasitic inductance within the ZVS sensing network resonating with C_{SWS}. Therefore, a series resistor (R_{sws}) between SWS pin and source-pin of Q_s is used to damp out the high-frequency ringing, helping to obtain a cleaner sensing signal on the SWS pin and preventing any high-frequency current from interfering with other noise-sensitive signals. The minimum R_{SWS} ($R_{SWS(min)}$) can be calculated as:

$$R_{SWS(\min)} = 10\sqrt{\frac{L_{SWS}}{C_{SWS} + C_{Dz}}} \tag{34}$$

Where, the damping factor of 10 is the recommended for the second-order circuit. L_{SWS} is the lump parasitic inductance, including the packaging of Q_s and PCB traces connected between Q_s and SWS pin.

Based on the above design guide, even though R_{sws} and C_{sws} are sufficient to manage the voltage overshoot in normal operation, a low-capacitance TVS diode (D_z) is still highly recommended to serve as a safety backup of the ZVS sensing network. A regular Zener diode is not suitable due to its high capacitance and slow clamping response.

Based on the above equations, a general recommendation is that a 50 V C0G-type ceramic capacitor with 22 pF for C_{sws}, a chip resistor of 120 Ω for R_{SWS}, and a TVS diode with the clamp voltage between 18 V to 24 V for D_z. Too large value for R_{sws} or C_{sws} introduces a sensing delay between V_{sw} and SWS pin, so the ZVS control will pull down V_{sw} earlier than expected before the end of t_Z by unnecessarily extending t_{DM}. The recommended R_{sws} and C_{sws} values only introduce a negligible 2.6-ns delay, so the ZVS control will not be affected. Furthermore, a high-impedance discharge resistor (R_{HVG}) between the gate and source pins of Q_s helps Q_s stay in off state, where there is no switching event on V_{sw}. R_{HVG} = 1 MΩ is enough to serve the purpose. Note that too small R_{HVG} can hurt standby power, since it creates a continuous current flowing though Q_s.

ADVANCE INFORMATION

8.2.2.7 Calculation of Compensation Network

UCC28780 integrates two control concepts to benefit high-efficient operation: peak current loop control and burst ripple control. Peak current loop in AAM can be analyzed based on the linear control theory, so the compensation target is to obtain enough phase margin and gain margin for a given small-signal property of ACF power stage. For transition-mode ACF operation, the power stage can be modeled as a voltage-controlled current source charging output capacitor as shown in Figure 19, so the first-order plant characteristic and high switching frequency operation in AAM make the peak current loop very easy to stabilize.

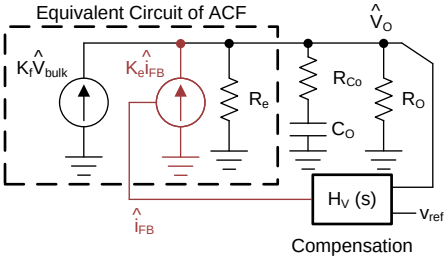


Figure 19. Small-Signal Model of ACF in AAM Loop

On the other hand, the burst mode is a ripple-based control, so the linear control theory for AAM cannot be applied. The most critical stability criterion of burst control is to make the burst ripple content of i_{FB} in-phase with the burst ripple of V_o. The fundamental frequency of burst ripple in ABM varies between 20 kHz and 40 kHz. Strong phase delay in the frequency range creates slope distortion around the intersection point between i_{FB} and i_{REF}, so the ripple regulator generates inconsistent burst off-times. As shown in Figure 20, the sub-harmonic oscillation at half of f_{BUR} is a typical phenomenon of unstable ABM loop. Two burst packets are adjacent each other and the pulse count (N_{SW}) are different by one pulse count.

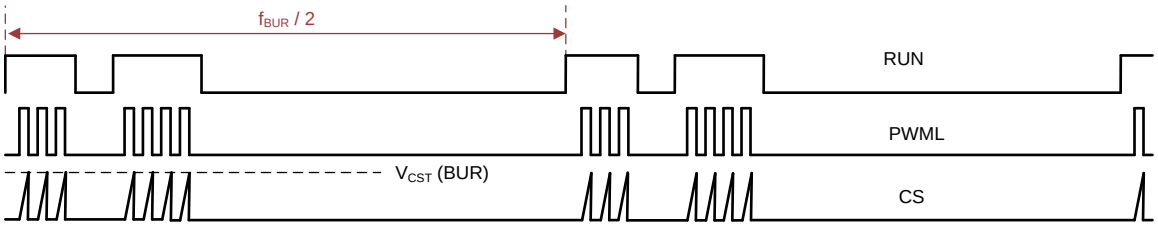


Figure 20. Typical Phenomenon of Unstable ABM Loop

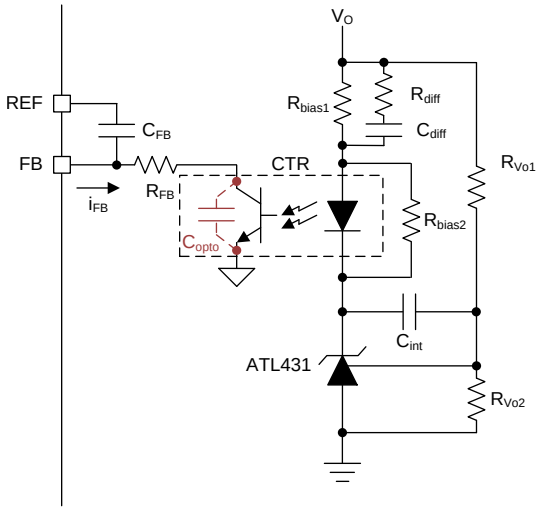


Figure 21. Compensation Network of UCC28780, H_v(s)

In order to minimize the phase delay between the two feedback signals, the transfer function from i_{FB} to V_o guides the pole/zero placement of secondary compensation network in Figure 21. In the primary-side control circuitry, two poles at ω_{FB} and ω_{opto} introduce phase delay on i_{FB}. ω_{FB} pole is formed by the internal 5-KΩ resistor in FB pin and the filter capacitor C_{FB}, while ω_{opto} pole is formed by the current-limiting resistor of FB pin (R_{FB}) and the parasitic capacitance of the optocoupler output (C_{opto}). Based on the recommended minimum C_{FB} value of 100 pF, the delay effect of ω_{FB} pole located at 318 kHz is negligible. However, ω_{opto} pole located less than 10 kHz will introduce large phase delay in the interested f_{BUR} range of ABM, since C_{opto} is in few nF range contributed by the Miller effect of collector-to-base capacitance of the BJT in optocoupler output. Therefore, an RC network (R_{diff}, C_{diff}) in parallel with R_{bias1} are used to compensate the phase delay of optocoupler, which introduce an extra pole/zero pair located at ω_{P1} and ω_{Z1} respectively. The basic design guide is to place the ω_{Z1} zero close to the ω_{opto} pole, and to place ω_{P1} pole away from highest f_{BUR}.

$$\frac{i_{FB}(s)}{V_o(s)} = \frac{CTR}{R_{bias1}} \frac{\omega_{Z0}+s}{s} \frac{1+(s/\omega_{Z1})}{1+(s/\omega_{P1})} \frac{1}{1+(s/\omega_{opto})} \frac{1}{1+(s/\omega_{FB})} \tag{35}$$

$$\omega_{Z0} = \frac{1}{R_{Vo1}C_{\text{int}}} \quad \omega_{Z1} = \frac{1}{(R_{diff}+R_{bias1})C_{diff}} \quad \omega_{P1} = \frac{1}{R_{diff}C_{diff}} \quad \omega_{opto} = \frac{1}{R_{FB}C_{opto}} \quad \omega_{FB} = \frac{1}{5K\Omega \times C_{FB}} \tag{36}$$

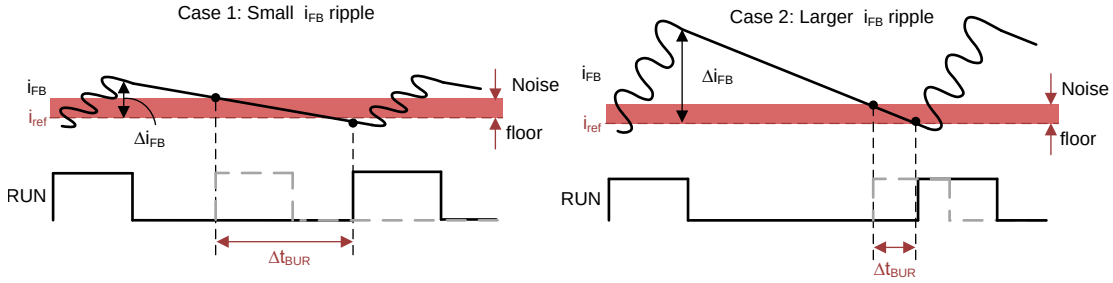


Figure 22. Effect of Signal-to-Noise Ratio of i_{FB} to ABM Operation

Another guideline of obtaining more consistent burst off-time is to maintain large enough ripple amplitude of i_{FB} in ABM mode (Δi_{FB}) for better signal-to-noise ratio. Figure 22 shows that when the noise floor alters the intersection point of each burst cycle, larger Δi_{FB} performs much less burst off-time variation if the noise floor stays the same. The minimum Δi_{FB} of 10~ 20 μA is a recommended initial design value. The ripple ratio (K_{ripple}) between Δi_{FB} and the burst voltage ripple of V_o in ABM ($\Delta V_{o(ABM)}$) is obtained by simplifying the small-signal gain of $i_{FB}(s)/V_o(s)$ transfer function between 20 kHz and 40 kHz.

$$\Delta i_{FB} = K_{ripple} \times \Delta V_{o(ABM)} \approx 10 \sim 20\mu A \tag{37}$$

$$K_{ripple} \equiv \left.\frac{i_{FB}(s)}{V_o(s)}\right|_{20kHz<f<40kHz} \approx \frac{CTR}{R_{bias1}} \frac{\omega_{opto}}{\omega_{Z1}} = \frac{CTR}{R_{bias1}} \frac{(R_{diff}+R_{bias1})C_{diff}}{R_{FB}C_{opto}} \tag{38}$$

With the above understanding on burst control, the step-by-step design procedure is:

1. R_{FB} selection needs to consider both output voltage regulation and compensation challenge on the low-frequency pole at ω_{opto}. R_{FB} must be less than the maximum value of 32 kΩ to provide a sufficient feedback current of 95 μA for the output voltage regulation in SBP mode. Besides, when R_{FB} increases close to 32 kΩ, the pole at ω_{opto} moves to lower frequency. For example, R_{FB} = 32 kΩ and C_{opto} = 2 nF result in the ω_{opto} pole located at 2.5 kHz. Such low-frequency pole forces ω_{Z1} zero designed around 2.5 kHz as well to compensate the phase delay. The challenge is that positioning ω_{Z1} at too low frequency means a large C_{diff} is required, so the high differentiation gain on the secondary-side compensator may increase noise floor of i_{FB}. Therefore, R_{FB} should be fine-tuned based on the actual noise level of a given ACF design. 10 to 20 kΩ is a recommended starting design point.

$$R_{FB(\max)} = \frac{4V - V_{CE(opto)}}{i_{FB(SBP)}} - 5k\Omega = \frac{3.6V}{95\mu A} - 5k\Omega = 32k\Omega \tag{39}$$

2. R_{bias1} is determined based on a given current transfer ratio (CTR) of optocoupler, $\Delta V_{o(ABM)}$, and target 10 μA of Δi_{FB} as example.

$$R_{bias1} = \frac{CTR}{\Delta i_{FB}} \Delta V_{o(ABM)} = \frac{CTR}{10\mu A} \Delta V_{o(ABM)} \tag{40}$$

3. C_{diff} is designed to position $\omega_{Z1} \approx \omega_{opto}$ and locate ω_{P1} at least two-times higher frequency than $2\pi \times f_{BUR(UP)}$ as example.

$$C_{diff} = \frac{1}{R_{bias1}} \frac{\omega_{P1} - \omega_{Z1}}{\omega_{P1} \times \omega_{Z1}} = \frac{1}{R_{bias1}} \frac{(4\pi f_{BUR(UP)}) - \omega_{opto}}{(4\pi f_{BUR(UP)}) \times \omega_{opto}} \tag{41}$$

4. R_{diff} is designed to position ω_{P1} two-times higher than $2\pi \times f_{BUR(UP)}$, but lower than the switching frequency in ABM. Too small R_{diff} moves ω_{P1} higher than $2\pi \times f_{sw(BUR)}$, so the high differentiation gain on the secondary-side compensator will amplify the switching ripple and increase the noise floor. Therefore, R_{diff} should be fine-tuned based on the actual noise level of a given ACF design.

$$R_{diff} = \frac{1}{\omega_{P1} C_{diff}} = \frac{1}{4\pi f_{BUR(UP)} C_{diff}} \tag{42}$$

ADVANCE INFORMATION

9 Power Supply Recommendations

The UCC28780 is intended to control active clamp flyback converters (ACF) in high efficiency offline applications, and is designed to be used with a universal AC input, from 85 VAC to 265 VAC, at 47 Hz to 63 Hz. An external depletion MOSFET connected between the switch node of ACF and the SWS/HVG pins of this controller is required to charge the VDD capacitor during start-up, and to perform ZVS sensing during normal operation. Once the V_{VDD} reaches the UVLO turn-on threshold at 17.5 V, the VDD rail should be kept within the limits of the Bias Supply Input section of the Electrical Characteristics table. To avoid the possibility that the device might stop switching, V_{VDD} must not be allowed to fall below the UVLO turn-off threshold at 10 V.

10 Layout

10.1 Layout Guidelines

10.1.1 RDM and RTZ Pins

Minimize stray capacitance to RDM and RTZ pins.

- Place R_{RDM} and R_{RTZ} as close as possible to the controller pins.
- Make opening in GND plane from below external surface pads and routes.

10.1.2 SWS Pin

Minimize stray potential noise coupling from SWS pin to noise-sensitive signals.

- Keep some distance between SWS pin and other connections
- The RC damping network (R_{sws}, C_{sws}) and the TVS diode (D_z) should be as close to the source pin of Q_s as possible instead of SWS pin, so the gate-to-source pin of Q_s can be effectively protected.
- Keep return path for di/dt current through C_{SWS} and D_z separating from IC local GND and FB signal return paths.

10.1.3 VS Pin

Minimize stray capacitance to VS pin.

- Make opening in GND plane below external surface pads and tracks

10.1.4 BUR Pin

The resistor divider (R_{BUR1}, R_{BUR2}) and the filter capacitor (C_{BUR}) on the BUR pin should to be as close to the BUR pin and IC GND as possible.

10.1.5 FB Pin

This pin can be noise-sensitive to the capacitive coupling of dV/dt switch node, or the flux coupling of magnetic components.

- Minimize the loop area for the PCB traces from the opto-coupler to the FB pin for minimizing the coupling from the magnetic field.
- Keep PCB trace away from the high dV/dt signals, such as the switch node of ACF (V_{sw}) and SWS pins. If possible, it is recommended to provide screening for the FB trace with ground planes.
- The filter capacitor between FB pin and REF pin (C_{FB}) needs to be as close to the two pins as possible.

10.1.6 GND Pin

The GND pin is the power and signal ground connection for the controller. The effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return.

- Place the decoupling and filter capacitors on VDD, REF, CS, and HVG pins as close as possible to the device pins with short traces.
- The device ground and power ground should meet at the bulk capacitor's return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.

ADVANCE INFORMATION

10.2 Layout Example

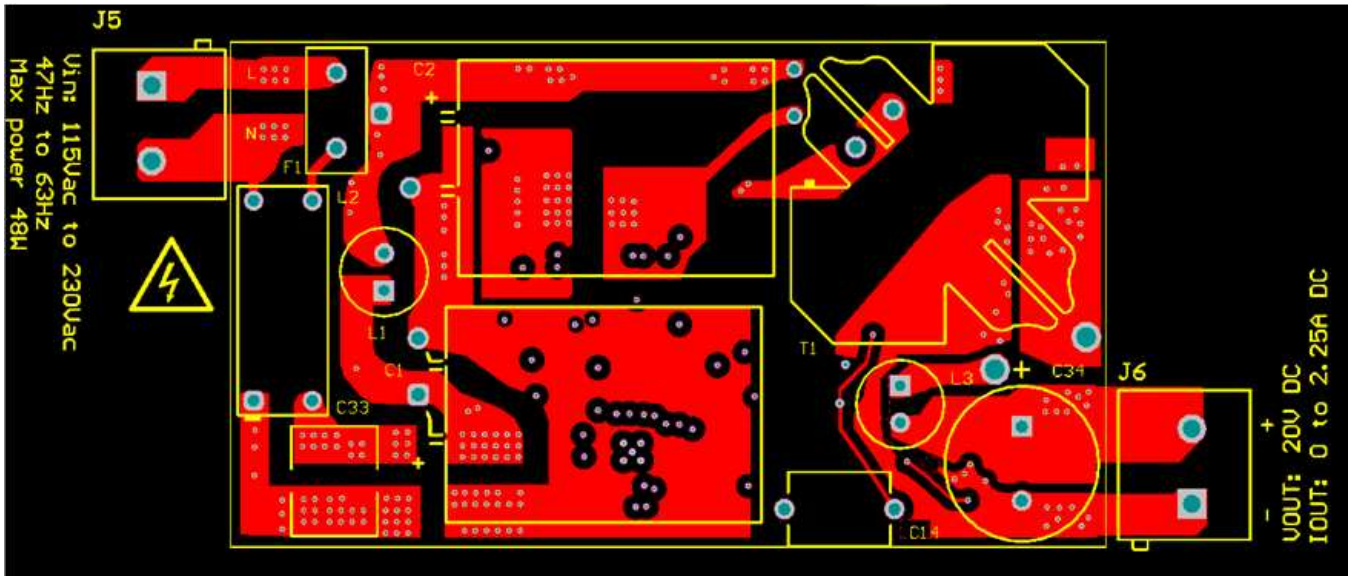


Figure 23. 45-W Power Stage Layout (Top View)

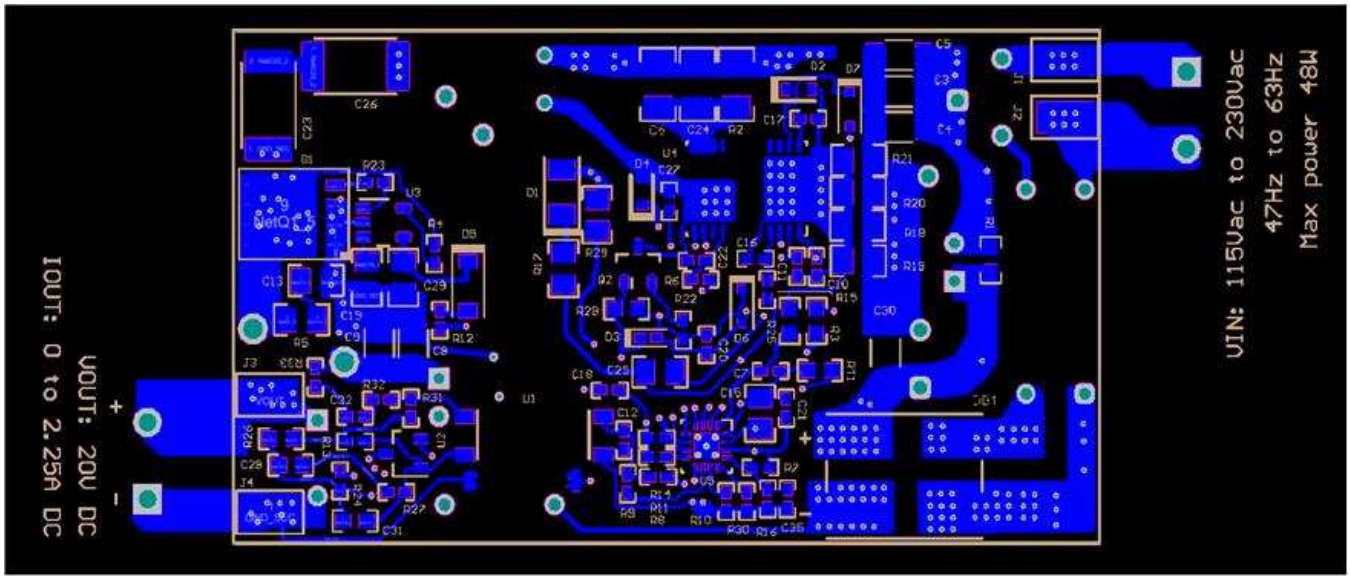


Figure 24. 45-W Power Stage Layout (Bottom View)

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Using the UCC28780EVM-022 45-W 20-V High Density GaN Active-Clamp Flyback Converter

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC28780D	ACTIVE	SOIC	D	16	40	TBD	Call TI	Call TI	-40 to 125		Samples
PUCC28780RTER	ACTIVE	WQFN	RTE	16	40	TBD	Call TI	Call TI	-40 to 125		Samples
UCC28780D	PREVIEW	SOIC	D	16	40	TBD	Call TI	Call TI	-40 to 125		
UCC28780DR	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125		
UCC28780DT	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125		
UCC28780RTE	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		
UCC28780RTER	PREVIEW	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28780	
UCC28780RTET	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

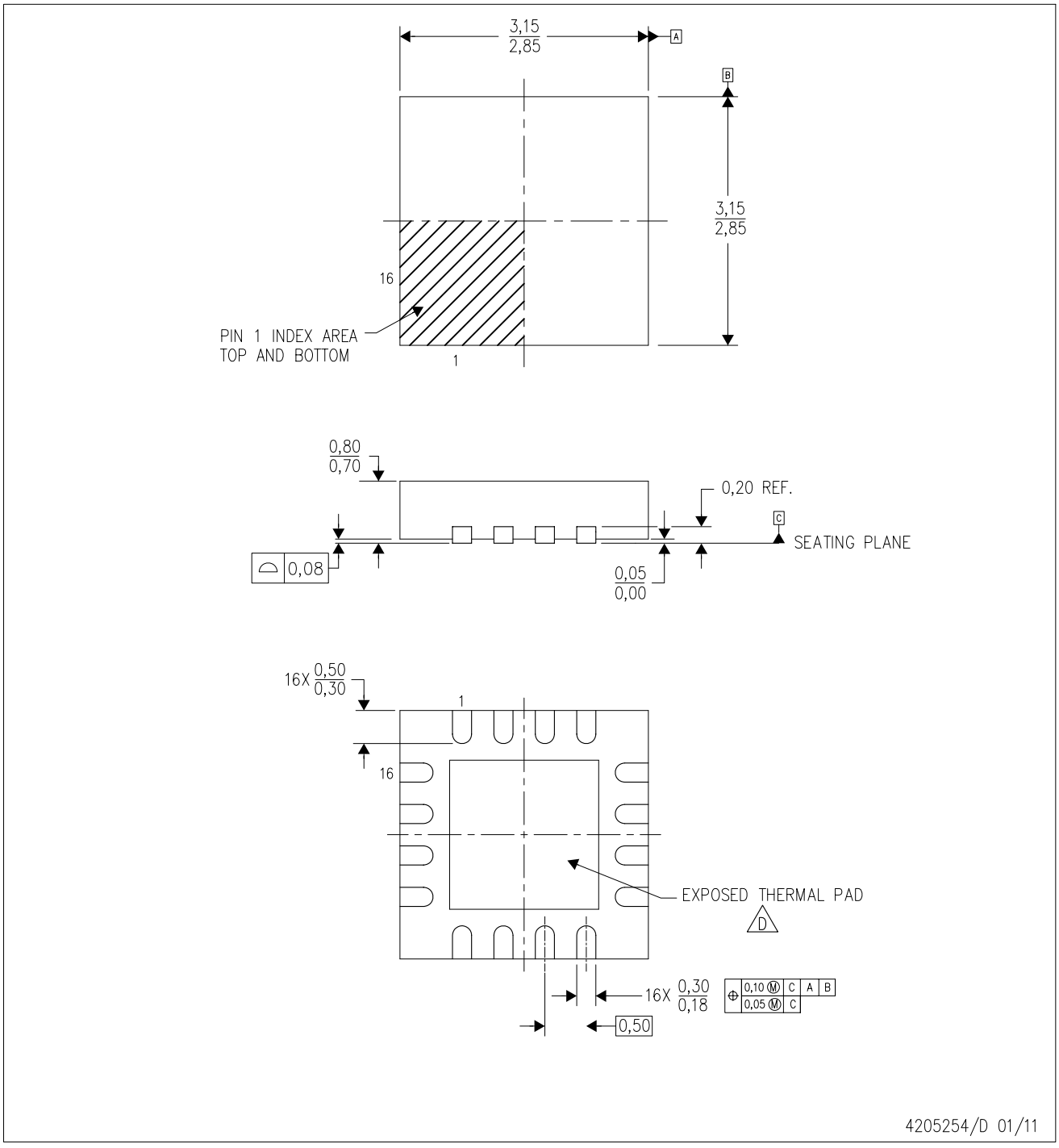
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

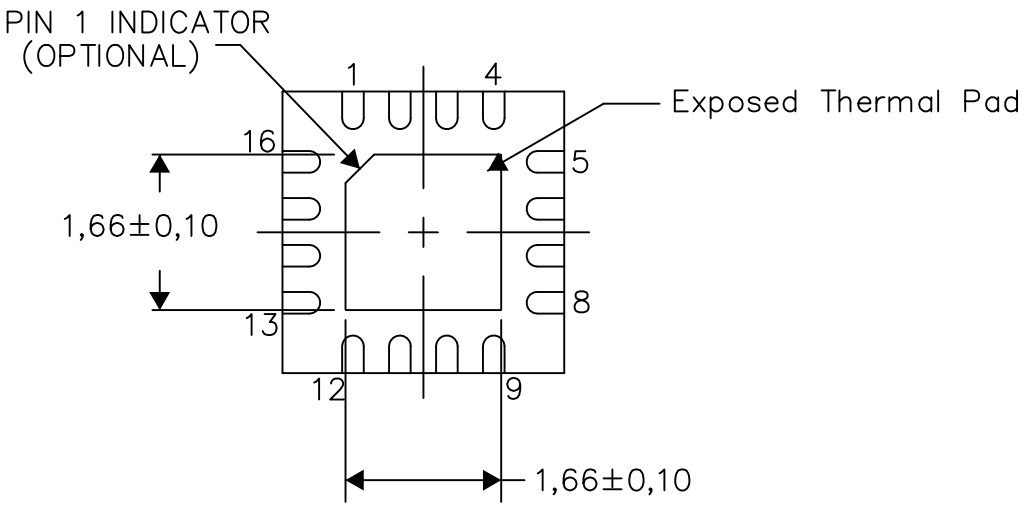
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



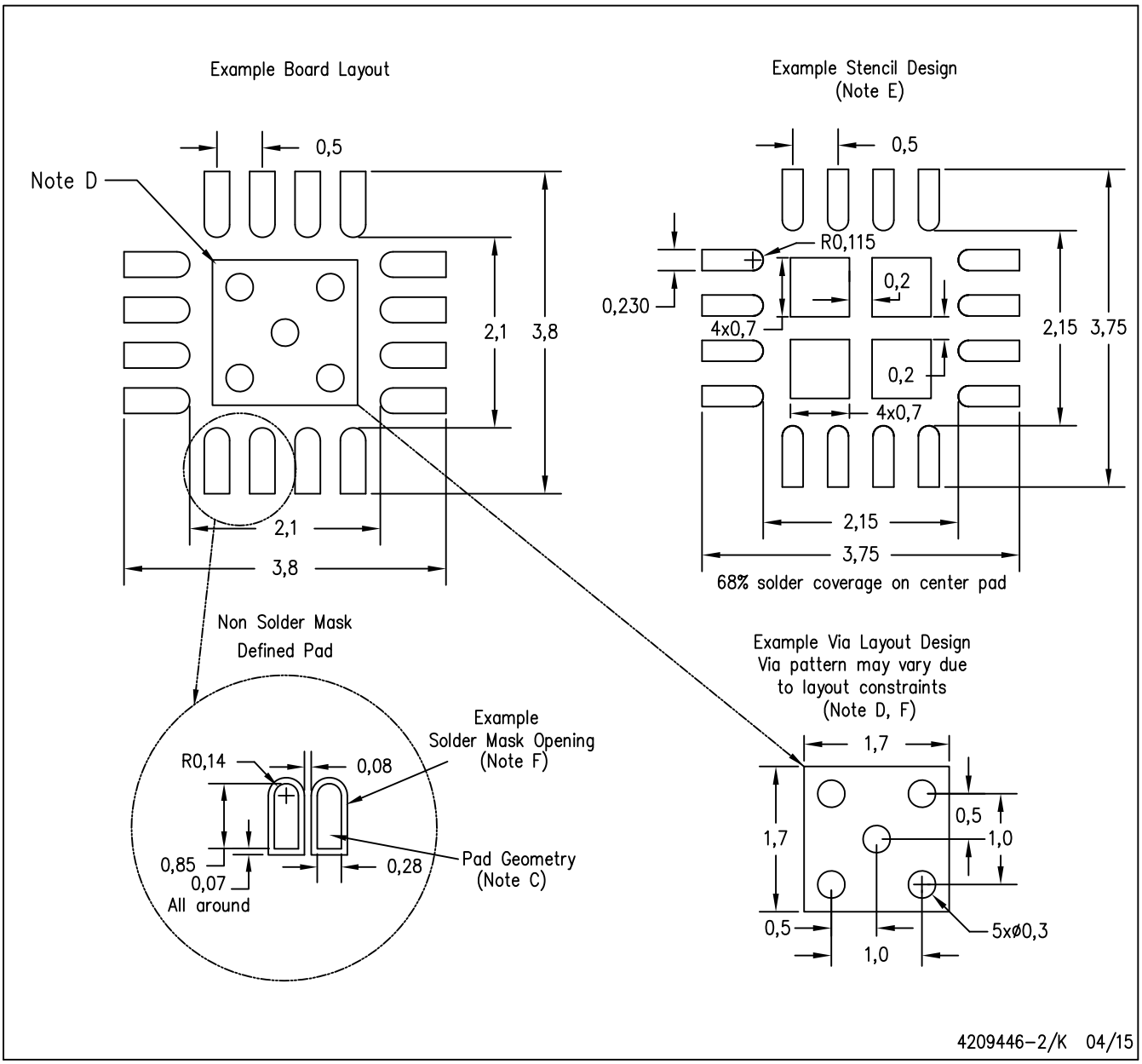
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

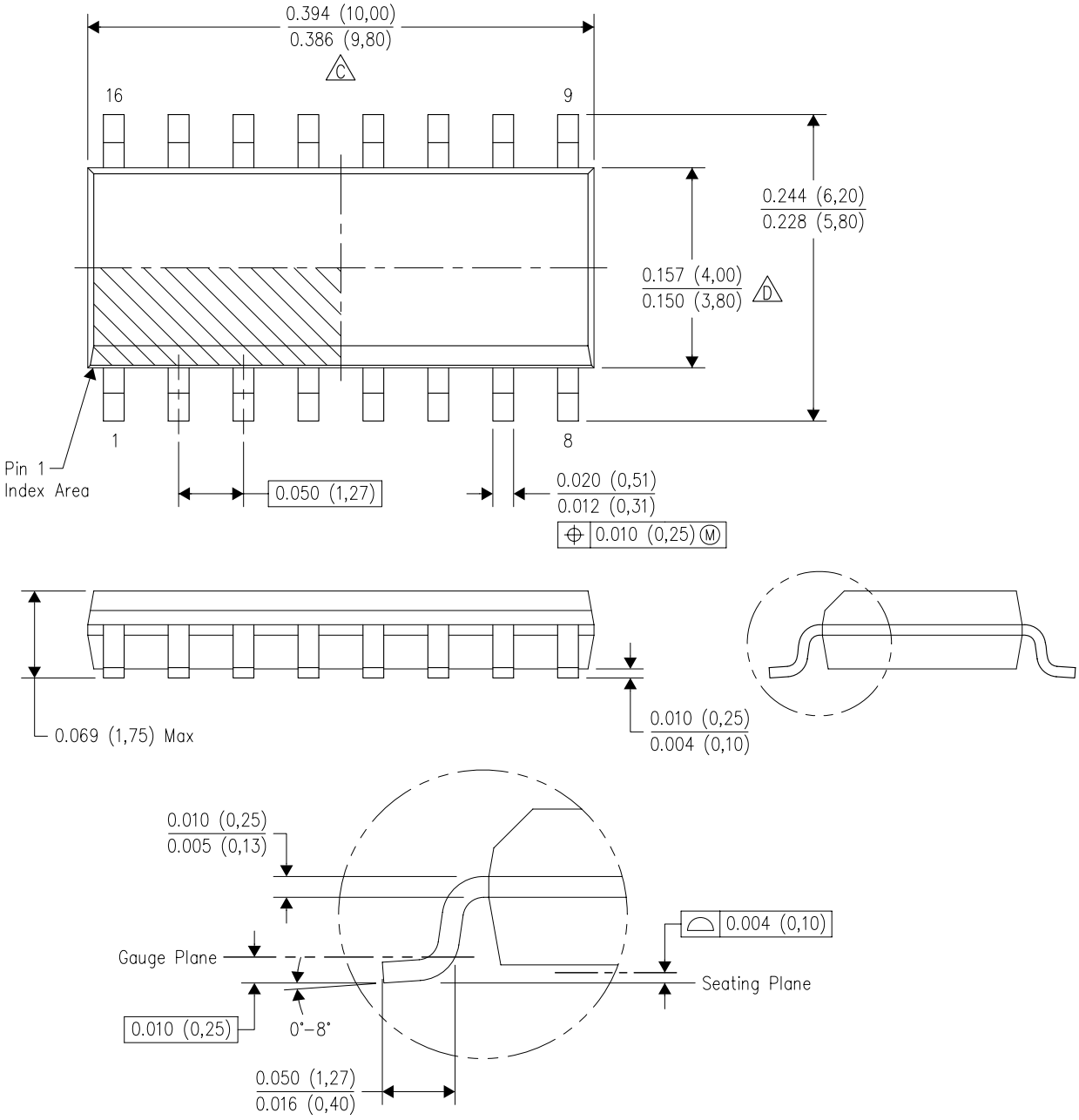
NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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