UCC256302 LLC Resonant Controller with High Voltage Startup Enabling Low Standby Power

1 Features

- Integrated High Voltage Startup
  - Eliminates Need for External Bias Supply
- Best-in-Class Transient Response
- Hybrid Hysteretic Control (HHC)
  - Best-in-Class Transient Response
  - Easy Compensation Design
- Optimized Low Power Features Enable 75 mW Standby Power Design with PFC on
  - Advanced Burst Mode Opto-Coupler Low Power Operation
  - Helps Enable Compliance to CoC Tier II Standard
- Fast Exit from Burst Mode
- Improved Capacitive Region Avoidance Scheme
- Adaptive Dead-Time
- Internal High-Side Gate Drivers (0.6-A and 1.2-A Capability)
- Robust Soft Start with No Hard Switching
- Over Temperature, Output Over Voltage, Input Over and Under Voltage Protection with Three Levels of Over Current Protections
- Wide Operating Frequency Range (35 kHz to 1 MHz)
- Select the appropriate LLC resonant controller for your design with UCC25630x Selection GuideUCC25630x Selection Guide
- Create a Custom Design Using the UCC256302 With the WEBENCH® Power Designer

2 Applications

- Digital TV SMPS
- AC-DC Adapter
- Multi-Functional Printers
- Projectors
- Merchant DC-to-DC
- High Power Battery Charging
- DIN Rail Power Supply
- Multi-Axis Servo
- ATX Power Supply
- Appliances
- LED Lighting Applications
- Industrial AC-DC

3 Description

The UCC256302 is a fully featured LLC controller with integrated high-voltage gate driver. It has been designed for use in offline AC-DC or isolated DC-DC to provide a complete power system using a minimum of external components. The resulting power system is designed to meet the most stringent requirements for standby power without the need for a separate standby power converter.

UCC256302 includes an integrated, high voltage startup function which eliminates the need for an external bias supply, reducing BOM count and minimizing solution size. UCC256302 uses hybrid hysteretic control to provide best in class line and load transient response. The control makes the open loop transfer function a first order system so that it's very easy to compensate.

UCC256302 provides a high efficient burst mode with consistent burst power level during each burst on cycle. The burst power level is programmable and adaptively changes with input voltage, making the optimization of efficiency very easy.

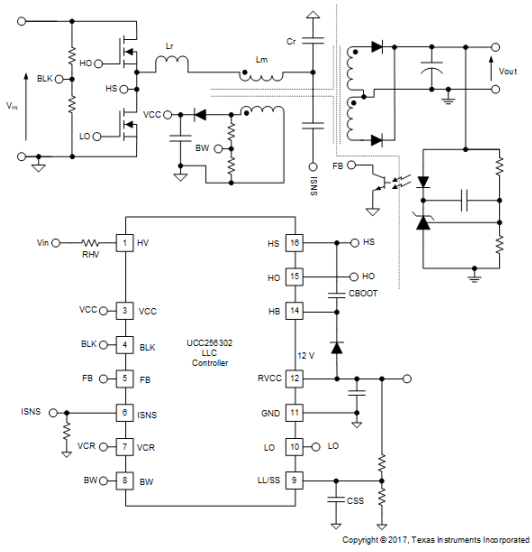
Select the appropriate LLC resonant controller for your design with UCC25630x Selection Guide

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC256302	SOIC (14)	9.9 mm x 3.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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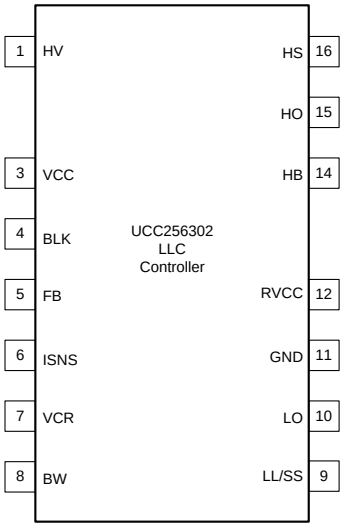
4 Pin Configuration and Functions

DDB Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLK	4	I	This pin is used to sense the PFC output voltage level. A resistive divider should be used to attenuate the signal before it is applied to this pin. The voltage level on this pin will determine when the LLC converter start/stops switching. The sensed BLK voltage is also used to adjust the burst mode threshold to improve efficiency over the input voltage range.
BW	8	I	This pin is used to sense the output voltage through the bias winding. The sensed voltage is used for output over voltage protection.
FB	5	I	LLC stage control feedback input. The amount of current sourced from this pin will determine the LLC input power level.
GND	11	G	Ground reference for all signals.
HB	14	I	High-side gate-drive floating supply voltage. The bootstrap capacitor is connected between this pin and pin HS. A high voltage, high speed diode should be connected from RVCC to this pin to supply power to the upper MOSFET driver during the period when the lower MOSFET is conducting.
HO	15	O	High-side floating gate-drive output.
HS	16	I	High-side gate-drive floating ground. Current return for the high-side gate-drive current.
HV	1	I	Connects to Internal HV startup JFET. This pin provides start up power for both PFC and LLC stage.
ISNS	6	I	Resonant current sense. The resonant capacitor voltage is differentiated with a first order filter to measure the resonant current
LL/SS	9	I	The capacitance value connected from this pin to ground will define the duration of the soft-start period. This pin is also used to program the burst mode threshold; the resistor divider on this pin programs the burst mode threshold and the threshold scaling factor with BLK pin voltage.
LO	10	O	Low-side gate-drive output.
Missing	2	N/A	Functional creepage and clearance
Missing	13	N/A	Functional creepage and clearance
RVCC	12	P	Regulated 12-V supply. This pin is used to supply the gate driver and PFC controller.
VCC	3	P	Supply input.
VCR	7	I	Resonant capacitor voltage sense

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltageages are with respect to GND, currents are positive into and negative out of the specified terminal.(1)

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	640	V
	BLK, FB, LL/SS	-0.3	7	V
	VCR	-0.3	7	V
	HB - HS	-0.3	17	V
	VCC	-0.3	30	V
	BW, ISNS	-5	7	V
RVCC output voltage	DC	-0.3	17	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100ns	HS - 2	HB + 0.3	
LO output voltage	DC	-0.3	RVCC + 0.3	V
	Transient, less than 100ns	-2	RVCC + 0.3	
Floating ground slew rate	dV_{HS}/dt	-50	50	V/ns
HO, LO pulsed current	I_{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T_J	-40	150	°C
Storage temperature range	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, high voltage pins(1)	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			600	V
V_{CC}	Supply voltage	13	15	26	V
HB - HS	Driver bootstrap voltage	10	12	16	V

Recommended Operating Conditions (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
C_B	Ceramic bypass capacitor from HB to HS	0.1		5	µF
C_{RVCC}	RVCC pin decoupling capacitor	4.7			µF
$I_{RVCCMAX}$	Maximum output current of RVCC (1)			100	mA
T_A	Operating ambient temperature	-40		125	°C

(1) Not tested in production. Insured by characterization

5.4 Thermal Information

THERMAL METRIC(1)		UCC25630 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{CCShort}$	Below this threshold, use reduced start up current		0.5	0.6	0.7	V
$V_{CCReStartJfet}$	Below this threshold, re-enable JFET.		10.2	10.5	10.8	V
$V_{CCStartSelf}$	In self bias mode, gate starts switching above this level		25	26	28	V
SUPPLY CURRENT						
$I_{CCSleep}$	Current drawn from VCC rail during burst off period	V_{CC} = 15V	475	565	700	µA
I_{CCRun}	Current drawn from VCC Pin while gate is switching. Excluding Gate Current	V_{CC} = 15V, maximum dead time	1.75	2.2	2.65	mA
REGULATED SUPPLY						
V_{RVCC}	Regulated supply voltage	V_{CC} = 15V	11.60	12	12.40	V
		V_{CC} = 13V	11.2	11.8	12.25	V
$V_{RVCCUVLO}$	RVCC under voltage lock out voltage (1)			7		V
HIGH VOLTAGE STARTUP						
I_{HVLow}	Reduced startup pin current		0.28	0.41	0.54	mA
I_{HVHigh}	Full startup pin current		7.6	10.20	12.6	mA
I_{HVLeak}	HV current source leakage current		1.40	3.37	7.55	µA
BULK VOLTAGE SENSE						
$V_{BLKStart}$	Input voltage that allows LLC to start switching	Voltage rising	2.99	3.05	3.095	V

(1) Not tested in production. Insured by characterization

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BLKStop}$	Input voltage that forces LLC operation to stop	Voltage falling	2.13	2.17	2.23	V
$V_{BLKOVRise}$	Input voltage that causes switching to stop	Voltage rising	3.94	4.03	4.11	V
$V_{BLKOVFall}$	Input voltage that causes switching to re-start	Voltage falling	3.64	3.76	3.86	V
FEEDBACK PIN						
$R_{FBInternal}$	Internal pull down resistor value		90.7	101.5	112.3	kΩ
I_{FB}	FB internal current source		76.5	85.1	93.6	µA
f_{-3dB}	Feedback chain -3dB cut off frequency (2)		1			MHz
RESONANT CURRENT SENSE						
V_{ISNS_OCP1}	OCP1 threshold		3.97	4.03	4.07	V
$V_{ISNS\_OCP1\_SS}$	OCP1 threshold during soft start (1)			5		V
V_{ISNS_OCP2}	OCP2 threshold		0.68	0.84	0.99	V
V_{ISNS_OCP3}	OCP3 threshold		0.49	0.64	0.79	V
T_{ISNS_OCP2}	The time the average input current needs to stay above OCP2 threshold before OCP2 is triggered (1)			2		ms
T_{ISNS_OCP3}	The time the average input current needs to stay above OCP3 threshold before OCP3 is triggered (1)			50		ms
$V_{IpolarityHyst}$	Resonant current polarity detection hysteresis		16.9	30.7	44.7	mV
n_{OCP1}	Number of OCP1 cycles before OCP1 fault is tripped (1)			4		
RESONANT CAPACITOR VOLTAGE SENSE						
V_{CM}	Internal common mode voltage		2.91	3.02	3.14	V
I_{RAMP}	Frequency compensation ramp current source value		1.63	1.84	2.10	mA
$I_{Mismatch}$	Pull up and pull down ramp current source mismatch (3)		-1.25		1.25	%
SOFT START						
I_{SSUp}	Current output from SS pin to charge up the soft start capacitor		21.8	25.8	29.8	µA
R_{SSDown}	SS pin pull down resistance	ZCS or OCP1	222	401	580	Ω
GATE DRIVER						
V_{LOL}	LO output low voltage	I_{sink} = 20mA	0.027	0.052	0.087	V
V_{RVCC} - V_{LOH}	LO output high voltage	I_{source} = 20mA	0.113	0.178	0.263	V
V_{HOL} - V_{HS}	HO output low voltage	I_{sink} = 20mA	0.027	0.053	0.087	V
V_{HB} - V_{HOH}	HO output high voltage	I_{source} = 20mA	0.113	0.173	0.263	V
$V_{HB-HSUVLORise}$	High side gate driver UVLO rise threshold		7.35	7.94	8.70	V
$V_{HB-HSUVLOFall}$	High side gate driver UVLO fall threshold		6.65	7.25	7.76	V
I_{source_pk}	HO, LO peak source current (2)			-0.6		A
I_{sink_pk}	HO, LO peak sink current (2)			1.2		A
BOOTSTRAP						

(2) Not tested in production. Insured by design
(3) $I_{Mismatch}$ calculated as average of $(I_{PD}-(I_{PD}+I_{PU})/(I_{PD}+I_{PU})/2))$ and $(I_{PU}-(I_{PD}+I_{PU})/((I_{PD}+I_{PU})/2)$

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BOOT\_QUIESCENT}$	(HB - HS) quiescent current	HB - HS = 12V	51.10	74.40	97.70	µA
I_{BOOT_LEAK}	HB to GND leakage current		0.02	0.40	5.40	µA
$t_{ChargeBoot}$	Length of charge boot state		234	267	296	µs
BIAS WINDING						
$V_{BWOVRise}$	Output voltage OVP		-4.1	-3.97	-3.86	V
BURST MODE						
R_{LL}	LL voltage scaling resistor value		240	250	258	kΩ
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable PSN slew rate (1)		±1		±50	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer (1)			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature (1)	Temperature rising	125	145		°C
T_{J_H}	Thermal shutdown hsyterisis (1)			20		°C

5.6 Switching Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =12V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1nF load	18	35	50	ns
$t_{f(LO)}$	Fall time	10% to 90%, 1nF load	15	25	50	ns
$t_{r(HO)}$	Rise time	10% to 90%, 1nF load	18	35	50	ns
$t_{f(HO)}$	Fall time	10% to 90%, 1nF load	15	25	50	ns
$t_{DT(min)}$	Minimum dead time (1)			100		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) (1)			150		µs
$t_{ON(min)}$	Minimum gate on time (1)			250		ns
$t_{ON(max)}$	Maximum gate on time (1)			14.5		µs

(1) Not tested in production. Insured by design

5.7 Typical Characteristics

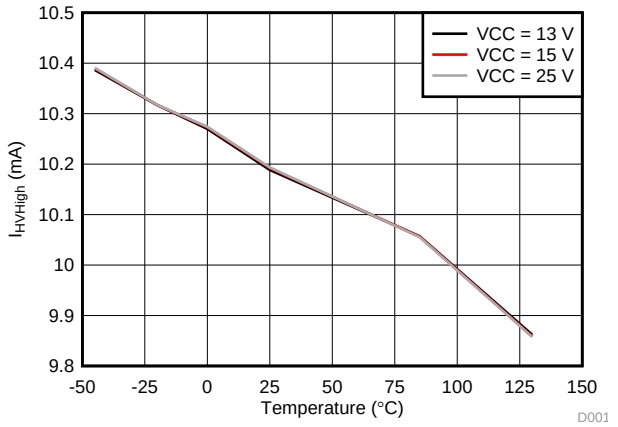


Figure 1. I_{HVHigh} vs Temperature

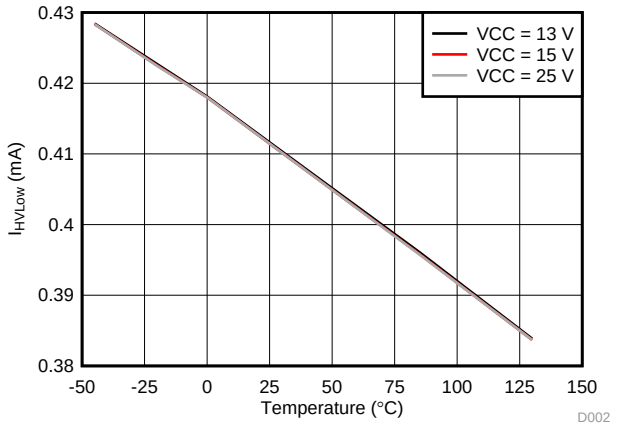


Figure 2. I_{HVLow} vs Temperature

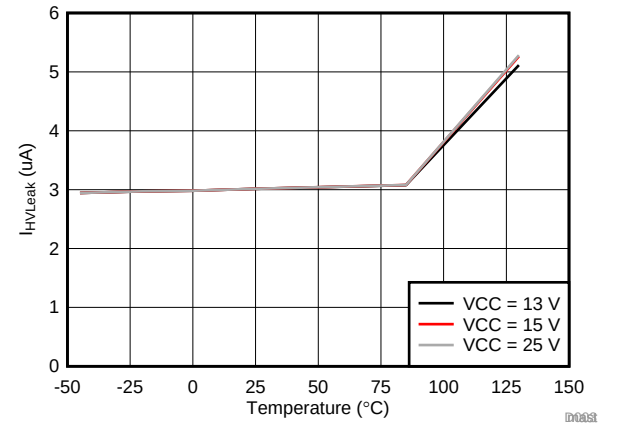


Figure 3. I_{HVLeak} vs Temperature

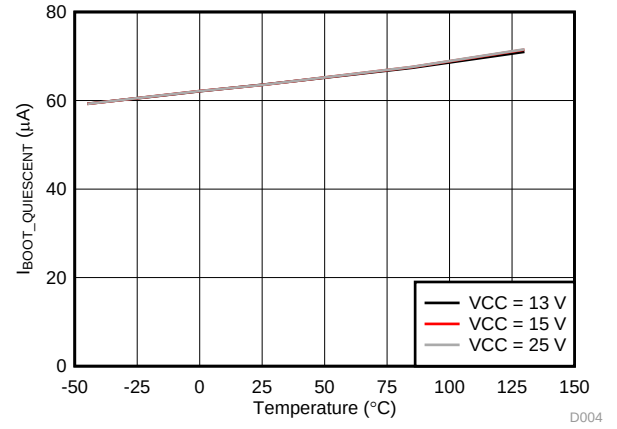


Figure 4. $I_{BOOT\_QUIESCENT}$ vs Temperature

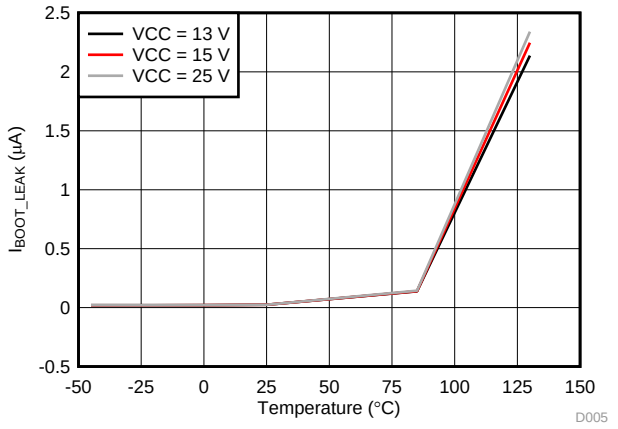


Figure 5. I_{BOOT_LEAK} vs Temperature

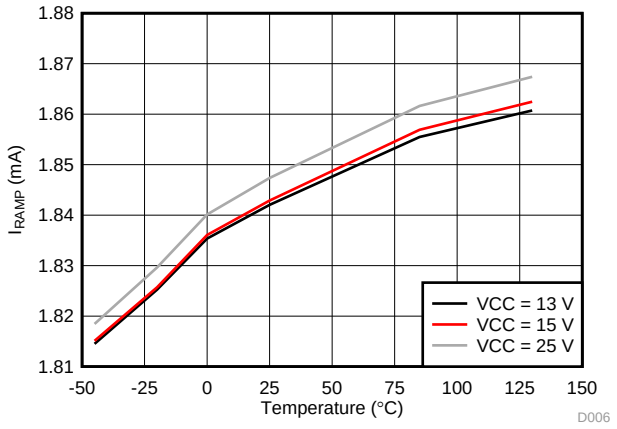


Figure 6. I_{RAMP} vs Temperature

Typical Characteristics (continued)

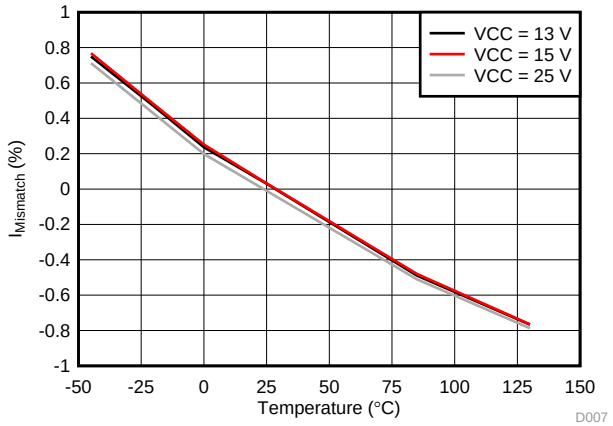


Figure 7. $I_{MISMATCH}$ vs Temperature

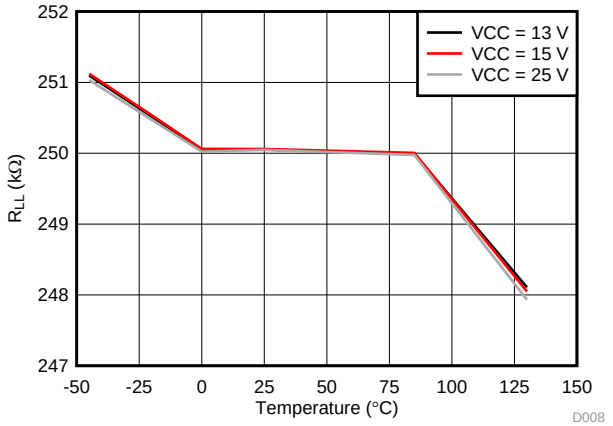


Figure 8. R_{LL} vs Temperature

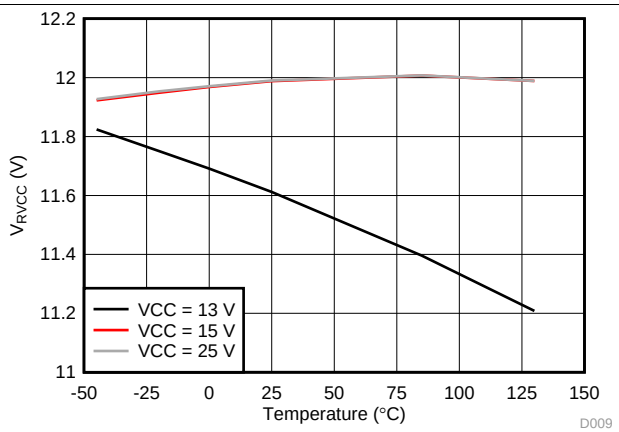


Figure 9. V_{RVCC} vs Temperature

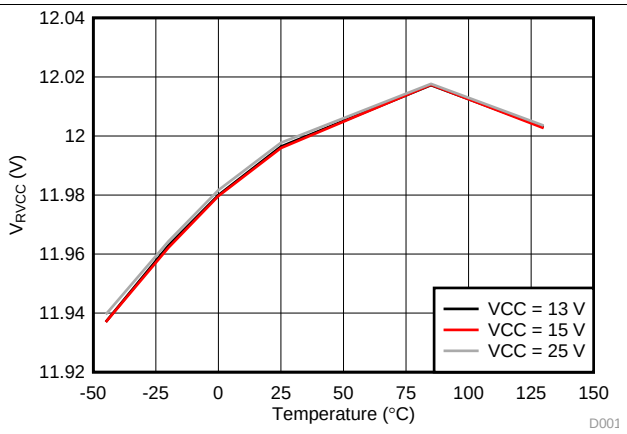


Figure 10. V_{RVCC} vs Temperature

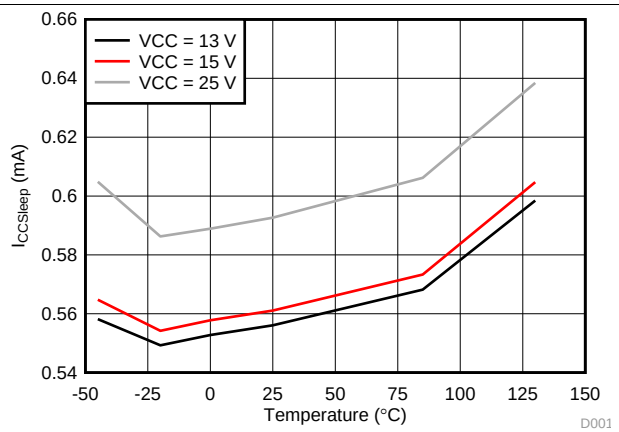


Figure 11. $i_{CCSleep}$ vs Temperature

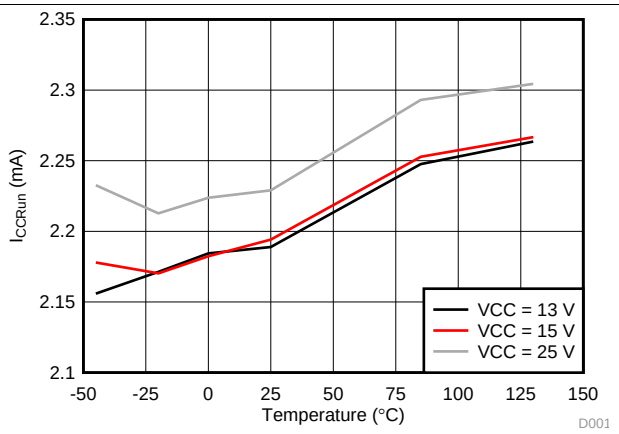


Figure 12. I_{CCRun} vs Temperature

Typical Characteristics (continued)

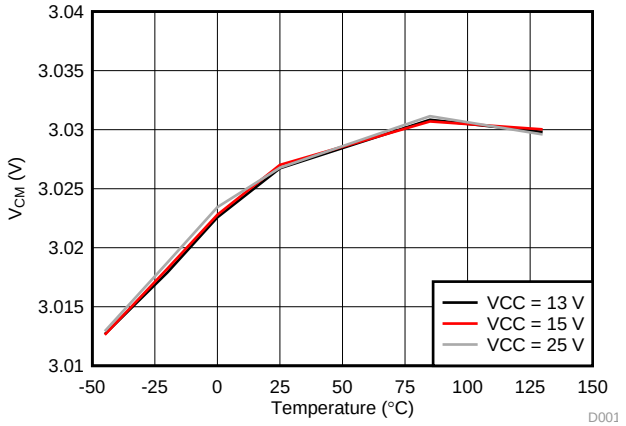


Figure 13. V_{CM} vs Temperature

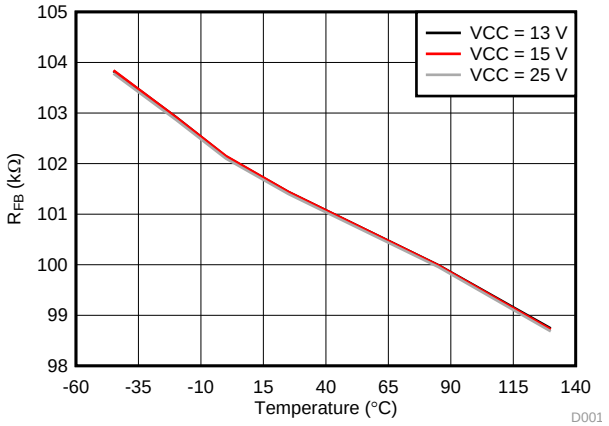


Figure 14. R_{FB} vs Temperature

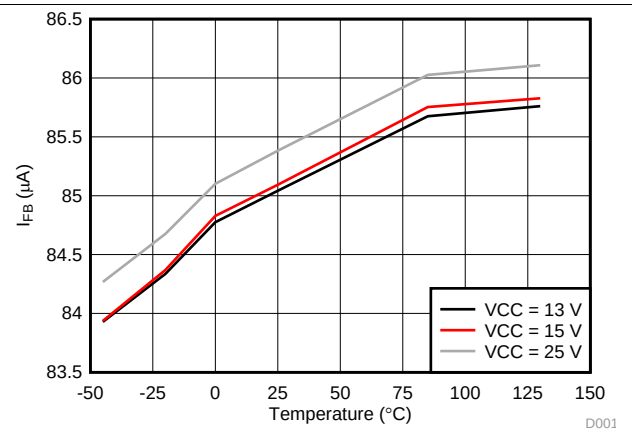


Figure 15. I_{FB} vs Temperature

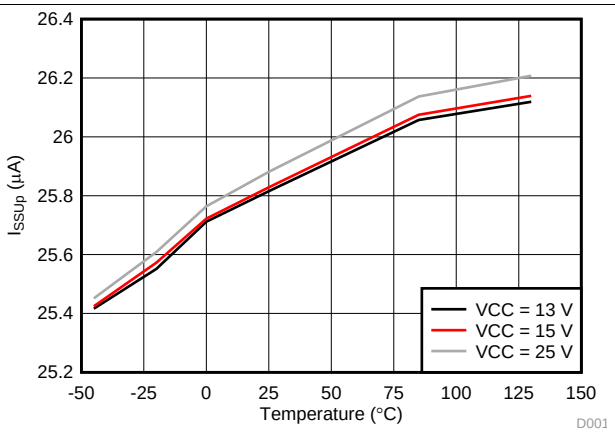


Figure 16. I_{SSUp} vs Temperature

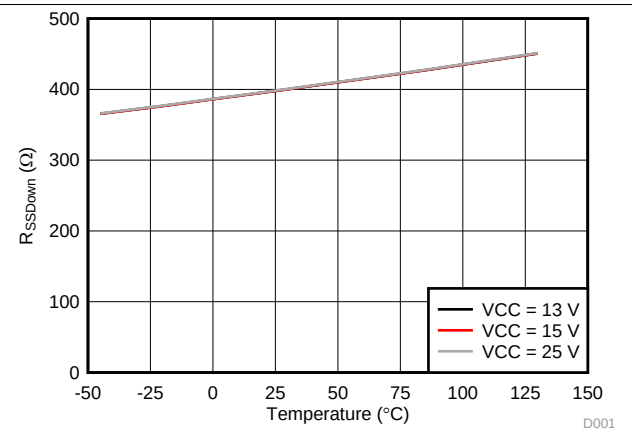


Figure 17. R_{SSDown} vs Temperature

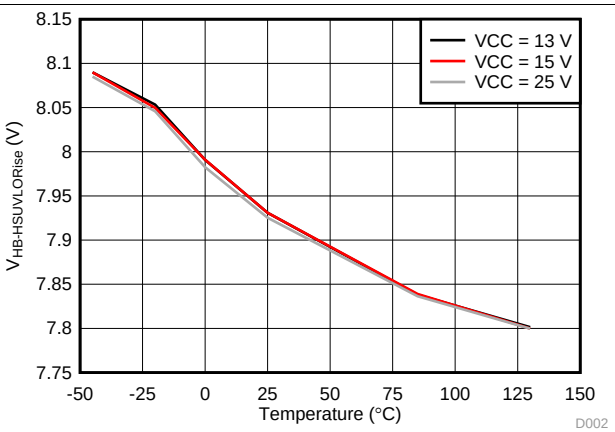


Figure 18. $I_{HB\text{-}HSUVLORise}$ vs Temperature

Typical Characteristics (continued)

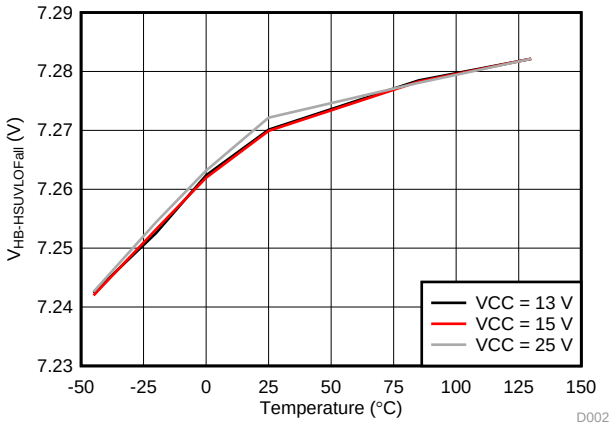


Figure 19. $I_{HB-HSUVLOFall}$ vs Temperature

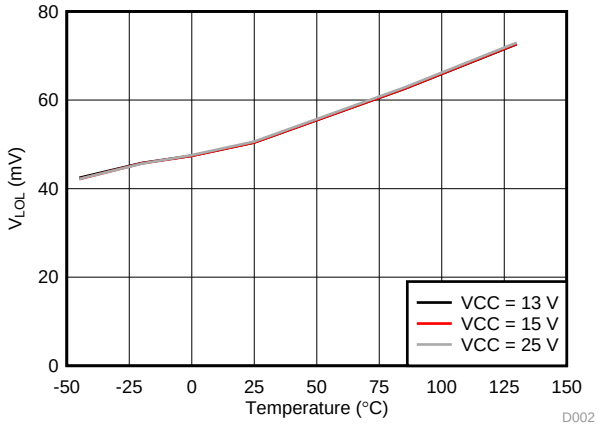


Figure 20. V_{LOL} vs Temperature

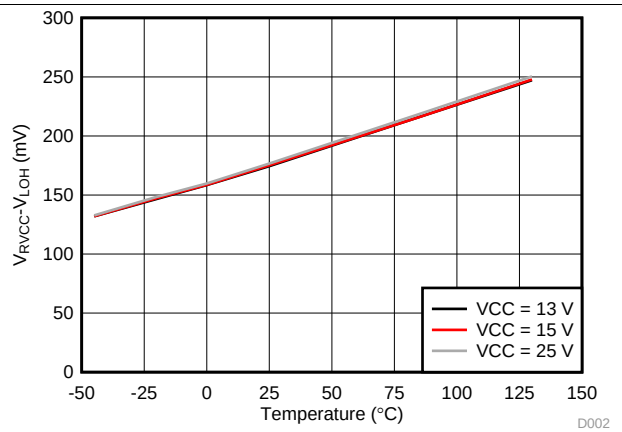


Figure 21. $V_{RVCC-VLOH}$ vs Temperature

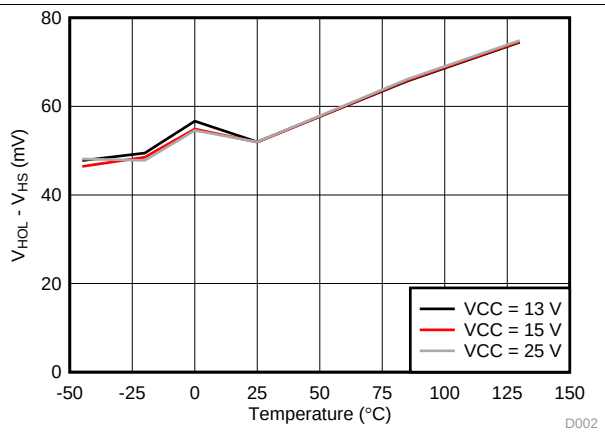


Figure 22. V_{HOL}- V_{HS} vs Temperature

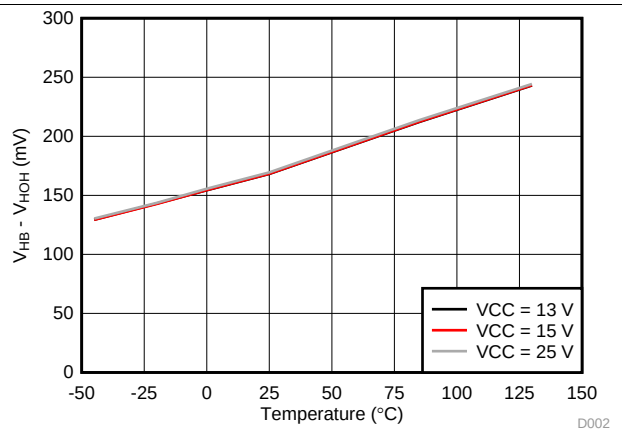


Figure 23. V_{HB} - V_{HOH} vs Temperature

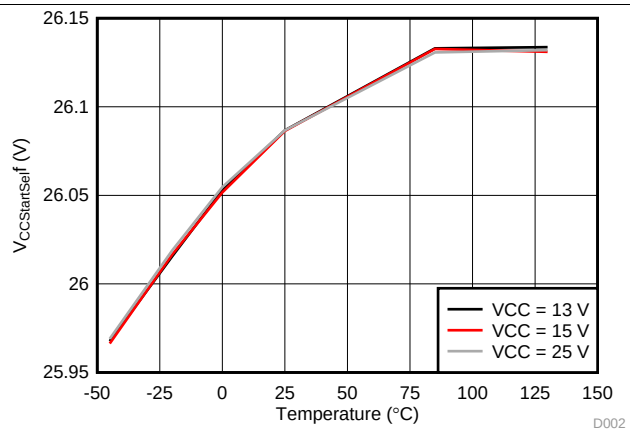


Figure 24. $V_{CCStartself}$ vs Temperature

Typical Characteristics (continued)

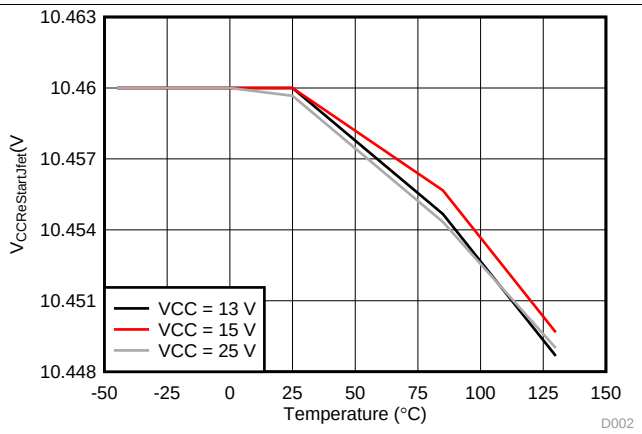


Figure 25. $V_{CCReStartJfet}$ vs Temperature

6 Detailed Description

6.1 Overview

The high level of integration of UCC256302 enables significant reduction in the list of materials and solution size without compromising functionality. UCC256302 achieves extremely low standby power using burst mode. The device's novel control scheme offers excellent transient performance and simplified compensation.

Many consumer and industrial applications with mid-high power consumption, including large screen televisions, AC-DC adapters, server power supplies, and LED drivers, employ PFC + LLC power supplies because they offer improved efficiency, and small size, compared with a PFC + Flyback topology. A disadvantage of the PFC + LLC power supply system is that it naturally offers poor light load efficiency and high no-load power because the LLC stage requires a minimum amount of circulating current to maintain regulation. To meet light load efficiency and no load power requirement it is therefore necessary to use an auxiliary flyback converter that runs continuously and allows the main PFC + LLC power system to be shut down when the system enters low power or standby mode. UCC256302 LLC controller is designed to make a LLC power supply system with advanced control algorithm and high efficient burst mode. UCC256302 contains a number of novel features that enable it to offer excellent light load efficiency and no load power. This will allow customers to design power systems that meet 150-mW no-load power target without needing an auxiliary flyback converter. UCC256302 includes a high-voltage startup JFET to initially charge the VCC capacitor to provide the energy needed to start the PFC and LLC power system. Once running, power for the PFC and LLC controllers is derived from a bias winding on the LLC transformer.

UCC256302 uses a novel control algorithm, Hybrid Hysteretic Control (HHC), to achieve regulation. In this control algorithm, the switching frequency is defined by the resonant capacitor voltage, which carries accurate input current information. Therefore, the control effort controls the input current directly. This enables excellent load and line transient response, and high efficient burst mode. In addition, comparing with traditional Direct Frequency Control (DFC), HHC changes the system to a first order system. Therefore, the compensation design is much easier and can achieve higher loop bandwidth.

UCC256302 includes robust algorithms for avoiding ZCS operation region. When near ZCS operation is detected, UCC256302 over-rides the feedback signal and ramps up the switching frequency until operation is restored. After which the switching frequency is ramped back down at a rate determined by the soft-start capacitor until control has been handed back to the voltage control loop.

UCC256302 monitors the half-bridge switched node to determine the required dead-time in the gate signals for the outgoing and incoming power switches. In this way the dead-time is automatically adjusted to provide optimum efficiency and security of operation. UCC256302includes an algorithm for adaptive dead-time that makes its operation inherently robust compared with alternative parts.

Overview (continued)

UCC256302 includes high and low-side drivers that can directly drive LLC power stage delivering up to 1-kW peak/500-W continuous power. This allows complete and fully featured power systems to be realized with minimum component count.

An integrated high voltage JFET allows the power system to be regulating its output voltage within one second of the mains voltage appearing at the input of the PFC stage. UCC256302 provides start-up power for both the LLC and PFC stages. Once operating, the JFET is switched OFF to limit power dissipation in the package and reduce standby power consumption.

At low output power levels UCC256302 automatically transitions into light-load burst mode. The LLC equivalent load current level during the burst on period is a programmable value. The space period between bursts is terminated by the secondary voltage regulator loop based on the FB pin voltage. During burst mode, the resonant capacitor voltage is monitored so that the first and last burst pulse widths are fully optimized for best efficiency. This method allows UCC256302 to achieve higher light-load efficiency and reduced no-load power compared with alternative parts.

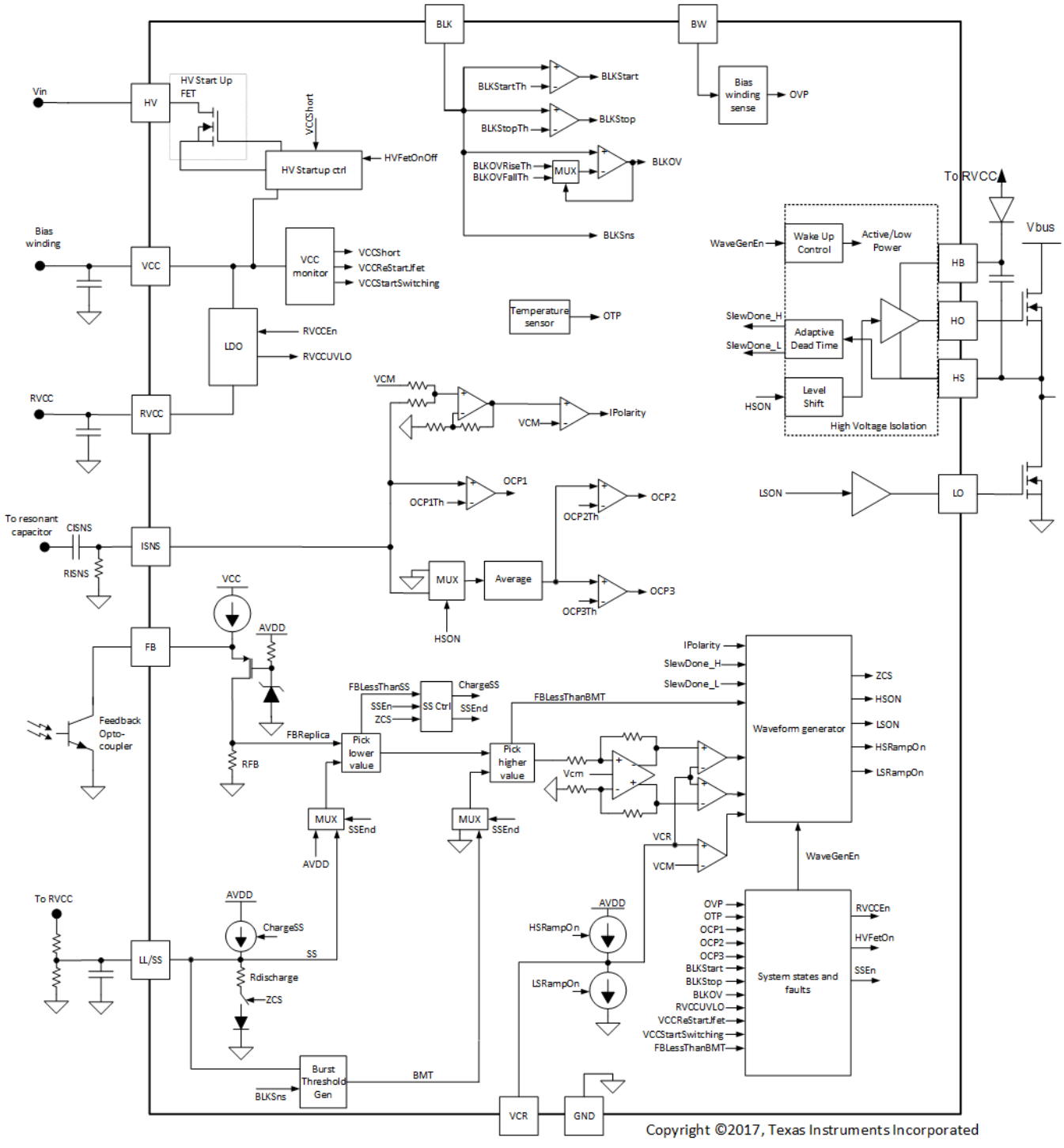
In addition, UCC256302 enables the opto-coupler to operate at a low power mode, which can save up to 20 mW at standby mode comparing with conventional solution.

Additional protection features of UCC256302 include three-level over current protection, output over voltage protection, input voltage OVP and UVP, gate driver UVLO protection, and over temperature protection.

The key features of UCC256302 can be summarized as follows:

- Integrated high voltage start up and high voltage gate driver
- Hybrid Hysteretic Control helps achieve best in class load and line transient response
- Optimized light load burst mode enables 150-mW standby power design
- Improved capacitive region operation prevention scheme
- Adaptive dead time
- Wide operating frequency range (35 kHz ~ 1 MHz)

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Hybrid Hysteretic Control

UCC256302 uses a novel control scheme – Hybrid Hysteretic Control (HHC) - to achieve best in class line and load transient performance. The control method makes the compensator very easy to design. The control method also makes light load management easier and more efficient. Improved line transient enables lower bulk capacitor/output capacitor value and saves system cost.

HHC is a control method which combines traditional frequency control and charge control – It is charge control with added frequency compensation ramp. Comparing with traditional frequency control, it changes the power stage transfer function from a 2nd order system to a 1st order system, so that it is very easy to compensate. The control effort is directly related to input current, so the line and load transients are best in class. Comparing with charge control, the hybrid hysteretic control avoids unstable condition by adding in a frequency compensation ramp. The frequency compensation makes the system always stable, and makes the output impedance lower as well. Lower output impedance makes the transient performance better than charge control.

In summary, the problems solved by HHC are:

- Help LLC converters achieve best in class load transient and line transient
- Changes the small-signal transfer function to a 1st order system which is very easy to compensate, and can achieve very high bandwidth
- Inherently stable via frequency compensation
- Makes burst mode control high efficiency optimization much easier

Figure 26 shows the HHC implementation in UCC25630: a capacitor divider (C1 and C2) and two well matched controlled current source.

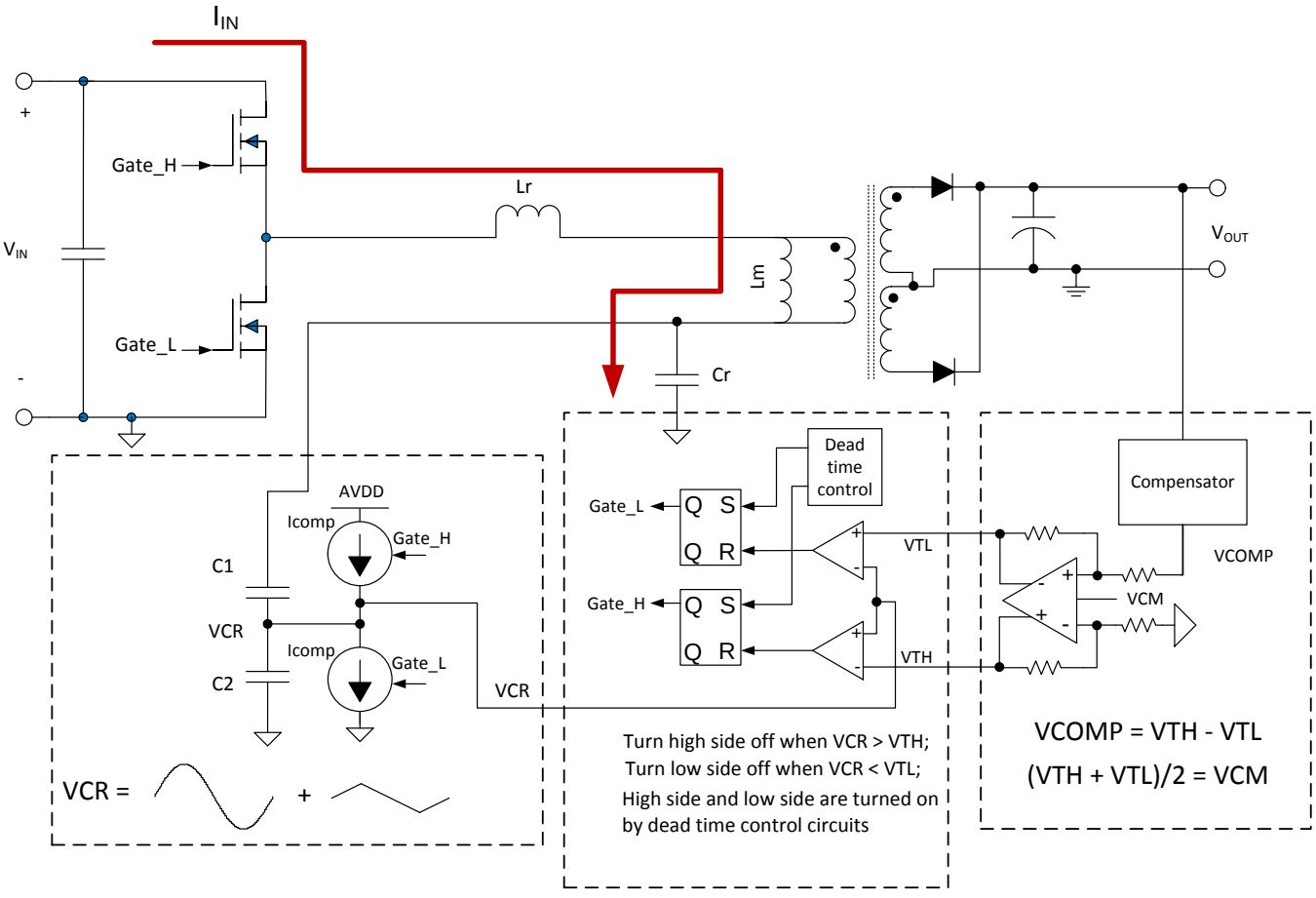


Figure 26. UCC256302 HHC Implementation

Feature Description (continued)

The resonant capacitor voltage is divided down by the capacitor divider formed by C1 and C2. The current sources are controlled by the gate drive signals. When high side switch is on, turn on the upper current source to inject a constant current into the capacitor divider; when low side switch is on, turn on the lower current source to pull the same amount of constant current outside of the capacitor divider. The two current sources add a triangular compensation ramp to the V_{CR} node. The current sources are supplied by a reference voltage V_{ref}. This voltage needs to be equal to or larger than twice of the common mode voltage V_{CM}. The divided resonant capacitor voltage and the compensation ramp voltage are then added together to get VCR node voltage. If the frequency compensation ramp dominates, the VCR node voltage will look like a triangular waveform, and the control will be similar to direct frequency control. If the resonant capacitor voltage dominates, the shape of the VCR node voltage will look like the actual resonant capacitor voltage, and the control will be similar to charge control. This is why the control method is called “hybrid” and the compensation ramp is called frequency compensation.

This set up has an inherent negative feedback to keep the high side and low side on time balanced, and also keep the common mode voltage at V_{CR} node at V_{CM}.

There are two input signals needed for the new control scheme: V_{CR} and V_{COMP}. V_{CR} is the sum of the scaled down version of the resonant capacitor voltage and the frequency compensation ramp. V_{COMP} is the voltage loop compensator output. The waveform below shows how the high-side and low-side switches are controlled based on VCR and V_{COMP}. The common mode voltage of VCR is VCM.

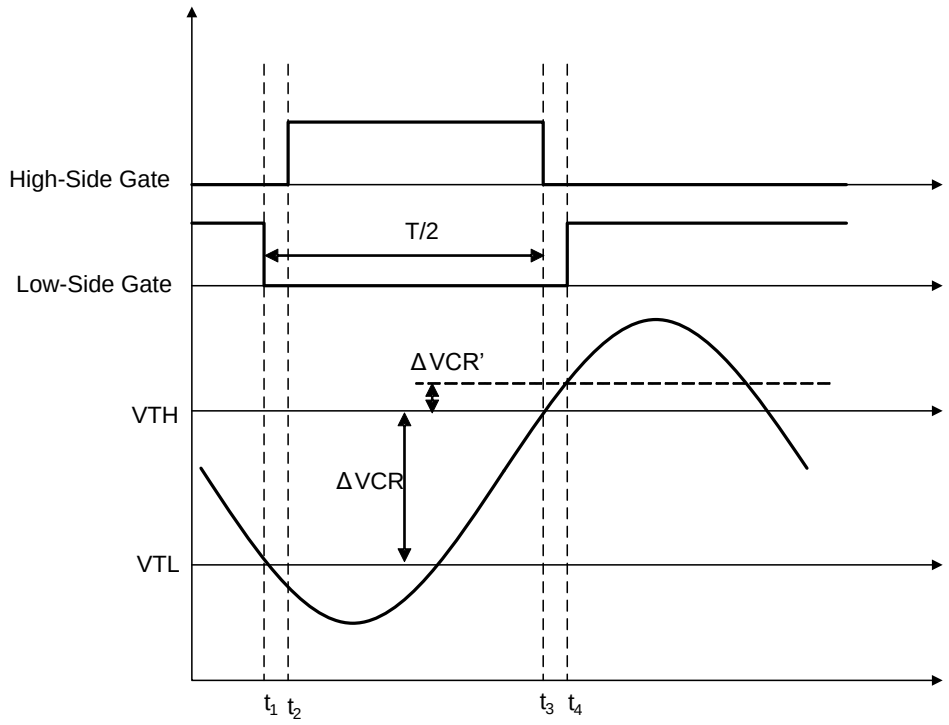


Figure 27. HHC Gate On/Off Control Principle

Based on V_{COMP} and VCM (3 V), two thresholds: Vthh and Vthl are created.

$$Vthh = VCM + \frac{Vcomp}{2} \quad (1)$$

$$Vthh = VCM - \frac{Vcomp}{2} \quad (2)$$

The VCR voltage is compared with the two thresholds. When VCR > Vthh, turn off high side switch; when VCR < Vthl, turn off low side switch. HO and LO turn on edges are controlled by adaptive dead time circuit.

Feature Description (continued)

6.3.2 Regulated 12-V Supply

RVCC pin is the regulated 12-V supply which can supply up to 100-mA current. The regulated rail is used to supply the PFC, and LLC gate driver. RVCC has under voltage lock out (UVLO) function. If during normal operation, RVCC voltage is less than RVCCUVLO threshold. It is treated as a fau*Device Functional Modes*lt and the system will enter FAULT state. Details about the FAULT handling will be discussed in the section.

6.3.3 Feedback Chain

Control of output voltage is provided by a voltage regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary regulator circuit is transferred across the isolation barrier using an opto-coupler and is fed into the FB pin on UCC25630. This section discusses about the whole feedback chain.

The feedback chain has the following functions:

- Optocoupler feedback signal input and bias
- System external shut down
- Soft start function selection by a pick lower block
- Burst mode selection by a pick higher block
- Convert single ended feedback demand to two thresholds V_{thh} and V_{thl}; and V_{CR} comparison with the thresholds and the common mode voltage V_{CM}

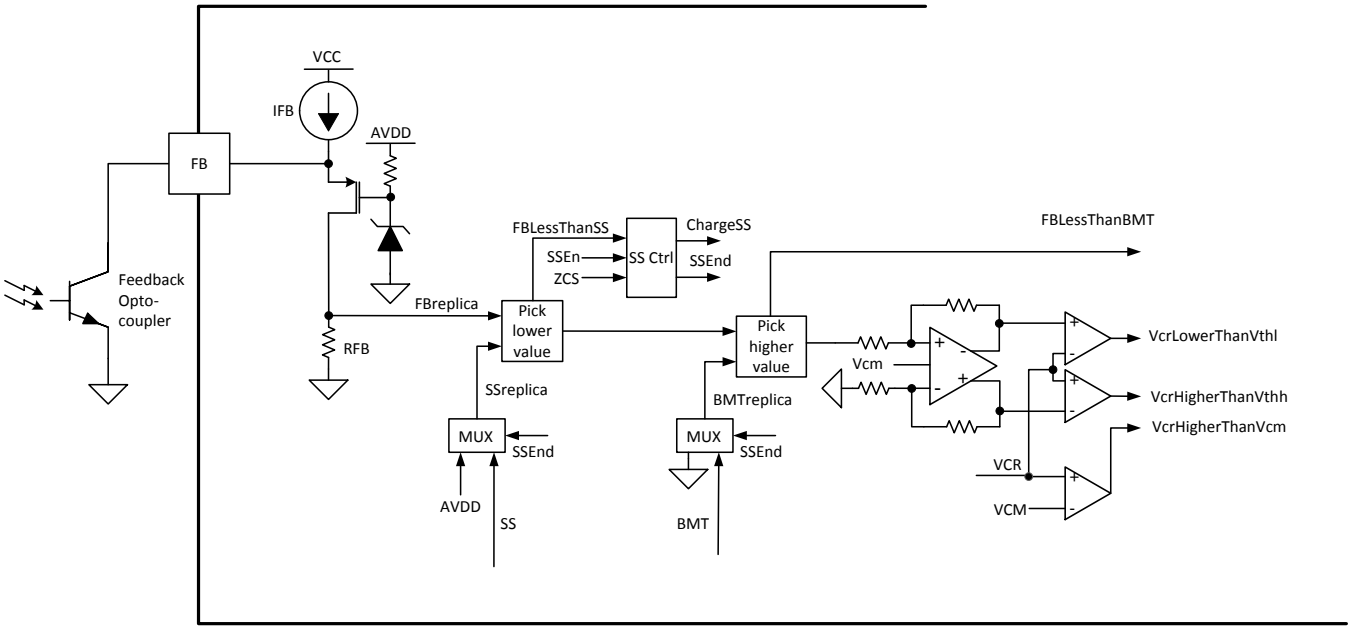


Figure 28. Feedback Chain Block Diagram

Feature Description (continued)

The timing diagram below shows the FB chain waveforms. The sequence is normal soft start followed by a ZCS event, and load step into burst mode, and then come out of burst mode.

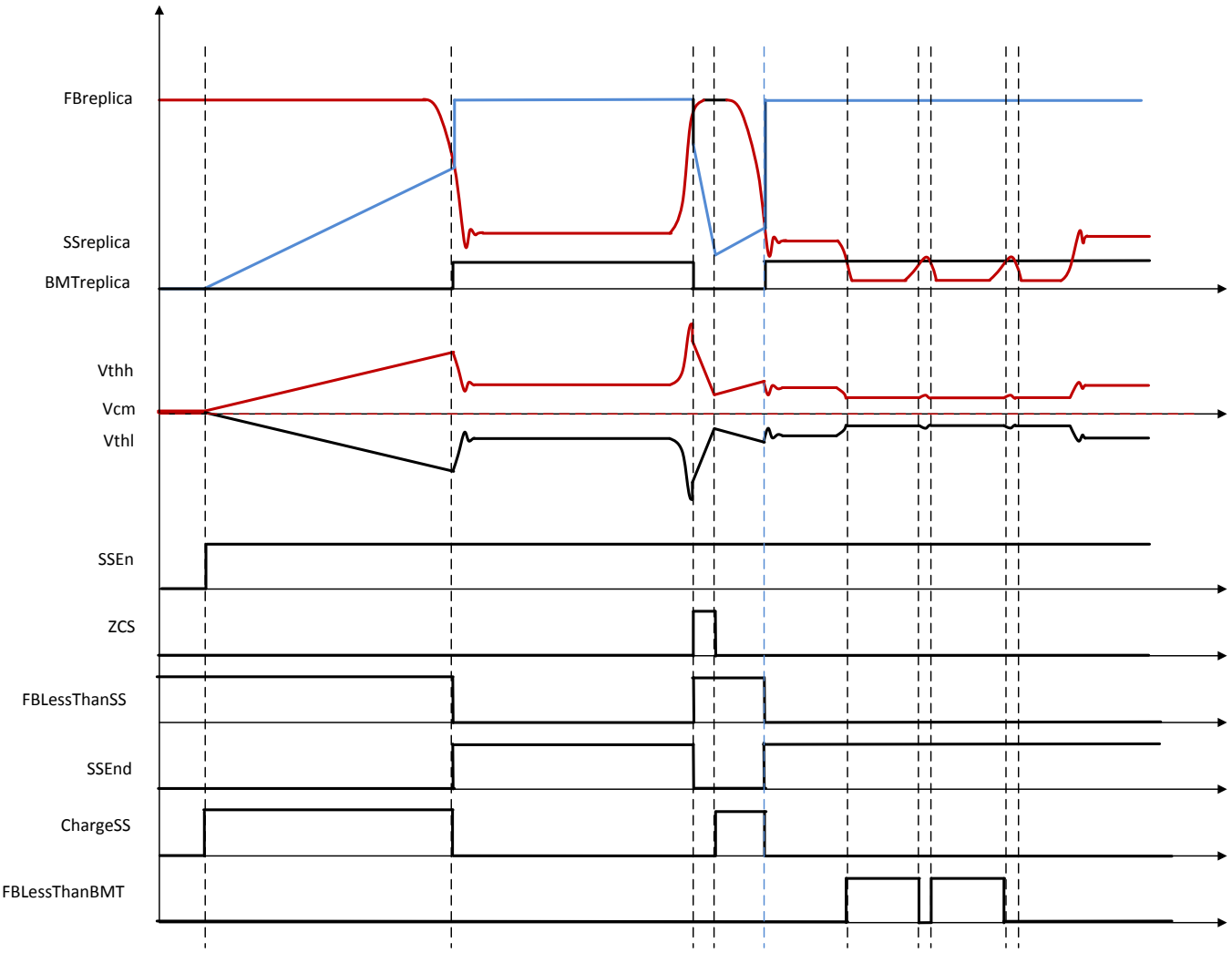


Figure 29. Feedback Chain Timing Diagram

6.3.4 Optocoupler Feedback Signal Input and Bias

The secondary regulator circuit and optocoupler feedback circuit all add directly to the no load power consumed by the system. To achieve very low no load power it is necessary to drive the optocoupler in a low current mode.

As shown in Figure 29, a constant current source IFB is generated out of VCC voltage and connected to FB pin. A resistor RFB is also connected to this current source with a PMOS in series. During normal operation, the PMOS is always on. The PMOS limits the maximum voltage on the FBreplica.

$$I_{FB} = I_{opto} + I_{RFB} \quad (3)$$

From this equation, when I_{opto} increases, I_{RFB} will decrease, making FBreplica decrease. In this way, the control effort is inverted. This circuit can also limit the optocoupler maximum current to be I_{FB}. A conventional way to bias the optocoupler is using a pull up resistor on the collector of the optocoupler output. To reduce the power consumption, the pull up resistor needs to be big, which will limit the loop bandwidth. For the bias current method used in UCC25630, the optocoupler current is limited and there is no loop bandwidth issue.

Feature Description (continued)

6.3.5 System External Shut Down

This function provides a way to shut down the system by an external signal. When the FBreplica is less than the burst mode threshold, stop LLC switching. When FBLessThanBMT is true for more than 200 ms, go to JFET OFF state and try to re-start. Before LLC starts switching, the system has to make sure that FBLessThanBMT is not true. If FBreplica is constantly held low by an external signal, the system will not start again.

This function can be used for system on/off control or any other fault shut down which isn't included in UCC25630. To implement this function, an external biased optocoupler is needed. The schematic below is an example of such implementation.

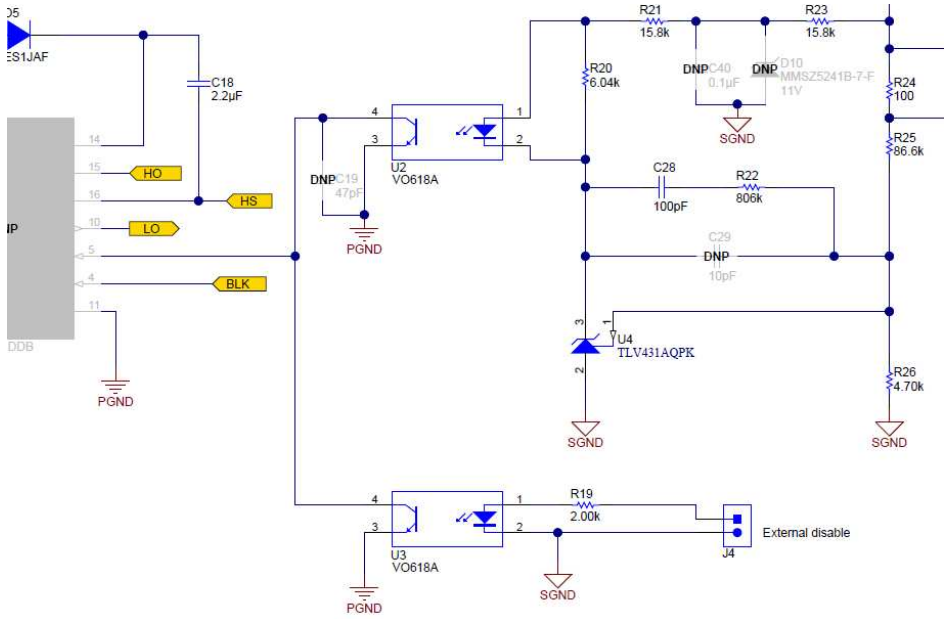


Figure 30. External Disable Example Circuit

Feature Description (continued)

6.3.6 Pick Lower Block and Soft Start Multiplexer

This part of the circuit consists of 3 elements:

- A pick lower block
- A MUX which selects AVDD or SS signal as the second input to the pick lower block
- A SS control block which handles the charge and discharge of the SS capacitor in cause of a ZCS fault

The pick lower block has two inputs. The first input is FBreplica. The second input is selected between AVDD and SS pin voltage. The other output of the block is the lower of the two inputs.

The MUX selects between SS and AVDD. The selection is based on SSEnd (soft start end) signal, which is an output of the SS Ctrl block. SSEnd is high when SS is higher than FBreplica, and soft start process has been initiated by the state machine, and there is no ZCS condition. Switching to AVDD after soft start has ended helps make sure that during non-soft start or non-ZCS fault condition, FBreplica signal is always sent through the pick lower block. It also releases the SS pin to do the other function – light load threshold programming.

The SS control block handles the charge and discharge of the SS capacitor in cause of a ZCS fault. It reset the SSEnd signal when ZCS happens, so the effect of pulling down on SS pin to increase the switching frequency can pass through the pick lower block. The relationship of the SS control block inputs and outputs is the following:

$$SSEnd = SSEn \,\&\, (!ZCS) \,\&\, (!FBLessThanSS) \quad (4)$$

$$ChargeSS = SSEn \,\&\, (!SSEnd) \,\&\, (!ZCS) \quad (5)$$

6.3.7 Pick Higher Block and Burst Mode Multiplexer

The output of the pick lower block goes into a pick higher block, which selects the higher of the pick lower block output and the burst mode threshold setting.

The burst mode multiplexer selects between BMT and ground. During soft start, the multiplexer selects ground. The startup process is open loop and controlled by the soft start ramp. Burst mode is not enabled during soft start phase.

After soft start, the higher of the two inputs are sent to the differential amplifier. The other output is a comparator output FBLessThanBMT. It is sent to the waveform generator state machine to control burst mode and system external shut down.

6.3.8 VCR Comparators

The output of the pick higher block is sent to a differential amplifier to convert the signal to two thresholds symmetrical to Vcm. The difference between the two thresholds Vthh and Vthl equals the input amplitude. The VCR pin voltage is then compared with Vthh, Vthl, and Vcm. The results are sent to the waveform generator.

Feature Description (continued)

6.3.9 Resonant Capacitor Voltage Sensing

The resonant capacitor voltage sense pin senses the resonant capacitor voltage through a capacitor divider. Inside the device, two well matched, controlled current sources are connected to VCR pin to generate the frequency compensation ramp. The on/off control signals in of the two current sources come from the waveform generator block.

During waveform generator IDLE state or before startup, short VCR node to Vcm. This action will help reduce the startup peak current, and help VCR voltage to settle down quickly during burst mode.

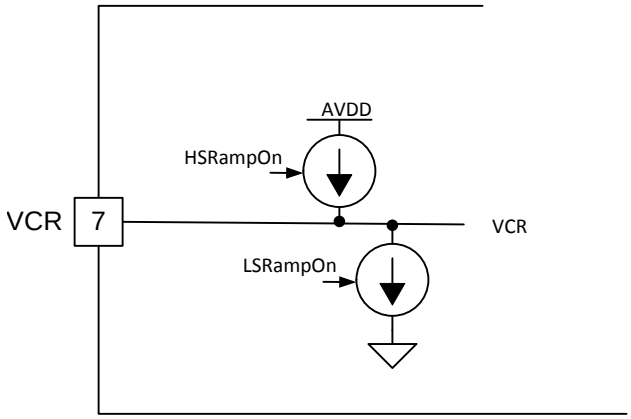


Figure 31. VCR Block Diagram

The ramp current on/off sequence is shown in Figure 32. The ramp current is on all the time. It changes direction at the falling edge of high side on or low side on signal.

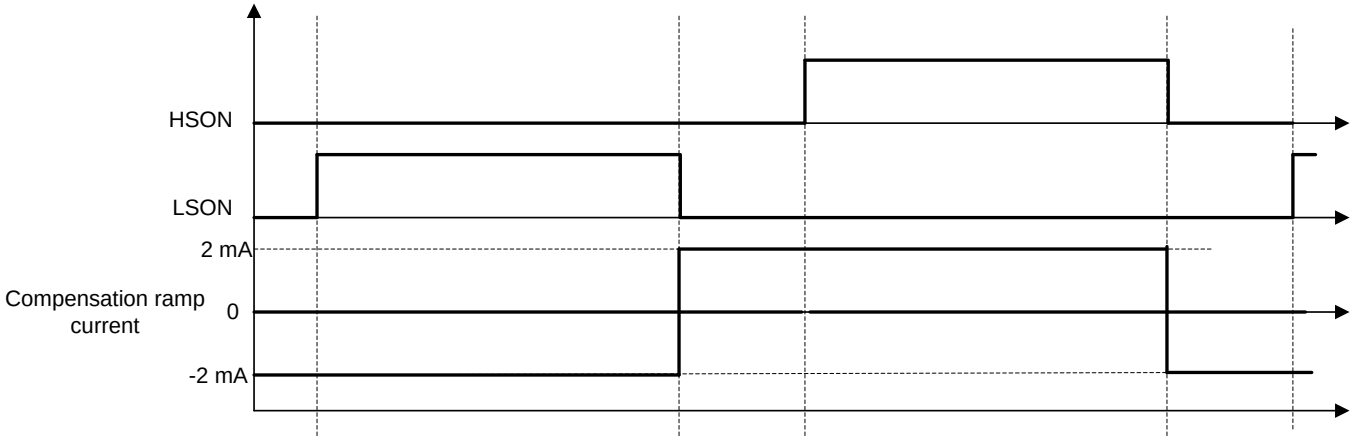


Figure 32. VCR Compensation Ramp Current On/Off

On VCR pin, a capacitor divider is used to mix the resonant capacitor waveform and the compensation ramp waveform. Adjusting the size of the external capacitors can change the contribution of charge control and direct frequency control. Assume the divided down version of the resonant capacitor voltage by the capacitor divider is V_{div}, the compensation ramp current resulted voltage on VCR pin is V_{ramp}. If V_{div} is much larger than V_{ramp}, the control method is similar to charge control, in which the control effort is proportional to the input charge of one switching cycle. If V_{ramp} is much larger than V_{div}, the control method is similar to direct frequency control, in which the control effort is proportional to the switching frequency. The most optimal transient response can be achieved by adjusting the ratio between V_{div} and V_{ramp}.

Feature Description (continued)

6.3.10 Resonant Current Sensing

The ISNS pin is connected to the resonant capacitor using a high voltage capacitor. The capacitor CISNS and the resistor RISNS form a differentiator. The resonant capacitor voltage is differentiated to get the resonant current. The differentiated signal is AC and goes both positive and negative. In order to sense the zero crossing, the signal is level shifted using an op amp adder. IPolarity comparator detects the direction of the resonant current. The digital state machine implements a blanking time on IPolarity – IPolarity edges during the first 400ns of dead time are ignored.

OCP2 and OCP3 thresholds are based on average input current. To get the average input current, the differentiator output is multiplexed with the high side switch on signal HSON: when HS is on, the MUX output is the differentiator output; when HS is off, the MUX output is 0. The MUX output is then averaged using a low pass filter. The output of the filter is the sensed average input current. Note that the MUX needs to pass through both positive and negative voltages. OCP2 and OCP3 faults have a 2ms and 50ms timer respectively. Only when the OCP2/OCP3 comparators output high for continuous 2ms or 50ms, the faults will be activated.

OCP1 threshold is set on the peak resonant current. The voltage on the ISNS pin gets compared to OCP1 threshold OCP1Th directly. The peak resonant current is checked once per cycle on the positive half cycle. OCP1 fault is only activated when there are 4 consecutive cycles of OCP1 event detected. During start up, the OCP1 comparator output of the first 15 cycles are ignored.

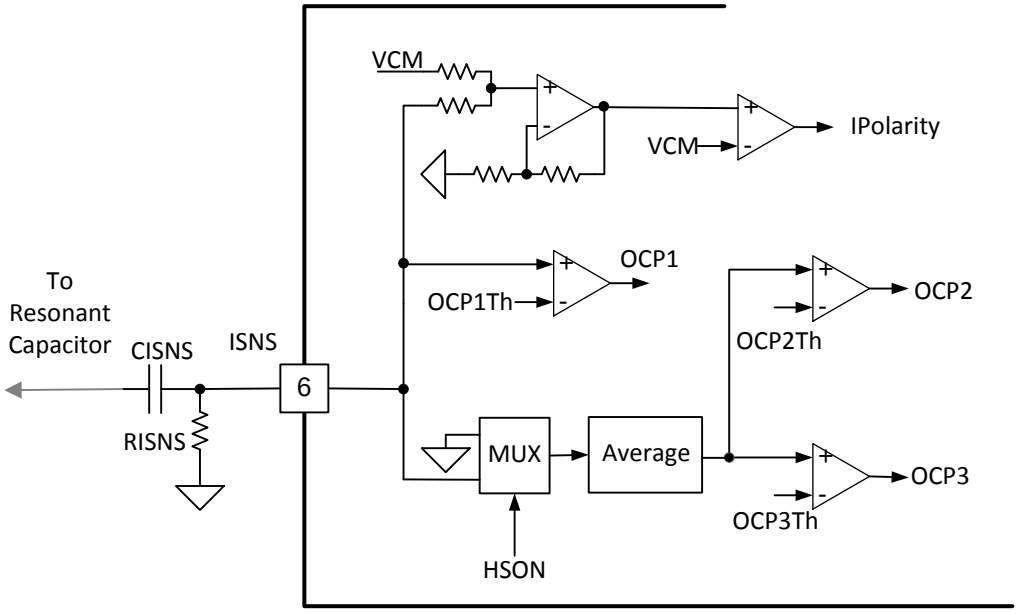


Figure 33. ISNS Block Diagram

Feature Description (continued)

6.3.11 Bulk Voltage Sensing

The BLK pin is used to sense the LLC DC input voltage (bulk voltage) level. The comparators on BLK pin set the following thresholds:

- Bulk voltage level when LLC starts switching – BLKStartTh
- Bulk voltage level when LLC stops switching – BLKStopTh
- Bulk voltage level when bulk over voltage fault is generated – BLKOVRiseTh
- Bulk voltage level when bulk over voltage fault is cleared – BLKOVFallTh

BLKOV signal is generated by one comparator with two thresholds selected by a MUX. This is to create necessary hysteresis for the BLKOV fault. The BLKSns signal is buffered and sent to burst mode threshold generation block to implement the adaptive burst mode threshold.

Figure 34 shows the block diagram of the BLK pin.

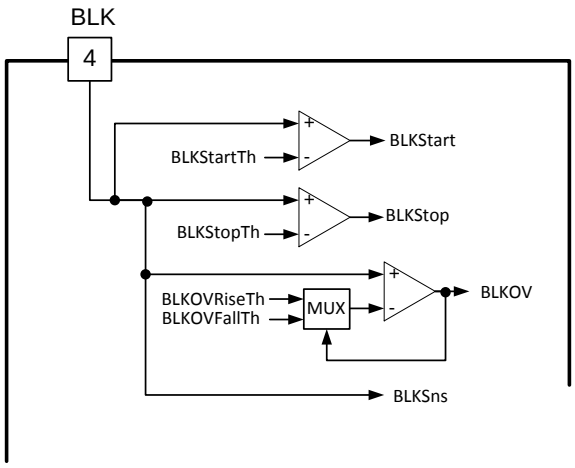


Figure 34. VCR Compensation Ramp Current On/Off

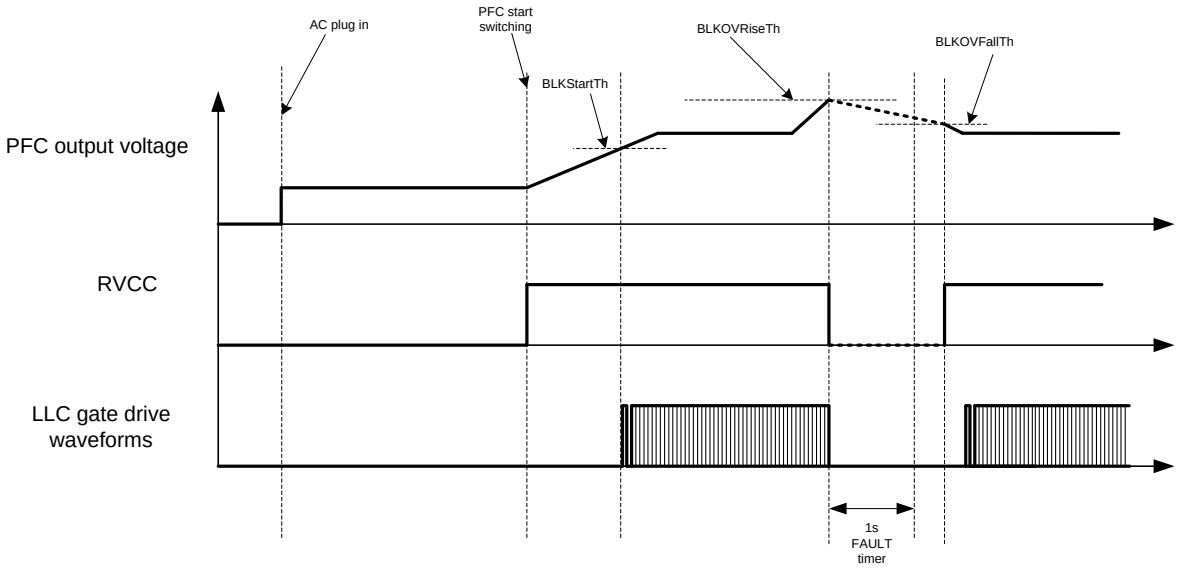


Figure 35. Timing Diagram of BLK Operations

Feature Description (continued)

6.3.12 Output Voltage Sensing

The output voltage is sensed through the bias winding (BW) voltage sense pin. The sensed output voltage is compared with a fixed threshold to generate output OVP fault. The block diagram of the bias winding voltage sense block is shown below.

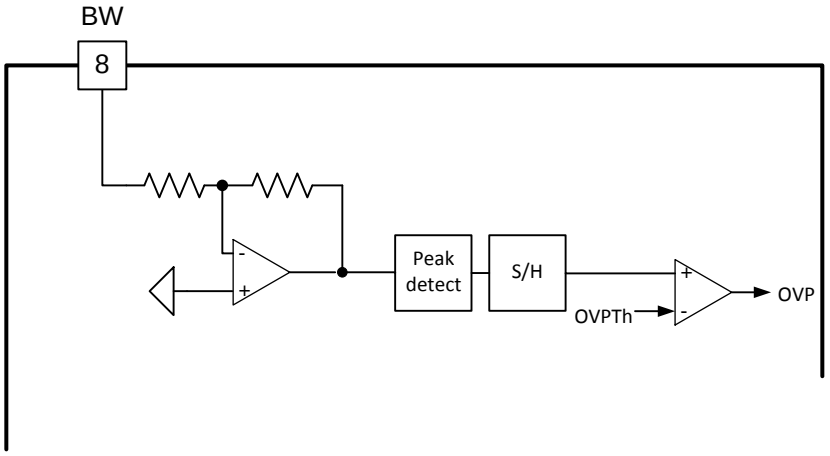


Figure 36. Bias Winding Sensing Block Diagram

The bias winding sense block consists of an inverting op amp to flip the BW signal. The flipped BW signal is then peak detected and sampled at low side turn off edge. The sampled voltage represents the output voltage during this cycle. The S/H output is them compared with OVP comparator. Shown below is the timing diagram of the BW sense block.

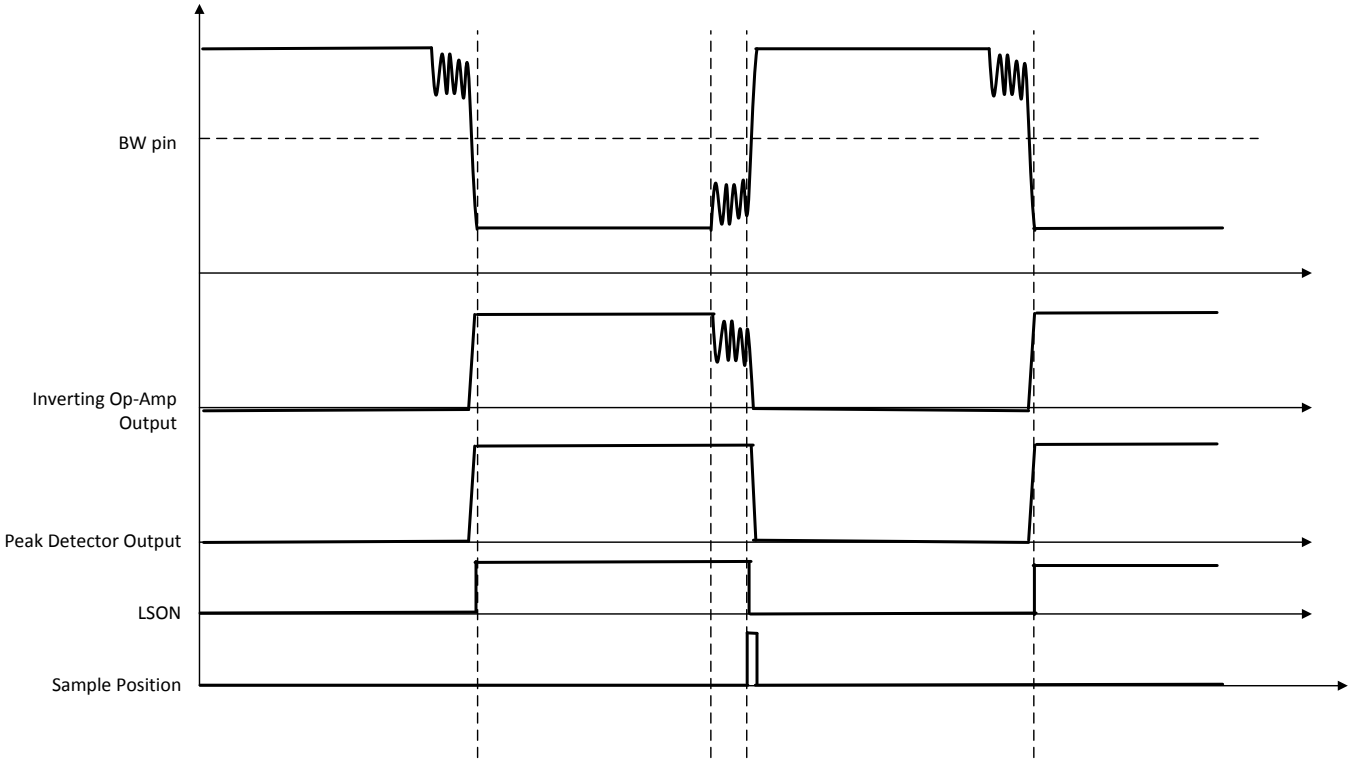


Figure 37. Timing Diagram of BW Sense Block

Feature Description (continued)

6.3.13 High Voltage Gate Driver

The low-side gate driver output is LO. The gate driver is supplied by the 12-V RVCC rail.

The high-side driver module consists of three physical device pins. HB and HS form the positive and negative rails, respectively, of the high-side driver, and HO connects to the gate of the upper half-bridge MOSFET.

During periods when the lower half-bridge MOSFET is conducting, HS is shorted to GND via the conducting lower MOSFET. At this time power for the high side driver is obtained from RVCC via high voltage diode DBOOT, and capacitor CBOOT is charged to RVCC minis the forward drop on the diode.

During periods when the upper half-bridge MOSFET is conducting, HS is connected the LLC input voltage rail. At this time the HV diode is reverse biased and the high side driver is powered by charge stored in CBOOT.

The slew on HS pin is detected for adaptive dead time adjustment. The next gate is only turned on when the slew on HS pin is finished.

Both the high-side and low side gate drivers have under voltage lock out (UVLO) protection. The low side gate driver UVLO is implemented on RVCC; the high side gate driver UVLO is implemented on (HB - HS) voltage.

When operating at light load, UCC256302 enters burst mode. During the burst off period, the gate driver enters low power mode to reduce power consumption.

The block diagram of the gate driver is shown in Figure 38.

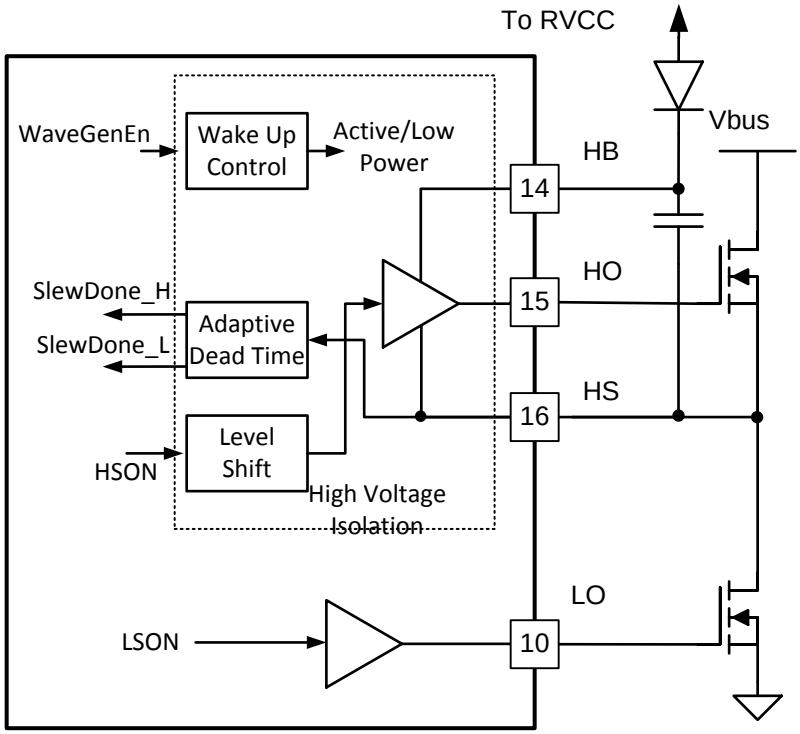


Figure 38. Gate Driver Block Diagram

Feature Description (continued)

6.3.14 Protections

6.3.14.1 ZCS Region Prevention

Capacitive region is an LLC operation region in which the voltage gain increases when the switching frequency increases. It is also called ZCS region. Capacitive mode operation should be avoided for two reasons:

- The feedback loop becomes positive feedback in capacitive region
- The MOSFET may be damaged because of body diode reverse recovery

To make sure that capacitive region operation does not happen, we need to first rely on the slew done signal. If there is a slew done signal detected, it suggests that the opposite body diode must not be conducting and to turn on the next FET. If there is no slew detected, IPolarity signal is used. The next gate will be turned on at the next IPolarity flip event. The IPolarity flip indicates that the capacitive operation cycle has already passed. The resonant current reverses the direction and begins to discharge the switch node. When the capacitive operation cycle has passed, the system enters a high frequency oscillation stage, where the oscillation frequency is determined by the parasitic elements in the circuit. In this stage, the body diode is no longer conducting and it is allowed to turn on the next gate.

However, in the high frequency oscillation stage, the resonant current may be so small that the IPolarity detection is missed. In this case, the next gate will be turned on by maximum dead time timer expiration.

In addition to preventing the next gate from turning on when the opposite body diode is conducting, the switching frequency is forced to ramp up until there is a cycle with no capacitive region operation detected

The capacitive region detection is done by checking the resonant current polarity at HSON or LSON falling edge. If the resonant current is positive at LSON falling edge, or negative at HSON falling edge, the ZCS signal in the waveform generator is turned high. The ZCS signal keeps high until there is a half cycle without capacitive region operation happens.

The force ramping up of the switching frequency is done by pull the SS pin down by a resistor to ground. Details will be discussed in SS pin section.

Below is the flow chart of capacitive region prevention algorithm:

Feature Description (continued)

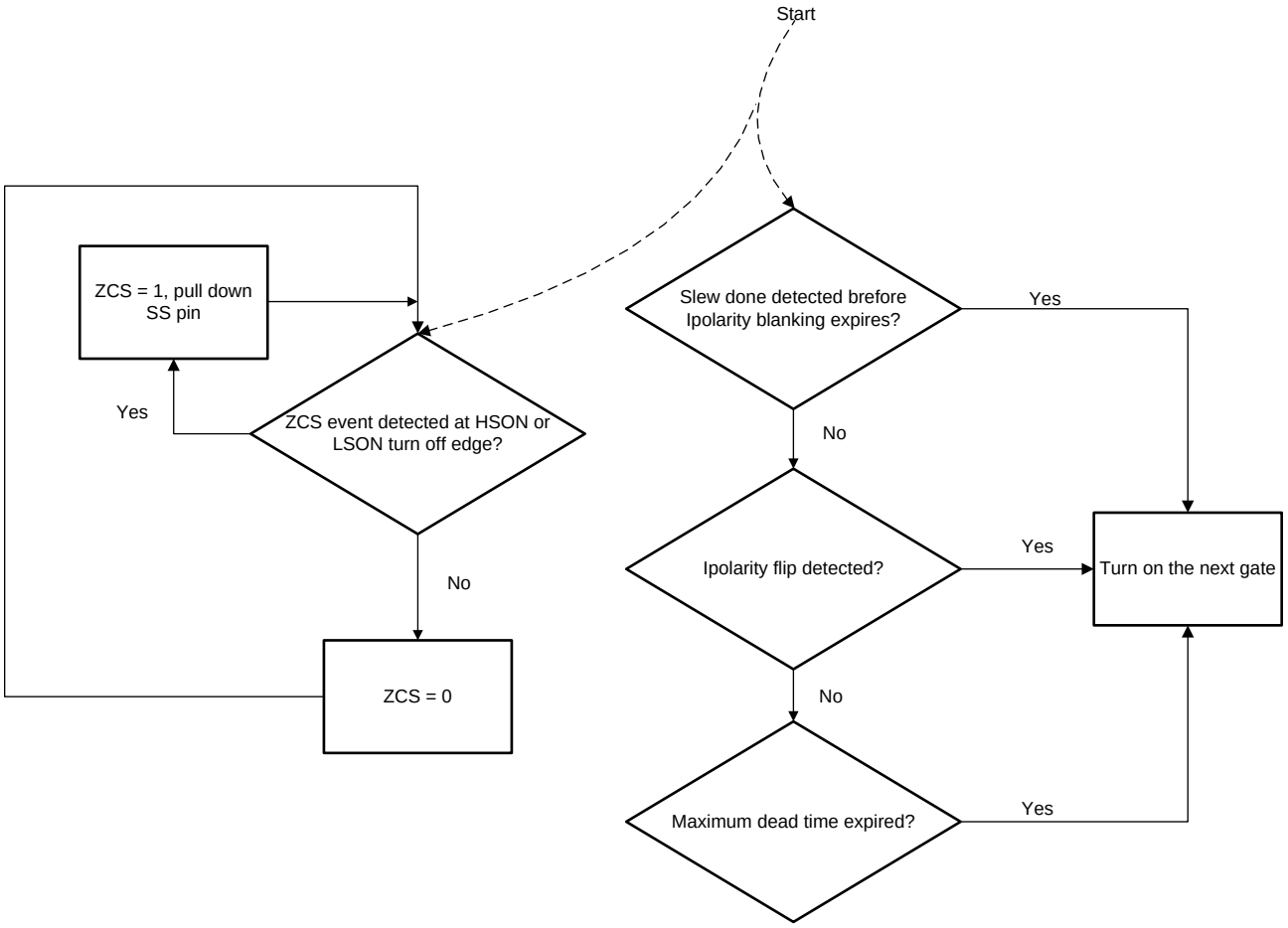


Figure 39. Gate Driver Block Diagram

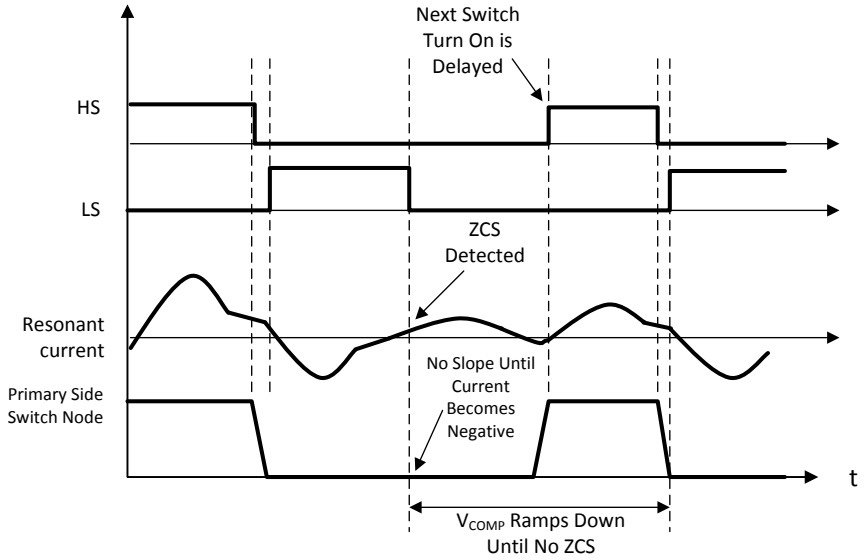


Figure 40. Timing Diagram of a ZCS Event

Feature Description (continued)

6.3.14.2 Over Current Protection (OCP)

There are three levels of OCP:

1. OCP1: peak current protection (highest threshold)
    1. Fault action: count OCP1 cycles and shut down power stage if counter exceeds preset value
2. OCP2: average input current protection (high threshold)
    1. Fault action: if above threshold for 2 ms, shut down
3. OCP3: average input current protection (low threshold)
    1. Fault action: if above threshold for 50 ms, shut down

The circuit block diagram has been discussed in the *Resonant Current Sensing* section.

6.3.14.3 Over Output Voltage Protection (VOUTOVP)

This is the output over voltage protection. VOUTOVP threshold is set on the bias winding voltage sense. The VOUTOVP trip point can be set by configuring the voltage divider on BW pin.

6.3.14.4 Over Input Voltage Protection (VINOVP)

This is the input over voltage protection. The fault actions have been discussed in the BLK section. The trip point can be set by configuring the voltage divider on BLK pin.

6.3.14.5 Under Input Voltage Protection (VINUVP)

This is the input under voltage protection. The fault actions have been discussed in the BLK section. The trip point can be set by configuring the voltage divider on BLK pin.

6.3.14.6 Boot UVLO

This is the high side gate driver UVLO. When (HB – HS) voltage is less than the threshold, the high side gate output will be shut down.

6.3.14.7 RVCC UVLO

This is the regulated 12-V UVLO. When RVCC voltage is less than the threshold, both the high side gate output and the low-side gate output will be turned off.

6.3.14.8 Over Temperature Protection (OTP)

This is the device over temperature protection. When OTP fault is tripped, if the device is switching, the switching will stop. If the device is in HV start up stage and JFET is on, the JFET will be turned off. Details of the OTP fault handling will be discussed in the *Device Functional Modes* section.

There are two digital state machines in the system:

- System States and Faults State Machine
- Waveform Generator Stage Machine

The system states control state machine controls system operation states and faults. The waveform generator state machine controls the gate driver behavior.

6.4 Device Functional Modes

6.4.1 Burst Mode Control

The efficiency of an LLC converter power stage drops rapidly with falling output power. To maintain reasonable light load efficiency it is necessary to operate the LLC converter in burst mode. In this mode the LLC converter operates at relatively high power for a short burst period and then all switching is stopped for a space period. During the Burst period excess charge is transferred to and stored in the output capacitor. During the Space period this stored charge is used to supply the load current. Providing an effective light-load scheme is a particular problem for an LLC controller that is located on the primary side of the isolation barrier. This is because the feedback demand signal (V_{COMP}) is mainly a function of input/output voltage ratio and only loosely related to

Device Functional Modes (continued)

load current. The normal method of placing a couple of thresholds in the V_{COMP} voltage window to switch OFF and ON the LLC converter does not work effectively. Another issue with the conventional method is that when burst on, the switching pulses are determined by V_{COMP}, which is usually at initial burst on, and decays as the output voltage rises. The resulting inductor current will be big at first and then decays. This is not optimal because the big current at first may create mechanical vibration. The high switching frequency afterwards may cause two much switching loss.

For an advanced burst mode, the following features are desired:

- The power delivered by each burst should be relatively constant for a certain load.
- The Burst power is set high enough to provide reasonable LLC converter efficiency and low enough to avoid acoustic noise and excessive output voltage ripple.
- When burst on, the average capacitor voltage should settle to $V_{IN}/2$ as fast as possible for best efficiency.
- The switching frequency or burst power level of each burst pulse should be optimized for efficient operation.
- The burst pattern of each burst should be relatively constant.
- There should be no audible noise.
- Burst mode performance should be consistent across input voltage range.

The HHC method makes the control of the burst mode very straight forward. The block diagram is a functionally accurate description of the burst mode control method in UCC25630.

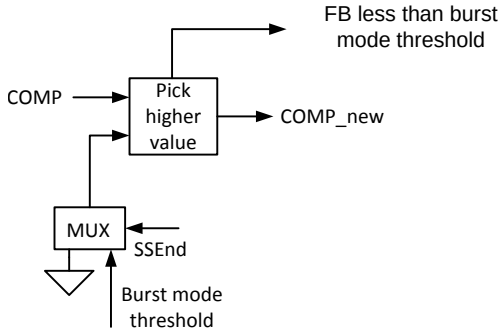


Figure 41. Burst Mode Control Block Diagram

The control effort is selected between the higher of the two signals: 1) the voltage loop compensator output (V_{COMP}) or 2) the Burst Mode Threshold level (BMT). When V_{COMP} goes below BMT, continue switching for a fixed number of switching cycles, then stop. Always switch while COMP is higher than BMT. If soft start isn't done yet, send the COMP (controlled by soft start ramp). BMT is programmable and adaptively changed with input voltage. The last pulse of each burst on period is turned off when the resonant capacitor voltage equals $V_{IN}/2$. In HHC method, this is approximately equivalent to VCR node voltage equals the common mode voltage VCM. This operation keeps the resonant capacitor voltage to about $V_{IN}/2$ for each burst off period, thus enabling the burst pattern to settle as soon as possible during burst on period.

Device Functional Modes (continued)

6.4.2 High Voltage Start-Up

UCC256302 uses a self bias start up scheme, thus eliminating the need of a separate auxiliary flyback power stage. When AC is first plugged in, PFC and LLC are both off. HV pin JFET will be enabled and will start to deliver current from a source connected to the HV pin to the VCC capacitor. Once the VCC pin voltage exceeds its VCCStartSwitching threshold, the current source will be turned off and RVCC will be enabled to turn on the PFC. When PFC output voltage reaches a certain level, LLC is turned on. When LLC is operating and the output voltage is established, the bias winding will supply current for both the PFC and the LLC controller devices.

6.4.3 Soft-Start and Burst-Mode Threshold

The soft-start programming and burst mode threshold programming are multiplexed on one pin – LL/SS. In addition, when ZCS region operation happens, this pin is pulled down to ground through a resistor to increase the switching frequency.

An internal constant current source charges the soft start capacitor to generate the soft-start command. Soft start period starts right after charge boot stage is done, and ends when FBreplica becomes lower than SS pin voltage.

After soft start is done, the SS voltage is replaced by AVDD to send to the FB chain. The LL/SS pin is then used to generate the burst mode threshold. In UCC256302 we try to maintain the same burst mode power level over the input voltage range. This is done by adaptively changing the burst mode threshold with sensed BLK voltage.

The programming resistors output provide two degrees of freedom, to set the burst mode threshold, as well as how the threshold changes with BLK voltage. When programmed correctly, the power stage will always enter burst mode at a certain output current level, making the system much easier to optimize.

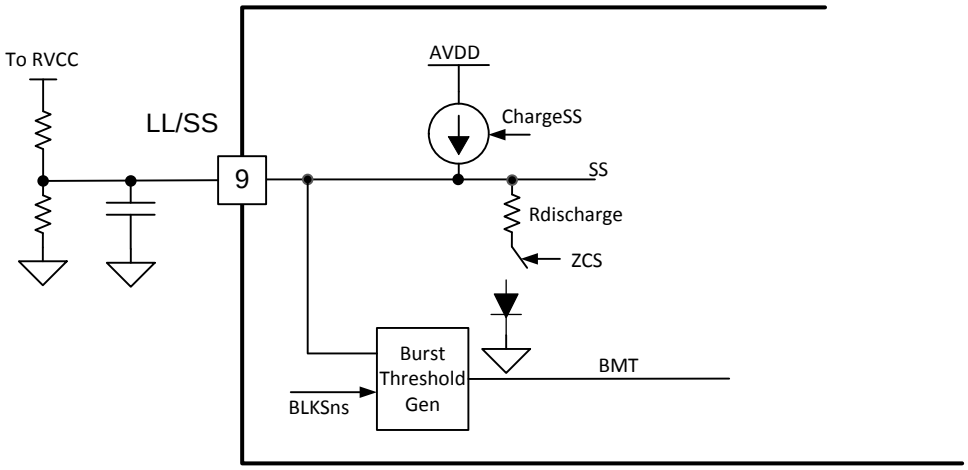


Figure 42. LL/SS Block Diagram

Device Functional Modes (continued)

6.4.4 System States and Faults State Machine

Below is an overview of the system states sequence:

The state transition diagram starts from the un-powered condition of UCC25630. As soon as the system is plugged in, HV pin JFET will be enabled and will start to deliver current from a source connected to the HV pin to the VCC capacitor. Once the VCC pin voltage exceeds its VCCStartSwitching threshold, system state will change to JFETOFF. When PFC output voltage reaches a certain level, LLC is turned on. Before LLC starts running, the LO pin is kept high to pull the HS node of the LLC bridge low, thus allowing the capacitor between HB and HS pins to be charged from VCC via the bootstrap diode. UCC256302 will remain in the CHARGE_BOOT state for a certain time to ensure the boot capacitor is fully charged. When LLC output voltage reaches a certain level, both PFC and LLC gets power from LLC transformer bias winding. When the load drops to below a certain level, LLC operates in burst mode

Fault conditions encountered by UCC256302 will cause operation to stop, or paused for a certain period of time followed by an automatic re-start. It is to ensure that while a persistent fault condition is present, it is not possible for UCC256302 or the power converter temperature to continue to rise as a result of the repeated re-start attempts.

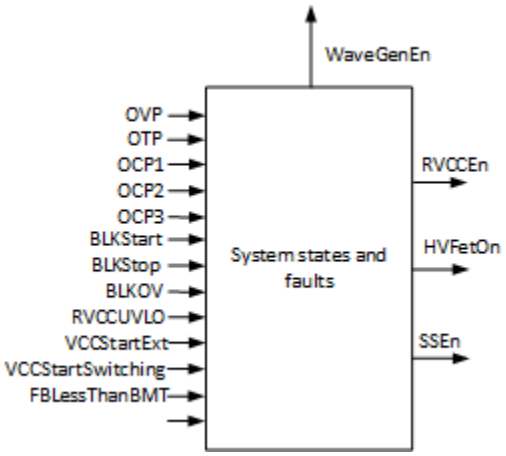


Figure 43. Block Diagram of System States and Faults State Machine

Device Functional Modes (continued)

Table 1 summarizes the inputs and outputs of Figure 43

Table 1. System States and Faults State Machine Block Inputs and Outputs

SIGNAL NAME	I/O	DESCRIPTION
OVP	I	Output over voltage fault
OTP	I	Over temperature fault
OCP1	I	Peak current fault
OCP2	I	Average current fault with 2ms timer
OCP3	I	Average current fault with 50ms timer
BLKStart	I	Bulk voltage is above start threshold
BLKStop	I	Bulk voltage is below stop threshold
BLKOV	I	Bulk over voltage fault
RVCCUVLO	I	RVCC UVLO fault
VCCReStartJfet	I	VCC is below restart threshold
VCCStartSwitching	I	VCC is above start switching threshold (the threshold is different in self bias mode and external bias mode)
FBLessThanBMT	I	FBReplica voltage is less than burst mode threshold
WaveGenEn	O	Waveform generator enable
RVCCEn	O	RVCC enable
SSEn	O	Soft start enable
HVFetOn	O	Turn on or off JFET

The state machine is shown in Figure 44 and the description of the states and state transition conditions are in the tables below.

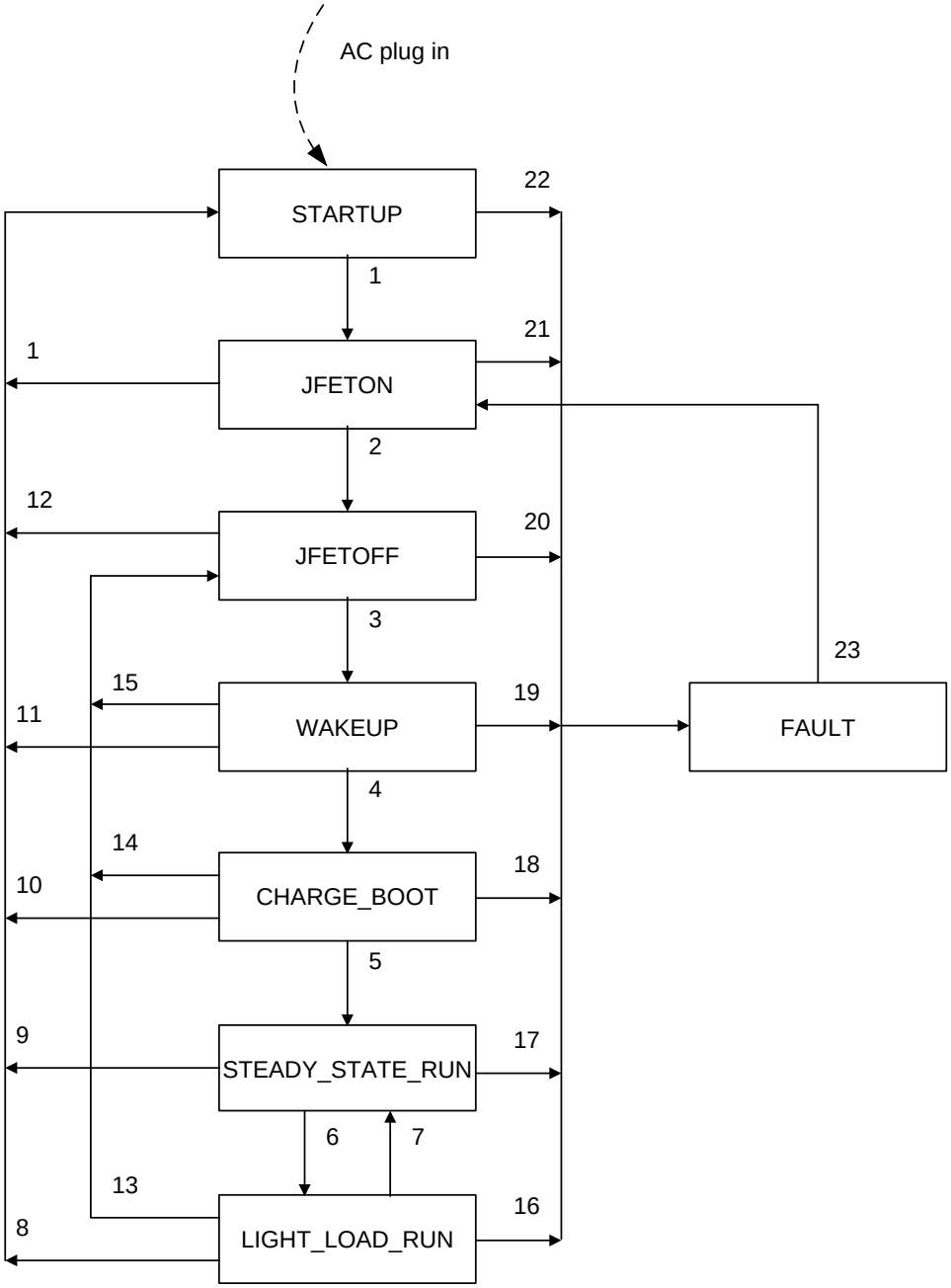


Figure 44. System States and Faults State Machine

Table 2. States in System States and Faults State Machine

STATE	OUTPUT STATUS	DESCRIPTION
STARTUP	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 1	This is the first state after power on reset (POR). In this state, the HV JEFT is on, and it's working in a voltage clamp state where the VCC voltage is regulated to 13V to allow internal circuits to load trim settings and start up.
JFETON	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 1	In this state, the JFET is on. HV start up current is regulated to IHVHigh.
JFETOFF	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When VCC is higher than VCCStartSwitching threshold, the JFET is turned off and system enters JFETOFF state. The regulated RVCC is turned on. PFC soft start begins.
WAKEUP	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When BLK voltage reaches BLKStart level, the system enters WAKEUP state and stay in WAKEUP state for 150us for the analog circuits to wake up.
CHARGE_BOOT	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	In this state, the BOOT capacitor is charged by turning on the low side switch for a certain period of time.
STEADY_STATE_RUN	WaveGenEn = 1 RVCCEn = 1 SSEn = 1 HVFetOn = 0	In this state, the waveform generator is enabled. Soft start module is enabled. LLC starts to soft start. When soft start is done, the system enters normal operation.
LIGHT_LOAD_RUN	WaveGenEn = 1 RVCCEn = 1 SSEn = 1 HVFetOn = 0	If FBReplica is less than burst mode threshold during normal operation, the system enters LIGHT_LOAD_RUN mode. The FBLessThanBMT time is counted. If the time is longer than 200ms, it is treated as a fault, restart the system.
FAULT	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 0	After any fault condition, the system enters FAULT state and waits for 1s before re-start. The 1s timer allows system to cool down and prevents frequent repetitive start up in case of a persistent fault.

Table 3. System States and Faults State Machine State Transition Conditions

STATE TRANSITION CONDITION	DESCRIPTION
1	System ready (trim load done)
2	VCCStartSwitching = 1 VCCReStartJfet = 0
3	BLKStart = 1 BLKStop = 0 BLKOV = 0 RVCCUVLO = 0
4	BLKStart = 1 BLKStop = 0 BLKOV = 0 RVCCUVLO = 0 FBLessThanBMT = 0
5	Charge boot done
6	FBLessThanBMT = 1
7	FBLessThanBMT = 0
8	VCCReStartJfet = 1
9	VCCReStartJfet = 1
10	VCCReStartJfet = 1
11	VCCReStartJfet = 1
12	VCCReStartJfet = 1
13	FBLessThanBMT time out
14	BLKOV = 1
15	BLKOV = 1
16	OTP = 1 or BLKOV = 1 or BLKStop = 1 or OVP or OCP1 or OCP2 time out or OCP3 time out or RVCCUVLO = 1
17	OTP = 1 or BLKOV = 1 or BLKStop = 1 or OVP or OCP1 or OCP2 time out or OCP3 time out or RVCCUVLO = 1
18	OTP = 1
19	OTP = 1
20	OTP = 1
21	OTP = 1
22	OTP = 1
23	1s pause time out

Figure 45 only shows the most commonly used state transition (assuming no faults during start up states so all the states are captured in the timing diagram). Many different ways of state transitions may happen according to the state machine, but are not captured in this section.

In Figure 45, a normal start up procedure is shown. The system enters normal operation and then a fault (OCP, OVP, or OTP) happens.

NOTE

OCP1 and OVP are fast faults and are first processed in the waveform generator state machine.

The system is configured to be restart after 1s pause time.

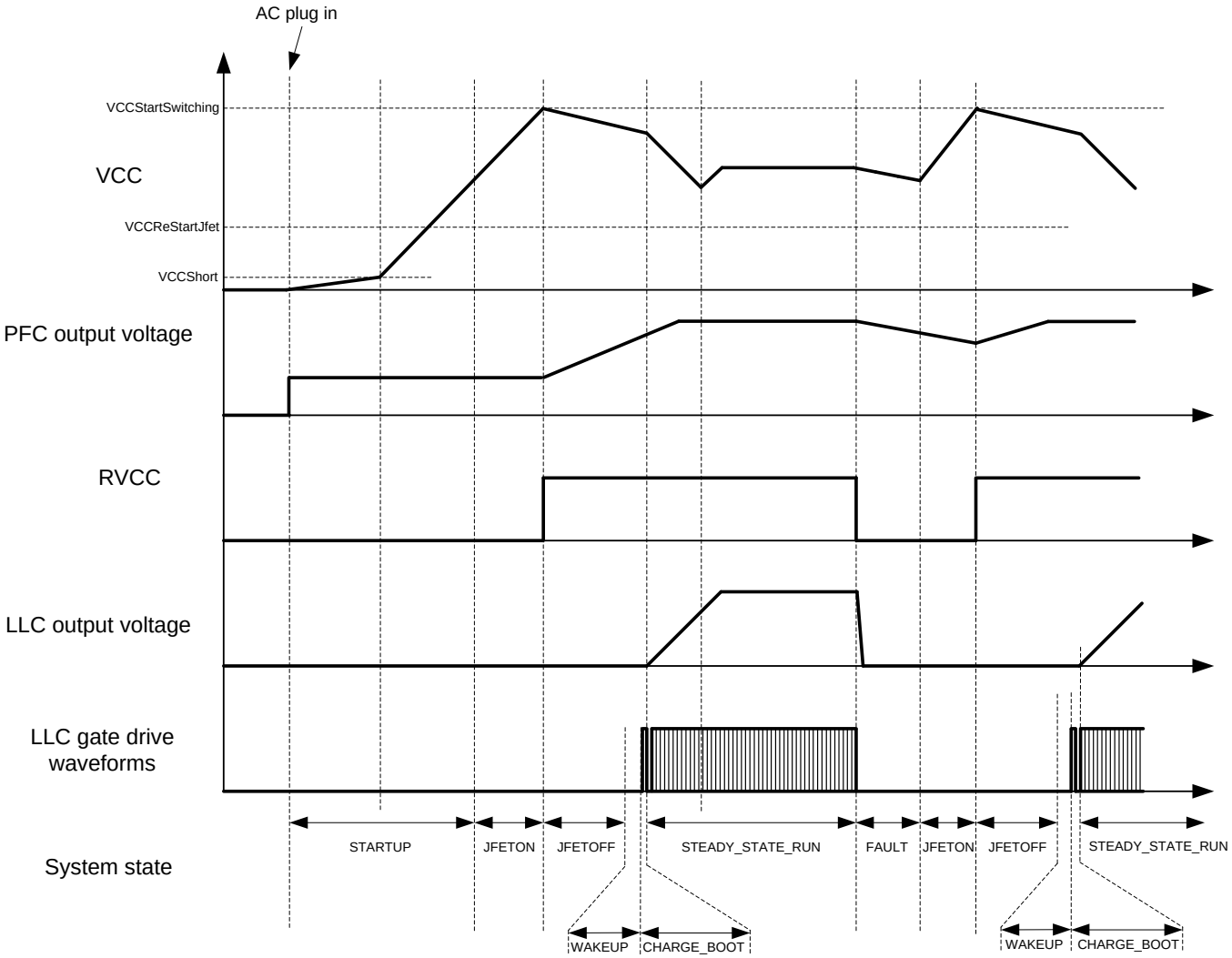


Figure 45. Timing Diagram of System States and Faults

6.4.5 Waveform Generator State Machine

The waveform generator module consists of a state machine that implements hybrid hysteretic control, adaptive dead time, and ZCS protection. Each cycle of LLC operation is broken down into 4 separate periods: HSON, DTHL, LSON, and DTLH. In addition, there is an IDLE state and a WAKEUP state.

The initial state of this state machine is IDLE. In IDLE state, the system is operating in a low power mode. When WaveGenEn command is received, the state machine enters WAKEUP state to turn on various circuit blocks. Once the WAKEUP timer is expired, the system enters LSON (low side on) state. LSON state is followed by DTLH (dead time high to low) state, which is the dead time state. After DTLH state, the high side turns on and system enters HSON. HSON state is followed by DTHL (dead time low to high) state. After DTHL, the system goes back to LSON state again.

There are minimum and maximum timers in each of the states. The state transition conditions and descriptions are discussed in detail below.

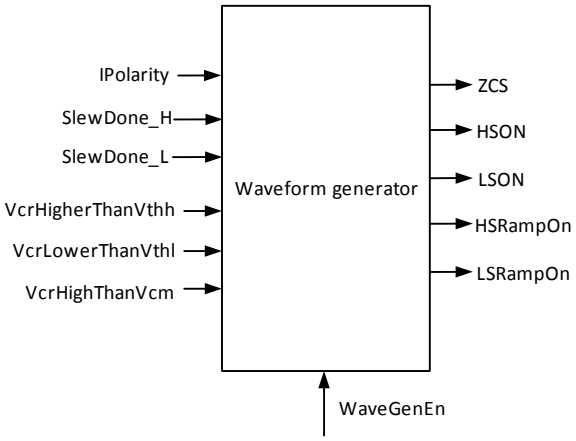


Figure 46. Waveform Generator State Machine Block Diagram

Table 4 summarizes the inputs and outputs of the Waveform Generator State Machine Block Diagram

NOTE

OVP and OCP1 faults are not listed here. But they are processed in the wave gen state machine before handled to system states and faults state machine.

Table 4. Waveform Generator State Machine Inputs and Outputs

SIGNAL NAME	I/O	DESCRIPTION
IPolarity	I	Polarity of the resonant current (Note: this signal has a 1us blanking time during dead time. IPolarity signal listed here is after blanking. See ISNS section for details.)
SlewDone_H	I	Primary side switch node completes slewing from low to high
SlewDone_L	I	Primary side switch node completes slewing from high to low
VcrHigherThanVthh	I	VCR voltage is higher than the high threshold Vthh
VcrLowerThanVthl	I	VCR voltage is lower than the low threshold Vthl
VcrHighThanVcm	I	VCR voltage is high than the common mode voltage Vcm
WaveGenEn	I	Waveform generator enable
ZCS	O	Zero current switching is detected
HSON	O	High side gate driver on
LSON	O	Low side gate driver on
HSRampOn	O	High side compensation current ramp on
LSRampOn	O	Low side compensation current ramp on

The state machine is shown in Figure 47 and the description of the states and state transition conditions are in Table 5.

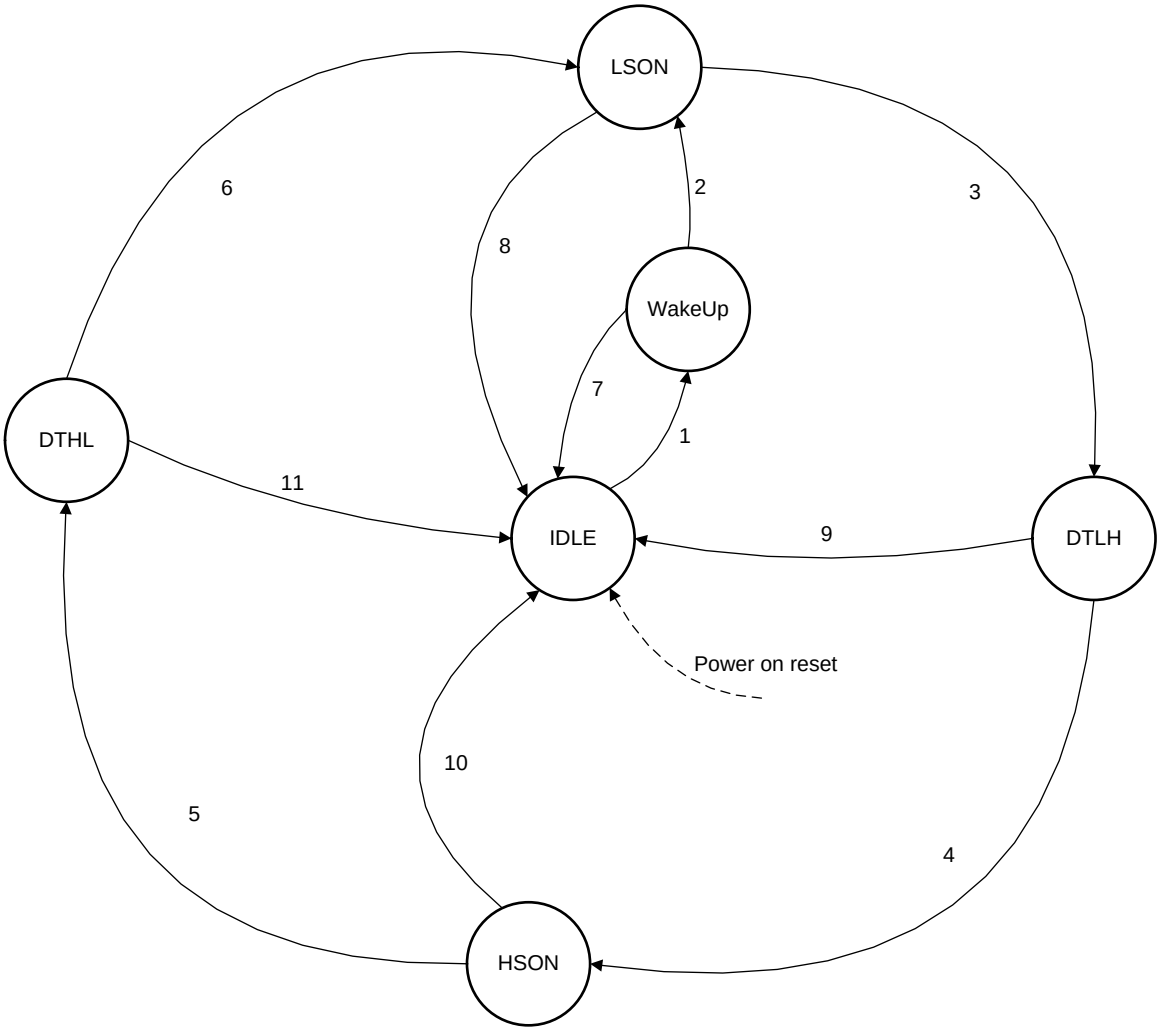


Figure 47. Waveform Generator State Machine

Table 5. States in Waveform Generator State Machine

STATE	OUTPUT STATUS	DESCRIPTION
IDLE	HSON = 0 LSON = 0 HSRampOn = 0 LSRampOn = 0 ZCS = 0	Both high side and low side are off in this state. Various circuits are operating in low power mode. This is the first state after POR. During burst off period, the system is in IDLE state as well. Upon entering IDLE state, load burst cycle counter, switching cycle counter, OCP1 counter, and OVP counter. Load startup cycle counter if WaveGenEn_Rising = 1
WakeUp	HSON = 0 LSON = 0 HSRampOn = 0 LSRampOn = 0 ZCS = 0	In this state, internal circuits wake up from low power mode.
LSON	HSON = 0 LSON = 1 HSRampOn = 0 LSRampOn = 1 ZCS = 0 or 1	In this state, the low side gate turns on; the low side ramp current source turns on. ZCS may be 0 or 1 depends on the detected result. More details will be described in ZCS section. Enable low side on timer.
DTLH	HSON = 0 LSON = 0 HSRampOn = 1 LSRampOn = 0 ZCS = 0 or 1	Dead time from low side on to high side on. Low side ramp current source turns off. High side ramp current source turns on. Enable dead time timer.
HSON	HSON = 1 LSON = 0 HSRampOn = 1 LSRampOn = 0 ZCS = 0 or 1	In this state, the high side gate turns on; the high side ramp current source turns on. ZCS may be 0 or 1 depends on the detected result. More details will be described in ZCS section. Enable high side on timer.
DTHL	HSON = 0 LSON = 0 HSRampOn = 0 LSRampOn = 1 ZCS = 0 or 1	Dead time from high side on to low side on. High side ramp current source turns off. Low side ramp current source turns on. Enable dead time timer.

Table 6. Waveform Generator State Machine State Transition Conditions

STATE TRANSITION CONDITION	DESCRIPTION
1	WaveGenEn = 1 and FBLessThanBMT = 0 and minimum IDLE time expired
2	Wake up time expired
3	(VcrLowerThanVthl = 1 or LSON max timer expired) and LSON min timer expired
4	StartUpCounterExpired = 0 and DTStartUpTimerExpired = 1 DTMaxTimerExpired = 1 SlewDone_H = 1 SlewDone_H = 1 and MeasuredDTExpired = 1; (Note: this condition and the condition above is selectable using a trim bit, depending on whether dead time measure and match feature is wanted) IPolarityFallingEdgeDetected = 1
5	(VcrHigherThanVthh = 1 or HSON max timer expired) and HSON min timer expired
6	StartUpCounterExpired = 0 and DTStartUpTimerExpired = 1 DTMaxTimerExpired = 1 SlewDone_L = 1 IPolarityFallingEdgeDetected = 1
7	WaveGenEn = 0
8	WaveGenEn = 0 (VcrLowerThanVthl = 1 or LSON max timer expired) and LSON min timer expired and (OCP1 counter expire or OVP counter expire)
9	WaveGenEn = 0
10	WaveGenEn = 0 BurstModeCountExpire = 1 and VcrHigherThanVcm = 1 and FBLessThanBMT = 1 and HSON min time expired
11	WaveGenEn = 0

Table 7. Waveform Generator State Machine Internal Counters and Timers

INTERNAL VARIABLE	DESCRIPTION
Switching cycle counter	This counter counts the switching cycle
OVP counter	Bias Winding Overvoltage counter. The counter decrements every time a Bias Winding Overvoltage occurs
Startup counter	Startup Counter. Counter gets set to 15 when wave generator enable toggles from low to high, and then decrements every switching cycle. When the count hits 0, the dead time state is no longer permitted to be exited via the startup dead time expiration.
Burst cycle counter	Burst counter. Counter gets set to 15 and then decrements every switching cycle until it hits ‘0’. If FBLessThanBMT = 1 when the counter is ‘0’, the switcher will stop until FBLessThanBMT = 0.
OCP1 counter	OCP1 counter. Counter gets set to 4 and then decrements every switching cycle when OCP1 occurs, until it hits ‘0’
Wakeup timer	Wakeup state timer
DT max timer	Maximum dead time timer
Startup dead time max timer	Dead time max clamp for the first few start up cycles before the startup counter expires
Gate on min timer	Minimum gate on time timer
Gate on max timer	Maximum gate on time timer

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

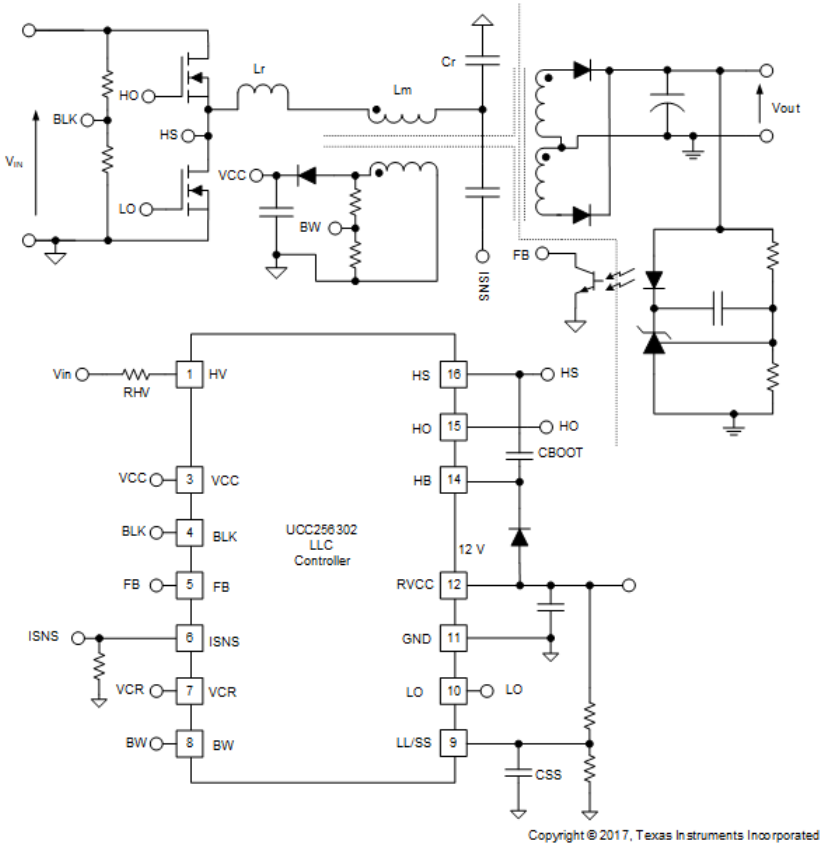
UCC256302 can be used in a wide range of applications in which LLC topology is implemented. In order to make the part easier to use, TI has prepared a list of materials to demonstrate the features of the device:

- Full featured EVM hardware
- A excel design calculator
- Simulation models
- Application notes on Hybrid Hysteretic Control theory

In the following sections, a typical design example is presented.

7.2 Typical Application

Shown below is a typical half bridge LLC application using UCC256302 as the controller.



Typical Application (continued)

7.2.1 Design Requirements

The design specifications are summarized in Table 8.

Table 8. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC Voltage range		340	390	410	VDC
AC Voltage range		85		264	VAC
AC Voltage frequency		47		63	Hz
Input DC UVLO On			320		VDC
Input DC UVLO Off			250		VDC
Input DC current	Input = 340 VDC, full load = 10 A		0.383		A
Input DC current	Input = 390 VDC, full load = 10 A		0.331		A
Input DC current	Input = 410 VDC, full load = 10 A		0.315		A
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	340 VDC to 410 VDC			10	A
Output voltage ripple	390 VDC and full load = 10 A		130		mVpp
SYSTEMS CHARACTERISTICS					
Switching frequency		53		160	kHz
Peak efficiency	390 VDC, load = A		92.9		
Operating temperature	Natural convection		25		ºC

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC256302 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 LLC Power Stage Requirements

Start the design by deciding the LLC power stage component values. The LLC power stage design procedure outlined here follows the one given in the TI application note “Designing an LLC Resonant Half-Bridge Power Converters”. The application note contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. An alternative design approach is given in TI application note SLUA733, LLC Design for UCC29950.

7.2.2.3 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$n = \frac{V_{IN(nom)} / 2}{V_{OUT(nom)}} = \frac{390 / 2}{12} = 16.25 \Rightarrow 16 \quad (6)$$

Then determine the LLC gain range $M_{g(min)}$ and $M_{g(max)}$. Assume there is a 0.5-V drop in the rectifier diodes (V_f) and a further 0.5-V drop due to other losses (V_{loss}).

$$M_{g(\min)} = n \frac{V_{OUT(min)} + V_f}{V_{IN(max)} / 2} = 16 \frac{12 + 0.5}{410 / 2} = 0.976 \quad (7)$$

$$M_{g(\max)} = n \frac{V_{OUT(max)} + V_f + V_{\text{loss}}}{V_{IN(min)} / 2} = 16 \frac{12 + 0.5 + 0.5}{340 / 2} = 1.224 \quad (8)$$

7.2.2.4 Select L_n and Q_e

L_n is the ratio between the magnetizing inductance and the resonant inductance.

$$L_n = \frac{L_m}{L_r} \quad (9)$$

Q_e is the quality factor of the resonant tank.

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e} \quad (10)$$

In this equation, R_e is the equivalent load resistance.

Selecting L_n and Q_e values should result in an LLC gain curve, as shown below, that intersects with $M_{g(min)}$ and $M_{g(max)}$ traces. The peak gain of the resulting curve should be larger than $M_{g(max)}$. Details of how to select L_n and Q_e are not discussed here. They are available in the Application Note, UCC25630x Practical Design Guidelines and UCC256302 Design Calculator.

In this case, the selected L_n and Q_e values are:

$$L_n = 13.5 \quad (11)$$

$$Q_e = 0.15 \quad (12)$$

7.2.2.5 Determine Equivalent Load Resistance

Determine the equivalent load resistance by Equation 13.

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times 16^2}{\pi^2} \times \frac{12}{10} = 249\,\Omega \quad (13)$$

7.2.2.6 Determine Component Parameters for LLC Resonant Circuit

Before determining the resonant tank component parameters, a nominal switching frequency (resonant frequency) should be selected. In this design, 100 kHz is selected as the resonant frequency.

$$f_0 = 100\,kHz \tag{14}$$

The resonant tank parameters can be calculated as the following:

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e} = \frac{1}{2\pi \times 0.15 \times 100\,kHz \times 249\,\Omega} = 42.6 \tag{15}$$

$$L_r = \frac{1}{\left(2\pi \times f_0\right)^2 C_r} = \frac{1}{\left(2\pi \times 100\,kHz\right)^2 \times 42.6\,nF} = 59.5\,\mu H \tag{16}$$

$$L_m = L_n \times L_r = 13.5 \times 59.5\,\mu H = 803\,\mu H \tag{17}$$

After the preliminary parameters are selected, find the closest actual component value that is available, re-check the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation.

The following resonant tank parameters are:

$$C_r = 44\,nF \tag{18}$$

$$L_r = 61.5\ \mu H \tag{19}$$

$$L_m = 830\,\mu H \tag{20}$$

Based on the final resonant tank parameters, the resonant frequency can be calculated:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{44\,nF \times 61.5\,\mu H}} = 96.8\,kHz \tag{21}$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

$$f_{n(Mgmax)} = 0.52 \tag{22}$$

$$f_{n(Mgmin)} = 1.15 \tag{23}$$

The maximum and minimum switching frequencies are:

$$f_{SW(Mgmax)} = 50.3\,kHz \tag{24}$$

$$f_{SW(Mgmin)} = 111.3\,kHz \tag{25}$$

7.2.2.7 LLC Primary-Side Currents

The primary-side currents are calculated for component selection purpose. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is given by:

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 10\,A}{16} = 0.764\,A \tag{26}$$

The RMS magnetizing current at minimum switching frequency is given by:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{nV_{OUT}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{16 \times 12}{2\pi \times 50.3\,kHz \times 830\,\mu H} = 0.659\,A \tag{27}$$

The total current in resonant tank is given by:

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = \sqrt{(0.764\,A)^2 + (0.659\,A)^2} = 1.009\,A \tag{28}$$

7.2.2.8 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{oe}) to the secondary side.

$$I_{oes} = n \times I_{oe} = 16 \times 0.764\,A = 12.218\,A \tag{29}$$

In this design, the transformer's secondary side has a center-tapped configuration. The current of each secondary transformer winding is calculated by:

$$I_{ws} = \frac{\sqrt{2} \times I_{oes}}{2} = \frac{\sqrt{2} \times 12.218\,A}{2} = 8.639\,A \tag{30}$$

The corresponding half-wave average current is:

$$I_{sav} = \frac{\sqrt{2} \times I_{oes}}{2} = \frac{\sqrt{2} \times 12.218\,A}{\pi} = 5.503\,A \tag{31}$$

7.2.2.9 LLC Transformer

A bias winding is needed in order to utilize the HV self start up function. It is recommended to design the bias winding so that the VCC voltage is greater than 13 V.

The transformer can be built or purchased according to these specifications:

- Turns ratio: Primary : Secondary : Bias = 32 : 2 : 3
- Primary terminal voltage: 450Vac
- Primary magnetizing inductance: L_M = 830 µH
- Primary side winding rated current: I_r = 1.009 A
- Secondary terminal voltage: $36V_{ac}$
- Secondary winding rated current: I_{ws} = 8.639 A
- Minimum switching frequency: 50.3 kHz
- Maximum switching frequency: 111.3 kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

7.2.2.10 LLC Resonant Inductor

The AC voltage across the resonant inductor is given by its impedance times the current:

$$V_{L_R} = \omega L_R I_R = 2\pi \times 50.3 \times 10^3 \times 61.5 \times 10^{-6} \times 1.009 = 19.607V \quad (32)$$

The inductor can be built or purchased according to the following specifications:

- Inductance: L_r = 61.5 µH
- Rated current: I_r = 1.009 A
- Terminal AC voltage:
- Frequency range: 50.3 kHz to 111.3 kHz

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

7.2.2.11 LLC Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_r}{\omega C_r} = \frac{1.009}{2\pi \times 50.3 \times 10^3 \times 44 \times 10^{-9}} = 72.5V \quad (33)$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^2} = \sqrt{\left(\frac{410}{2}\right)^2 + 72.5^2} = 217.4V \quad (34)$$

Peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 72.5 = 307.5V \quad (35)$$

Valley voltage:

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 72.5 = 102.5V \quad (36)$$

Rated current:

$$I_r = 1.009A \quad (37)$$

7.2.2.12 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage:

$$V_{QLLC(peak)} = 1.5 \times V_{IN(max)} = 615V \quad (38)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current:

$$I_{QLLC} = 1.1 \times I_r = 1.109A \quad (39)$$

7.2.2.13 Design Considerations for Adaptive Dead-Time

After the resonant tank is designed and the primary side MOSFET is selected, the ZVS operation of the converter needs to be double checked. ZVS can only be achieved when there is enough current left in the resonant inductor at the gate turn off edge to discharge the switch node. UCC256302 implements adaptive dead-time based on the slewing of the switch node. The slew detection circuit has a detection range of 1V/ns to 50 V/ns.

To check the ZVS operation, a series of time domain simulations are conducted, and the resonant current at the gate turn off edges are captured. An example plot is shown below:

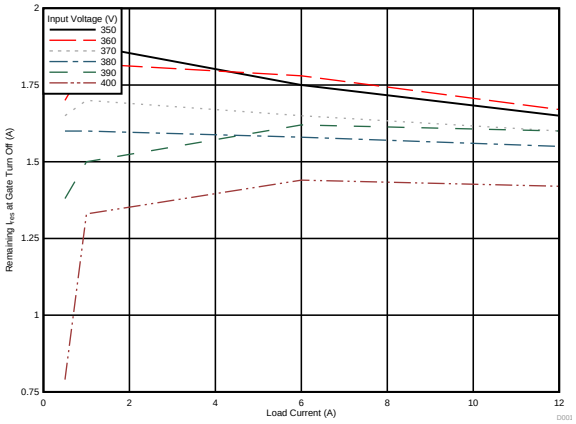


Figure 48. Adaptive Dead-Time

The figure above assumes the maximum switching frequency occurs at 5% load, and system starts to burst at 5% load.

From this plot, the minimum resonant current left in the tank is I_{min} = 0.8 A in the interested operation range. In order to calculate the slew rate, the primary side switch node parasitic capacitance must be known. This value can be estimated from the MOSFET datasheet. In this case, $C_{switchnode}$ = 400 pF. The minimum slew rate is given by:

$$\frac{I_{MIN}}{C_{switchnode}} = \frac{0.8\,A}{400\,pF} = 2V\,/\,ns \tag{40}$$

This is larger than 1 V/ns minimum detectable slew rate.

7.2.2.14 LLC Rectifier Diodes

The voltage rating of the output diodes is given by:

$$V_{DB} = 1.2 \times \frac{V_{IN(max)}}{n} = 1.2 \times \frac{410}{16} = 30.75V \tag{41}$$

The current rating of the output diodes is given by:

$$I_{SAV} = \frac{\sqrt{2} \times I_{oes}}{\pi} = \frac{\sqrt{2} \times 12.218}{\pi} = 5.5\,A \tag{42}$$

7.2.2.15 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second stage filter inductor may be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the rectifier's full wave output current then the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 10 = 11.11A \tag{43}$$

Use 20 V rating for 12-V output voltage:

$$V_{LLCcap} = 20V \tag{44}$$

The capacitor's RMS current rating is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{OUT}\right)^2 - I_{OUT}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 10\right)^2 - 10^2} = 4.84A \tag{45}$$

Solid Aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice here. The ripple-current rating for a single capacitor may not be sufficient so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.3V}{2\frac{\pi}{4} \times 10A} = 19m\Omega \tag{46}$$

The capacitor specifications are:

- Voltage Rating: 20 V
- Ripple Current Rating: 4.84 A
- ESR: < 19 mΩ

7.2.2.16 HV Pin Series Resistors

Multiple resistors are connected in series with the HV pin to limit the power dissipation of the UCC256302 device. The recommended series resistor for the HV pin is 5kΩ.

7.2.2.17 BLK Pin Voltage Divider

BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of UCC256302 have different BLK thresholds.

Choose bulk startup voltage at 340 V, then the BLK resistor divider ratio can be calculated as below:

$$k_{BLK} = \frac{340V}{3V} = 113.33 \tag{47}$$

The desired power consumption of the BLK pin resistor divider is P_{BLKsns} = 10 mW. The BLK sense resistor total value is given by:

$$R_{BLKsns} = \frac{V_{IN(nom)}^2}{P_{BLKsns}} = \frac{390^2}{0.01} = 15.21M\Omega \tag{48}$$

The lower BLK divider resistor value is given by:

$$R_{BLKlower} = \frac{R_{BLKsns}}{k_{BLK}} = \frac{15.21M\Omega}{113.33} = 134k\Omega \tag{49}$$

The higher BLK divider resistor value is given by:

$$R_{BLKupper} = R_{BLKsns} - R_{BLKlower} = 15.08M\Omega \tag{50}$$

The actual bulk voltage thresholds can be calculated:

$$V_{BulkStart} = 340V \tag{51}$$

$$V_{BulkStop} = 340V \times \frac{2.2}{3} = 249V \tag{52}$$

$$V_{BulkOVRise} = 340V \times \frac{4}{3} = 453V \tag{53}$$

$$V_{BulkOVFall} = 340V \times \frac{3.75}{3} = 425V \tag{54}$$

7.2.2.18 BW Pin Voltage Divider

BW pin senses the output voltage through the bias winding and protects the power stage from over voltage. The nominal output voltage is 12 V. The bias winding has 3 turns, and the secondary side winding has 2 turns. So the nominal voltage of the bias winding is given by:

$$V_{BiasWindingNom} = 12V \times \frac{3}{2} = 18V \tag{55}$$

The desired OVP threshold in this design is 115% of the nominal value. The OVP threshold level in UCC256302 device is 4 V, so the nominal BW pin voltage is given by:

$$V_{BWnom} = \frac{4V}{115\%} = 3.48V \tag{56}$$

Choose the lower resistor of the BW resistor divider to be 10 kΩ.

$$R_{BWlower} = 10k\Omega \tag{57}$$

The upper resistor can be calculated by:

$$R_{BWupper} = R_{BWlower} \times \left(\frac{V_{BiasWindingNom} - V_{BWnom}}{V_{BWnom}} \right) = 10k\Omega \times \left(\frac{18 - 3.48}{3.48} \right) = 41.75k\Omega \tag{58}$$

7.2.2.19 ISNS Pin Differentiator

ISNS pin sets the over current protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 0.6 V, 0.8 V, and 4 V, respectively.

Set OCP3 level at 150% of full load. Thus, the sensed average input current level at full load is given by:

$$V_{ISNSfullload} = \frac{0.6V}{150\%} = 0.4V \tag{59}$$

The current sense ratio can then be calculated:

$$k_{ISNS} = \frac{V_{ISNSfullload}}{\left(\frac{P_{OUT}}{\eta} \times \frac{1}{V_{bulknom}}\right)} = \frac{0.4V}{\left(\frac{120W}{0.94} \times \frac{1}{390V}\right)} = 1.222\ \Omega \tag{60}$$

Select a current sense capacitor first, since there are less high voltage capacitor choices than resistors:

$$C_{ISNS} = 150\,pF \tag{61}$$

Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{k_{ISNS}C_r}{C_{ISNS}} = \frac{1.222\ \Omega \times 44n}{150\,p} = 358.45\ \Omega \tag{62}$$

After the current sense ratio is determined, the peak ISNS pin voltage at full load can be calculated:

$$V_{ISNSpeak} = \sqrt{2}I_r \times k_{ISNS} = \sqrt{2} \times 1.009A \times 1.222\ \Omega = 1.74V \tag{63}$$

The peak resonant current at OCP1 level is given by:

$$I_{respeakOCP1} = \frac{4V}{1.222\Omega} = 3.27A \tag{64}$$

The peak secondary-side current at OCP1 level is given by:

$$I_{secpeakOCP1} = I_{respeakOCP1}\frac{N_{pri}}{N_{sec}} = 3.27A \times \frac{32}{2} = 52.37A \tag{65}$$

7.2.2.20 VCR Pin Capacitor Divider

The capacitor divider on the VCR pin sets two parameters: (1) the divider ratio of the resonant capacitor voltage; (2) the amount of frequency compensation to be added. The first criteria the capacitor divider needs to meet is that under over load condition, the peak-to-peak voltage on VCR pin is with in 6 V.

As derived earlier, the following relationship between VCOMP voltage, ΔVCR, switching period, input average current, and the VCR capacitor divider is shown in Equation 66

$$VCOMP = \Delta VCR \approx \frac{C_1}{C_1 + C_2}\frac{1}{C_r} \times I_{IN(avg)} \times T + I_{COMP} \times \frac{1}{C_1 + C_2} \times \frac{T}{2} \tag{66}$$

In this equation, C_1 is the upper capacitor on the capacitor divider; C_2 is the lower capacitor on the capacitor divider. VCOMP is contributed by two parts – the divided resonant capacitor voltage, and the voltage generated by the VCR pin internal current sources. Define the contribution of the internal current source to be $K_{VCRRamp}$.

$$k_{VCRRamp} = \frac{I_{COMP} \times \frac{1}{C_1 + C_2} \times \frac{T}{2}}{\frac{C_1}{C_1 + C_2}\frac{1}{C_r} \times I_{IN(avg)} \times T + I_{COMP} \times \frac{1}{C_1 + C_2} \times \frac{T}{2}} = \frac{1}{\frac{C_1}{C_r}\frac{I_{IN(avg)}}{I_{COMP}} \times 2 + 1} \tag{67}$$

Select C_1 and C_2 so that $K_{VCRRamp}$ is within 0.1 ~ 0.6 range, and at over load condition, VCOMP is less than 6 V. In this example C_1 = 150 pF and C_2 = 15 nF is select.

7.2.2.21 Burst Mode Programming

The burst mode programming interface enables user to program a burst mode threshold voltage (VLL) which adaptively changes with input voltage. This way, consistent burst threshold can be achieved across V_{IN} range, thus making the efficiency curve more consistent across V_{IN} range.

The following relationship exists between VLL voltage and BLK pin voltage:

$$VLL = a \times VBLK + b \tag{68}$$

In this equation, VLL is the burst mode threshold voltage; VBLK is BLK pin voltage; two parameters a and b can be programmed by two external resistors.

After soft start is done, the sensed BLK pin voltage is applied to LL/SS pin from inside the IC through a buffer. As shown in the figure below, this creates a difference between the current flowing through the programming resistor $R_{LLUpper}$ and $R_{LLLower}$. The difference between the current flows into the LL/SS pin, mirrored and then applied to a 250-kΩ resistor R_{LL}. The voltage on R_{LL} is used as VLL.

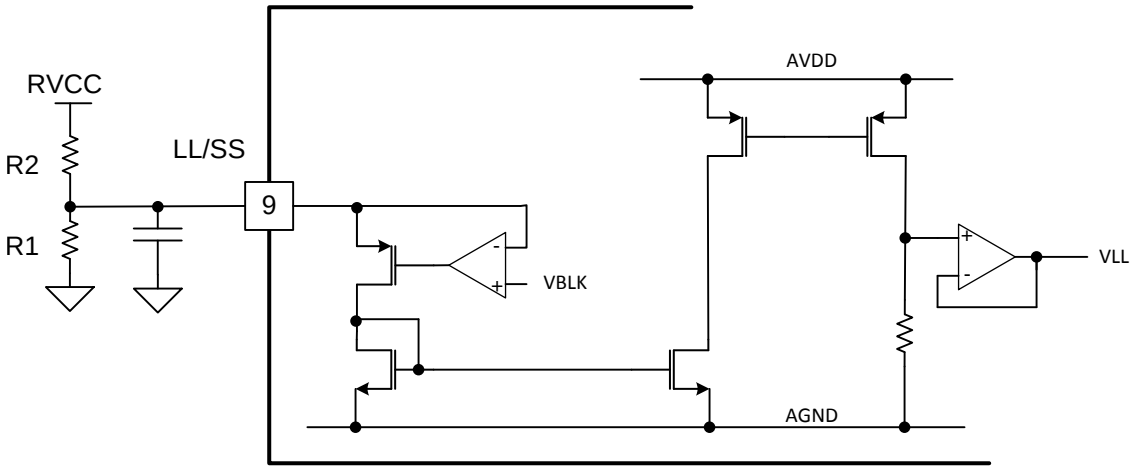


Figure 49. Burst Mode Programming

The relationship between VLL and VBLK can then be derived:

$$\frac{VRVCC - VBLK}{R_{LLUpper}} - \frac{VBLK}{R_{LLLower}} = \frac{VLL}{R_{LL}} \tag{69}$$

Equation 69 rearranged produces Equation 70

$$VLL = -\frac{\left(R_{LLUpper} + R_{LLLower}\right) \times R_{LL}}{R_{LLUpper} R_{LLLower}} \times VBLK + \frac{R_{LL}}{R_{LLUpper}} VRVCC \tag{70}$$

To determine $R_{LLUpper}$ and $R_{LLLower}$, two sets of (VLL, VBLK) values are required. VBLK can be measured directly from BLK pin. VLL level can be measured by inserting a 10-kΩ resistor between the feedback optocoupler emitter and ground. Assume the voltage measured on the 10-kΩ resistor is V_{10k}. Then VLL voltage can be calculated as:

$$VLL = \left(I_{FB} - \frac{V_{10k\Omega}}{10k\Omega}\right) \times 100k\Omega \tag{71}$$

Remove the $R_{LLUpper}$. In this way, the VLL voltage is at its minimal value 0.7 V, which is determined by the internal circuit design. Then adjust the load current to the desired burst mode threshold load level, and make sure the power stage does not burst in this condition. For example, 10% load is the desired burst mode threshold level. With 10 A as the full-load condition, set the load current to 1 A. After the load current is set, change the input voltage to two different voltages and record two different readings (V10k, VBLK). Then based on Equation 70 and Equation 71, $R_{LLUpper}$ and $R_{LLLower}$ can be solved.

In this example select the lower resistor to be 402 kΩ and the upper resistor to be 732 kΩ.

7.2.2.22 Soft-Start Capacitor

The soft-start capacitor sets the speed of the soft-start ramp. The soft start time varies with load condition. At full load or over load condition, the soft start time is the longest. It is not easy to calculate the exact soft start time value. However, it can be estimated that under full load condition, the longest possible soft start time is given by:

$$T_{SS} = \frac{7V \times C_{SS}}{25\,\mu A} \quad (72)$$

Using a 150-nF soft-start capacitor, gives the longest possible soft-start time as 42 ms according to Equation 72.

7.2.3 Application Curves

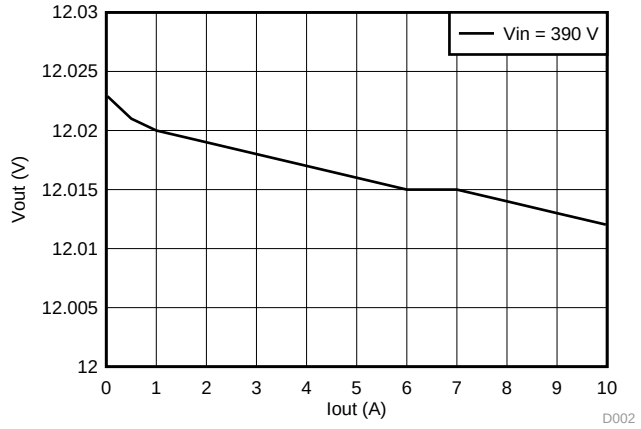


Figure 50.

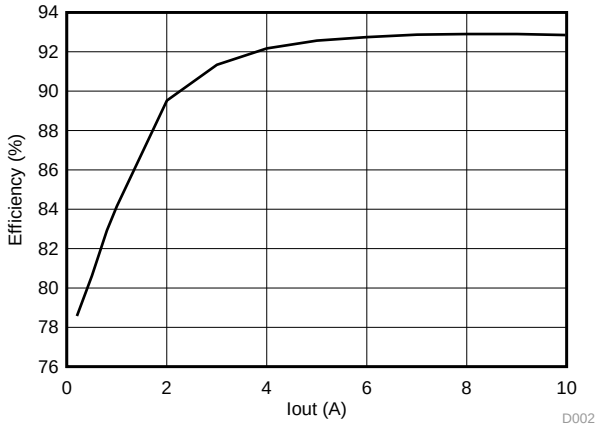


Figure 51.

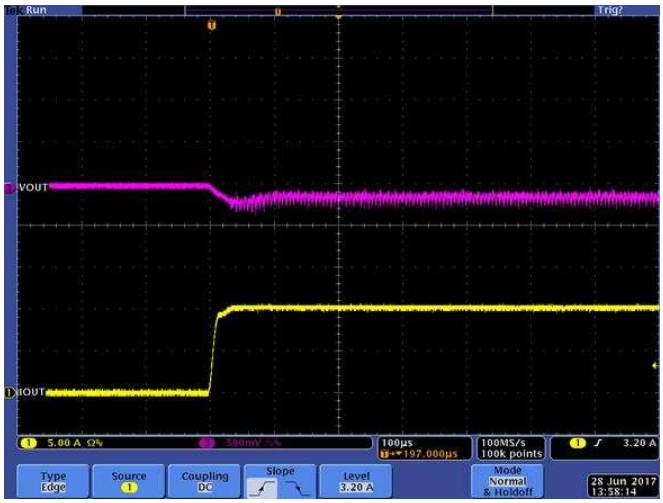


Figure 52.

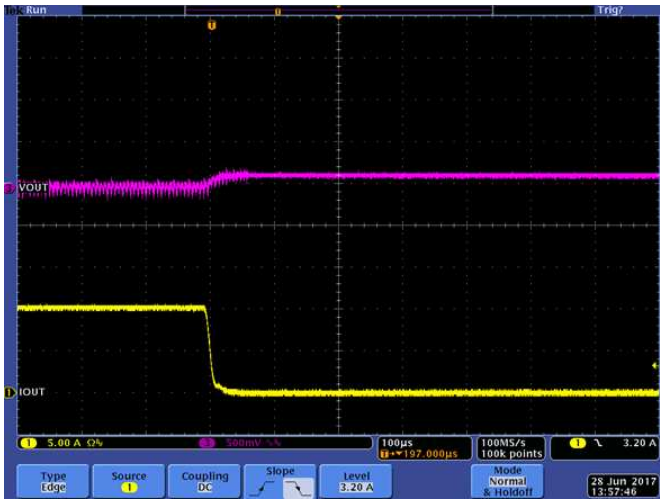
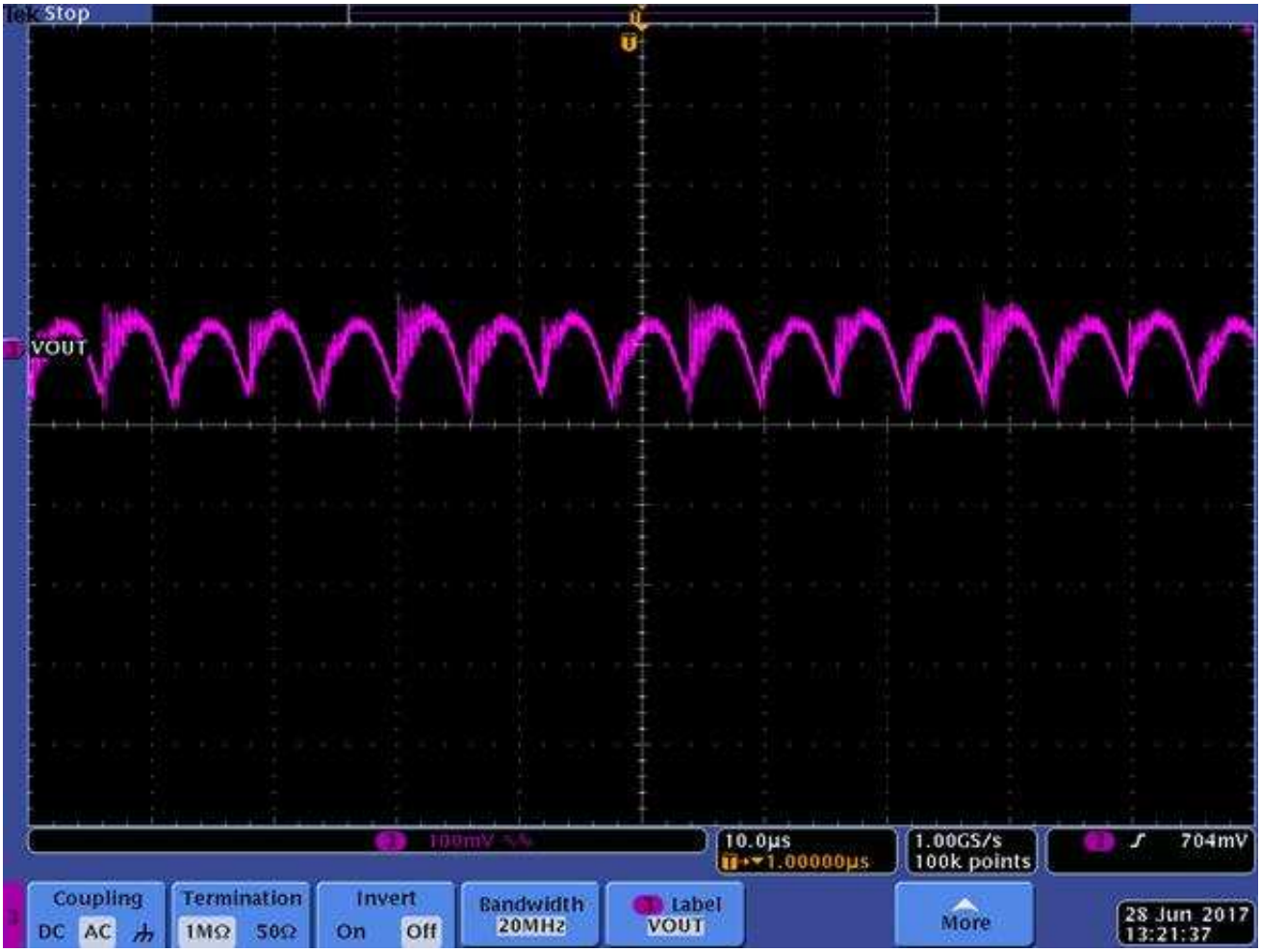


Figure 53.



Output Ripple

Figure 54.

8 Power Supply Recommendations

8.1 VCC Pin Capacitor

The VCC capacitor should be sized based on the total start-up charge required by the system. The start-up charge will mostly be consumed by the gate driver circuit. Thus the total start-up charge can be estimated by the start-up switching frequency, MOSFET gate charge, and the soft-start time.

Assume the total start-up charge required by the system is shown in Equation 73

$$Q_{tot} = 1.6 mC \tag{73}$$

During PFC and LLC startup phase, the maximum VCC voltage drop allowed is

$$V_{ccdropmax} = 26V - 10.5V = 15.5V \tag{74}$$

The minimum VCC capacitor needed:

$$C_{VCC} = \frac{Q_{tot}}{V_{ccdropmax}} = 103 \mu F \tag{75}$$

Choose 110-µF capacitor.

8.2 Boot Capacitor

During burst off period, power consumed by the high side gate driver from the HB pin must be drawn from C_{BOOT} and will cause its voltage to decay. At the start of the next burst period there must be sufficient voltage remaining on C_{BOOT} to power the high side gate driver until the conduction period of LO allows it to be replenished from C_{RVCC}. The power consumed by the high side driver during this burst off period will therefore have a direct impact on the size and cost of capacitors that must be connected to C_{BOOT} and RVCC.

Assume the system has a maximum burst off period of 10 ms.

$$t_{maxoff} = 10 ms \tag{76}$$

Assume the bootstrap diode has a forward voltage drop of 1 V:

$$V_{bootforwarddrop} = 1V \tag{77}$$

Assume the boot voltage to be always above 8 V to avoid UVLO fault. Then the maximum allowed voltage drop on boot capacitor is:

$$V_{bootmaxdrop} = V_{RVCC} - V_{bootforwarddrop} - 8V = 12V - 1V - 8V = 3V \tag{78}$$

Boot capacitor can then be sized:

$$C_{boot} = \frac{I_{bootleak} t_{maxoff}}{V_{bootmaxdrop}} = \frac{85 \mu A \times 10 ms}{3V} = 284 nF \tag{79}$$

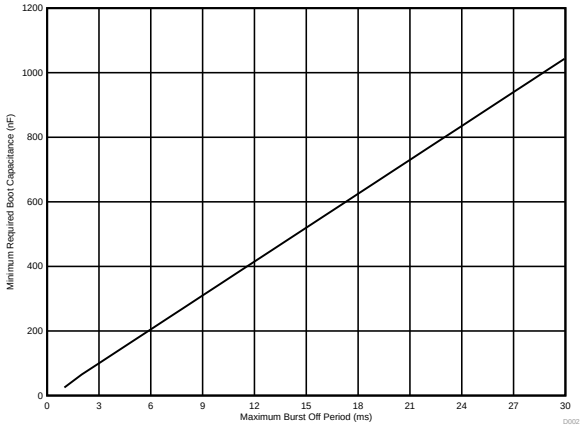


Figure 55. Minimum Required Boot Capacitance vs. Maximum Burst Off Period

8.3 RVCC Pin Capacitor

RVCC capacitor needs to be at least 5 times of boot capacitor. In addition, sizing of the RVCC capacitor depends on the stability of RVCC LDO. If load is light on RVCC, smaller capacitors can be used. The larger the load, the larger the capacitor is needed. In a typical system, the RVCC LDO powers the PFC and LLC gate drivers. The plot below shows the worst case RVCC LDO phase margin versus RVCC capacitor for various load currents. RVCC capacitor should be sized based on the figure below.

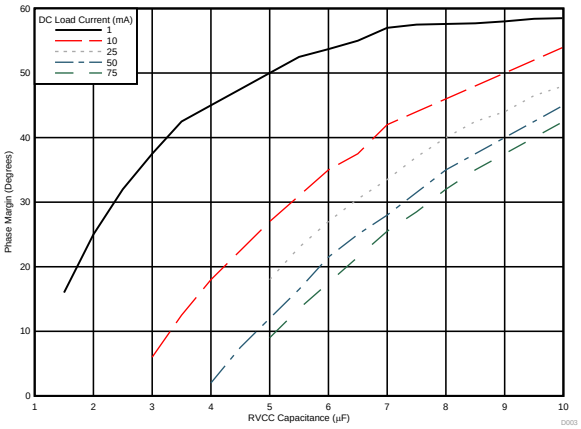


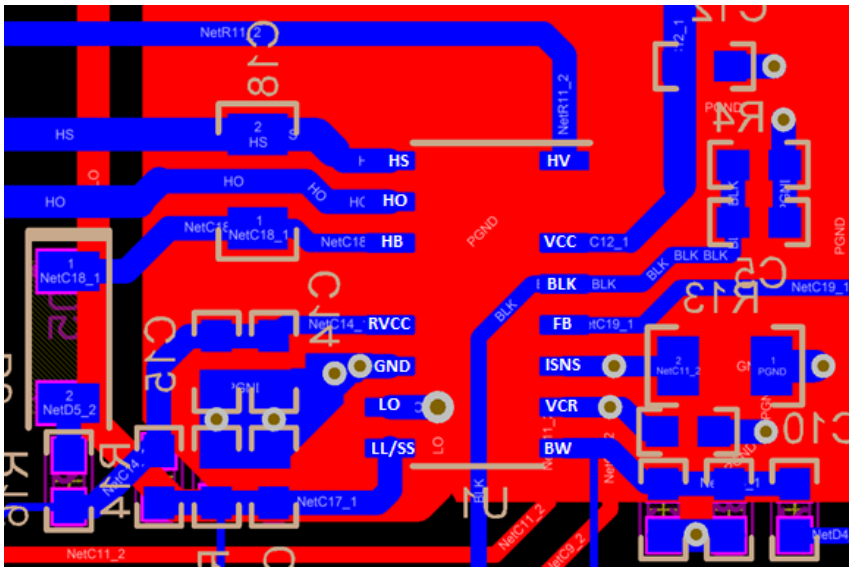
Figure 56. RVCC Pin Capacitor

9 Layout

9.1 Layout Guidelines

- Put a 2.2-µF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. The 2.2-µF ceramic capacitor should be put as close as possible to the VCC pin.
- RVCC pin should have a bypass capacitor of 4.7 µF or more. It is recommended to add a 0.1-µF ceramic capacitor in addition to the 4.7 µF. The capacitors should be put as close as possible to the RVCC pin. RVCC cap needs to be at least 5 times of boot capacitor.
- Minimum recommended boot capacitor is 0.1 µF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor should be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table.
- Use large copper pour around GND pin
- The filtering capacitor on BW, ISNS, BLK should be put as close as possible to the pin
- FB trace should be as short as possible
- Soft-start capacitor should be put as close as possible to LL/SS pin
- Use film capacitor or C0G, NP0 ceramic capacitor on VCR divider and ISNS capacitor for low distortion
- It is recommended that ISNS resistor is less than 500 Ω to keep the node impedance low
- Add necessary filtering capacitors on BW pin to filter out the high spikes on the bias winding waveform. It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low side turn off edge.
- Do not put any capacitor on HV pin to ground. The layout of this pin should result in low parasitic capacitance (<60 pF) from HV pin to ground.
- Keep necessary high voltage clearance

9.2 Layout Example



10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC256302 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Design Spreadsheet, *UCC25630 Design Calculator*, UCC634
- User Guide, *Using UCC25630-1EVM-291*,

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks

E2E is a trademark of Texas Instruments.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC25630-2DDBR	ACTIVE	SOIC	DDB	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256302	Samples
UCC25630-2DDBT	ACTIVE	SOIC	DDB	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

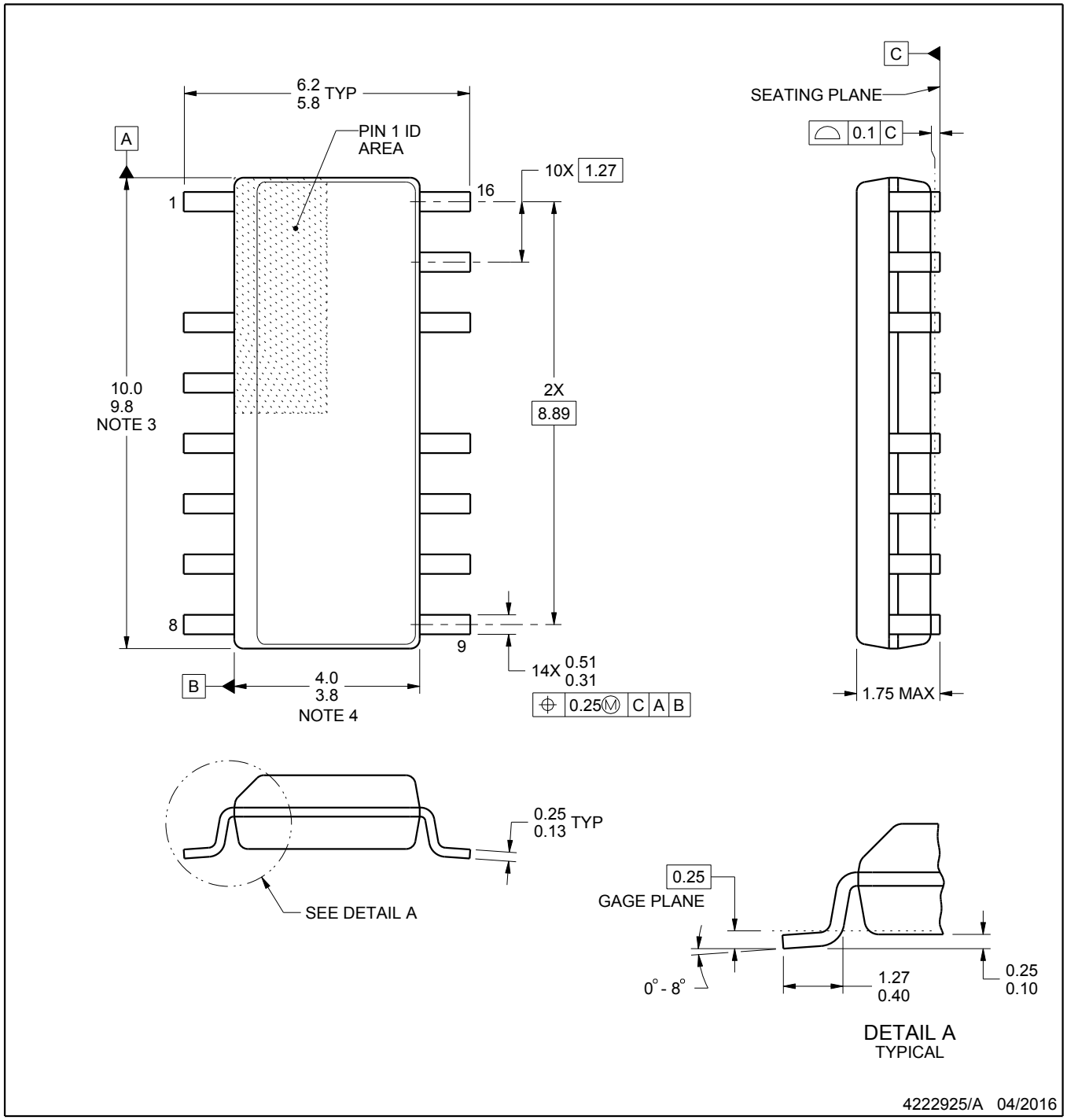
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDB0014A

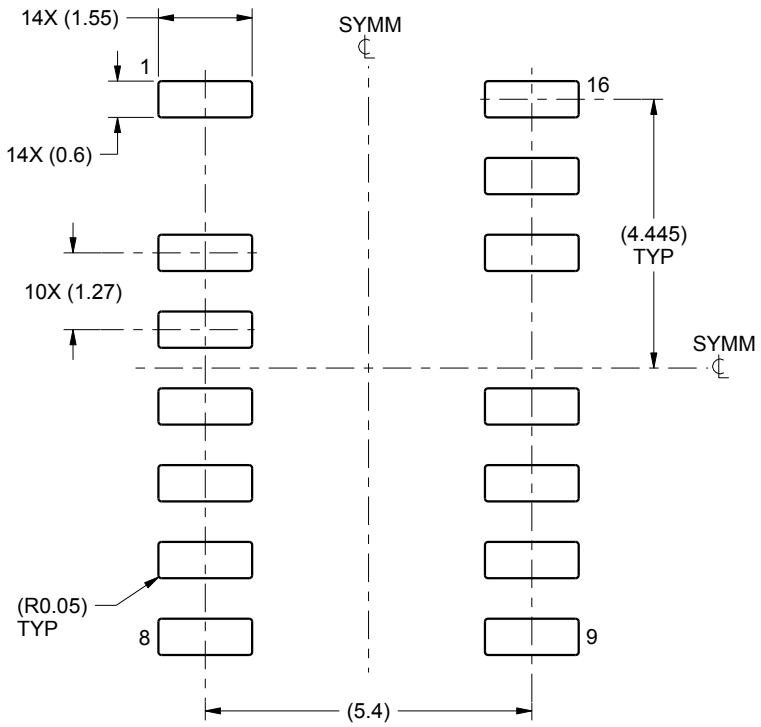
SOIC - 1.75 mm max height

SOIC

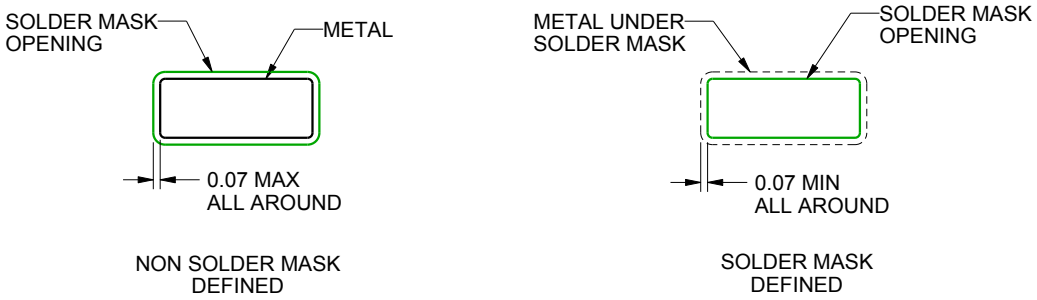


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.



LAND PATTERN EXAMPLE
SCALE:8X

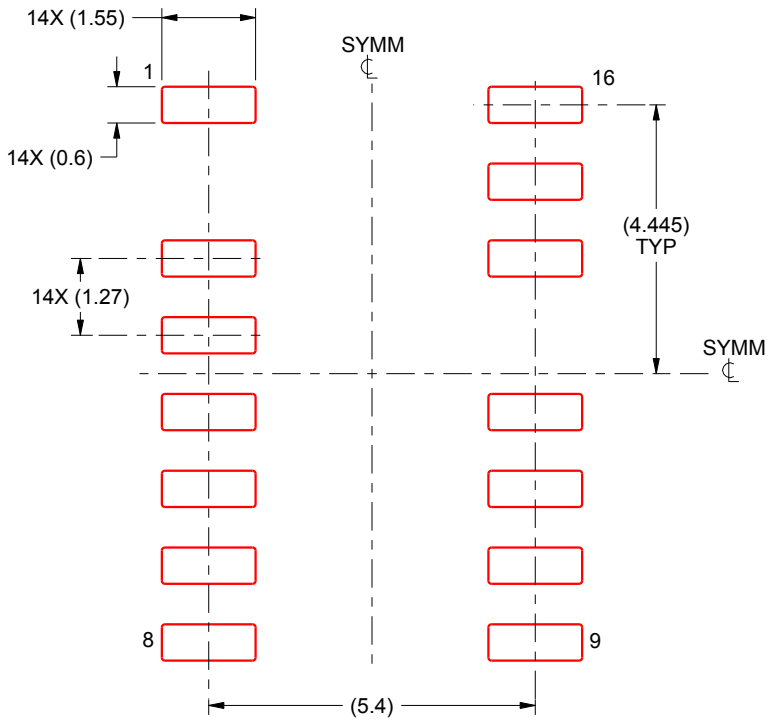


SOLDER MASK DETAILS

4222925/A 04/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222925/A 04/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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