TVS3300 33-V Precision Surge Protection Clamp

1 Features

- Ultra-Low and Flat Clamping Voltage
  - 38 V at 35 A (8/20 µs)
  - R_{DYN}: 40 mΩ
- Standoff Voltage: 33 V
- Low Leakage Current
  - 19 nA at 27°C
  - 28 nA at 85°C
- Peak Pulse Power:
  - 1330-W (8/20 µs)
  - 150-W (10/1000 µs)
- IEC 61000-4-2 Level 4 ESD Protection
  - ±14-kV Contact Discharge
  - ±30-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 35 A (8/20 µs)
- Industrial Temperature Range: –40°C to +125°C
- Compact Packages
  - 4-pin WCSP Package (1.062 mm × 1.116 mm)
  - 6-pin SON Package (2 mm × 2 mm)

2 Applications

- Factory Automation Sensors
- 4-20-mA Current Loop
- 24-V Power and Signal Rails
- PLCs IO Modules
- 24-V Switch Output Sensors
- Sensor Transmitter
- Field Actuator
- IO Link
- Machine Vision and Bar Code Reader Systems

3 Description

The TVS3300 is a transient voltage suppressor which provides robust protection for electronic circuits exposed to high transient voltage events. Unlike a traditional TVS diode, the TVS3300 precision clamp triggers at a lower breakdown voltage and regulates to maintain a flat clamping voltage throughout a transient overvoltage event. The lower clamping voltage combined with a low dynamic resistance enables a unique TVS protection solution that can lower the voltage a system is exposed during a surge event by up to 30% in unidirectional configuration and up to 20% in bidirectional configuration when compared to traditional TVS diodes. The low clamping voltage and flat clamping performance allow designers to confidently select downstream system components with maximum voltage rating than is possible with traditional TVS diodes, saving system cost, board area and improving overall performance.

The TVS3300 is a unidirectional precision surge protection clamp with a 33-V working voltage designed specifically to protect systems with mid-voltage rails in industrial, communication, and factory automation applications. The TVS3300 has a fast response time when surge current is applied so there is no overshoot voltage during clamping, making it ideal to replace traditional TVS and zener diodes.

The TVS3300 is available in two small footprint packages which, when used in place of an industry standard SMB package, can reduce footprint by 94% (WCSP package) and 79% (QFN) for space constrained applications. Both package options robustly dissipate the surge power and provide up to 58% lower leakage current compared to traditional TVS diodes in SMA and SMB package, allowing for higher accuracy 4-20-mA current loop measurements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TVS3300	WCSP(4)	1.062 mm × 1.116 mm
	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

System Diagram

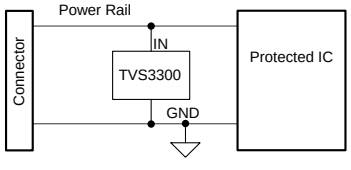

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Table of Contents

4 Revision History

DATE	REVISION	NOTES
February 2017	*	Initial release.

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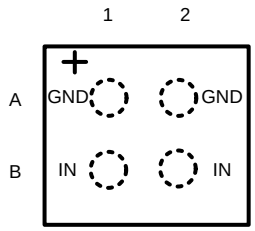
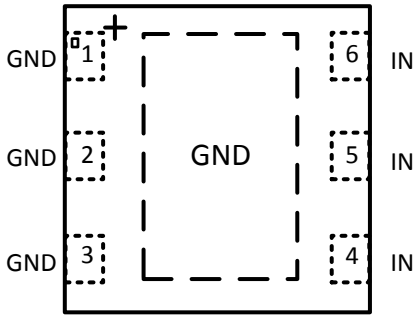
5 Pin Configuration and Functions

YZF Package
4-Pin WCSP
Top View



DRV Package
6-Pin SON
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	YZF	DRV		
IN	B1, B2	4, 5, 6	I	ESD and surge protected channel
GND	A1, A2	1, 2, 3, exposed thermal pad	GND	Ground

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse—clamping direction	IEC 61000-4-5 current (8/20 µs)		35	A
	IEC 61000-4-5 power (8/20 µs)		1330	W
	IEC 61000-4-5 current (10/1000 µs)		4	A
	IEC 61000-4-5 power (10/1000 µs)		150	W
Peak pulse—forward direction	IEC 61000-4-5 current (8/20 µs)		50	A
	IEC 61000-4-5 power (8/20 µs)		80	W
	IEC 616434-321 current (10/1000 µs)		4	A
	IEC 616434-321 power (10/1000 µs)		10	W
I_F	Forward biased DC current		0.5	A
IN	DC voltage between IN and GND, across T_A range	–0.3	33.3	V
T_{stg}	DMD storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2	kV
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±0.5	

(1) HBM was done per ANSI/ESDA/JEDEC JS-001 standard
(2) CDM was done per ANSI/ESDA/JEDEC JS-002 standard

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±14	kV
		IEC 61000-4-2 air-gap discharge	±30	
		IEC 61000-4-4 EFT protection (5/50 ns)	80	A

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	IN pin voltage	0	33	V
T_A	Ambient operating temperature	–40	125	°C
I_F	Forward biased DC current, $T_j \leq 125$°C		0.5	A

6.5 Thermal Information

THERMAL METRIC(1)		TVS3300		UNIT
		YZF (WCSP)	DRV (SON)	
		4-PINS	6-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.8	70.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	73.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.1	40	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.5	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.1	40.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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Thermal Information (continued)

THERMAL METRIC(1)		TVS3300		UNIT
		YZF (WCSP)	DRV (SON)	
		4-PINS	6-PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	11	°C/W

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage	Measured I_N = 1 µA			33	V
I_{LEAK}	Leakage current	Measured at V_{IN} = 33 V T_A = 27℃		19	150	nA
		Measured at V_{IN} = 33 V T_A = 85℃		28	600	nA
V_F	Forward voltage	I_{IN} = –0.5 A	0.5	0.7	1	V
V_{BR}	Breakdown voltage	I_{IN} = 1 mA	34	35.8	39	
V_{FCLAMP}	Forward voltage	I_{PP} = –35 A, IEC 61000-4-5 surge (8/20 µs)	1	2	5	
V_{CLAMP}	Clamp voltage	I_{PP} = 15 A, IEC 61000-4-5 surge (8/20 µs), V_{IN} = 0 V before surge	34	37	40	V
		I_{PP} = 35 A, IEC 61000-4-5 surge (8/20 µs), V_{IN} = 0 V before surge	34	38	40	V
R_{DYN}	8/20-µs surge dynamic resistance	Calculated from V_{CLAMP} at 15 A and 30-A surge current levels		40	60	mΩ
C_{IN}	Input pin capacitance	V_{IN} = 12 V, f = 1 MHz, 30 mVpp, IO to GND	110	130	150	pF

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6.7 Typical Characteristics

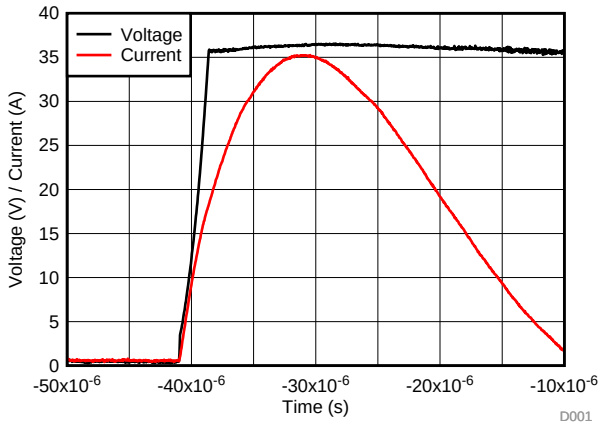


Figure 1. Surge Response at 35 A

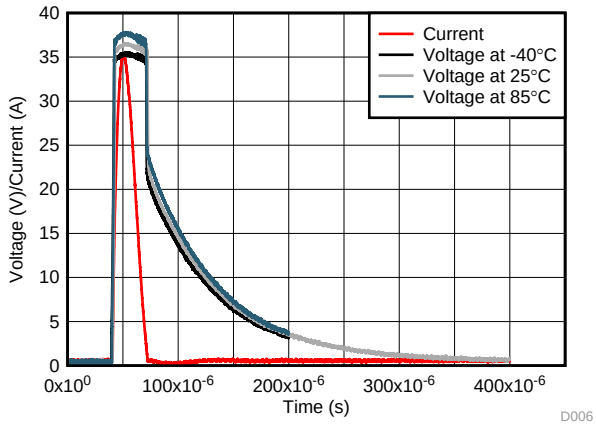
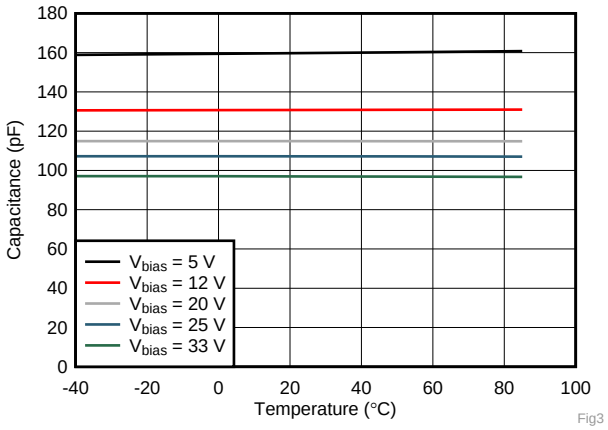


Figure 2. Surge Response at 35 A across Temperature



f = 1 MHz, 30 mVpp, IO to GND

Figure 3. Capacitance vs Temperature Across Bias

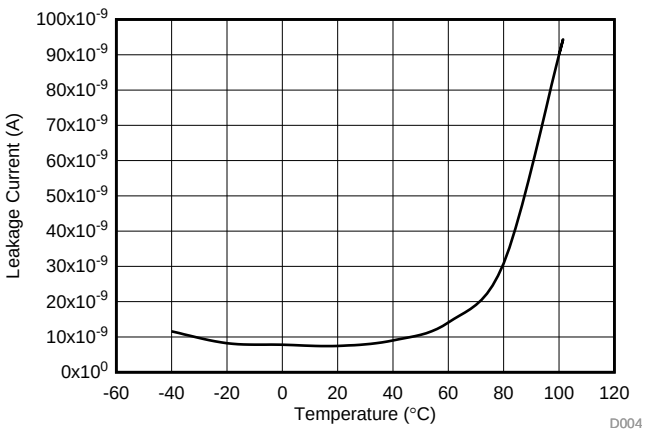


Figure 4. Leakage Current vs Temperature at 33 V

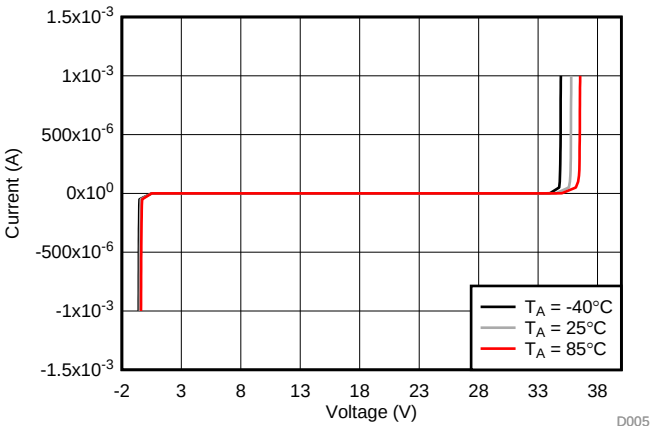


Figure 5. IV Across Temperature

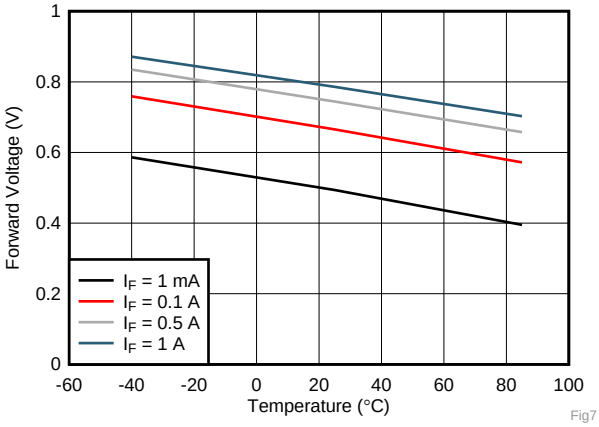


Figure 6. Forward Voltage vs Temperature Across Current

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Typical Characteristics (continued)

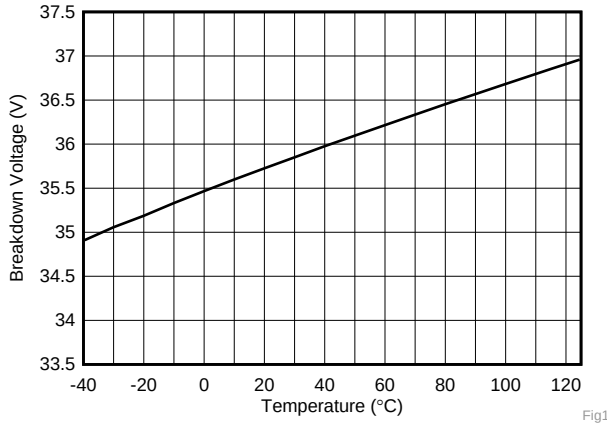


Figure 7. Breakdown Voltage at 1 mA vs Temperature

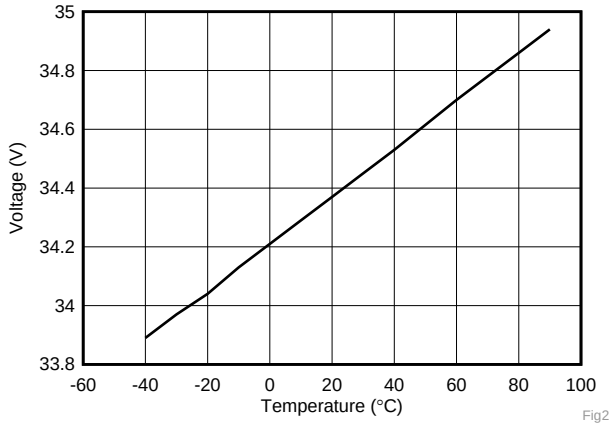


Figure 8. Voltage at 1 µA

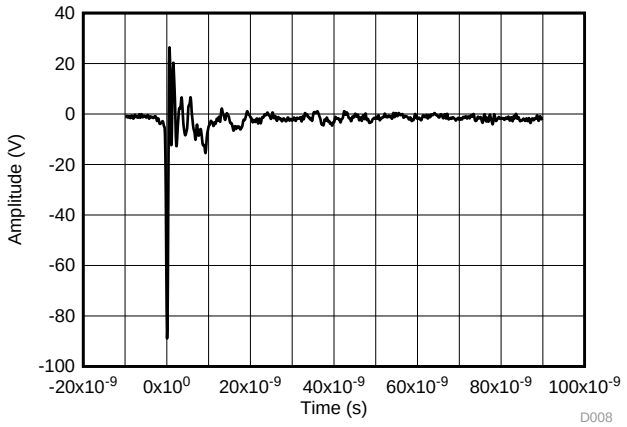


Figure 9. –8-kV IEC Response

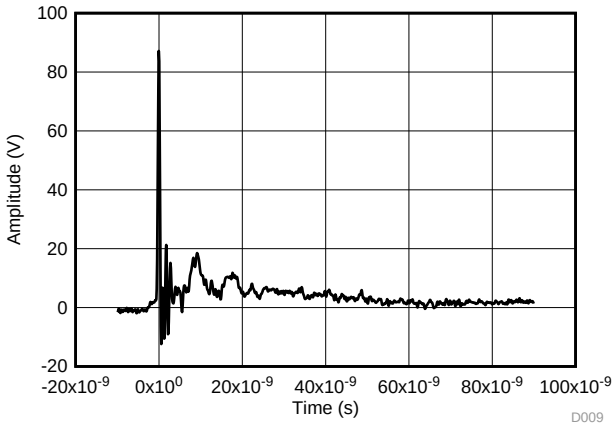


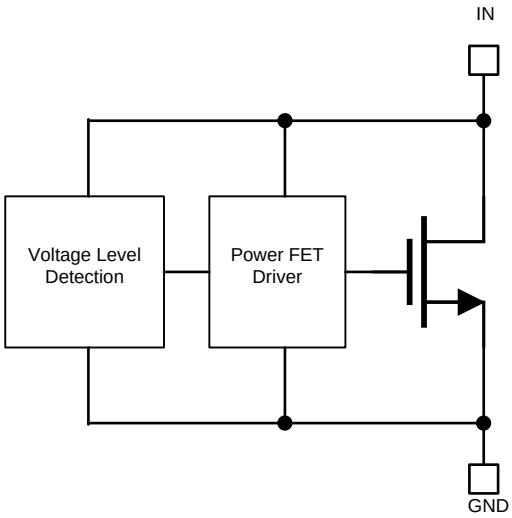
Figure 10. 8-kV IEC Response

7 Detailed Description

7.1 Overview

The TVS3300 is a precision clamp that keeps ultra-low and flat clamping voltage during transient overvoltage events like surge. The TVS3300 also responds fast to the surge so there is no overshoot voltage during clamping.

7.2 Functional Block Diagram



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7.3 Feature Description

The TVS3300 is a precision clamp that handles 35 A of 8/20-µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost lower voltage tolerant downstream ICs. The TVS3300 has minimal leakage under the standoff voltage of 33 V, making it an ideal candidate, but not limited to for majority of factory and process automation applications. IEC61000-4-2 and IEC61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of –40°C to +125°C makes it a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

7.4 Device Functional Modes

The TVS3300 is a passive device that does not trigger below V_{BR}. During transient overvoltage events, pulses can be clamped and current is directed to ground. When the voltages on the protected line fall below the breakdown voltage the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TVS3300 is a precision clamp that keeps ultra-low and flat clamping voltage during transient overvoltage events like surge. The TVS3300 also responds fast to surge so there is no overshoot voltage during clamping. The TVS3300 can be used in unidirectional configuration and bi directional configuration. Figure 11 shows typical application usage.

Figure 12 illustrates usage in a 4-20-mA system. Two TVS3300's (D1 and D2) can be combined to protect the 4-20-mA sensor transmitter in a back-to-back configuration by limiting the voltage difference between the two wires connected to the transmitter. In miswiring and negative surge situations, Schottky diode D0 keeps the current from flowing reversely from the transmitter.

Figure 13 shows the three TVS3300's application. Three TVS3300's protect the switch output sensor transmitter from surge and miswiring conditions. D1 is put in parallel with the Schottky diode D0. When working in the normal condition, D0 is forward biased and passing the working current while only creating low voltage drop to help meet the total voltage drop budget from the wiring. D0 and D1 block the reverse current when the system is miswired. D1 takes most of the current during positive and negative surge. D2 protects the sensor transmitter by clamping the voltage between power supply and the digital output during surge. D3 protects the sensor transmitter by clamping the voltage between power supply and the ground return during surge.

8.2 Typical Application

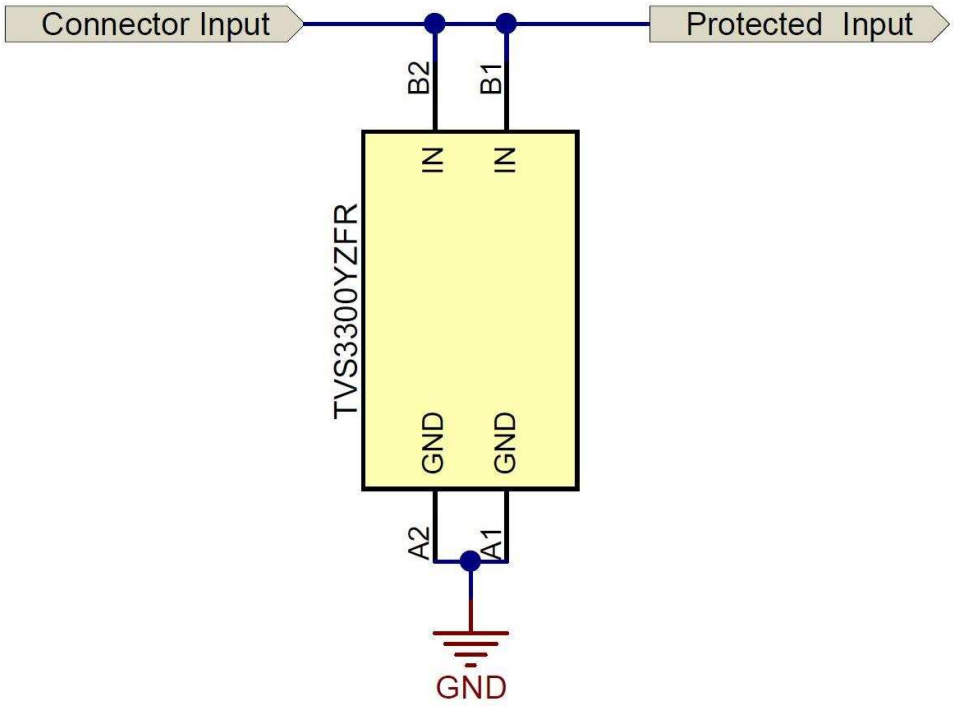

Figure 11. TVS3300 Application Schematic

Typical Application (continued)

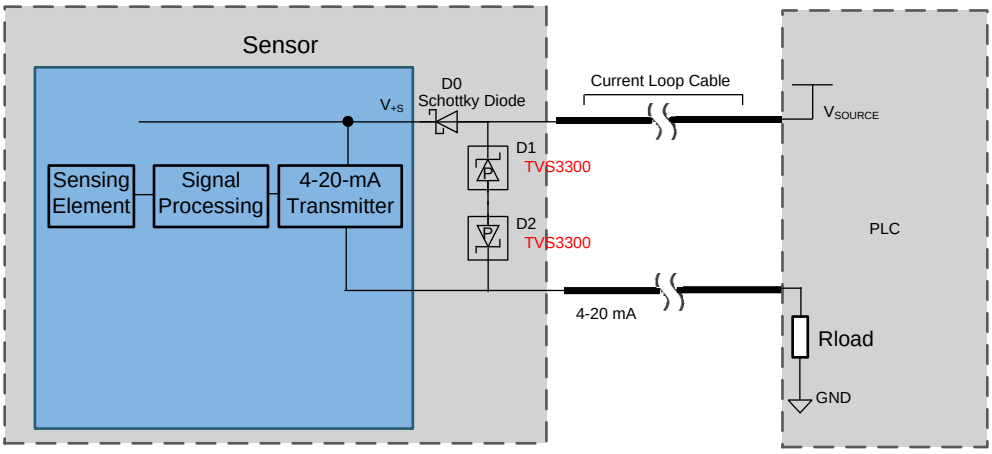

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Figure 12. Two TVS3300's Application

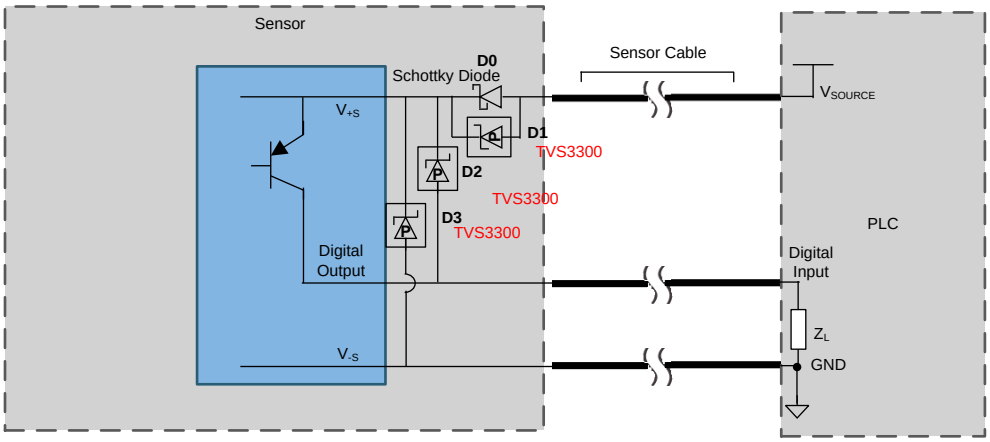

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Figure 13. Three TVS3300's Application

8.2.1 Design Requirements

The TVS3300 has two types of leakage:

Static leakage:

Static leakage from the device starts to increase as the working voltage is beyond breakdown voltage. Static leakage increases to few µA if the operating temperature is above 105°C.

Dynamic leakage:

The TVS3300 can have dynamic leakage during fast transition of the input signal. It is recommended to use the TVS3300 for signal lines <4 kHz. The TVS3300 can slow down the behavior of the clamped signal.

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TVS3300 works in applications with working voltage 33 V, higher voltages are going to cause the the device to leak.

Typical Application (continued)

8.2.2.2 Signal Frequency

The TVS3300 is recommended for signal lines <4 kHz to avoid dynamic leakage. Capacitance offered by the TVS3300 to the signal line being clamped is 130 pF. Care must be taken to ensure that the line has good connection and width to handle the surge current and short path to ground in the board. It is recommended to use all the pins to provide good signal and gnd connection for the TVS3300.

8.2.2.3 Surge Test Setup

Positive and negative surges are imposed to the TVS3300 by combinational waveform generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. In some proprietary test standards, the same level of surge pulses can be imposed repetitively on the DUT at a certain time interval.

The TVS3300 is post tested by characterizing the breakdown curve. For power on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply.

8.2.3 Application Curves

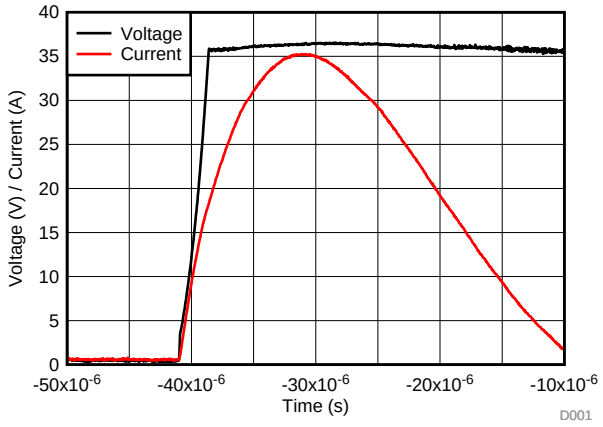

Figure 14. Uni-Directional Configuration 8/20-µs Surge Response

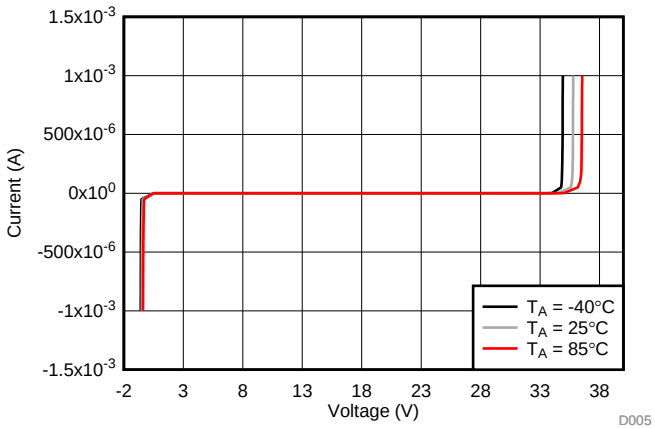

Figure 15. IV Across Temperature

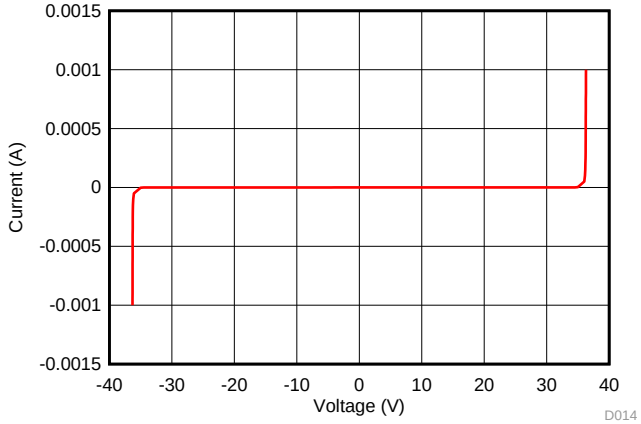

Figure 16. TVS3300 Bi-Directional IV Curve

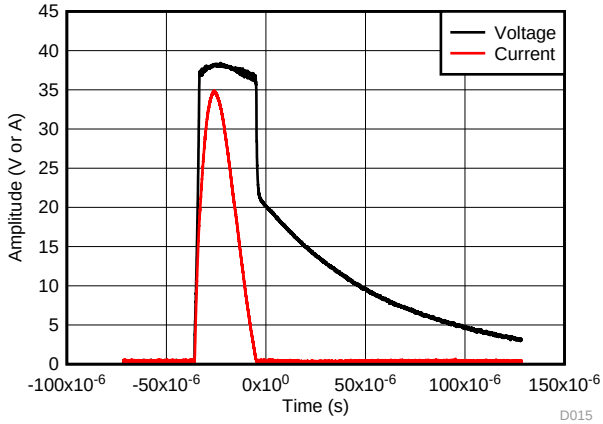

Figure 17. Bi-Directional Configuration 8/20-µs Surge Response

9 Power Supply Recommendations

The TVS3300 is a clamping device so there is no need to power it. Take care not to violate the recommended V_{IN} voltage range (0 V to 33 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

The optimum placement is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Eliminate any sharp corners on the protected traces between the TVS3300 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

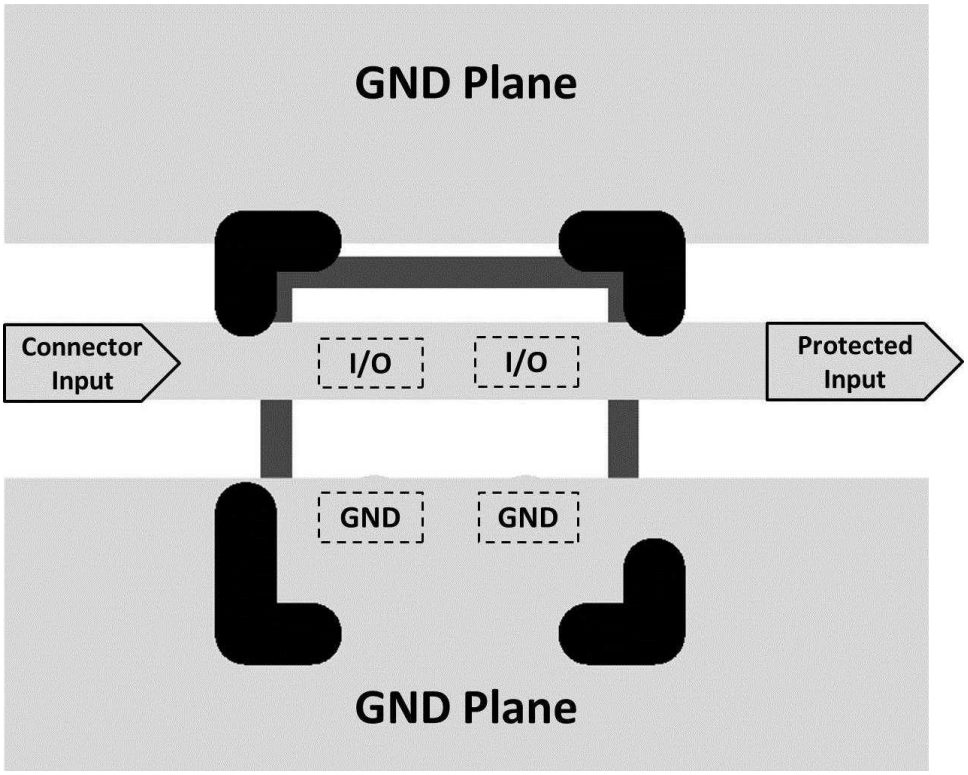

Figure 18. TVS3300 Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *TVS3300 Evaluation Module—Unidirectional Adaptor Board*
- *TVS3300 Evaluation Module—Bidirectional Adaptor Board*
- *TVS3300 Evaluation Module User's Guide*
- *TVS3300DRV Evaluation Module User's Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS3300DRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17JH	
TVS3300YZFR	ACTIVE	DSBGA	YZF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15K	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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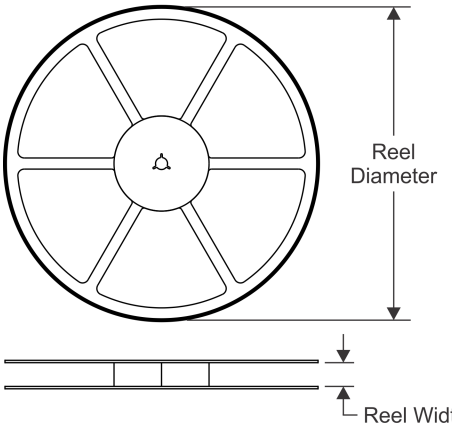
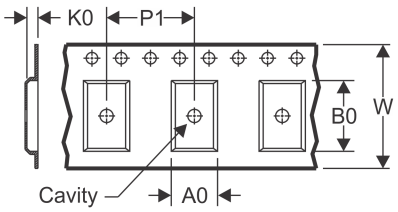
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

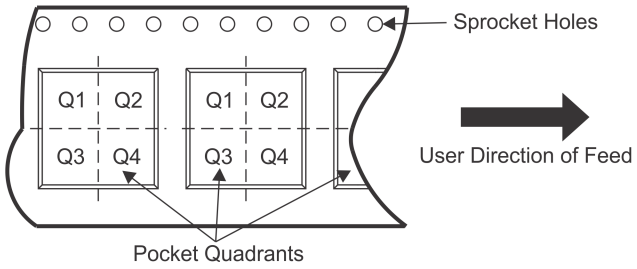


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

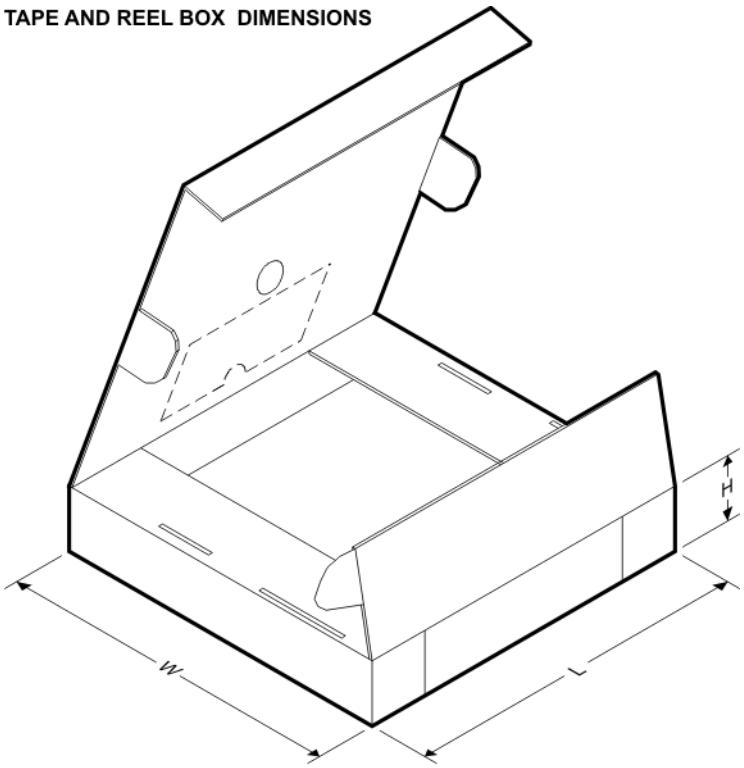
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS3300YZFR	DSBGA	YZF	4	3000	180.0	8.4	1.17	1.22	0.72	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

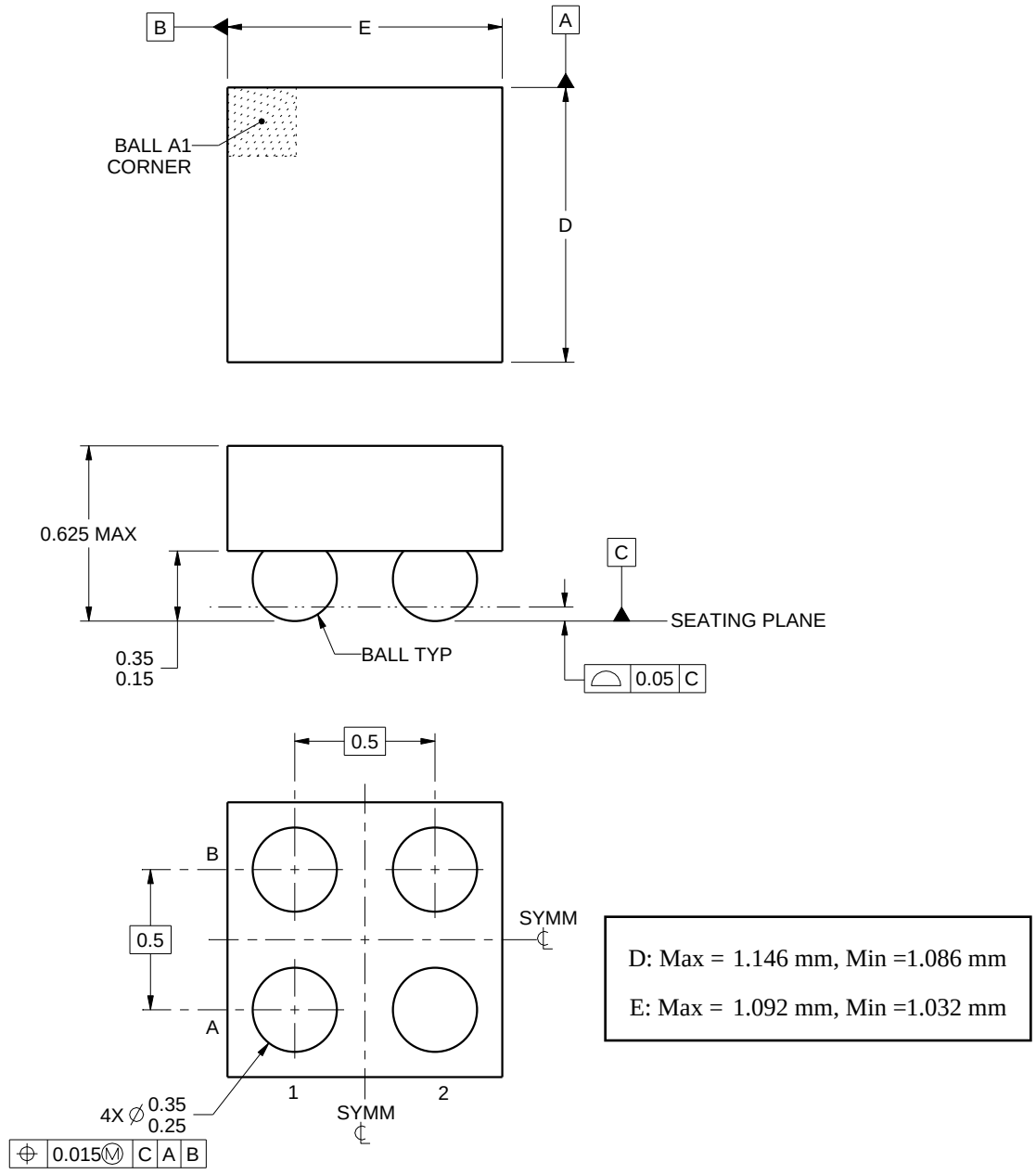
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS3300YZFR	DSBGA	YZF	4	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YZF0004

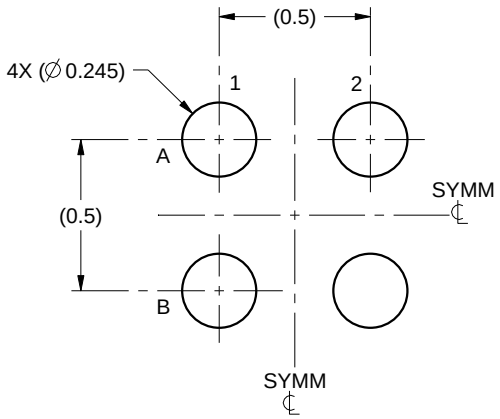
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

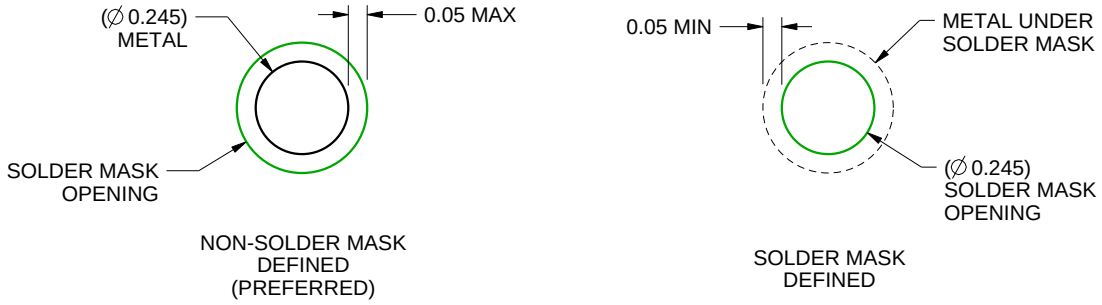


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223221/A 08/2016

NOTES: (continued)

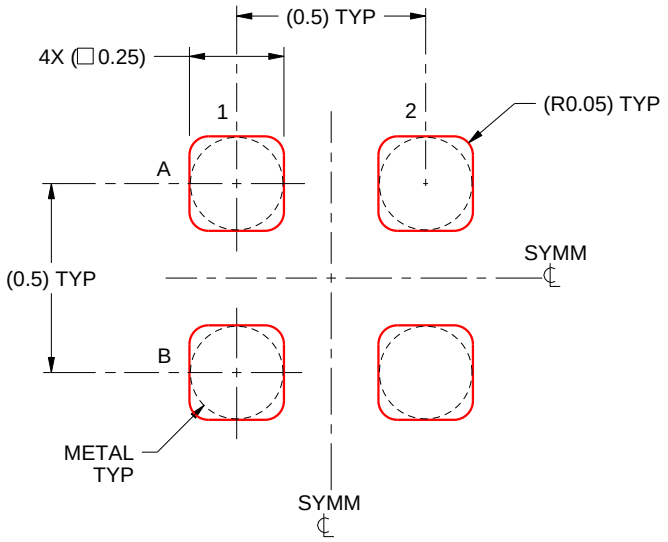
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



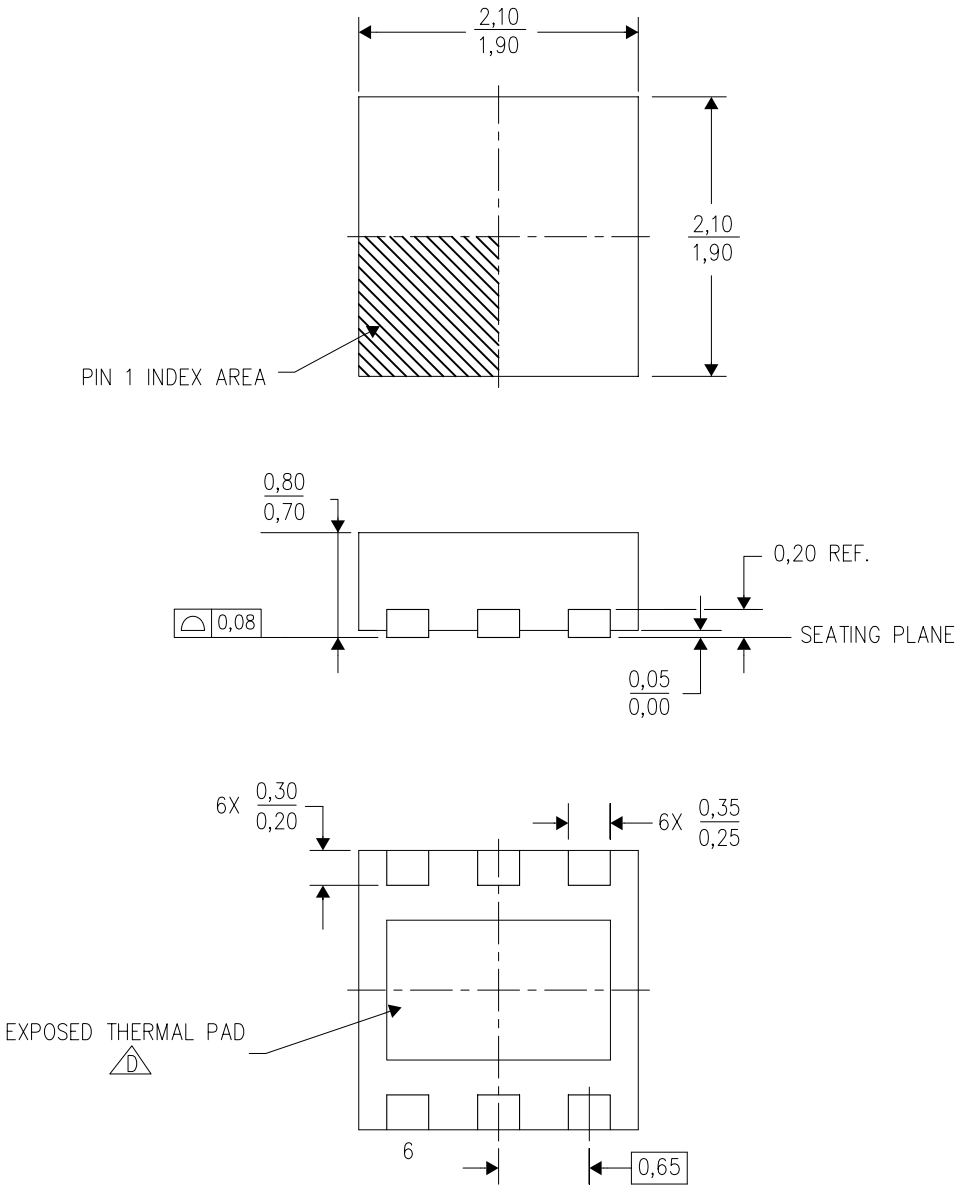
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223221/A 08/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

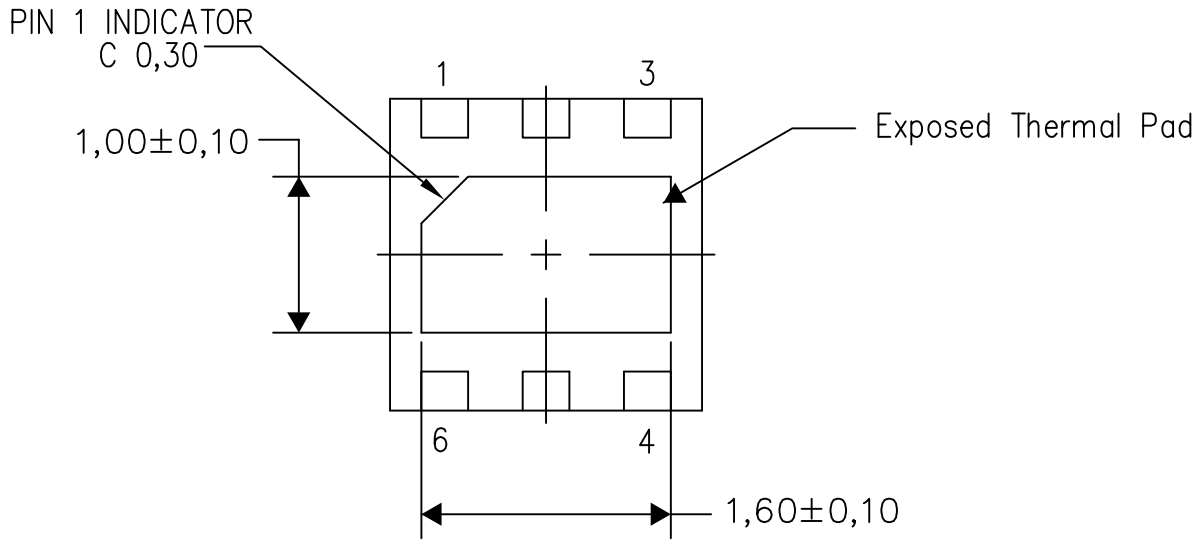
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



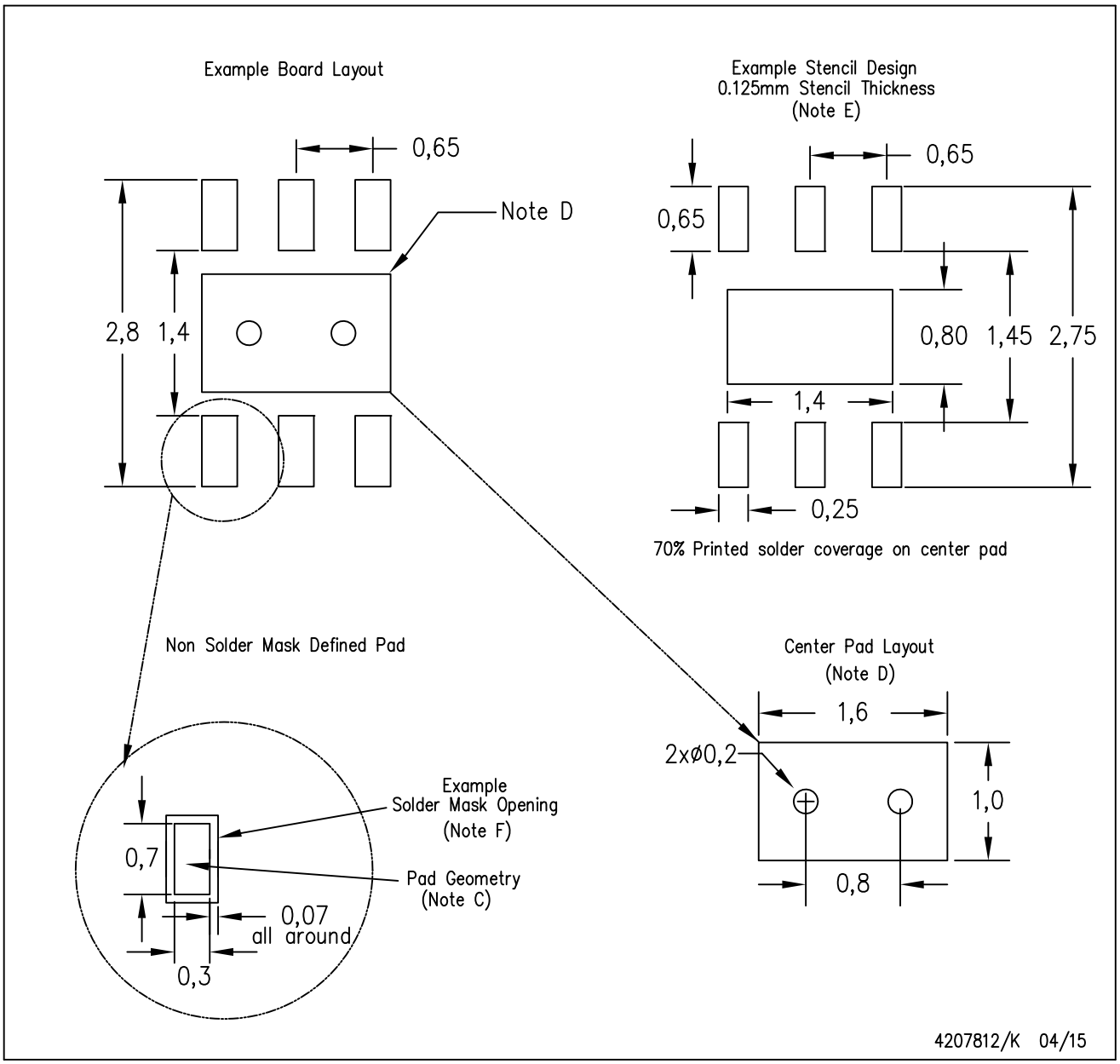
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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