



TSV521, TSV522, TSV524, TSV521A, TSV522A, TSV524A

High merit factor (1.15 MHz for 45 μ A) CMOS op amps

Datasheet –preliminary data

Features

- Gain bandwidth product: 1.15 MHz typ. at 5 V
- Low power consumption: 45 μ A typ. at 5 V
- Rail-to-rail input and output
- Low input bias current: 1 pA typ.
- Supply voltage: 2.7 to 5.5 V
- Low offset voltage: 800 μ V max.
- Unity gain stable on 100 pF capacitor
- Automotive grade

Benefits

- Increased lifetime in battery powered applications
- Easy interfacing with high impedance sensors

Related products

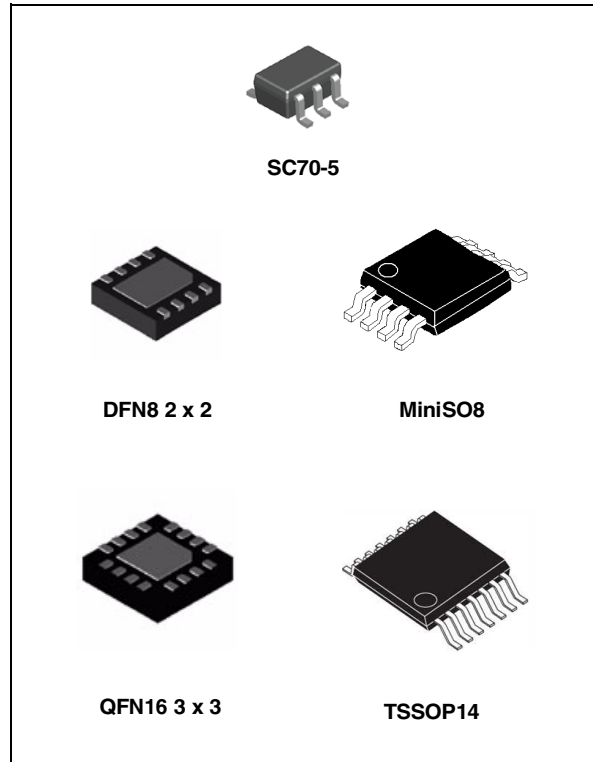
- See TSV6x series for lower minimum supply voltage (1.5 V)
- See LMV82x series for higher gain bandwidth products (5.5 MHz)

Applications

- Battery powered applications
- Portable devices
- Automotive signal conditioning
- Active filtering
- Medical instrumentation

Description

The TSV52x series of operational amplifiers offers low voltage operation and rail-to-rail input and output. The TSV521 device is the single version, the TSV522 device the dual version, and the TSV524 device the quad version, with pinouts compatible with industry standards.



The TSV52x series offers an outstanding speed/power consumption ratio, 1.15 MHz gain bandwidth product while consuming only 45 μ A at 5 V. The devices are housed in the smallest industrial packages.

These features make the TSV52x family ideal for sensor interfaces, battery supplied and portable applications. The wide temperature range and high ESD tolerance facilitate their use in harsh automotive applications.

Table 1. Device summary

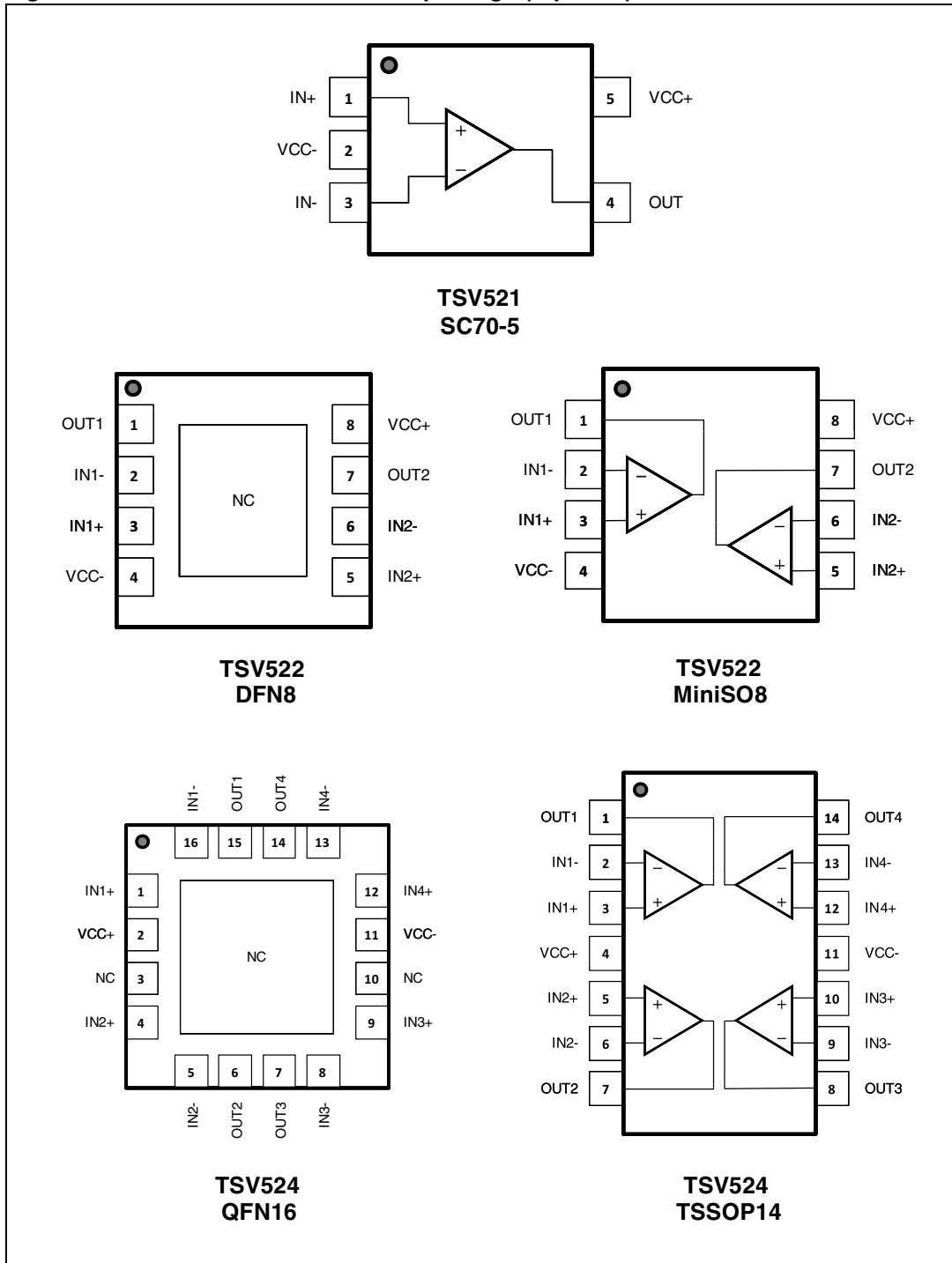
| | Standard V_{io} | Enhanced V_{io} |
|--------|-------------------|-------------------|
| Single | TSV521 | TSV521A |
| Dual | TSV522 | TSV522A |
| Quad | TSV524 | TSV524A |

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1 Package pin connections

Figure 1. Pin connections for each package (top view)



2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

| Symbol | Parameter | Value | Unit |
|------------|---|------------------------------------|------|
| V_{CC} | Supply voltage ⁽¹⁾ | 6 | V |
| V_{id} | Differential input voltage ⁽²⁾ | $\pm V_{CC}$ | V |
| V_{in} | Input voltage ⁽³⁾ | $V_{CC-} - 0.2$ to $V_{CC+} + 0.2$ | V |
| I_{in} | Input current ⁽⁴⁾ | 10 | mA |
| T_{stg} | Storage temperature | -65 to +150 | °C |
| R_{thja} | Thermal resistance junction-to-ambient ^{(5), (6)} SC70-5 DFN8 2 x 2 QFN16 3 x 3 MiniSO8 TSSOP14 | 205 57 45 190 100 | °C/W |
| T_j | Maximum junction temperature | 150 | °C |
| ESD | HBM: human body model ⁽⁷⁾ | 4 | kV |
| | MM: machine model ⁽⁸⁾ | 300 | V |
| | CDM: charged device model ⁽⁹⁾ (all packages except SC70-5 and DFN8) | 1.5 | kV |
| | CDM: charged device model (SC70-5 and DFN8) ⁽⁹⁾ | 1.3 | kV |
| | Latch-up immunity | 200 | mA |

- All voltage values, except differential voltages are with respect to network ground terminal.
- Differential voltages are the non inverting input terminal with respect to the inverting input terminal.
- $V_{CC-} - V_{in}$ must not exceed 6 V, V_{in} must not exceed 6 V.
- Input current must be limited by a resistor in series with the inputs.
- Short-circuits can cause excessive heating and destructive dissipation.
- R_{th} are typical values.
- Human body model: 100 pF discharged through a 1.5 k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
- Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 3. Operating conditions

| Symbol | Parameter | Value | Unit |
|------------|--------------------------------------|------------------------------------|------|
| V_{CC} | Supply voltage | 2.7 to 5.5 | V |
| V_{icm} | Common mode input voltage range | $V_{CC-} - 0.1$ to $V_{CC+} + 0.1$ | V |
| T_{oper} | Operating free air temperature range | -40 to +125 | °C |

3 Electrical characteristics

Table 4. Electrical characteristics at $V_{CC+} = +2.7\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|--|--|------|------|-------------|-------------------------|
| DC performance | | | | | | |
| V_{io} | Offset voltage | TSV52xA, $T = 25\text{ °C}$ | | | 800 | μV |
| | | TSV52xA, $-40\text{ °C} < T < 125\text{ °C}$ | | | 2600 | μV |
| | | TSV52x, $T = 25\text{ °C}$ | | | 1.5 | mV |
| | | TSV52x, $-40\text{ °C} < T < 125\text{ °C}$ | | | 3.3 | mV |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | $-40\text{ °C} < T < 125\text{ °C}^{(1)}$ | | 3 | 18 | $\mu\text{V}/\text{°C}$ |
| I_{io} | Input offset current ($V_{out} = V_{CC}/2$) | $T = 25\text{ °C}$ | | 1 | $10^{(3)}$ | pA |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | | 1 | $100^{(3)}$ | pA |
| I_{ib} | Input bias current ($V_{out} = V_{CC}/2$) | $T = 25\text{ °C}$ | | 1 | $10^{(3)}$ | pA |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | | 1 | $100^{(3)}$ | pA |
| CMR | Common mode rejection ratio $20 \log(\Delta V_{ic}/\Delta V_{io})$ $V_{ic} = -0.1\text{ V}$ to $V_{CC}+0.1\text{ V}$, $V_{out} = V_{CC}/2$, $R_L = 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | 50 | 72 | | dB |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | 46 | | | |
| A_{vd} | Large signal voltage gain $V_{out} = 0.5\text{ V}$ to $(V_{CC} - 0.5\text{ V})$, $R_L = 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | 90 | 105 | | dB |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | 60 | | | |
| V_{OH} | High level output voltage | $T = 25\text{ °C}$ $-40\text{ °C} < T < 125\text{ °C}$ | | 3 | 35 50 | mV |
| V_{OL} | Low level output voltage | $T = 25\text{ °C}$ $-40\text{ °C} < T < 125\text{ °C}$ | | 6 | 35 50 | mV |
| I_{out} | I_{sink} | $V_{out} = V_{CC}$, $T = 25\text{ °C}$ | 12 | 22 | | mA |
| | | $V_{out} = V_{CC}$, $-40\text{ °C} < T < 125\text{ °C}$ | 8 | | | |
| | I_{source} | $V_{out} = 0\text{ V}$, $T = 25\text{ °C}$ | 12 | 18 | | mA |
| | | $V_{out} = 0\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$ | 8 | | | |
| I_{CC} | Supply current (per channel) $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | | 30 | 51 | μA |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | | 30 | 51 | |
| AC performance | | | | | | |
| GBP | Gain bandwidth product | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | 0.62 | 1 | | MHz |
| F_u | Unity gain frequency | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 900 | | kHz |
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 55 | | degrees |
| G_m | Gain margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 7 | | dB |
| SR | Slew rate | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$ | | 0.74 | | V/ μs |

Table 4. Electrical characteristics at $V_{CC+} = +2.7$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T = 25$ °C, and $R_L = 10$ k Ω connected to $V_{CC}/2$ (unless otherwise specified) (continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------------------------------|--|------|----------|------|------------------------|
| e_n | Equivalent input noise voltage | f = 1 kHz f = 10 kHz | | 61 43 | | $\frac{nV}{\sqrt{Hz}}$ |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in} = 1$ kHz, $R_L = 100$ k Ω , $V_{icm} = V_{CC}/2$, BW = 22 kHz, $V_{out} = 1$ V _{pp} | | 0.003 | | % |

Table 5. Electrical characteristics at $V_{CC+} = +3.3$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T = 25$ °C, and $R_L = 10$ k Ω connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|---|--|------|------|--------------------|------------------------------|
| DC performance | | | | | | |
| V_{io} | Offset voltage | TSV52xA, $T = 25$ °C | | | 600 | μV |
| | | TSV52xA, -40 °C < T < 125 °C | | | 2400 | μV |
| | | TSV52x, $T = 25$ °C | | | 1.3 | mV |
| | | TSV52x, -40 °C < T < 125 °C | | | 3.1 | mV |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T < 125 °C ⁽¹⁾ | | 3 | 18 | $\mu V/^\circ C$ |
| ΔV_{io} | Long term input offset voltage drift | $T = 25$ °C ⁽²⁾ | | 0.3 | | $\frac{\mu V}{\sqrt{month}}$ |
| I_{io} | Input offset current ($V_{out} = V_{CC}/2$) | $T = 25$ °C | | 1 | 10 ⁽³⁾ | pA |
| | | -40 °C < T < 125 °C | | 1 | 100 ⁽³⁾ | pA |
| I_{ib} | Input bias current ($V_{out} = V_{CC}/2$) | $T = 25$ °C | | 1 | 10 ⁽³⁾ | pA |
| | | -40 °C < T < 125 °C | | 1 | 100 ⁽³⁾ | pA |
| CMR | Common mode rejection ratio $20 \log(\Delta V_{ic}/\Delta V_{io})$ $V_{ic} = -0.1$ V to $V_{CC} + 0.1$ V, $V_{out} = V_{CC}/2$, $R_L = 1$ M Ω | $T = 25$ °C | 51 | 73 | | dB |
| | | -40 °C < T < 125 °C | 47 | | | |
| A_{vd} | Large signal voltage gain $V_{out} = 0.5$ V to $(V_{CC} - 0.5$ V), $R_L = 1$ M Ω | $T = 25$ °C | 91 | 106 | | dB |
| | | -40 °C < T < 125 °C | 63 | | | |
| V_{OH} | High level output voltage | $T = 25$ °C -40 °C < T < 125 °C | | 3 | 35 50 | mV |
| V_{OL} | Low level output voltage | $T = 25$ °C -40 °C < T < 125 °C | | 7 | 35 50 | mV |
| I_{out} | I_{sink} | $V_{out} = V_{CC}$, $T = 25$ °C | 20 | 31 | | mA |
| | | $V_{out} = V_{CC}$, -40 °C < T < 125 °C | 17 | | | |
| | I_{source} | $V_{out} = 0$ V, $T = 25$ °C | 19 | 27 | | mA |
| | | $V_{out} = 0$ V, -40 °C < T < 125 °C | 17 | | | |
| I_{CC} | Supply current (per channel) $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω | $T = 25$ °C | | 32 | 55 | μA |
| | | -40 °C < T < 125 °C | | 32 | 55 | |

Table 5. Electrical characteristics at $V_{CC+} = +3.3\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^\circ\text{C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------------------------|--|------|----------|------|------------------------|
| AC performance | | | | | | |
| GBP | Gain bandwidth product | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | 0.64 | 1 | | MHz |
| F_u | Unity gain frequency | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 900 | | kHz |
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 55 | | degrees |
| G_m | Gain margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 7 | | dB |
| SR | Slew rate | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$ | | 0.75 | | V/ μs |
| e_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ $f = 10\text{ kHz}$ | | 60 42 | | $\frac{nV}{\sqrt{Hz}}$ |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in} = 1\text{ kHz}$, $R_L = 100\text{ k}\Omega$, $V_{icm} = V_{CC}/2$, $BW = 22\text{ kHz}$, $V_{out} = 1\text{ V}_{pp}$ | | 0.003 | | % |

Table 6. Electrical characteristics at $V_{CC+} = +5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^\circ\text{C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|---|--|------|------|-------------|---|
| DC performance | | | | | | |
| V_{io} | Offset voltage | TSV52xA, $T = 25\text{ }^\circ\text{C}$ | | | 600 | μV |
| | | TSV52xA, $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | | | 2400 | μV |
| | | TSV52x, $T = 25\text{ }^\circ\text{C}$ | | | 1 | mV |
| | | TSV52x, $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | | | 2.8 | mV |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}^{(1)}$ | | 3 | 18 | $\mu\text{V}/^\circ\text{C}$ |
| ΔV_{io} | Long term input offset voltage drift | $T = 25\text{ }^\circ\text{C}^{(2)}$ | | 0.7 | | $\frac{\mu\text{V}}{\sqrt{\text{month}}}$ |
| I_{io} | Input offset current ($V_{out} = V_{CC}/2$) | $T = 25\text{ }^\circ\text{C}$ | | 1 | $10^{(3)}$ | pA |
| | | $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | | 1 | $100^{(3)}$ | pA |
| I_{ib} | Input bias current ($V_{out} = V_{CC}/2$) | $T = 25\text{ }^\circ\text{C}$ | | 1 | $10^{(3)}$ | pA |
| | | $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | | 1 | $100^{(3)}$ | pA |
| CMR1 | Common mode rejection ratio $20\log(\Delta V_{ic}/\Delta V_{io})$ $V_{ic} = -0.1\text{ V}$ to $V_{CC} + 0.1\text{ V}$, $V_{out} = V_{CC}/2$, $R_L = 1\text{ M}\Omega$ | $T = 25\text{ }^\circ\text{C}$ | 54 | 76 | | dB |
| | | $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | 50 | | | |
| CMR2 | Common mode rejection ratio $20\log(\Delta V_{ic}/\Delta V_{io})$ $V_{ic} = 1\text{ V}$ to $V_{CC} - 1\text{ V}$, $V_{out} = V_{CC}/2$, $R_L = 1\text{ M}\Omega$ | $T = 25\text{ }^\circ\text{C}$ | 63 | 84 | | dB |
| | | $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$ | 58 | | | |

Table 6. Electrical characteristics at $V_{CC+} = +5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--|--|------|----------|----------|--------------------------------------|
| SVR | Supply voltage rejection ratio $20 \log(\Delta V_{CC}/\Delta V_{io})$ $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{out} = V_{CC}/2$ | $T = 25\text{ °C}$ | 65 | 87 | | dB |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | 60 | | | |
| A_{vd} | Large signal voltage gain $V_{out} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V})$, $R_L = 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | 94 | 109 | | dB |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | 68 | | | |
| V_{OH} | High level output voltage | $T = 25\text{ °C}$ $-40\text{ °C} < T < 125\text{ °C}$ | | 5 | 35 50 | mV |
| V_{OL} | Low level output voltage | $T = 25\text{ °C}$ $-40\text{ °C} < T < 125\text{ °C}$ | | 9 | 35 50 | mV |
| I_{out} | I_{sink} | $V_{out} = V_{CC}$, $T = 25\text{ °C}$ | 36 | 55 | | mA |
| | | $V_{out} = V_{CC}$, $-40\text{ °C} < T < 125\text{ °C}$ | 27 | | | |
| | I_{source} | $V_{out} = 0\text{ V}$, $T = 25\text{ °C}$ | 36 | 55 | | mA |
| | | $V_{out} = 0\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$ | 27 | | | |
| I_{CC} | Supply current (per channel) $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | | 45 | 60 | μA |
| | | $-40\text{ °C} < T < 125\text{ °C}$ | | 45 | 60 | |
| AC performance | | | | | | |
| GBP | Gain bandwidth product | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | 0.73 | 1.15 | | MHz |
| F_u | Unity gain frequency | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 900 | | kHz |
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 55 | | degrees |
| G_m | Gain margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 7 | | dB |
| SR | Slew rate | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V to } V_{CC} - 0.5\text{ V}$ | | 0.89 | | V/ μs |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: $f = 0.1\text{ to }10\text{ Hz}$ | | 14 | | μV_{pp} |
| e_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ $f = 10\text{ kHz}$ | | 57 39 | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in} = 1\text{ kHz}$, $R_L = 100\text{ k}\Omega$, $V_{icm} = V_{CC}/2$, BW = 22 kHz, $V_{out} = 1\text{ V}_{pp}$ | | 0.002 | | % |

1. See [Section 4.6: Input offset voltage drift over temperature on page 15](#).
2. Typical value is based on the V_{io} drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
3. Guaranteed by design.

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

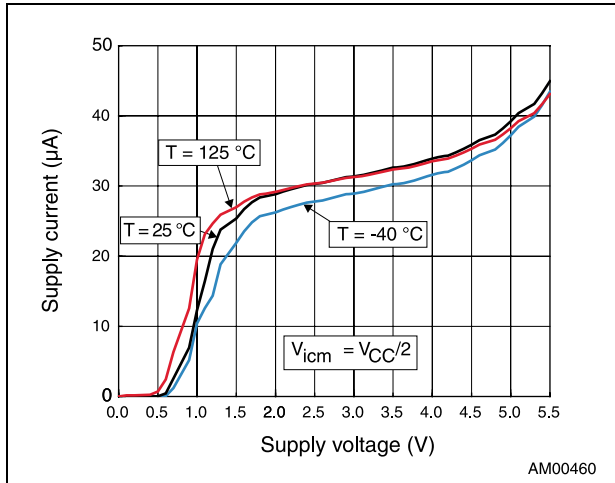


Figure 3. Input offset voltage distribution at $V_{CC} = 5\text{ V}$, $V_{icm} = 2.5\text{ V}$

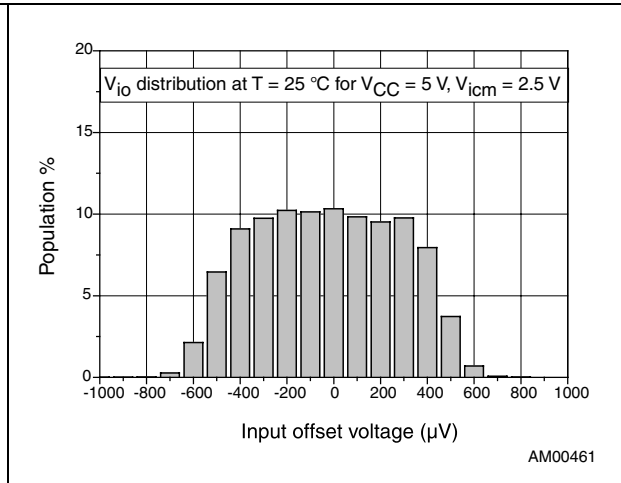


Figure 4. Input offset voltage temperature coefficient distribution

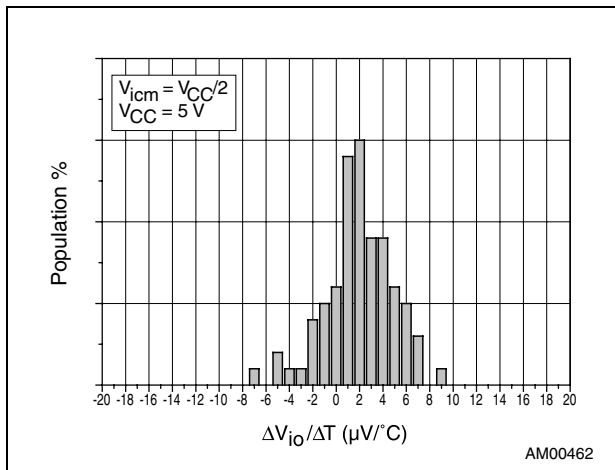


Figure 5. Input offset voltage vs. input common mode voltage at $V_{CC} = 5\text{ V}$

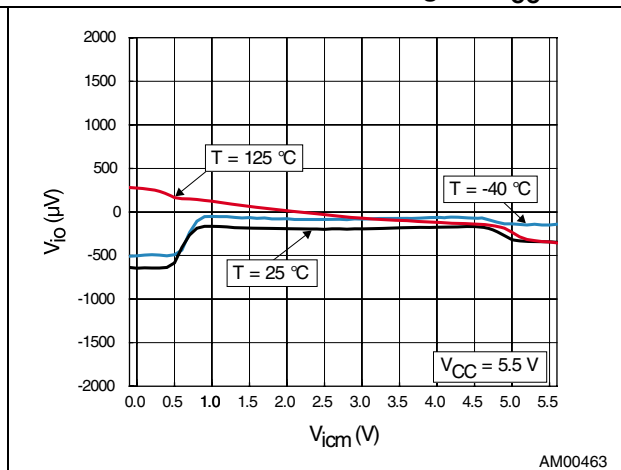


Figure 6. Input offset voltage vs. temperature at $V_{CC} = 5\text{ V}$

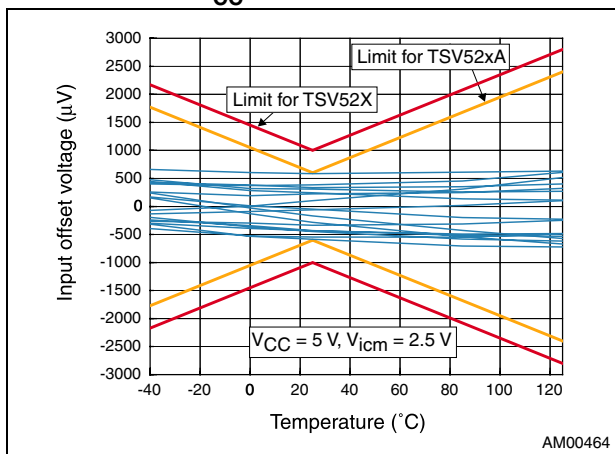


Figure 7. Output current vs. output voltage at $V_{CC} = 2.7\text{ V}$

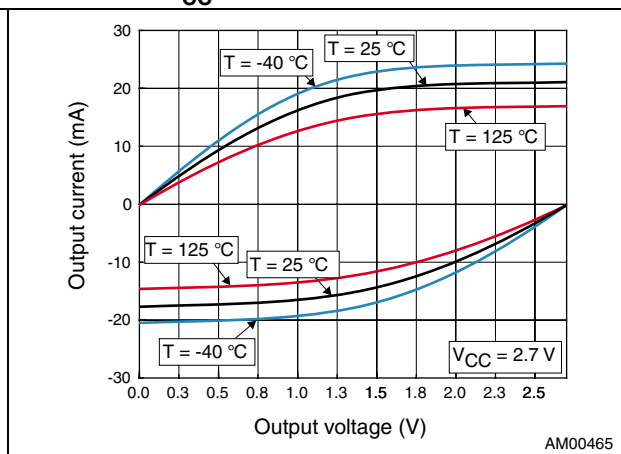


Figure 8. Output current vs. output voltage at $V_{CC} = 5.5\text{ V}$

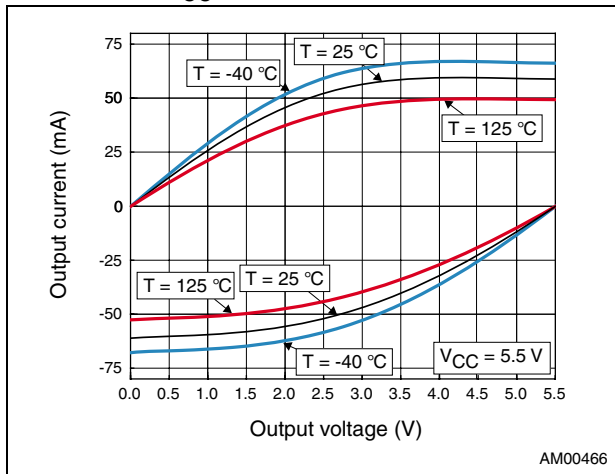


Figure 9. Bode diagram at $V_{CC} = 2.7\text{ V}$, $R_L = 10\text{ k}\Omega$

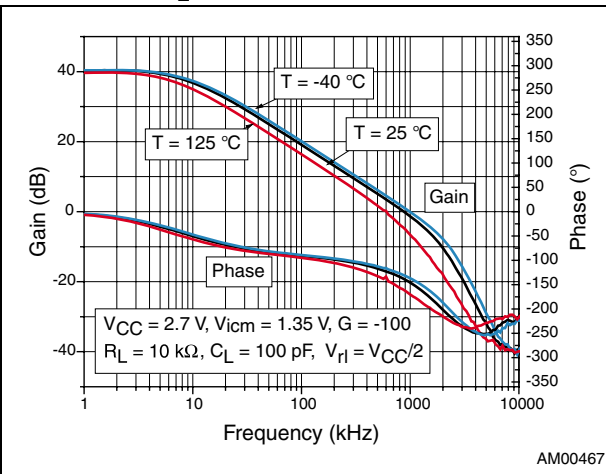


Figure 10. Bode diagram at $V_{CC} = 2.7\text{ V}$, $R_L = 2\text{ k}\Omega$

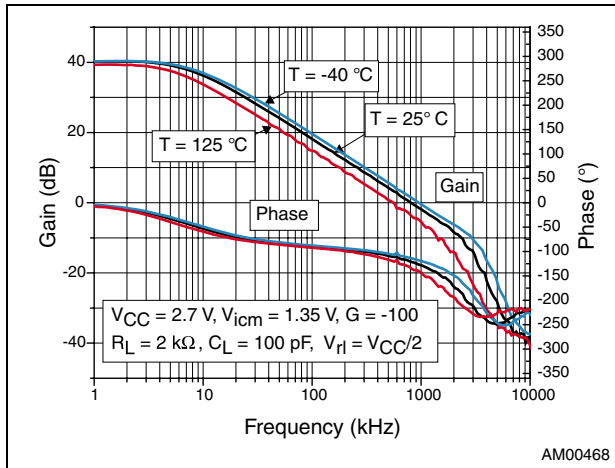


Figure 11. Bode diagram at $V_{CC} = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$

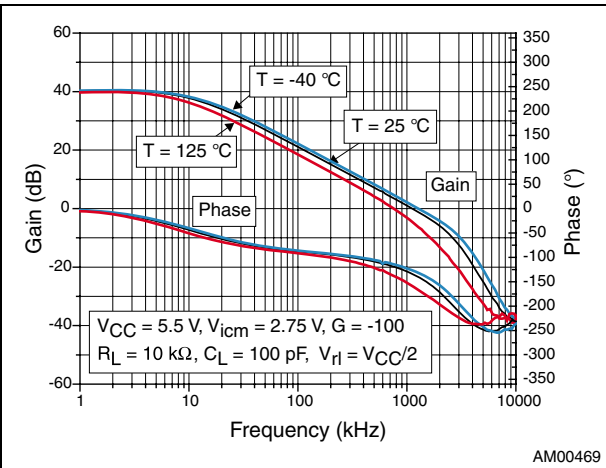


Figure 12. Bode diagram at $V_{CC} = 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$

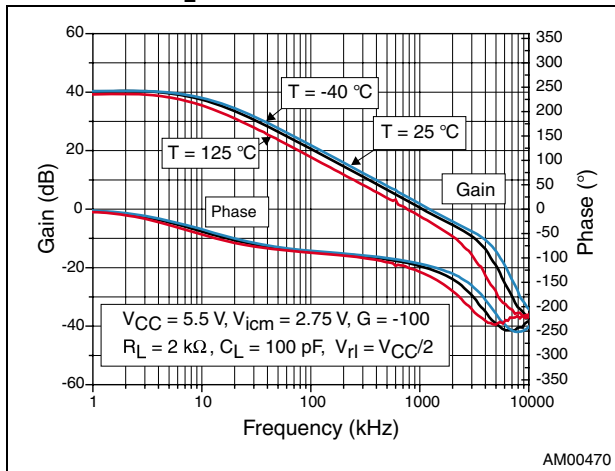


Figure 13. Noise vs. frequency

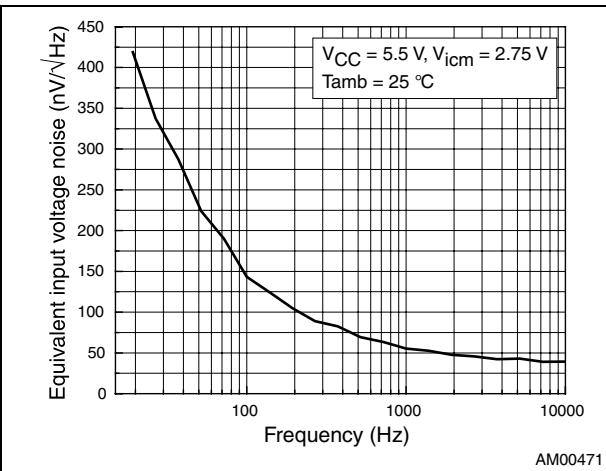


Figure 14. Positive slew rate vs. supply voltage

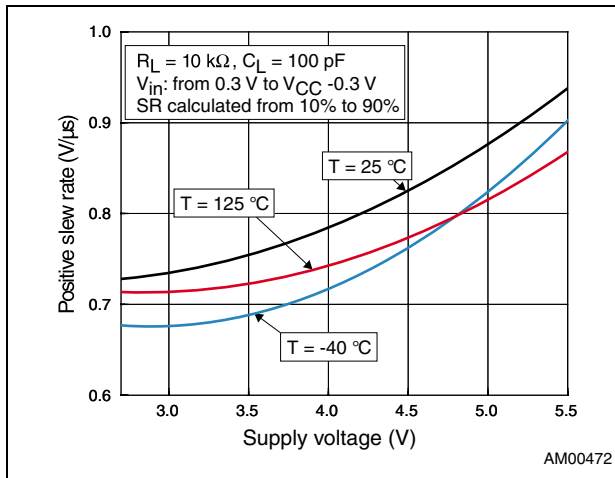


Figure 15. Negative slew rate vs. supply voltage

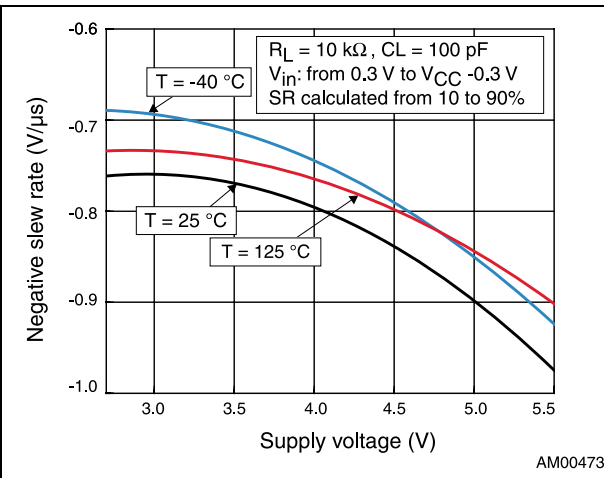


Figure 16. THD+N vs. frequency at VCC = 2.7 V Figure 17. THD+N vs. frequency at VCC = 5.5 V

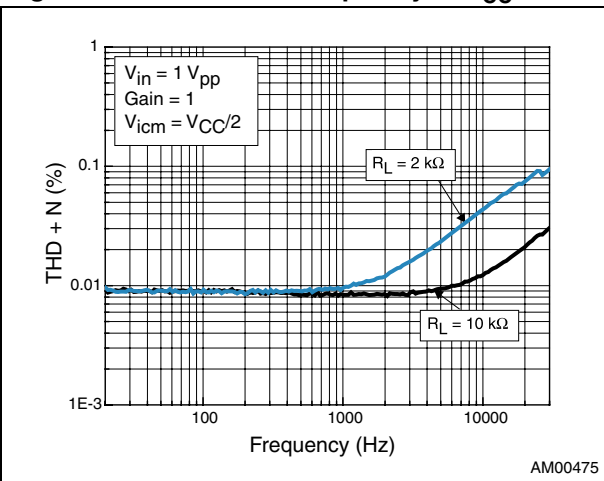
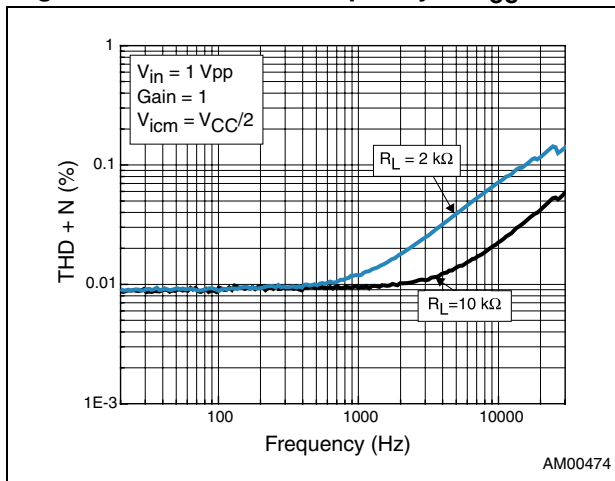


Figure 18. THD+N vs. output voltage at VCC = 2.7 V

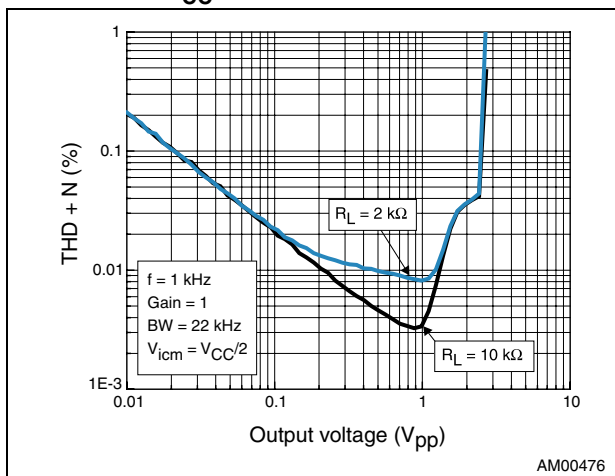


Figure 19. THD+N vs. output voltage at VCC = 5.5 V

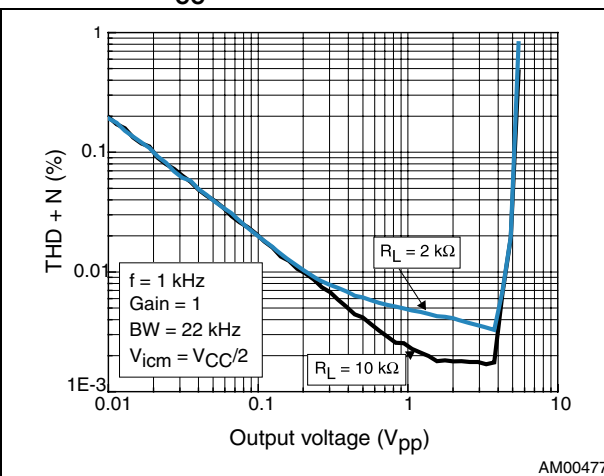


Figure 20. Output impedance versus frequency in closed-loop configuration

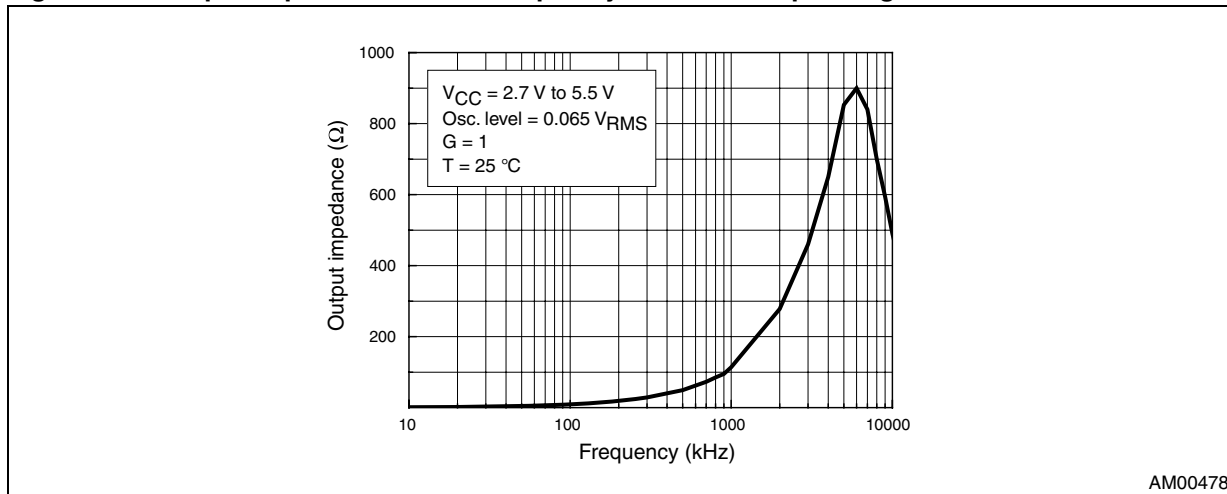


Figure 21. Response to a 100 mV input step for gain = 1 at V_{CC} = 5.5 V rising edge

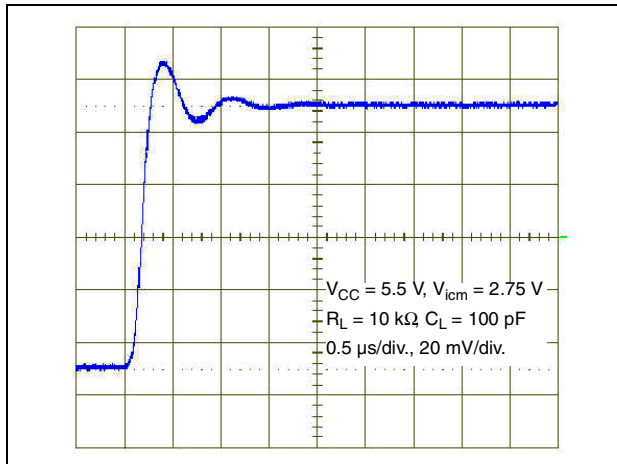


Figure 22. Response to a 100 mV input step for gain = 1 at V_{CC} = 5.5 V falling edge

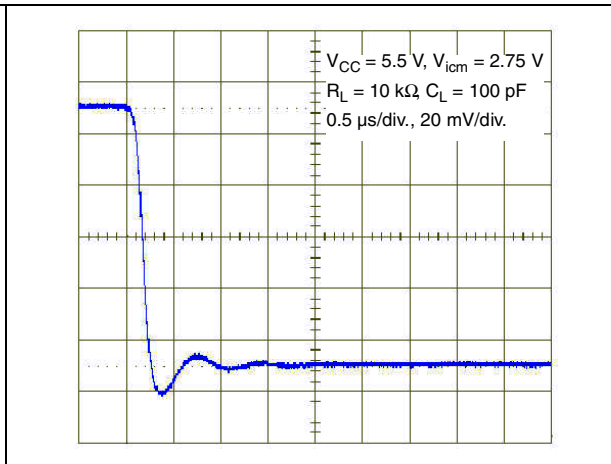


Figure 23. PSRR vs. frequency at V_{CC} = 2.7 V

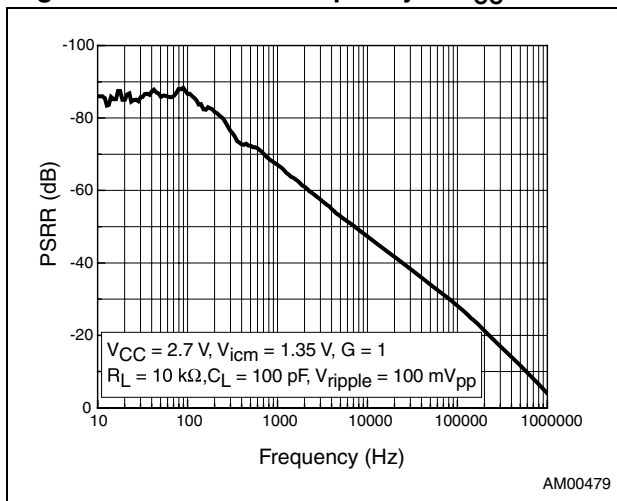
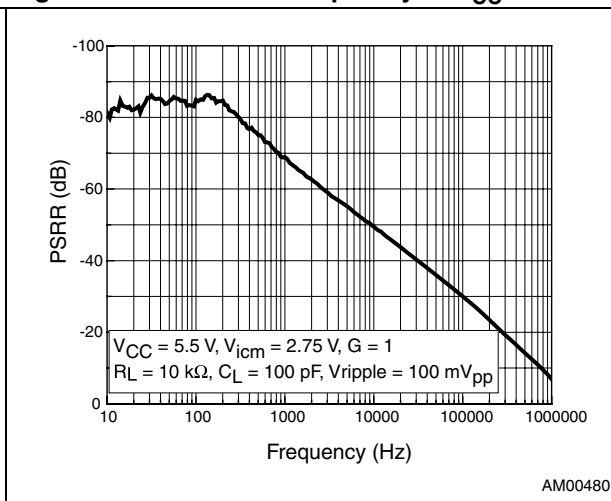


Figure 24. PSRR vs. frequency at V_{CC} = 5.5 V



4 Application information

4.1 Operating voltages

The amplifiers of the TSV52x series can operate from 2.7 to 5.5 V. Their parameters are fully specified for 2.7, 3.3 and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSV52x device characteristics at 2.7 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 °C.

4.2 Common mode voltage range

The TSV52x devices are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input and the input common mode range is extended from $V_{CC-} - 0.1$ V to $V_{CC+} + 0.1$ V.

The N channel pair is active for input voltage close to the positive rail typically ($V_{CC+} - 0.7$ V) to 100 mv above the positive rail.

The P channel pair is active for input voltage close to the negative rail typically 100 mV below the negative rail to $V_{CC-} + 0.7$ V.

And between $V_{CC-} + 0.7$ V and $V_{CC+} - 0.7$ V the both N and P pairs are active.

When the both pairs work together it allows to increase the speed of the TSV52x device. This architecture improves a lot the merit factor of the whole device. In the transition region, the performance of CMR, SVR, V_{io} (Figure 25 and Figure 26) and THD is slightly degraded.

Figure 25. Input offset voltage vs. input common mode at $V_{CC} = 2.7$ V

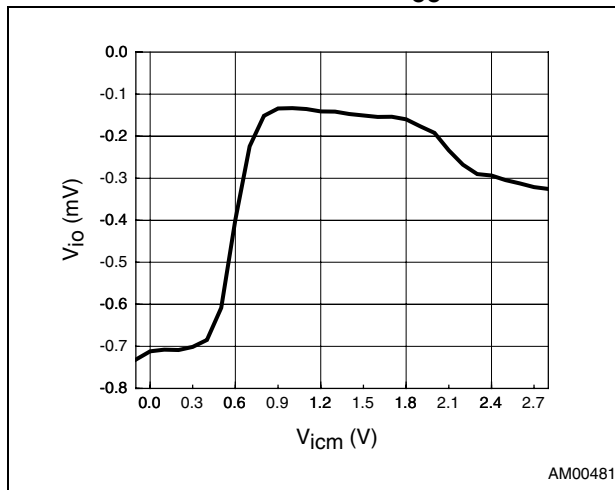
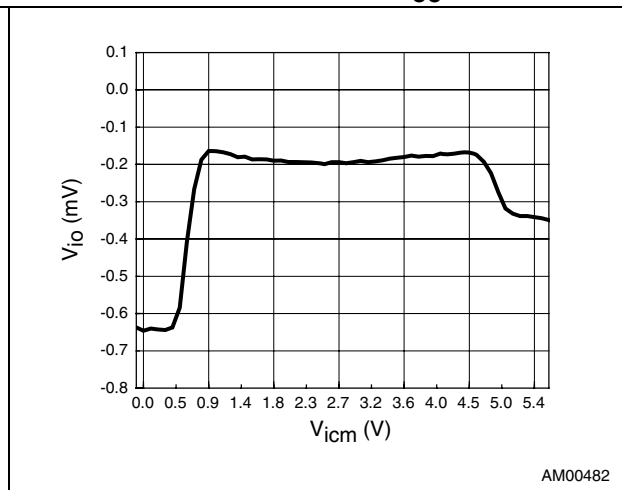


Figure 26. Input offset voltage vs. input common mode at $V_{CC} = 5.5$ V



4.3 Rail-to-rail input

The TSV52x series are guaranteed without phase reversal as shown in [Figure 28](#).

It is extremely important that the current flowing in the input pin does not exceed 10 mA. In order to limit this current a serial resistor can be added on the V_{in} path.

Figure 27. Phase reversal test schematic

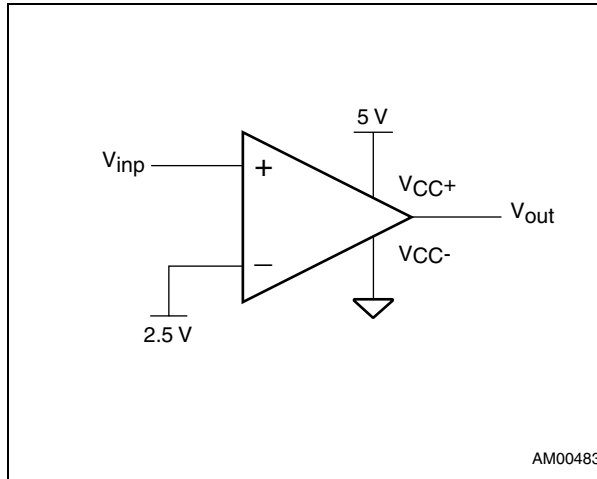
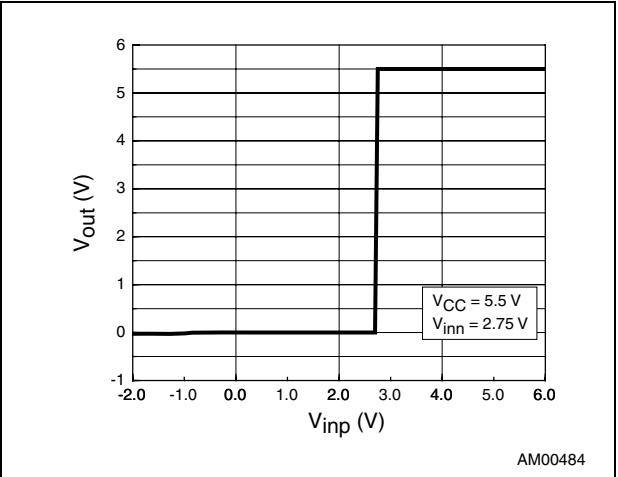


Figure 28. No phase reversal



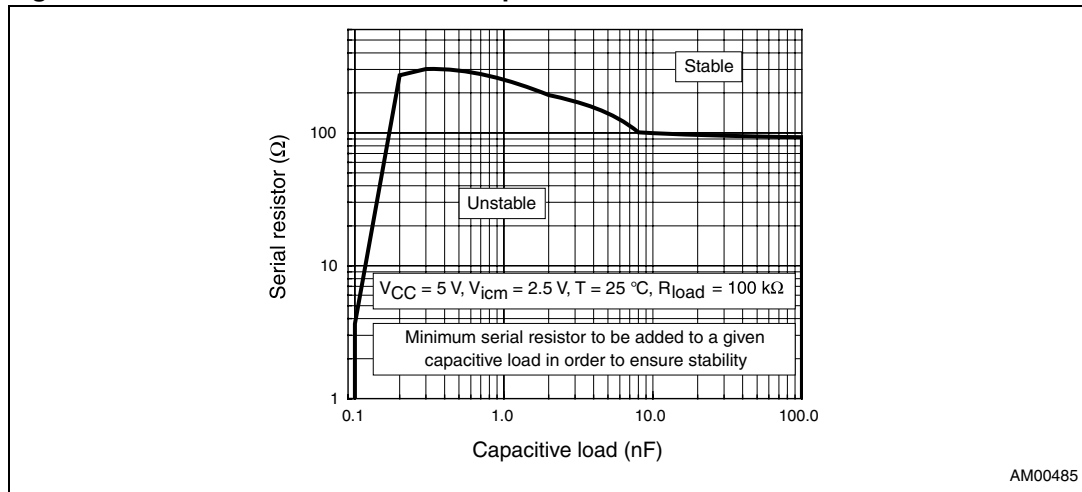
4.4 Rail-to-rail output

The operational amplifiers output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 k Ω resistive load to $V_{CC}/2$.

4.5 Driving resistive and capacitive loads

To drive high capacitive load, adding in series resistor at the output can improve the stability of the device (see [Figure 29](#) for recommended in series value). Once the in series resistor has been selected, the stability of the circuit should be tested on bench and simulated with simulation models. The R_{load} is placed in parallel with capacitive load. The R_{load} and the in series resistor create a voltage divider introducing an error proportional to the ratio R_s/R_{load} . By choosing R_s as low as possible, this error is generally negligible.

Figure 29. In series resistor versus capacitive load



4.6 Input offset voltage drift over temperature

The maximum input voltage drift over temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effects of temperature variations.

The maximum input voltage drift over temperature is computed in [Equation 1](#):

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25^\circ\text{C})}{T - 25^\circ\text{C}} \right|$$

with $T = -40\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C}$.

The datasheet maximum value is guaranteed by measurement on a representative sample size ensuring a C_{pk} greater than 2.

4.7 Long term input offset voltage drift

In a product reliability evaluation, two types of stress acceleration are usable:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature

The voltage acceleration has been defined based on JEDEC results, and is defined by:

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter

V_S is the stress voltage used for the accelerated test

V_U is the use voltage for the application

The temperature acceleration is driven by the Arrhenius model, and is defined by:

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S} \right)}$$

where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on failure rate

k is the Boltzmann's constant

T_U is the temperature of the die when V_U is used

T_S is the temperature of the die under temperature stress

The final acceleration factor, A_F is the multiplication of these two acceleration factors, which is:

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

Based on this A_F calculated following the defined usage temperature and usage voltage of the product, the 1000 h duration of the stress corresponds to a number of equivalent months of usage.

Equation 5

$$\text{Months} = A_F \times 1000 \text{ h} \times 12 \text{ months} / (24 \text{ h} \times 365.25 \text{ days})$$

For the operational amplifier, a follower stress condition is used for the reliability evaluation, with V_{CC} defined in function of the Maximum operating voltage and the absolute maximum rating (as recommended by the JEDEC standards).

The V_{io} drift, in μV , of the product after 1000 h duration of stress is tracked with parameters at different measurement conditions, as for example:

Equation 6

$$V_{CC} = \max. V_{op} \text{ with } V_{icm} = V_{CC}/2$$

Finally, knowing the calculated number of months and with the measured drift value of the V_{io} (corresponding to the electrical characteristics of the respective table) after 1000 h duration of stress, the ratio of the V_{io} drift over the square of months, ΔV_{io} in $\mu\text{V}/\sqrt{\text{month}}$, is defined as the long term drift parameter, the parameter estimating the reliability performance of the product.

Equation 7

$$\Delta V_{io} = V_{io} \text{ drift} / \sqrt{\text{months}}$$

4.8 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4.9 Macromodel

Accurate macromodels of the TSV52x device are available on STMicroelectronics™ website at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV52x operational amplifiers. It emulates the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the appropriate operational amplifier, *but it does not replace onboard measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 30. SC70-5 package outline

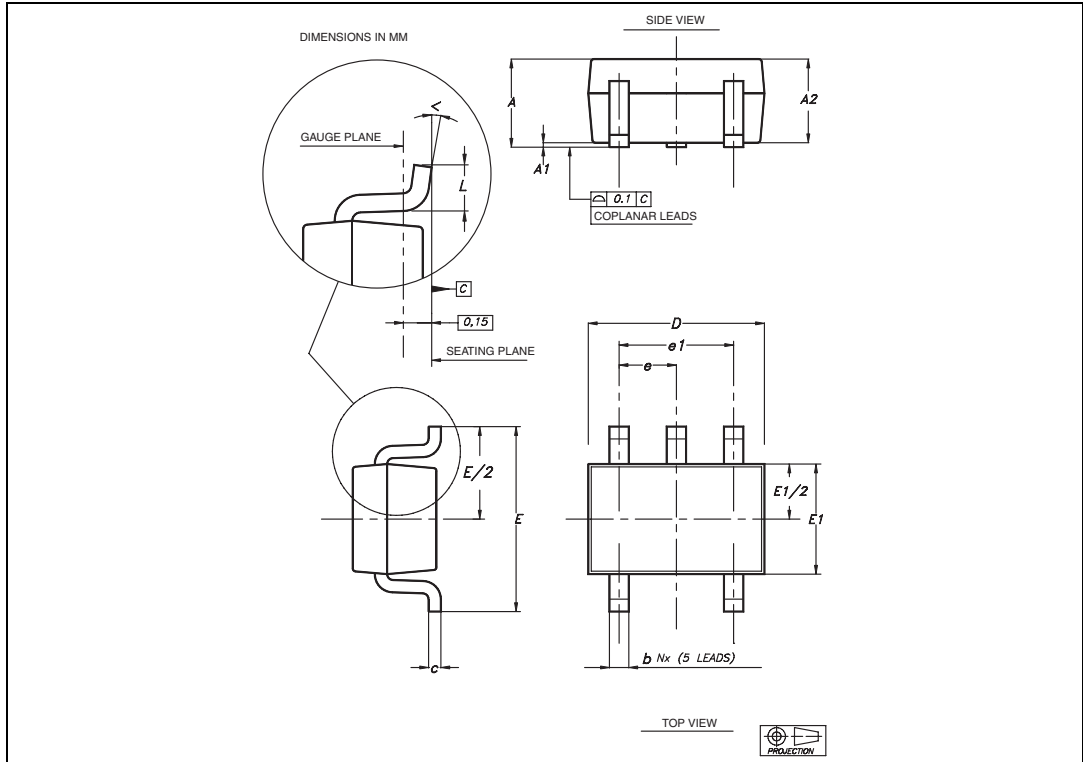


Table 7. SC70-5 package mechanical data

| Ref | Dimensions | | | | | |
|-----|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | | 1.10 | 0.032 | | 0.043 |
| A1 | 0 | | 0.10 | | | 0.004 |
| A2 | 0.80 | 0.90 | 1.00 | 0.032 | 0.035 | 0.039 |
| b | 0.15 | | 0.30 | 0.006 | | 0.012 |
| c | 0.10 | | 0.22 | 0.004 | | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.071 | 0.079 | 0.087 |
| E | 1.80 | 2.10 | 2.40 | 0.071 | 0.083 | 0.094 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | | 0.65 | | | 0.025 | |
| e1 | | 1.30 | | | 0.051 | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| < | 0° | | 8° | | | |

Figure 31. DFN8 2 x 2 x 0.6, 8 pitch, 0.5 mm package outline

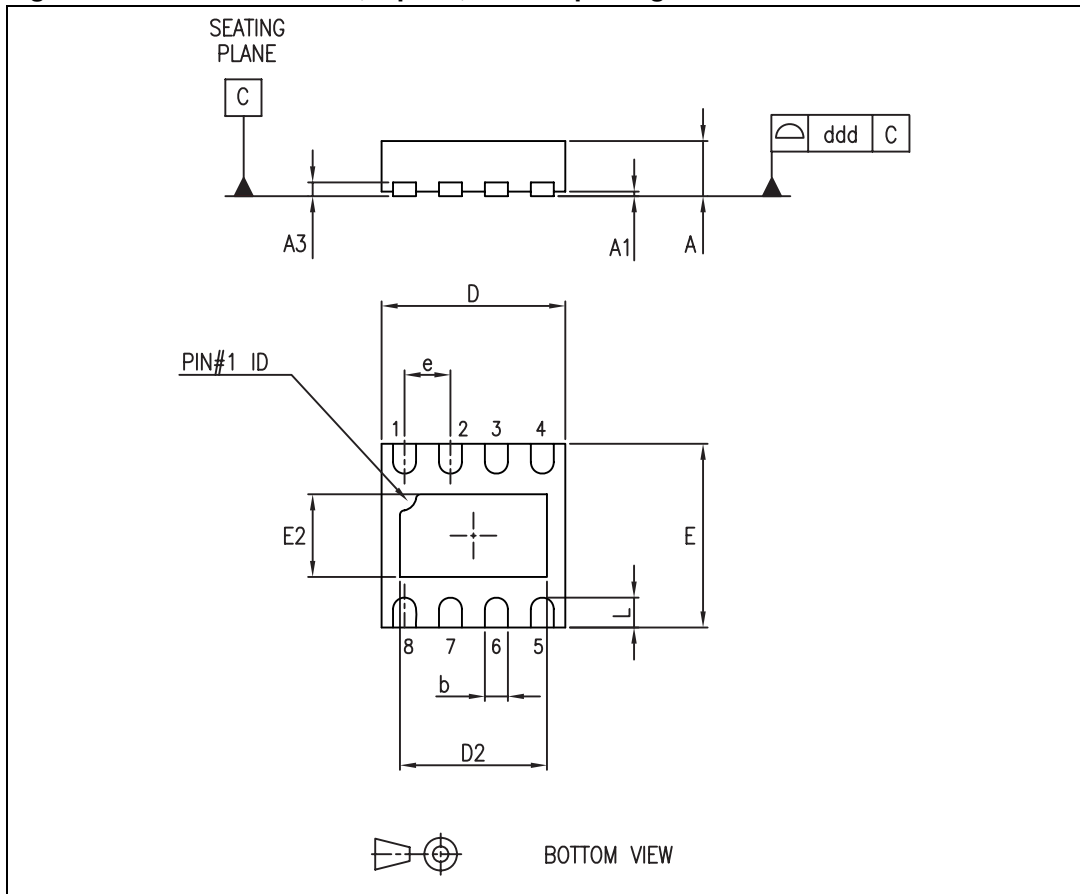


Table 8. DFN8 2 x 2 x 0.6, 8 pitch, 0.5 mm package mechanical data

| Ref. | Dimensions | | | | | |
|------|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.51 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | | | 0.05 | | | 0.002 |
| A3 | | 0.15 | | | 0.006 | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | 1.85 | 2.00 | 2.15 | 0.073 | 0.079 | 0.085 |
| D2 | 1.45 | 1.60 | 1.70 | 0.057 | 0.063 | 0.067 |
| E | 1.85 | 2.00 | 2.15 | 0.073 | 0.079 | 0.085 |
| E2 | 0.75 | 0.90 | 1.00 | 0.030 | 0.035 | 0.039 |
| e | | 0.50 | | | 0.020 | |
| L | | | 0.50 | | | 0.020 |
| ddd | | | 0.08 | | | 0.003 |

Figure 32. DFN8 2 x 2 0.6, 8 pitch, 0.5 mm footprint recommendation

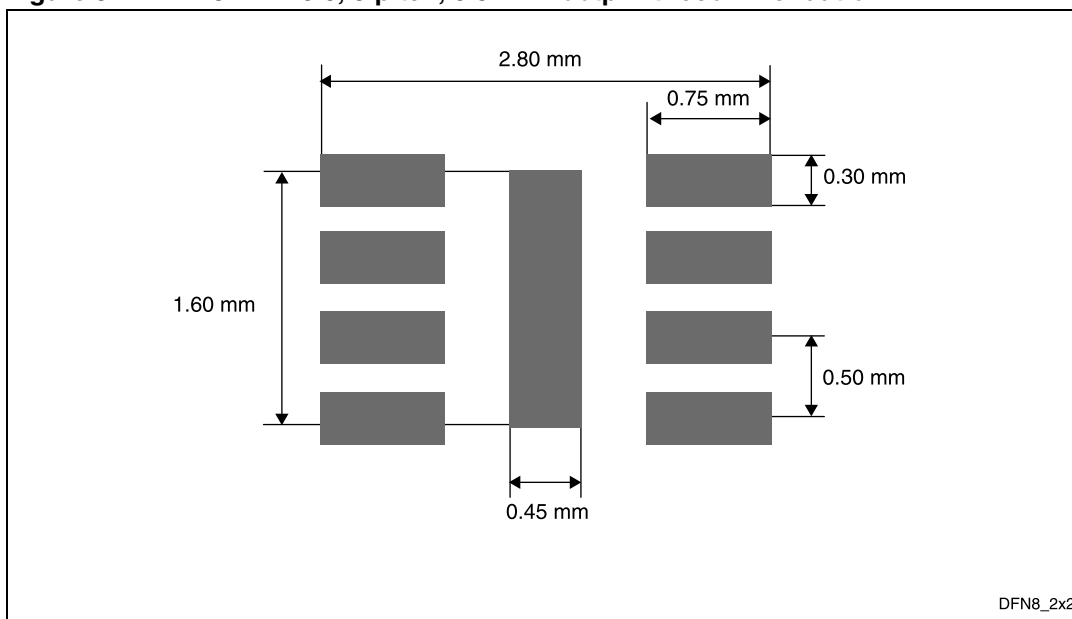


Figure 33. MiniSO8 package outline

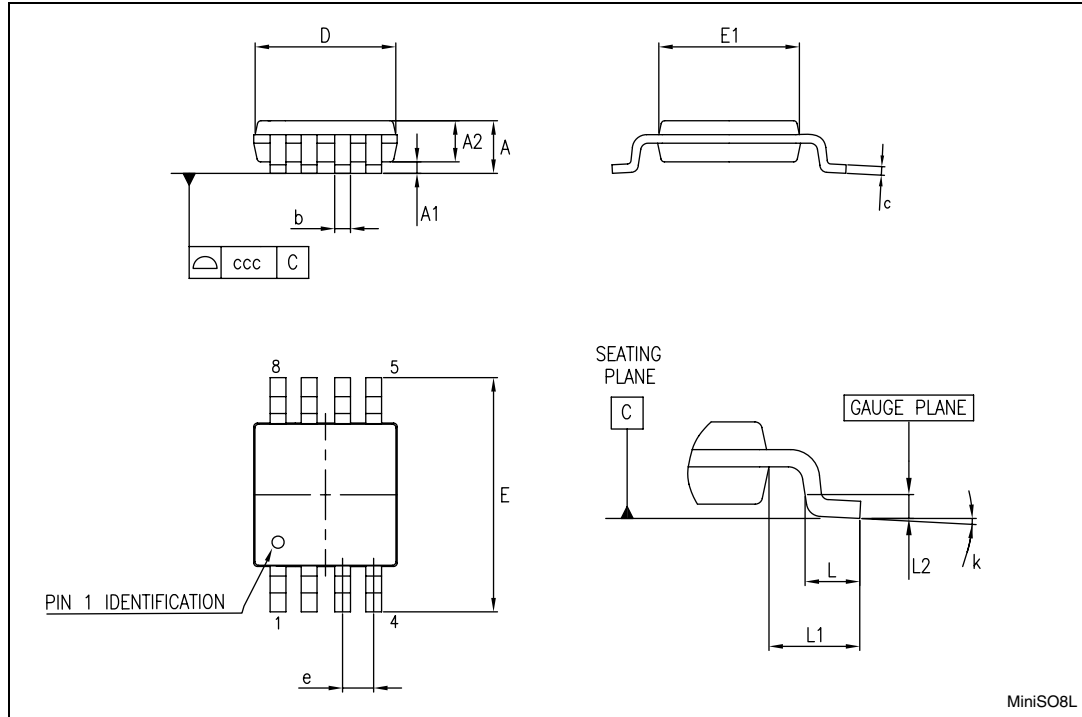
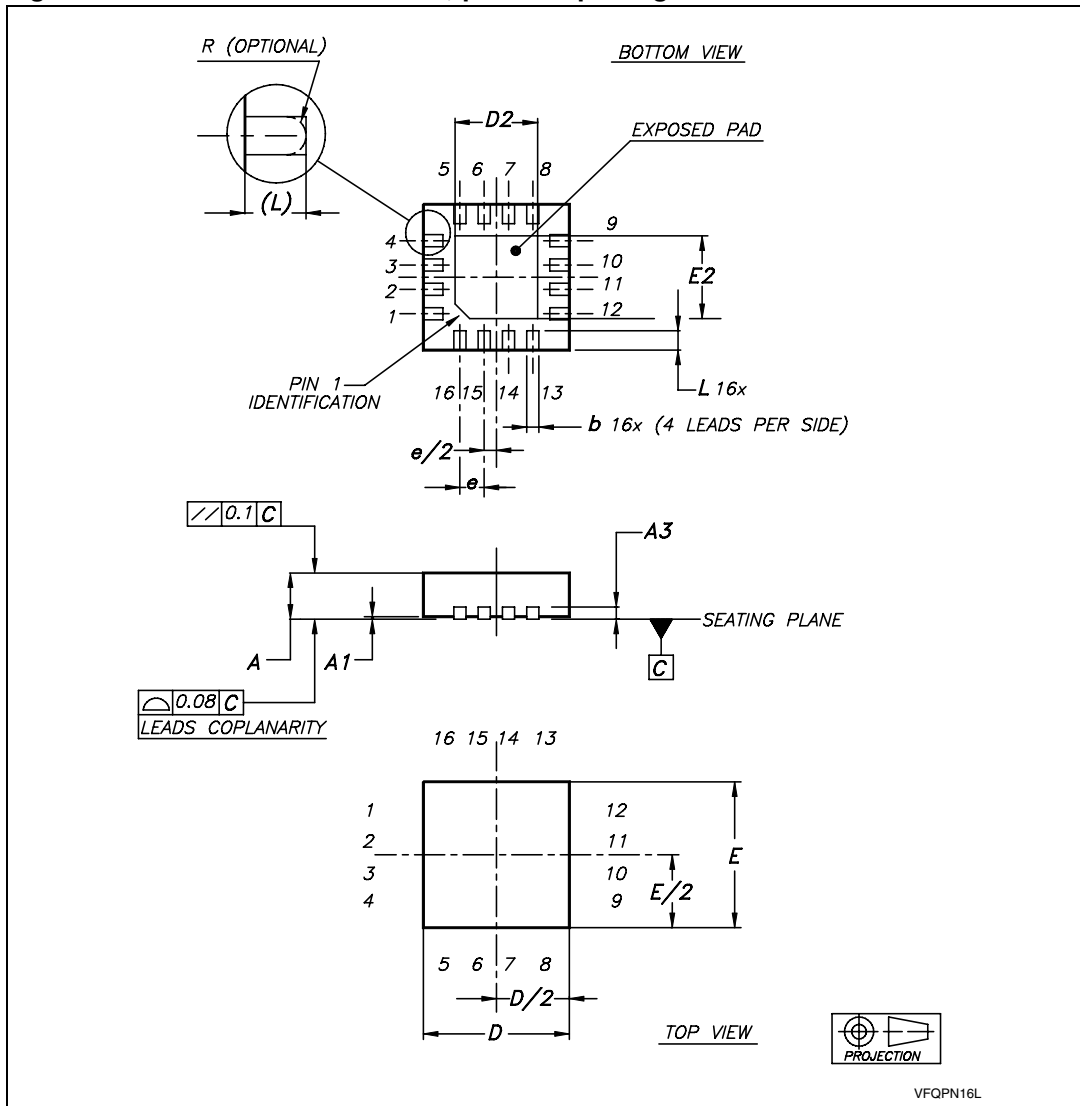


Table 9. MiniSO8 package mechanical data

| Symbol | Dimensions | | | | | |
|--------|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.10 | | | 0.043 |
| A1 | 0 | | 0.15 | 0 | | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | | 0.40 | 0.009 | | 0.016 |
| c | 0.08 | | 0.23 | 0.003 | | 0.009 |
| D | 2.80 | 3.00 | 3.20 | 0.11 | 0.118 | 0.126 |
| E | 4.65 | 4.90 | 5.15 | 0.183 | 0.193 | 0.203 |
| E1 | 2.80 | 3.00 | 3.10 | 0.11 | 0.118 | 0.122 |
| e | | 0.65 | | | 0.026 | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | | 0.95 | | | 0.037 | |
| L2 | | 0.25 | | | 0.010 | |
| k | 0° | | 8° | 0° | | 8° |
| ccc | | | 0.10 | | | 0.004 |

Figure 34. QFN16 - 3 x 3 x 0.9 mm, pad 1.7 - package outline



VFQPN16L

Table 10. QFN16 - 3 x 3 x 0.9 mm, pad 1.7 - package mechanical data

| Symbol | Dimensions | | | | | |
|-----------|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Nom. | Min. | Max. | Nom. | Min. | Max. |
| A | 0.90 | 0.80 | 1.00 | 0.035 | 0.032 | 0.039 |
| A1 | | 0.00 | 0.05 | | 0.000 | 0.002 |
| A3 | 0.20 | | | 0.008 | | |
| b | | 0.18 | 0.30 | | 0.007 | 0.012 |
| D | 3.00 | 2.90 | 3.10 | 0.118 | 0.114 | 0.122 |
| D2 | | 1.50 | 1.80 | | 0.061 | 0.071 |
| E | 3.00 | 2.90 | 3.10 | 0.118 | 0.114 | 0.122 |
| E2 | | 1.50 | 1.80 | | 0.061 | 0.071 |
| e | 0.50 | | | 0.020 | | |
| L | | 0.30 | 0.50 | | 0.012 | 0.020 |

Figure 35. QFN16 - 3 x 3 x 0.9 mm, pad 1.7 - footprint recommendation

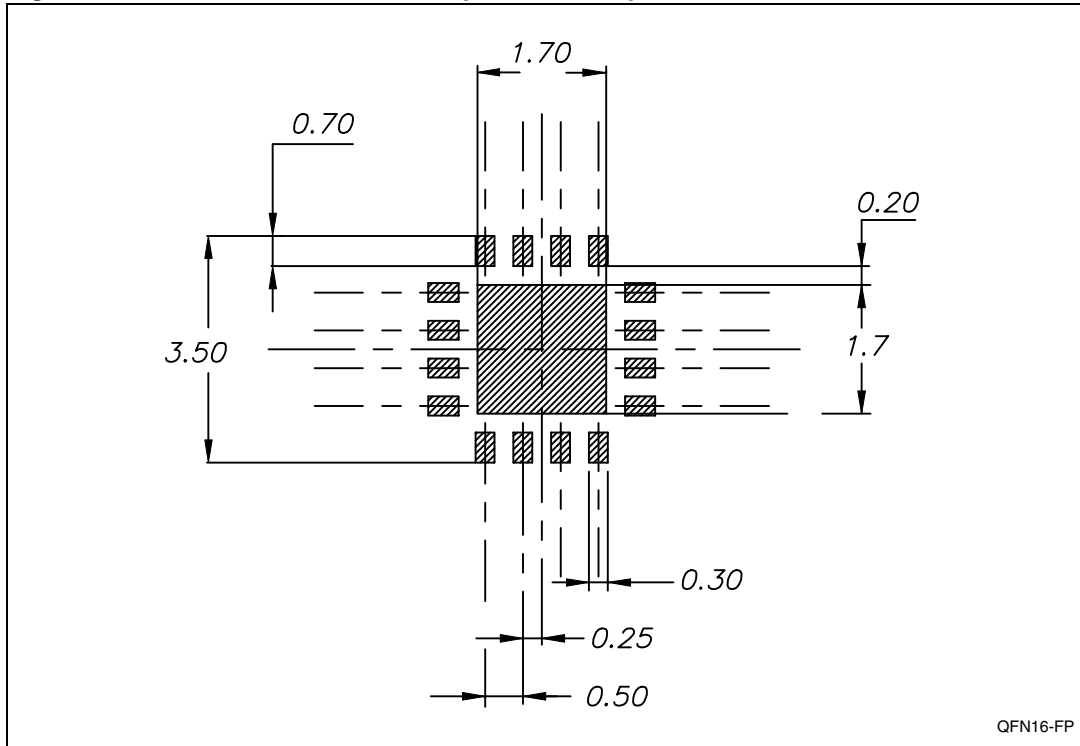


Figure 36. TSSOP14 body 4.40 mm, lead pitch 0.65 mm - package outline

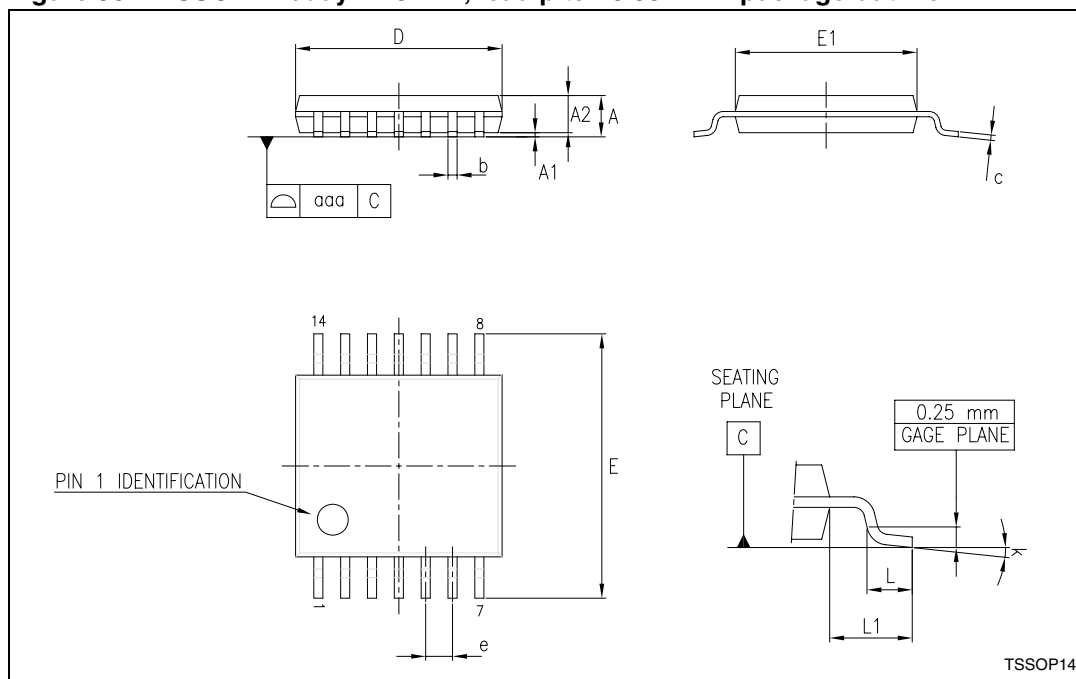


Table 11. TSSOP14 body 4.40 mm, lead pitch 0.65 mm - package mechanical data

| Symbol | Dimensions | | | | | |
|--------|-------------|------|------|--------|------------|--------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E | 6.20 | 6.40 | 6.60 | 0.244 | 0.252 | 0.260 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 | | | 0.0256 BSC | |
| L | 0.45 | 0.60 | 0.75 | | | |
| L1 | | 1.00 | | | | |
| k | 0° | | 8° | 0° | | 8° |
| aaa | | | 0.10 | 0.018 | 0.024 | 0.030 |

6 Ordering information

Table 12. Order codes

| Order code | Temperature range | Package | Packing | Marking |
|-------------|--|-------------|---------------|----------|
| TSV521ICT | -40 to 125 °C | SC70-5 | Tape and reel | K1G |
| TSV522IQ2T | | DFN8 2 x 2 | | K1G |
| TSV522IST | | MiniSO8 | | K1G |
| TSV524IQ4T | | QFN16 3 x 3 | | K1G |
| TSV524IPT | | TSSOP14 | | TSV524 |
| TSV522IYST | -40 to 125 °C Automotive grade ⁽¹⁾ | MiniSO8 | Tape and reel | K1H |
| TSV524IYPT | | TSSOP14 | | TSV524Y |
| TSV521AICT | -40 to 125 °C | SC70-5 | Tape and reel | K1K |
| TSV522AIQ2T | | DFN8 2 x 2 | | K1K |
| TSV522AIST | | MiniSO8 | | K1K |
| TSV524AIQ4T | | QFN16 3 x 3 | | K1K |
| TSV524AIPT | | TSSOP14 | | TSV524A |
| TSV522AIYST | -40 to 125 °C Automotive grade ⁽¹⁾ | MiniSO8 | Tape and reel | K1L |
| TSV524AIYPT | | TSSOP14 | | TSV524AY |

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 19-Jun-2012 | 1 | Initial release. |

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