

## DUAL SP4T ANALOG SWITCH

### 3.3-V/2.5-V DUAL 4:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

#### FEATURES

- Isolation in the Powered-Down Mode,  $V_+ = 0$
- Low ON-State Resistance
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.3-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

#### APPLICATIONS

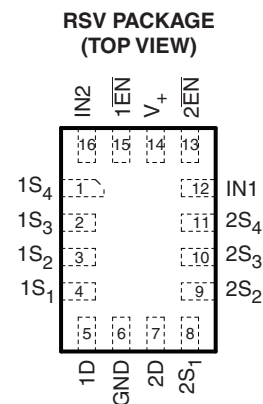
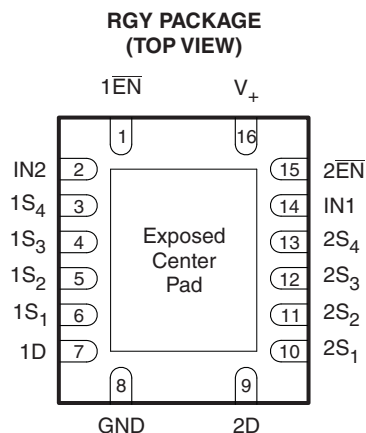
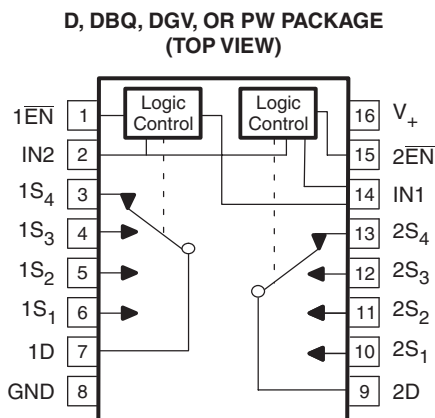
- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

#### DESCRIPTION

The TS3A5017 is a dual single-pole quadruple-throw (4:1) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals, and signals up to  $V_+$  can be transmitted in either direction.

**FUNCTION TABLE**

$\overline{EN}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S <sub>1</sub>
L	L	H	D = S <sub>2</sub>
L	H	L	D = S <sub>3</sub>
L	H	H	D = S <sub>4</sub>
H	X	X	OFF



If exposed center pad is used, it must be connected as a secondary ground or left electrically open.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	$\mu$ QFN – RSV	Tape and reel	TS3A5017RSVR	ZVL
	QFN – RGY	Tape and reel	TS3A5017RGYR	YA017
	SOIC – D	Tube	TS3A5017D	TS3A5017
		Tape and reel	TS3A5017DR	
	SSOP (QSOP) – DBQ	Tape and reel	TS3A5017DBQR	YA017
	TSSOP – PW	Tube	TS3A5017PW	YA017
		Tape and reel	TS3A5017PWR	
	TVSOP – DGV	Tape and reel	TS3A5017DGVR	YA017

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**SUMMARY OF CHARACTERISTICS**

$$V_+ = 3.3 \text{ V}, T_A = 25^\circ\text{C}$$

Configuration	Dual Analog Multiplexer/Demultiplexer (4:1 Mux/Demux)
Number of channels	2
ON-state resistance ( $r_{on}$ )	11 $\Omega$
ON-state resistance match ( $\Delta r_{on}$ )	1 $\Omega$
ON-state resistance flatness ( $r_{on(flat)}$ )	7 $\Omega$
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	5 ns/1.5 ns
Charge injection ( $Q_C$ )	5 pC
Bandwidth (BW)	165 MHz
OFF isolation ( $O_{ISO}$ )	–48 dB at 10 MHz
Crosstalk ( $X_{TALK}$ )	–49 dB at 10 MHz
Total harmonic distortion (THD)	0.21%
Leakage current ( $I_{D(OFF)}/I_{S(OFF)}$ )	$\pm 0.1 \mu\text{A}$
Power-supply current ( $I_+$ )	2.5 $\mu\text{A}$
Package options	16-pin QFN, $\mu$ QFN, SOIC, SSOP, TSSOP, or TVSOP

**ABSOLUTE MINIMUM AND MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
$V_+$	Supply voltage <sup>(3)</sup>	–0.5	4.6	V
$V_S, V_D$	Analog voltage <sup>(3)(4)</sup>	–0.5	4.6	V
$I_{SK}, I_{DK}$	Analog port clamp current	$V_S, V_D < 0$		mA
$I_S, I_D$	On-state switch current	$V_S, V_D = 0$ to 7 V		mA
$V_I$	Digital input voltage	–0.5	4.6	V
$I_{IK}$	Digital input clamp current <sup>(3)(4)</sup>	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	–100		mA
$T_{stg}$	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**PACKAGE THERMAL IMPEDANCE**

			<b>UNIT</b>
$\theta_{JA}$	Package thermal impedance <sup>(1)</sup>	D package	73
		DB package	82
		DGV package	120
		DW package	108
		RGY package	91.6
		RSV package	184

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY<sup>(1)</sup>**
 $V_+ = 2.7\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
Analog signal range	$V_D, V_S$					0		$V_+$	V
ON-state resistance	$r_{on}$	$0 \leq V_S \leq V_+$ , $I_D = -32\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	11		12	$\Omega$
				Full		14			
ON-state resistance match between channels	$\Delta r_{on}$	$V_S = 2.1\text{ V}$ , $I_D = -32\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	1		2	$\Omega$
				Full		3			
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_S \leq V_+$ , $I_D = -32\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	7		9	$\Omega$
				Full		10			
S OFF leakage current	$I_{S(OFF)}$	$V_S = 1\text{ V}, V_D = 3\text{ V}$ , or $V_S = 3\text{ V}, V_D = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V	-0.1	0.05	0.1	$\mu\text{A}$
				Full		-0.2		0.2	
	$I_{SPWR(OFF)}$	$V_S = 0\text{ to }3.6\text{ V}$ , $V_D = 3.6\text{ V to }0$ ,		25°C	0 V	-1	0.5	1	
				Full		-5		5	
D OFF leakage current	$I_{D(OFF)}$	$V_S = 1\text{ V}, V_D = 3\text{ V}$ , or $V_S = 3\text{ V}, V_D = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V	-0.1	0.05	0.1	$\mu\text{A}$
				Full		-0.2		0.2	
	$I_{DPWR(OFF)}$	$V_D = 0\text{ to }3.6\text{ V}$ , $V_S = 3.6\text{ V to }0$ ,		25°C	0 V	-1	0.5	1	
				Full		-5		5	
S ON leakage current	$I_{S(ON)}$	$V_S = 1\text{ V}, V_D = \text{Open}$ , or $V_S = 3\text{ V}, V_D = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V	-0.1	0.05	0.1	$\mu\text{A}$
				Full		-0.2		0.2	
D ON leakage current	$I_{D(ON)}$	$V_D = 1\text{ V}, V_S = \text{Open}$ , or $V_D = 3\text{ V}, V_S = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V	-0.1	0.05	0.1	$\mu\text{A}$
				Full		-0.2		0.2	
<b>Digital Control Inputs (IN1, IN2, <math>\overline{\text{EN}}</math>)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$			Full		2		$V_+$	V
Input logic low	$V_{IL}$			Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_+ \text{ or } 0$		25°C	3.6 V	-1	0.05	1	$\mu\text{A}$
				Full		-1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)**
 $V_+ = 2.7\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_D = 2\text{ V}$ , $R_L = 300\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	1	5	9.5	ns
				Full	3 V to 3.6 V	1		10.5	
Turn-off time	$t_{OFF}$	$V_D = 2\text{ V}$ , $R_L = 300\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	0.5	1.5	3.5	ns
				Full	3 V to 3.6 V	0.5		4.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ ,	See <a href="#">Figure 22</a>	25°C	3.3 V		5	pC	
S OFF capacitance	$C_{S(OFF)}$	$V_S = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	3.3 V		4.5	pF	
D OFF capacitance	$C_{D(OFF)}$	$V_D = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	3.3 V		19	pF	
S ON capacitance	$C_{S(ON)}$	$V_S = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	3.3 V		25	pF	
D ON capacitance	$C_{D(ON)}$	$V_D = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	3.3 V		25	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	3.3 V		165	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 19</a>	25°C	3.3 V		-48	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 20</a>	25°C	3.3 V		-49	dB	
Crosstalk adjacent	$X_{TALK(ADJ)}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 21</a>	25°C	3.3 V		-74	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 23</a>	25°C	3.3 V		0.21	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	7	$\mu\text{A}$
				Full				10	

**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_D, V_S$				0		$V_+$	V	
ON-state resistance	$r_{on}$	$0 \leq V_S \leq V_+$ , $I_D = -24 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		20.5	22 24	$\Omega$	
ON-state resistance match between channels	$\Delta r_{on}$	$V_S = 1.6 \text{ V}$ , $I_D = -24 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		1	2 3	$\Omega$	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_S \leq V_+$ , $I_D = -24 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		16	18 20	$\Omega$	
S OFF leakage current	$I_{S(OFF)}$	$V_S = 0.5 \text{ V}$ , $V_D = 2.2 \text{ V}$ , or $V_S = 2.2 \text{ V}$ , $V_D = 0.5 \text{ V}$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	$\mu\text{A}$	
	$I_{SPWR(OFF)}$	$V_S = 0 \text{ to } 2.7 \text{ V}$ , $V_D = 2.7 \text{ V to } 0$ ,	25°C Full	0 V	-1	0.5	1 5		
D OFF leakage current	$I_{D(OFF)}$	$V_S = 0.5 \text{ V}$ , $V_D = 2.2 \text{ V}$ , or $V_S = 2.2 \text{ V}$ , $V_D = 0.5 \text{ V}$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	$\mu\text{A}$	
	$I_{DPWR(OFF)}$	$V_D = 0 \text{ to } 2.7 \text{ V}$ , $V_S = 2.7 \text{ V to } 0$ ,	25°C Full	0 V	-1	0.5	1 5		
S ON leakage current	$I_{S(ON)}$	$V_S = 0.5 \text{ V}$ , $V_D = \text{Open}$ , or $V_S = 2.2 \text{ V}$ , $V_D = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	$\mu\text{A}$	
D ON leakage current	$I_{D(ON)}$	$V_D = 0.5 \text{ V}$ , $V_S = \text{Open}$ , or $V_D = 2.2 \text{ V}$ , $V_S = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	2.7 V	-0.1	0.05	0.1 0.2	$\mu\text{A}$	
<b>Digital Control Inputs (IN1, IN2, EN)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full		1.7		$V_+$	V	
Input logic low	$V_{IL}$		Full		0		0.7	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_+ \text{ or } 0$	25°C	2.7 V		-1	0.05	1	$\mu\text{A}$
			Full						

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_D = 2 \text{ V}$ , $R_L = 300 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	1.5	5	8	ns
				Full	2.3 V to 2.7 V	1		10	
Turn-off time	$t_{OFF}$	$V_D = 2 \text{ V}$ , $R_L = 300 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	0.3	2	4.5	ns
				Full	2.3 V to 2.7 V	0.3		6	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 0.1 \text{ nF}$ ,	See <a href="#">Figure 22</a>	25°C	2.5 V			pC	
S OFF capacitance	$C_{S(OFF)}$	$V_S = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	2.5 V		4.5	pF	
D OFF capacitance	$C_{D(OFF)}$	$V_D = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	2.5 V		18.5	pF	
S ON capacitance	$C_{S(ON)}$	$V_S = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		24	pF	
D ON capacitance	$C_{D(ON)}$	$V_D = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		24	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		2	pF	
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	2.5 V		165	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	See <a href="#">Figure 19</a>	25°C	2.5 V		-48	dB	
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	See <a href="#">Figure 20</a>	25°C	2.5 V		-49	dB	
Crosstalk adjacent	$X_{TALK(ADJ)}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	See <a href="#">Figure 21</a>	25°C	2.5 V		-74	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		0.29	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	7	$\mu\text{A}$
				Full				10	

TYPICAL PERFORMANCE

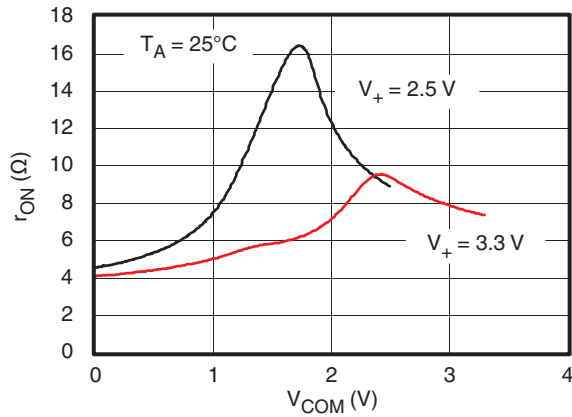


Figure 1.  $r_{on}$  vs  $V_{COM}$

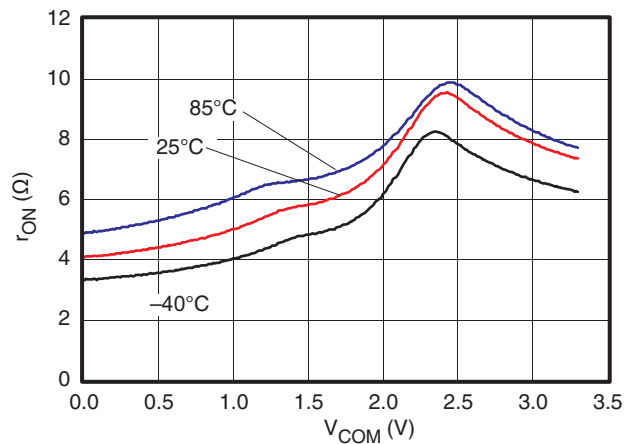


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)

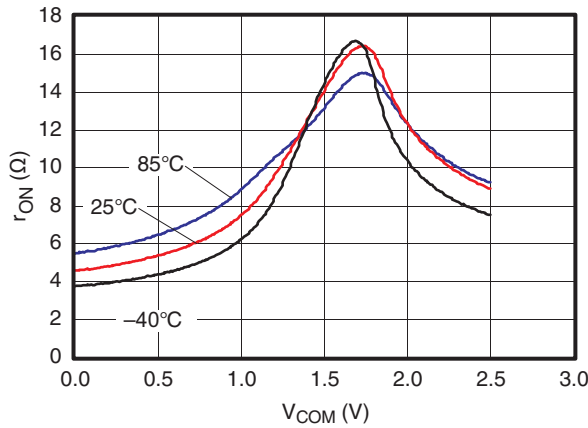


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 2.5$  V)

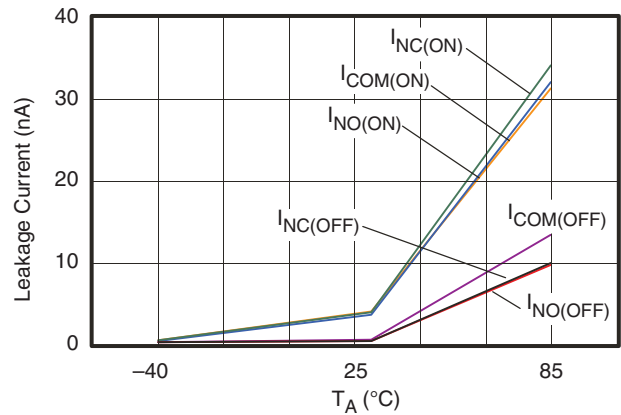


Figure 4. Leakage Current vs Temperature ( $V_+ = 3.6$  V)

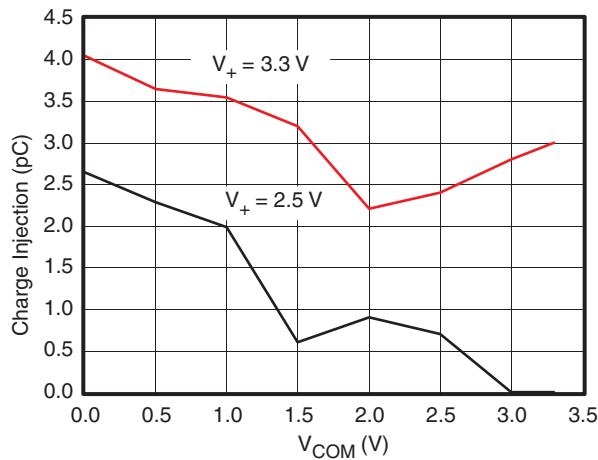


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

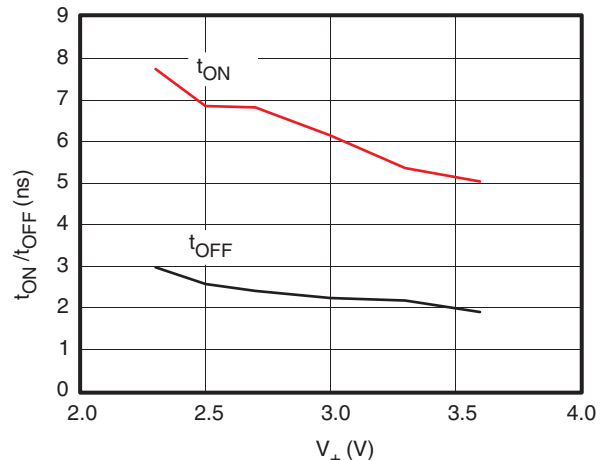


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage



TYPICAL PERFORMANCE (continued)

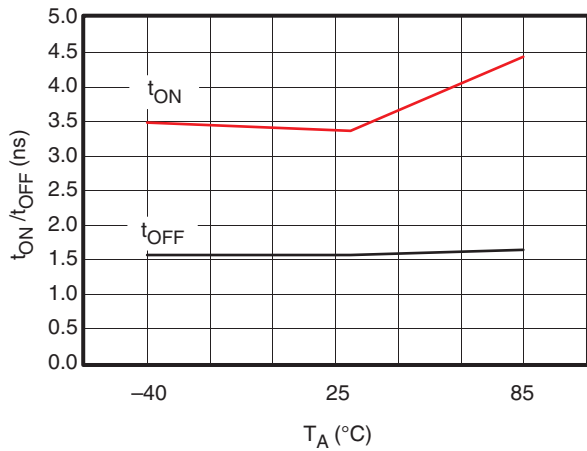


Figure 7. t<sub>ON</sub> and t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 3.3 V)

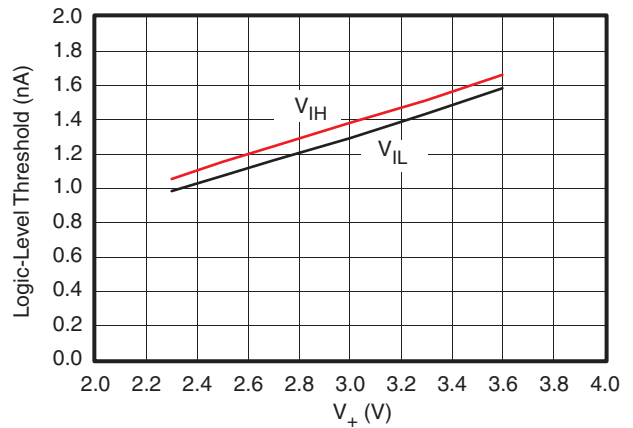


Figure 8. Logic-Level Threshold vs V<sub>+</sub>

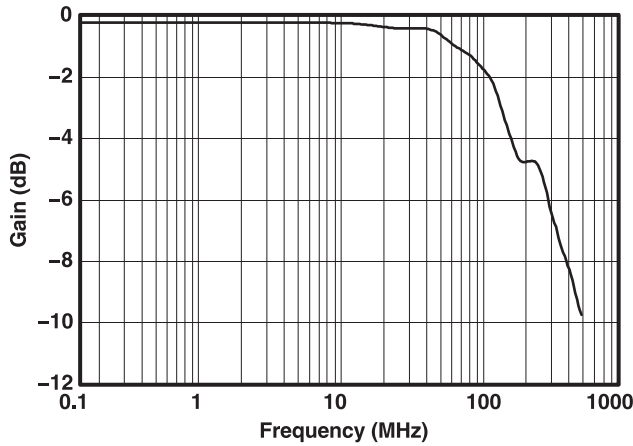


Figure 9. Bandwidth (Gain vs Frequency) (V<sub>+</sub> = 3.3 V)

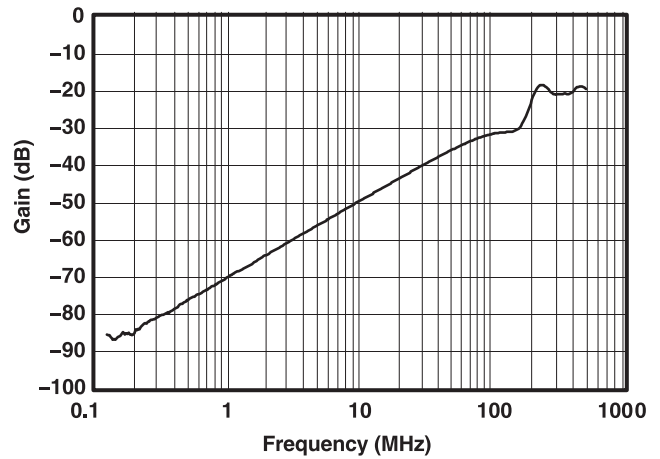


Figure 10. OFF Isolation and Crosstalk vs Frequency (V<sub>+</sub> = 3.3 V)

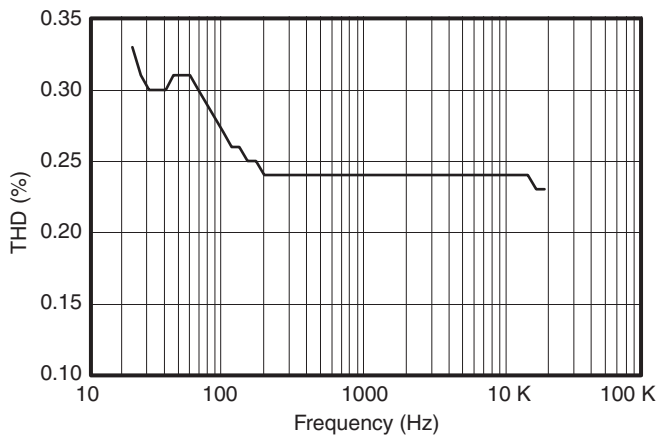


Figure 11. Total Harmonic Distortion vs Frequency

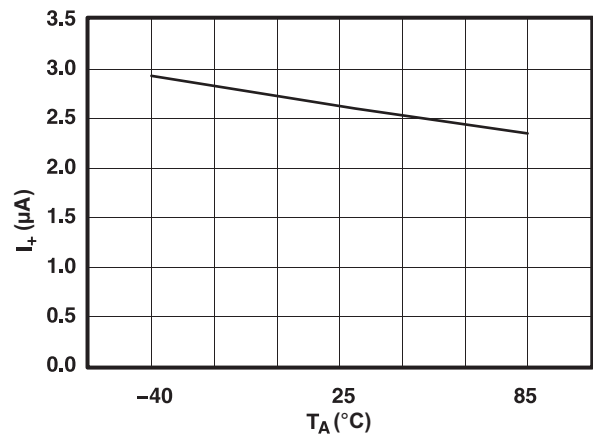


Figure 12. Power-Supply Current vs Temperature (V<sub>+</sub> = 3.6 V)

**PIN DESCRIPTION**

<b>PIN NO.</b>	<b>NAME</b>	<b>DESCRIPTION</b>
1	$1\overline{EN}$	Enable (active low)
2	IN2	Digital control to connect D to S
3	1S <sub>4</sub>	Analog I/O
4	1S <sub>3</sub>	Analog I/O
5	1S <sub>2</sub>	Analog I/O
6	1S <sub>1</sub>	Analog I/O
7	1D	Common
8	GND	Ground
9	2D	Common
10	2S <sub>1</sub>	Analog I/O
11	2S <sub>2</sub>	Analog I/O
12	2S <sub>3</sub>	Analog I/O
13	2S <sub>4</sub>	Analog I/O
14	IN1	Digital control to connect D to S
15	$2\overline{EN}$	Enable (active low)
16	V <sub>+</sub>	Power supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
$V_D$	Voltage at D
$V_{NC}$	Voltage at S
$r_{on}$	Resistance between D and S ports when the channel is ON
$\Delta r_{on}$	Difference of $r_{on}$ between channels in a specific device
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{S(OFF)}$	Leakage current measured at the S port, with the corresponding channel (S to D) in the OFF state
$I_{SPWR(OFF)}$	Leakage current measured at the S port under the powered down mode, $V_+ = 0$
$I_{S(ON)}$	Leakage current measured at the S port, with the corresponding channel (S to D) in the ON state and the output (D) open
$I_{D(OFF)}$	Leakage current measured at the D port, with the corresponding channel (D to S) in the OFF state
$I_{DPWR(OFF)}$	Leakage current measured at the D port under the powered down mode, $V_+ = 0$
$I_{D(ON)}$	Leakage current measured at the D port, with the corresponding channel (D to S) in the ON state and the output (S) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$ )
$V_{IL}$	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$ )
$V_I$	Voltage at the control input (IN, $\overline{EN}$ )
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN, $\overline{EN}$ )
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (D or S) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (D or S) signal when the switch is turning OFF.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (S or D) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_D$ , $C_L$ is the load capacitance and $\Delta V_D$ is the change in analog output voltage.
$C_{S(OFF)}$	Capacitance at the S port when the corresponding channel (S to D) is OFF
$C_{S(ON)}$	Capacitance at the S port when the corresponding channel (S to D) is ON
$C_{D(OFF)}$	Capacitance at the D port when the corresponding channel (D to S) is OFF
$C_{D(ON)}$	Capacitance at the D port when the corresponding channel (D to S) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (S to D) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (1S <sub>1</sub> to 2S <sub>1</sub> ). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

PARAMETER MEASUREMENT INFORMATION

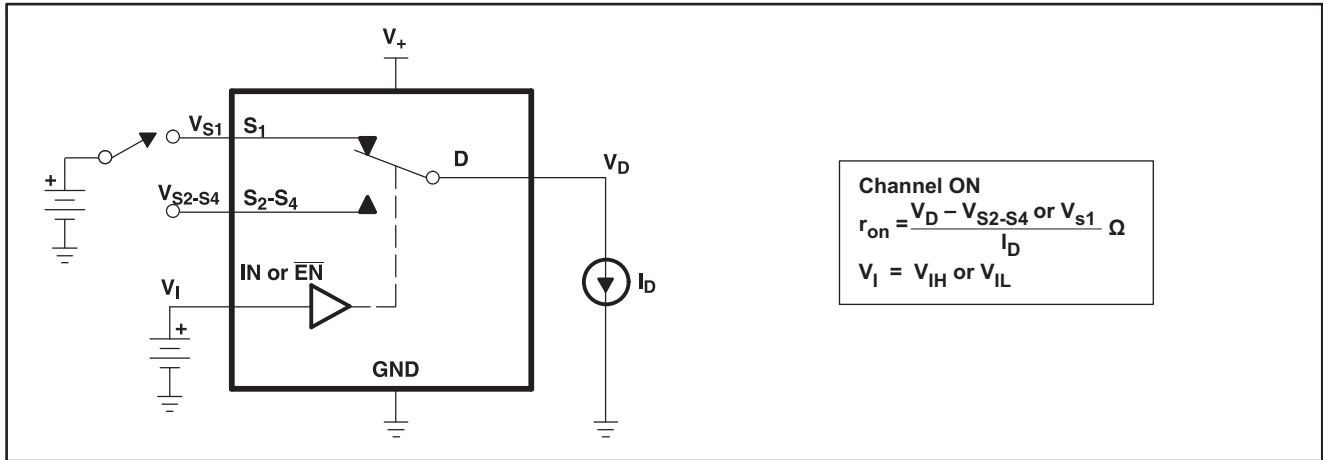


Figure 13. ON-State Resistance ( $r_{on}$ )

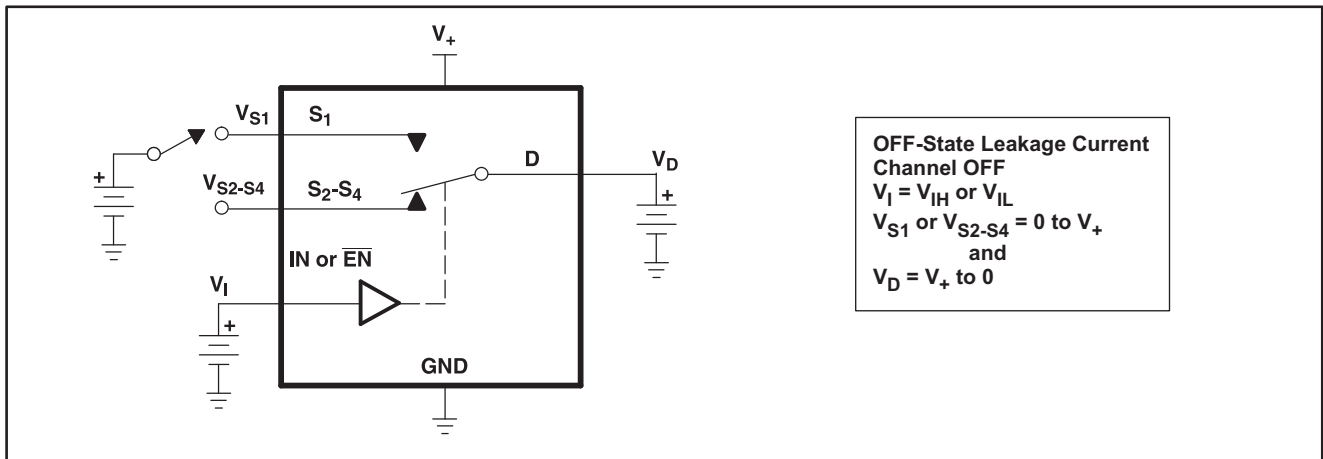


Figure 14. OFF-State Leakage Current ( $I_{D(OFF)}$ ,  $I_{S(OFF)}$ )

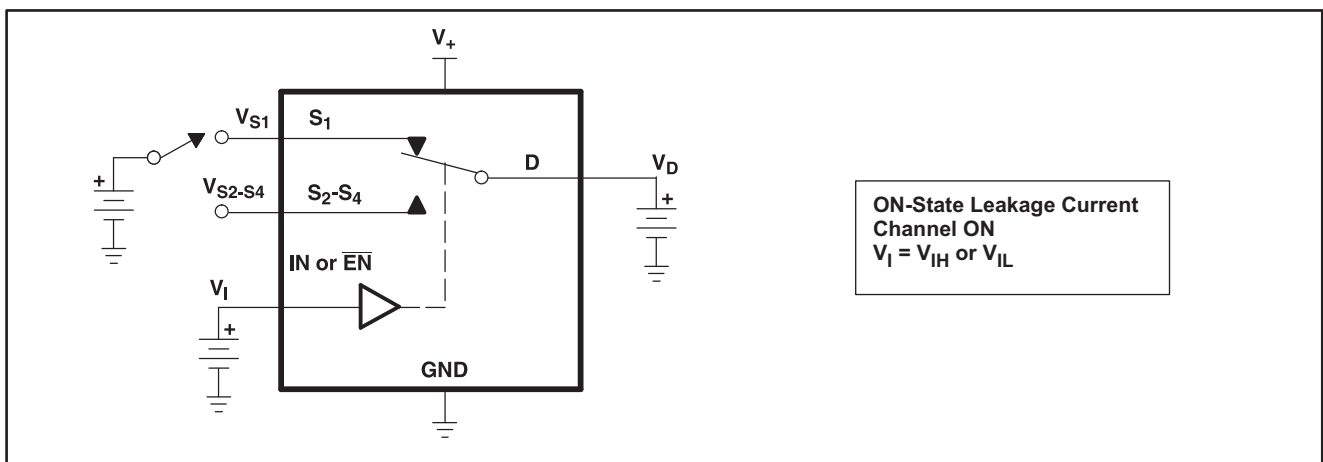


Figure 15. ON-State Leakage Current ( $I_{D(ON)}$ ,  $I_{S(ON)}$ )

PARAMETER MEASUREMENT INFORMATION (continued)

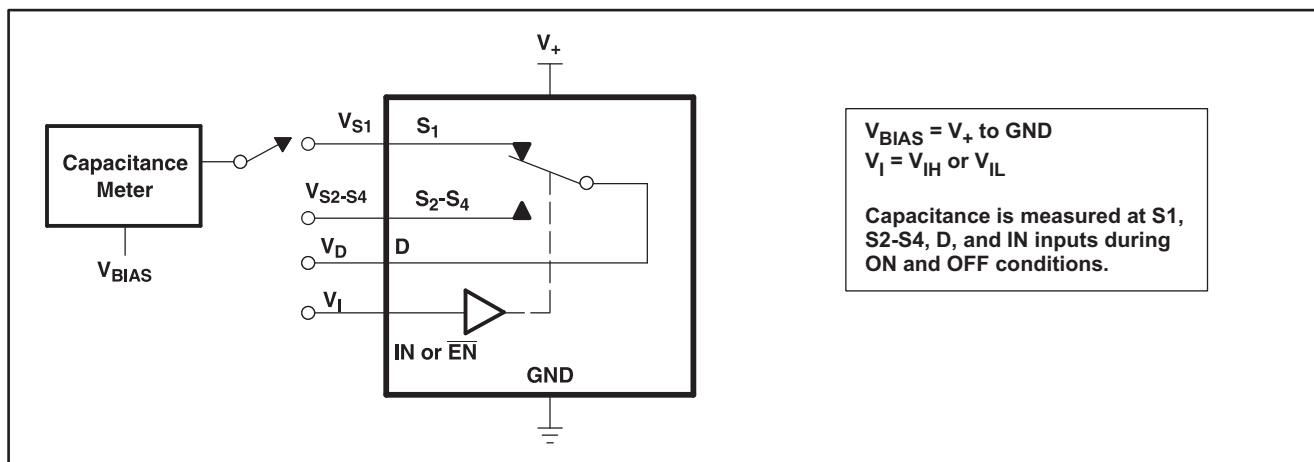
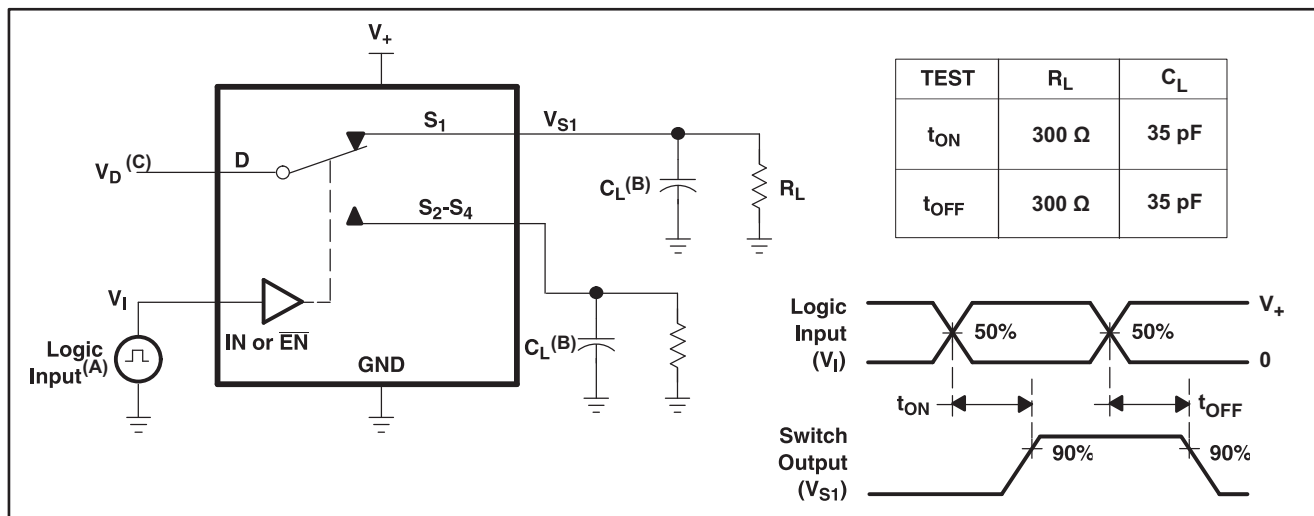


Figure 16. Capacitance ( $C_I$ ,  $C_{D(OFF)}$ ,  $C_{D(ON)}$ ,  $C_{S(OFF)}$ ,  $C_{S(ON)}$ )



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- B. C<sub>L</sub> includes probe and jig capacitance.
- C. See Electrical Characteristics for V<sub>D</sub>.

Figure 17. Turn-On (t<sub>ON</sub>) and Turn-Off Time (t<sub>OFF</sub>)

PARAMETER MEASUREMENT INFORMATION (continued)

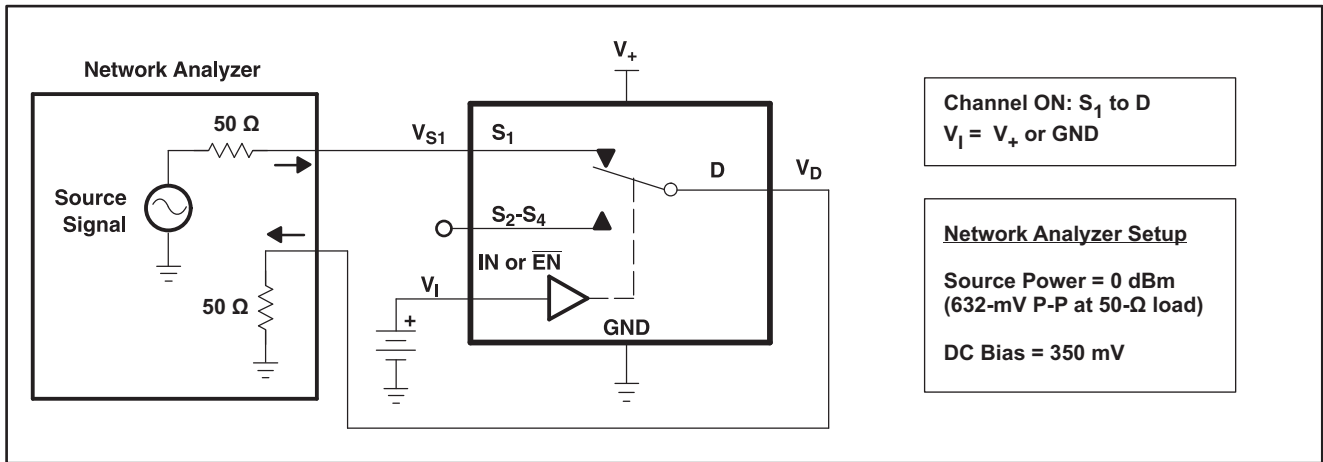


Figure 18. Bandwidth (BW)

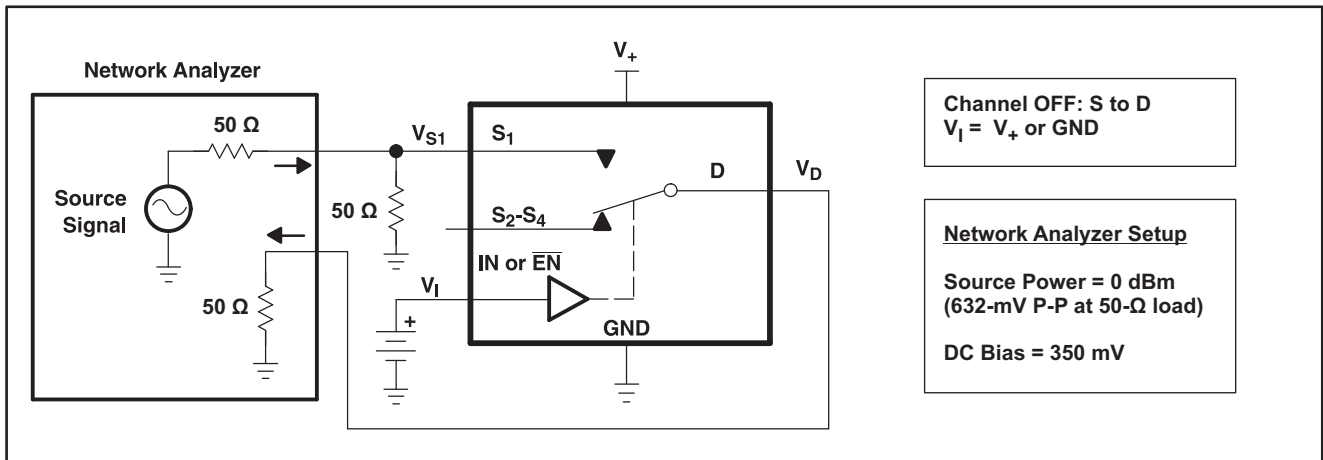


Figure 19. OFF Isolation (O<sub>ISO</sub>)

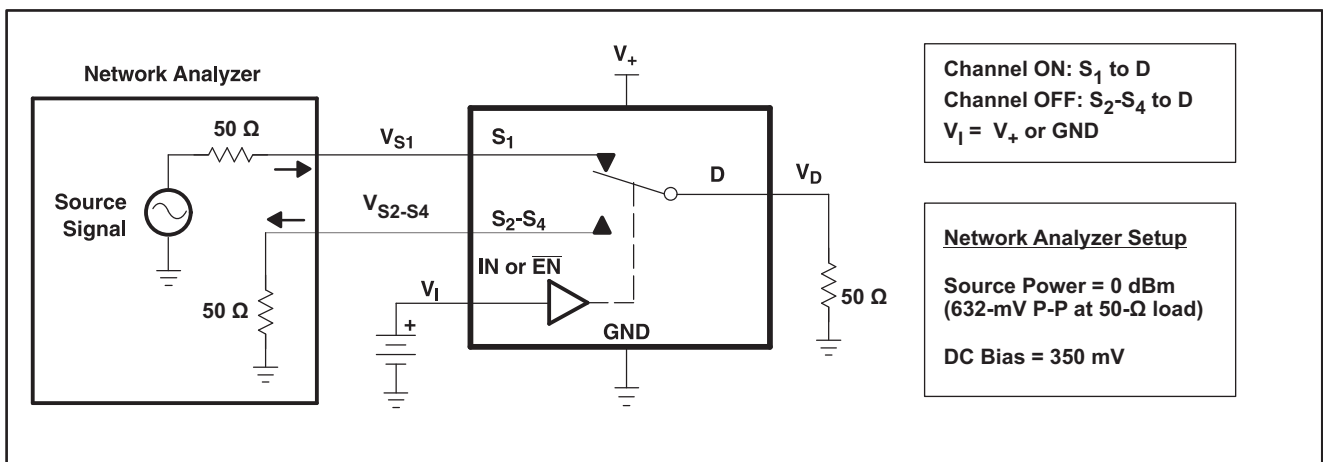


Figure 20. Crosstalk (X<sub>TALK</sub>)

PARAMETER MEASUREMENT INFORMATION (continued)

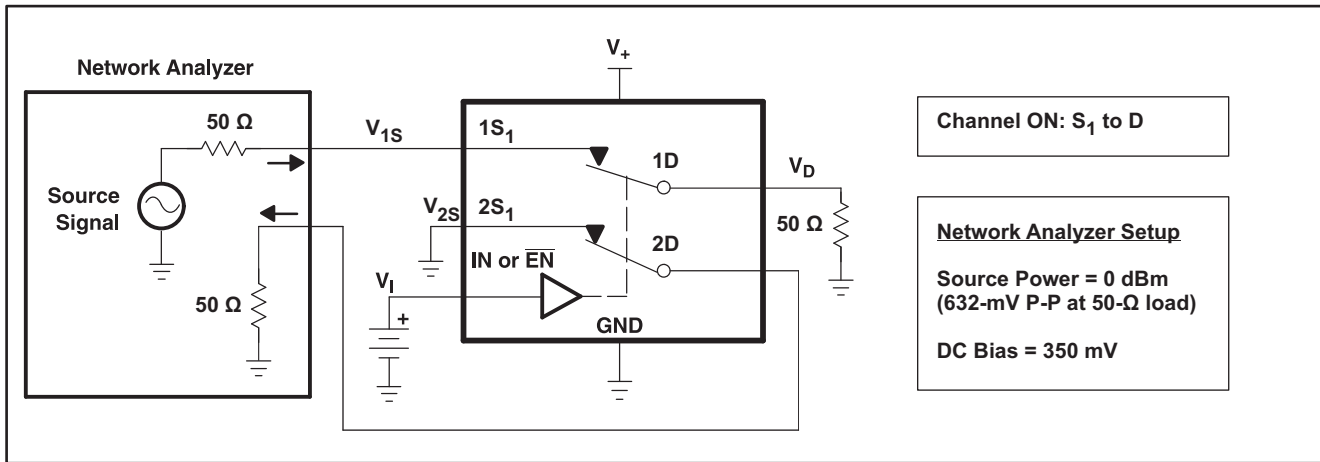
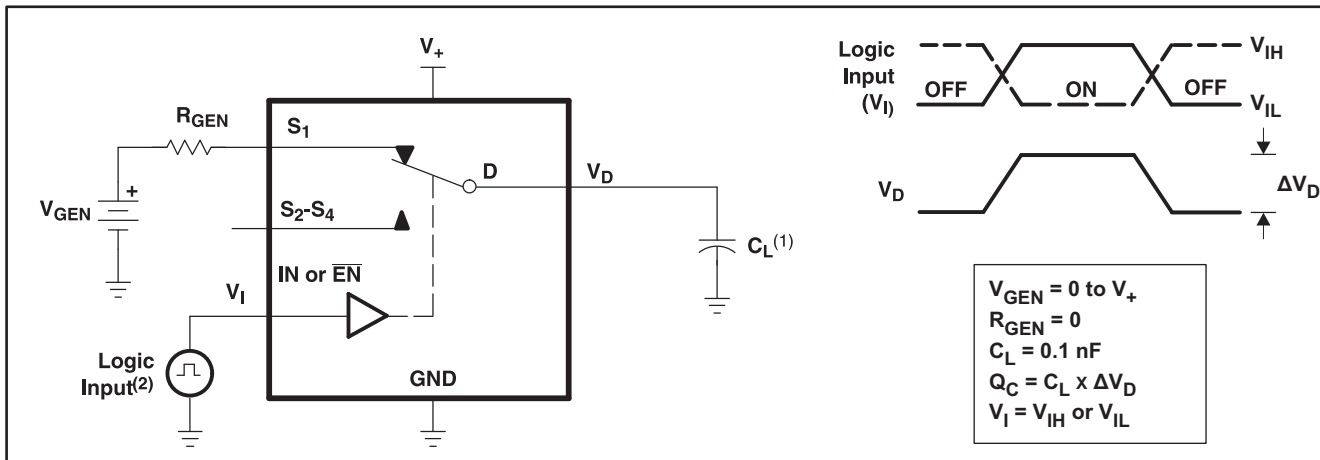


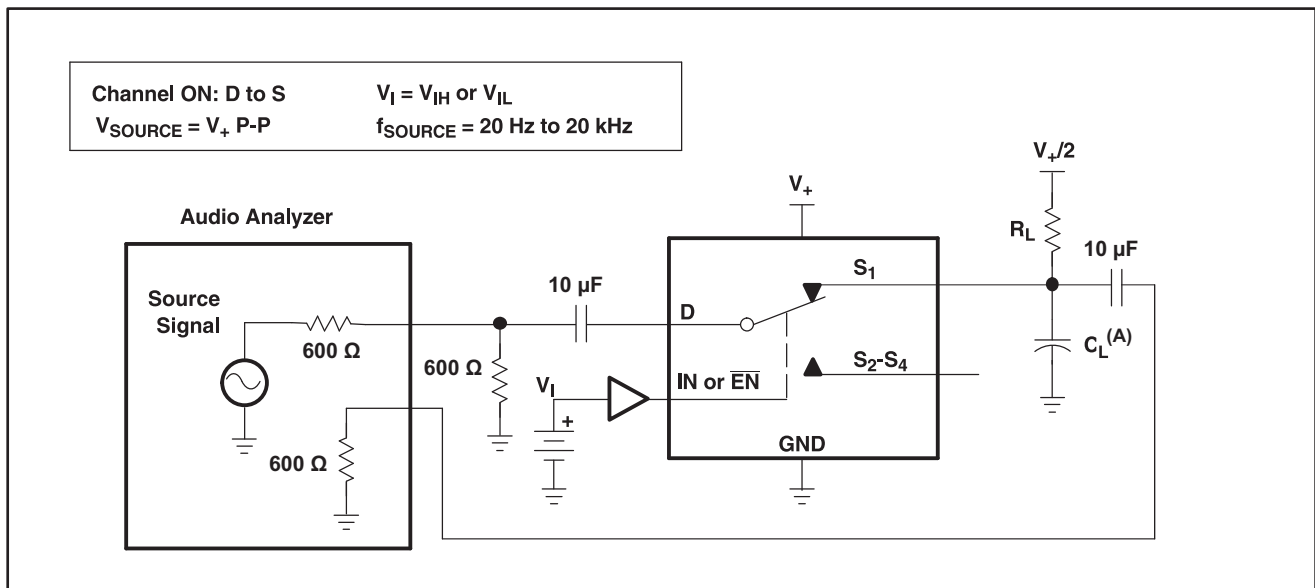
Figure 21. Adjacent Crosstalk ( $X_{TALK}$ )



- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

Figure 22. Charge Injection ( $Q_C$ )

**PARAMETER MEASUREMENT INFORMATION (continued)**






A.  $C_L$  includes probe and jig capacitance.

**Figure 23. Total Harmonic Distortion (THD)**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	<a href="#">Samples</a>
TS3A5017DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017DBQRE4	ACTIVE	SSOP	DBQ	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DBQRG4	ACTIVE	SSOP	DBQ	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017DGVRE4	ACTIVE	TVSOP	DGV	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DGVRG4	ACTIVE	TVSOP	DGV	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	<a href="#">Samples</a>
TS3A5017DRE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017PWE4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017PWRE4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TS3A5017PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	<a href="#">Samples</a>
TS3A5017RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	
TS3A5017RSV	PREVIEW	UQFN	RSV	16		TBD	Call TI	Call TI	-40 to 85		
TS3A5017RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVL	
TS3A5017RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVL	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5017DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5017PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A5017RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3A5017RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
TS3A5017DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3A5017PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TS3A5017RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
TS3A5017RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

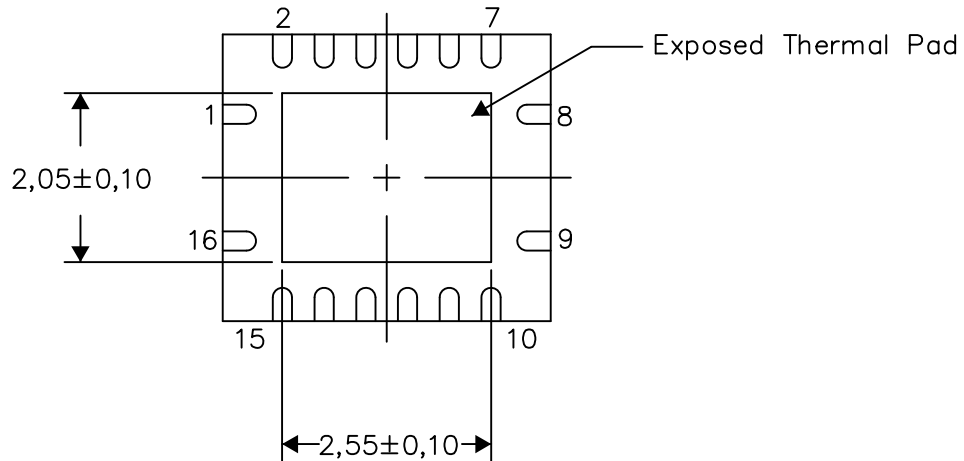
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

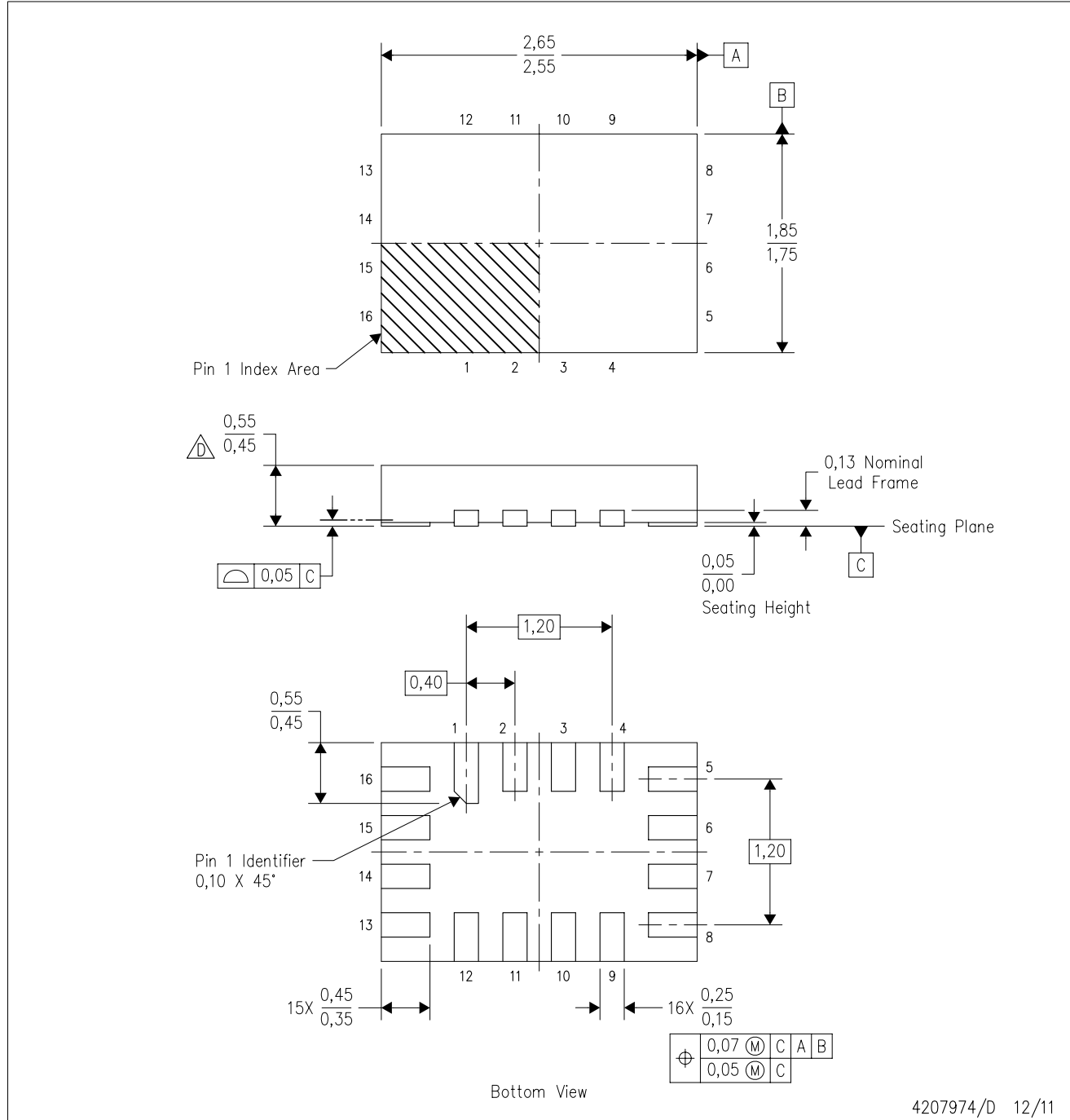
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

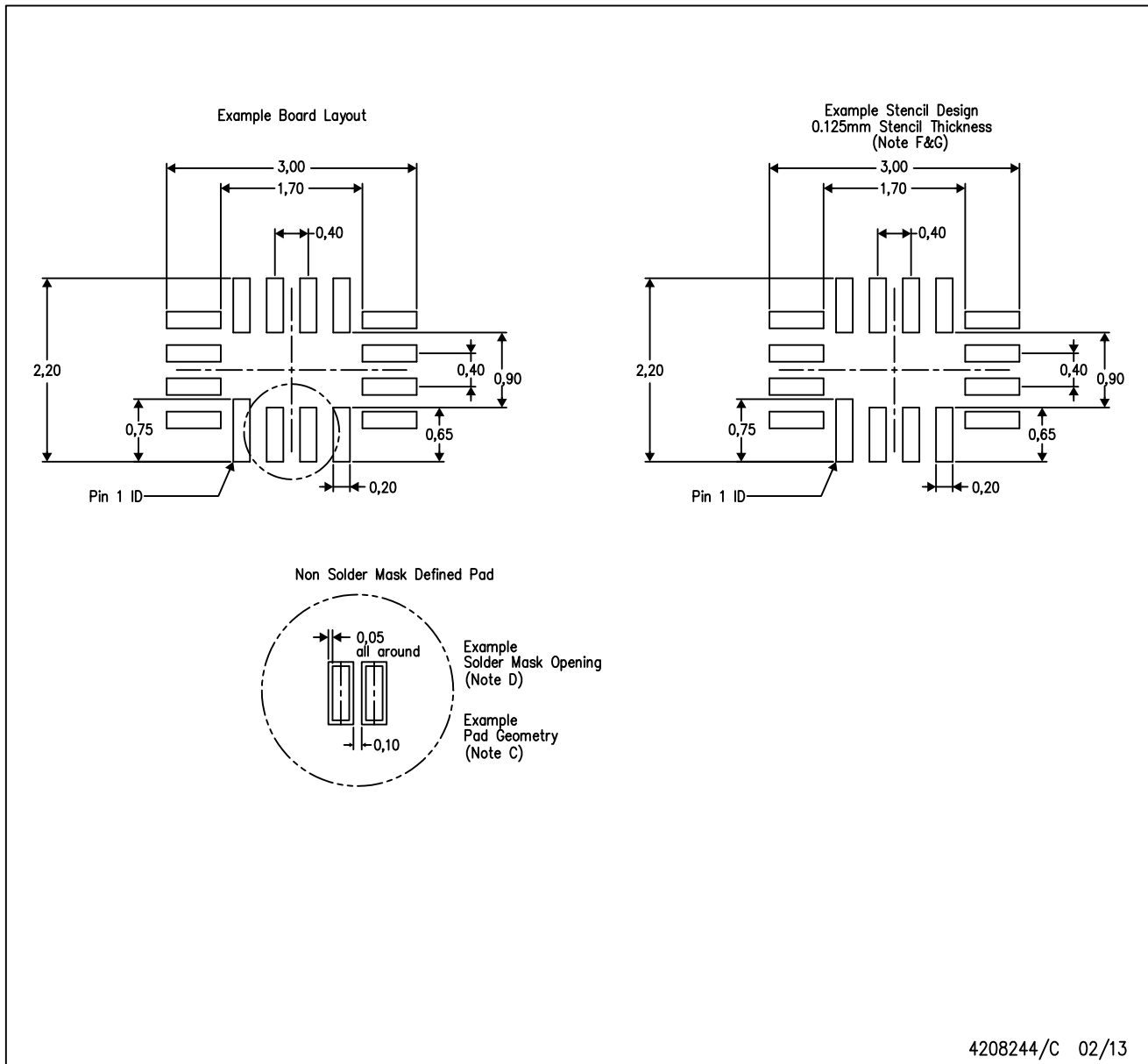


4207974/D 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

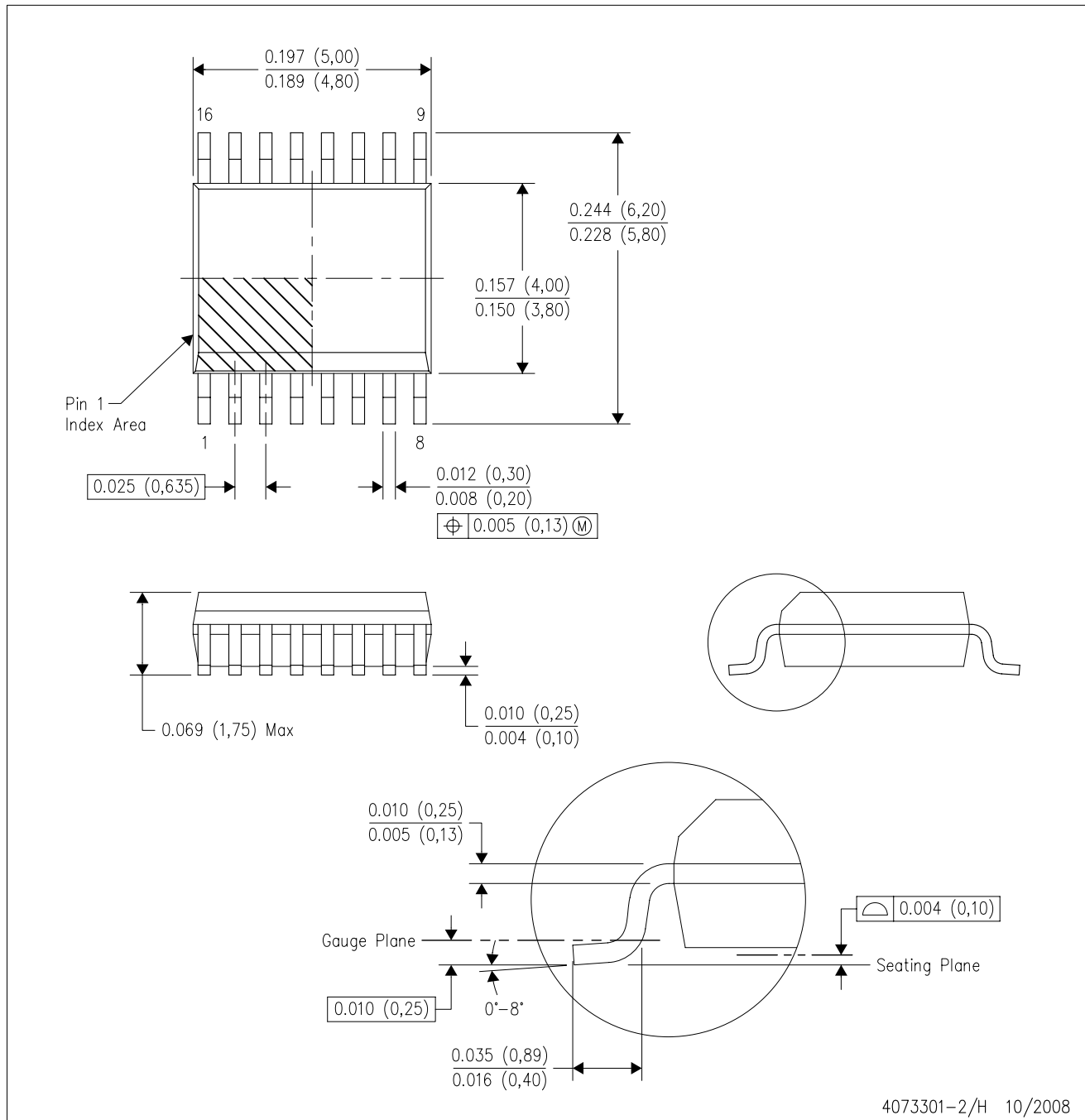


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

# MECHANICAL DATA

DBQ (R-PDSO-G16)

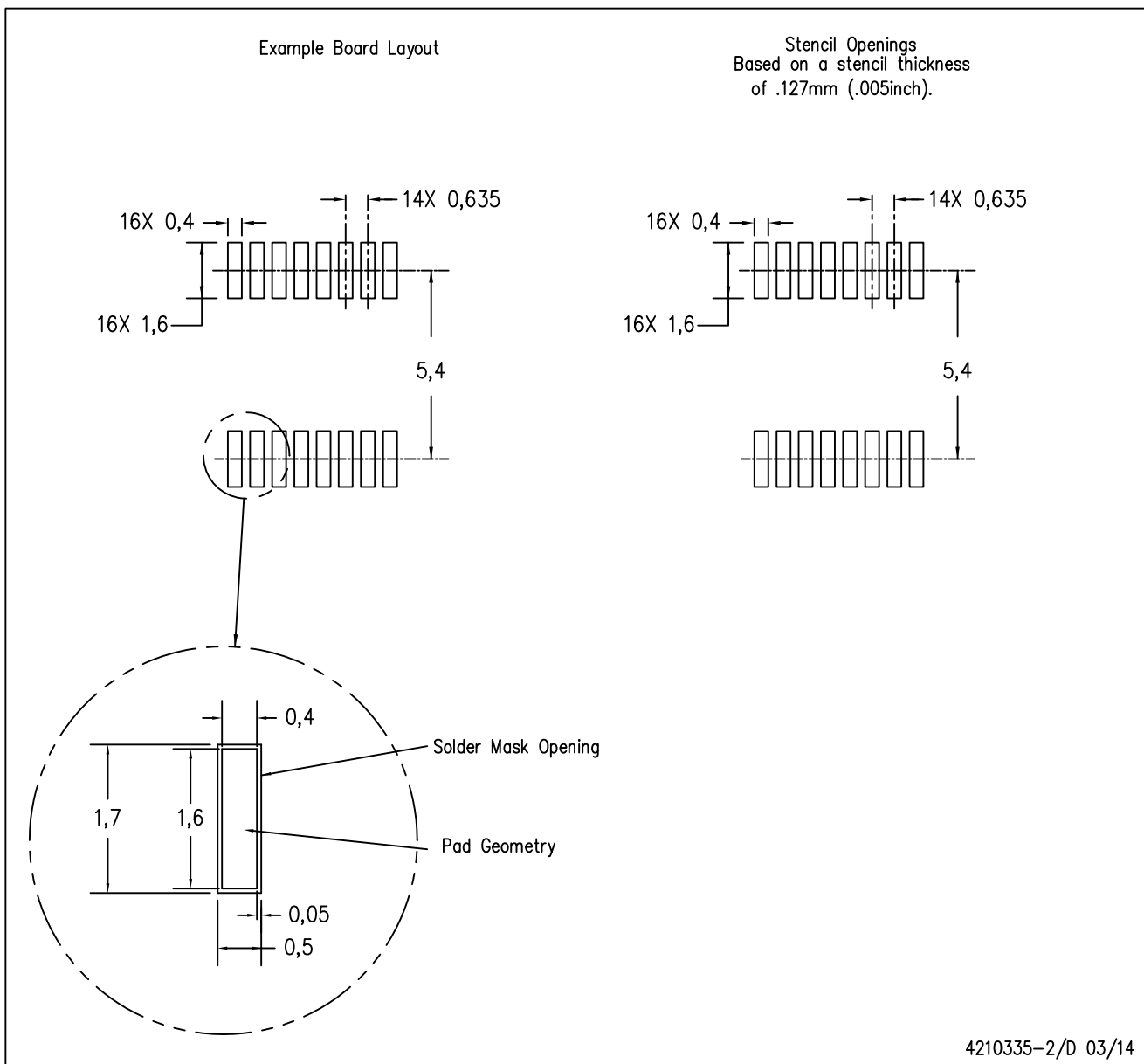
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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