# 0.9-Ω LOW-VOLTAGE SINGLE-SUPPLY QUAD SPST ANALOG SWITCH

FEATURES
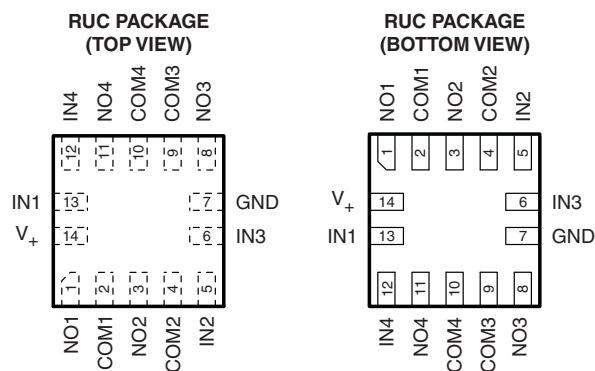
- **Low ON-State Resistance (r_{ON})**
  - **0.9 Ω Max (3-V Supply)**
  - **1.5 Ω Max (1.8-V Supply)**
- **r_{ON} Flatness: 0.4 Ω Max (3-V)**
- **r_{ON} Matching**
  - **0.05 Ω Max (3-V Supply)**
  - **0.25 Ω Max (1.8-V Supply)**
- **1.6-V to 3.6-V Single-Supply Operation**
- **1.8-V CMOS Logic Compatible (3-V Supply)**
- **High Current-Handling Capacity (100 mA Continuous)**
- **Fast Switching: t_{ON} = 14 ns, t_{OFF} = 9 ns**
- **ESD Protection Exceeds JESD-22**
  - **4000-V Human Body Model (A114-A)**
  - **300-V Machine Model (A115-A)**
  - **1000-V Charged Device Model (C101)**

APPLICATIONS

- **Power Routing**
- **Battery Powered Systems**
- **Audio and Video Signal Routing**
- **Low-Voltage Data-Acquisition Systems**
- **Communications Circuits**
- **PCMCIA Cards**
- **Cellular Phones**
- **Modems**
- **Hard Drives**

PW PACKAGE
(TOP VIEW)

RGY PACKAGE
(TOP VIEW)

RGY PACKAGE
(BOTTOM VIEW)
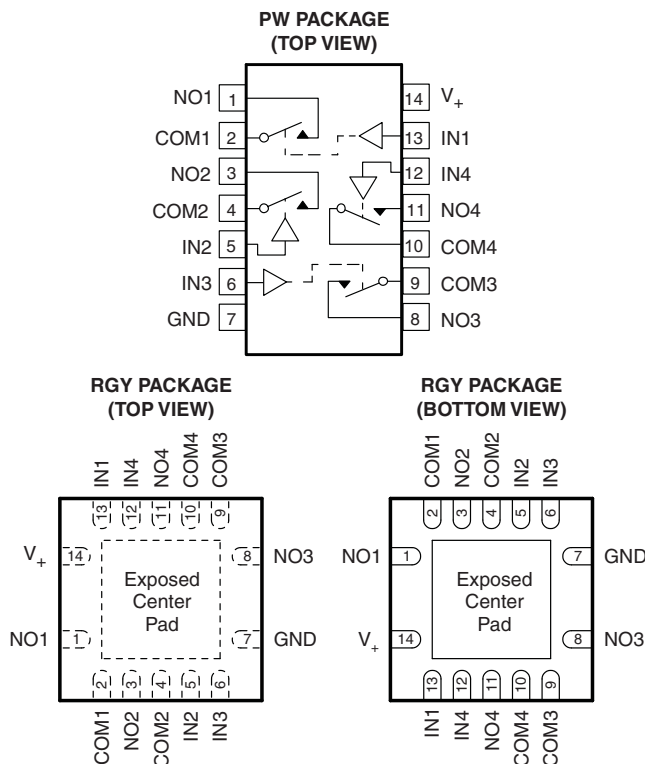
If the exposed center pad is used, it must be connected as a secondary ground or left electrically open.

RUC PACKAGE
(TOP VIEW)

RUC PACKAGE
(BOTTOM VIEW)

DESCRIPTION/ORDERING INFORMATION

The TS3A4751 is a low ON-state resistance (r_{on}), low-voltage, quad, single-pole/single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin SON (RGY) and micro QFN (RUC) packages.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SON – RGY	Reel of 2000	TS3A4751RGYR	YC751
	micro QFN – RUC	Reel of 2000	TS3A4751RUCR	3M
	TSSOP – PW	Reel of 2000	TS3A4751PWR	YC751

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range referenced to GND[2]		−0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range		−0.3	$V_+ + 0.3$	V
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	−100	100	mA
I_+ I_{GND}	Continuous current through V_+ or GND			±100	mA
	Peak current pulsed at 1 ms, 10% duty cycle	COM, $V_{I/O}$		±200	mA
T_A	Operating temperature range		−40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

PACKAGE THERMAL IMPEDANCE

				UNIT
θ_{JA}	Package thermal impedance[1]	PW package	88	°C/W
		RGY package	91.6	
		RUC package	216.7	

(1) The package thermal impedance is measured in accordance with JESD 51-7.

Product Folder Link(s): *TS3A4751*

ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY[(1)(2)]

V_+ = 2.7 V to 3.6 V, T_A = −40°C to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted).

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP[(3)]	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 2.7 V, I_{COM} = −100 mA, V_{NO} = 1.5 V		25°C		0.7	0.9	Ω
				Full			1.1	
ON-state resistance match between channels[(4)]	Δr_{on}	V_+ = 2.7 V, I_{COM} = −100 mA, V_{NO} = 1.5 V		25°C		0.03	0.05	Ω
				Full			0.15	
ON-state resistance flatness[(5)]	$r_{on(flat)}$	V_+ = 2.7 V, I_{COM} = −100 mA, V_{NO} = 1 V, 1.5 V, 2 V		25°C		0.23	0.4	Ω
				Full			0.5	
NO OFF leakage current[(6)]	$I_{NO(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	−2	1	2	nA
				Full	−18		18	
COM OFF leakage current[(6)]	$I_{COM(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	−2	1	2	nA
				Full	−18		18	
COM ON leakage current[(6)]	$I_{COM(ON)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 0.3 V, 3 V, or floating		25°C	−2.5	0.01	2.5	nA
				Full	−5		5	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	14	ns
				Full			15	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		4	9	ns
				Full			10	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		125		MHz
OFF isolation[(7)]	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		−40		dB
			f = 1 MHz			−62		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		−73		dB
			f = 1 MHz			−95		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.04		%
			R_L = 600 Ω			0.003		
Digital Control Inputs (IN1–IN4)								
Input logic high	V_{IH}			Full	1.4			V
Input logic low	V_{IL}			Full			0.5	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.5	1	nA
				Full	−20		20	
Supply								
Power-supply range	V_+				1.6		3.6	V
Positive-supply current	I_+	V_+ = 3.6 V, V_{IN} = 0 or V_+		25°C			0.075	μA
				Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at V_+ = 3 V, T_A = 25°C.
(4) Δr_{on} = $r_{on(max)}$ − $r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY[1][2]

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C, V_{IH} = 1 V, V_{IL} = 0.4 V (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP[3]	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 1.8 V, I_{COM} = −10 mA, V_{NO} = 0.9 V		25°C		1	1.5	Ω
				Full			2	
ON-state resistance match between channels[4]	Δr_{on}	V_+ = 1.8 V, I_{COM} = −10 mA, V_{NO} = 0.9 V		25°C		0.09	0.15	Ω
				Full			0.25	
ON-state resistance flatness[5]	$r_{on(flat)}$	V_+ = 1.8 V, I_{COM} = −10 mA, $0 \leq V_{NO} \leq V_+$		25°C		0.7	0.9	Ω
				Full			1.5	
NO OFF leakage current[6]	$I_{NO(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10		10	
COM OFF leakage current[6]	$I_{COM(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.65 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10		10	
COM ON leakage current[6]	$I_{COM(ON)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 0.15 V, 1.65 V, or floating		25°C	−1	0.01	1	nA
				Full	−3		3	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		6	18	ns
				Full			20	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	10	ns
				Full			12	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3.2		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		123		MHz
OFF isolation[7]	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		−61		dB
			f = 100 MHz			−36		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		−95		dB
			f = 100 MHz			−73		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.14		%
			R_L = 600 Ω			0.013		
Digital Control Inputs (IN1–IN4)								
Input logic high	V_{IH}			Full	1			V
Input logic low	V_{IL}			Full			0.4	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.1	5	nA
				Full	−10		10	
Supply								
Power-supply range	V_+				1.6		3.6	V
Positive-supply current	I_+	V_I = 0 or V_+		25°C		0.05		μA
				Full			0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at T_A = 25°C.
(4) Δr_{on} = $r_{on(max)}$ − $r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = 20$_{log}$10 (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

Product Folder Link(s): *TS3A4751*
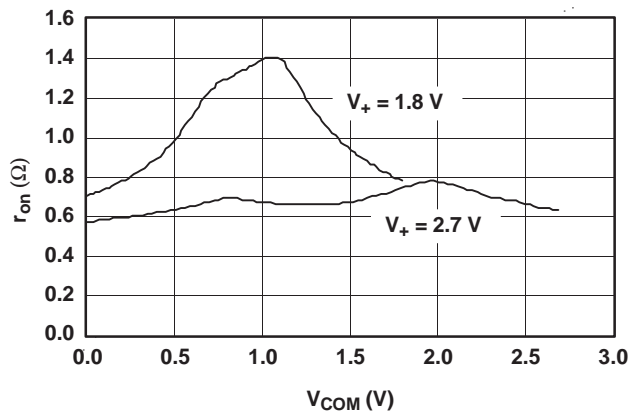
TYPICAL PERFORMANCE
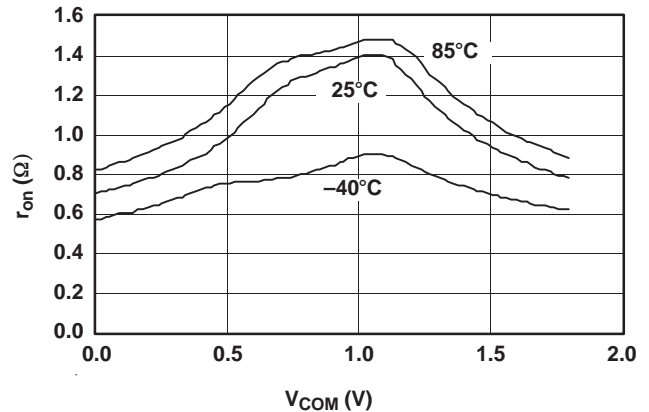

Figure 1. r_{on} vs V_{COM}

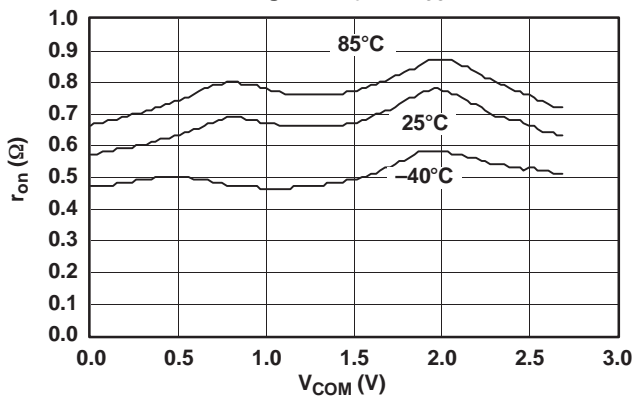Figure 2. r_{on} vs V_{COM} (V_+ = 1.8 V)

Figure 3. r_{on} vs V_{COM} (V_+ = 2.7 V)
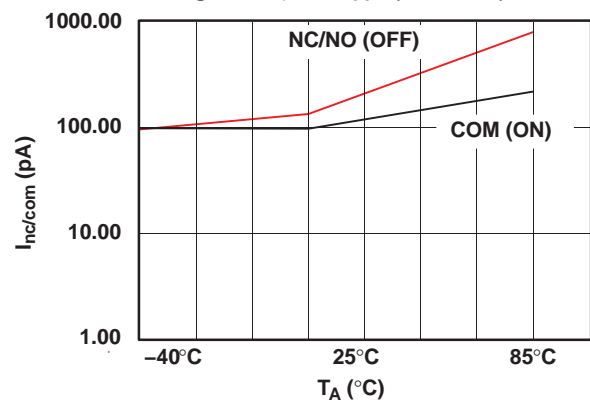

Figure 4. I_{ON} and I_{OFF} vs Temperature (V_+ = 3.6 V)
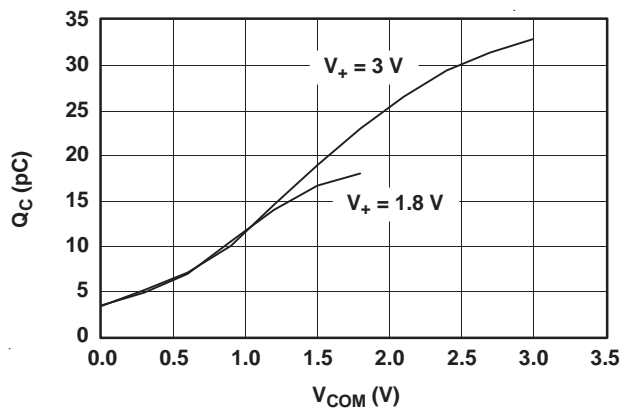

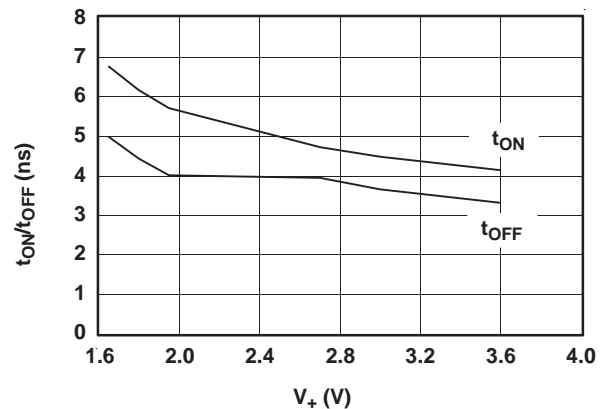Figure 5. Q_C vs V_{COM}

Figure 6. t_{ON} and t_{OFF} vs Supply Voltage
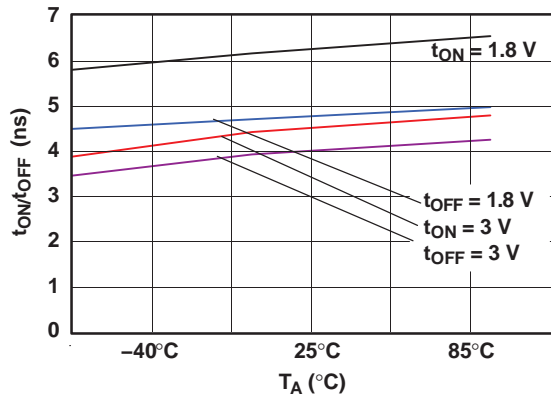
TYPICAL PERFORMANCE (continued)
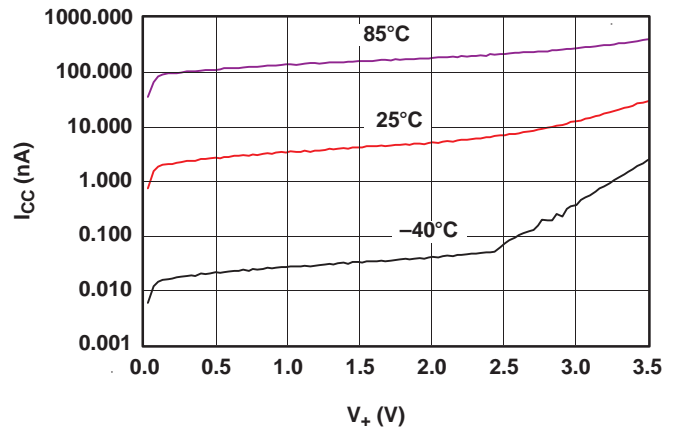
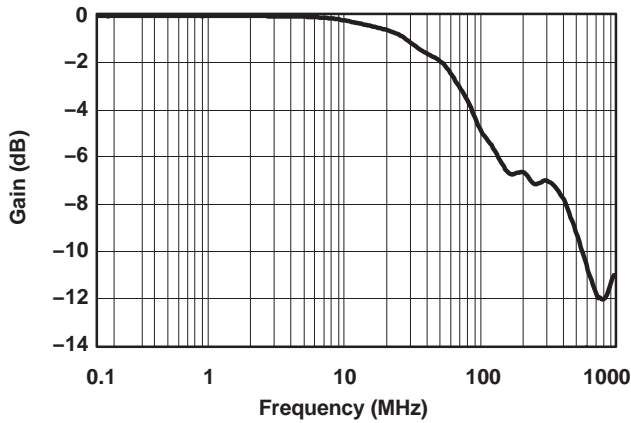Figure 7. t_{ON} and t_{OFF} vs Temperature

Figure 8. I_{CC} vs V_+

Figure 9. Gain vs Frequency
(V_+ = 3 V)
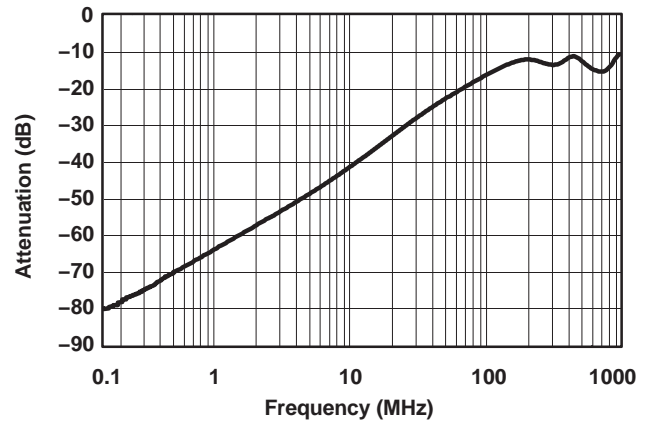
Figure 10. OFF Isolation vs Frequency
(V_+ = 3 V)
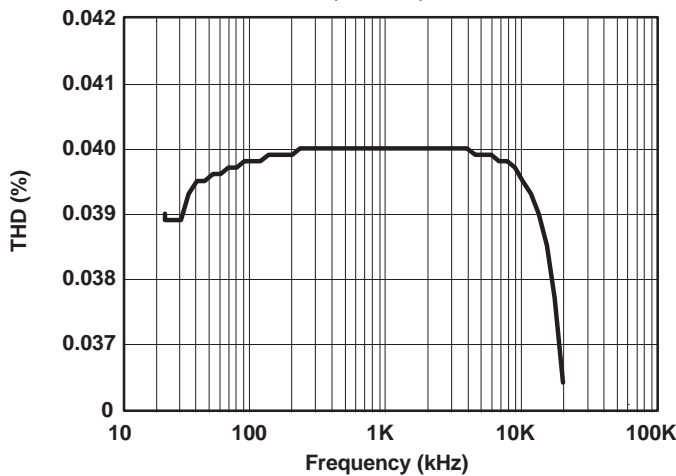
Figure 11. Total Harmonic Distortion vs Frequency
(R_L = 32 Ω)
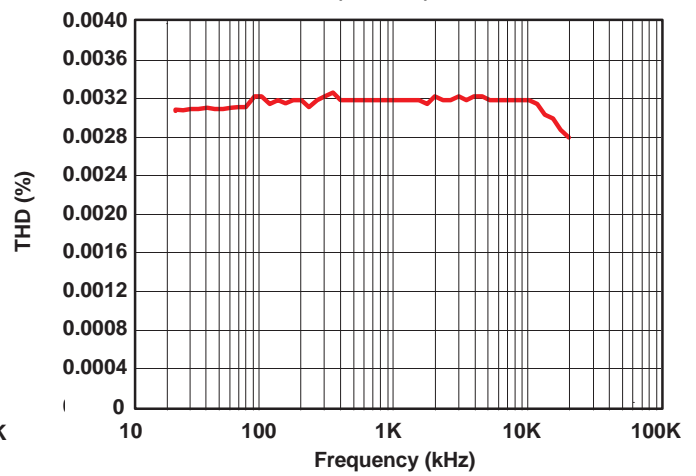
Figure 12. Total Harmonic Distortion vs Frequency
(R_L = 600 Ω)

Product Folder Link(s): *TS3A4751*

TYPICAL PERFORMANCE (continued)
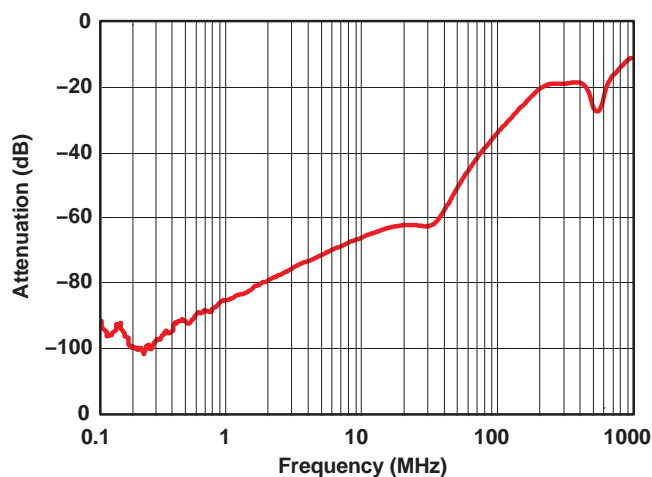
Figure 13. Crosstalk vs Frequency (V_+ = 3 V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1, 3, 8, 11	NO1, NO2, NO3, NO4	Normally open
2, 4, 9, 10	COM1, COM2, COM3, COM4	Common
7	GND	Ground
13, 5, 6, 12	IN1, IN2, IN3, IN4	Logic control inputs
14	V_+	Positive supply voltage

APPLICATION INFORMATION

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1-µF capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in r_{on} (see Typical Operating Characteristics). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Product Folder Link(s): *TS3A4751*

TEST CIRCUITS/TIMING DIAGRAMS
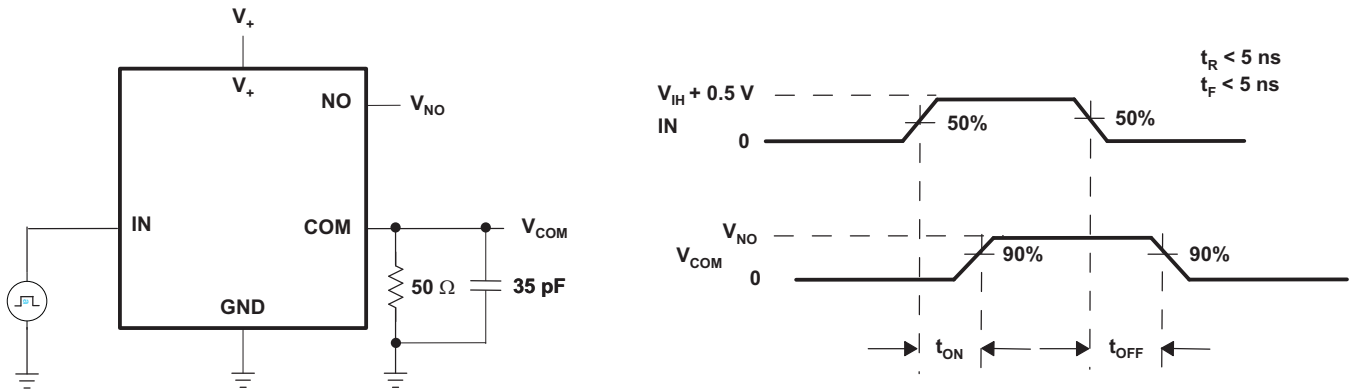
Figure 14. Switching Times
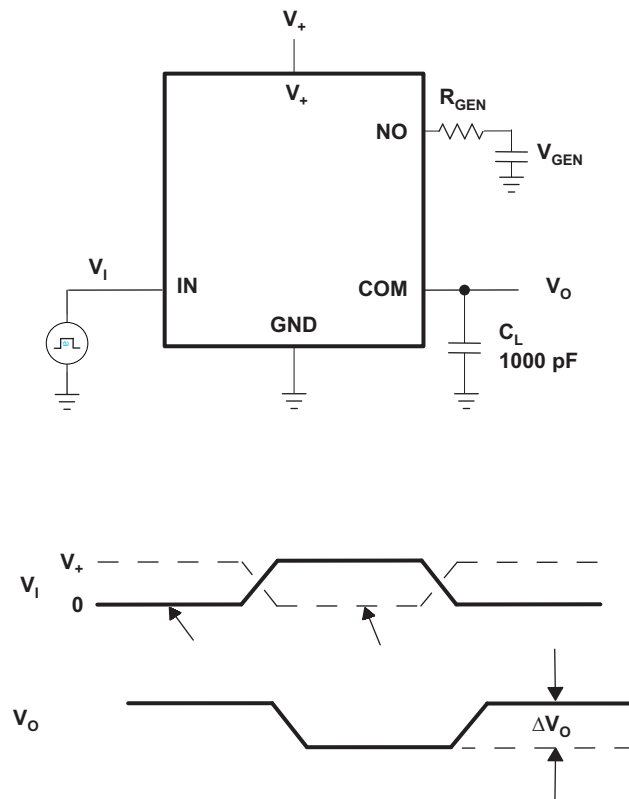
Figure 15. Charge Injection (Q_C)

Product Folder Link(s): TS3A4751
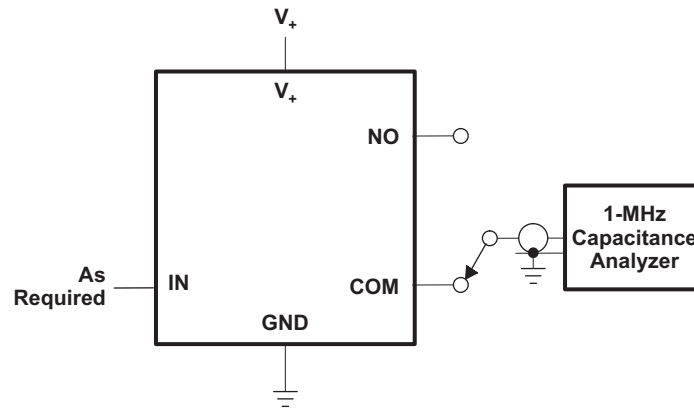
Figure 16. NO and COM Capacitance
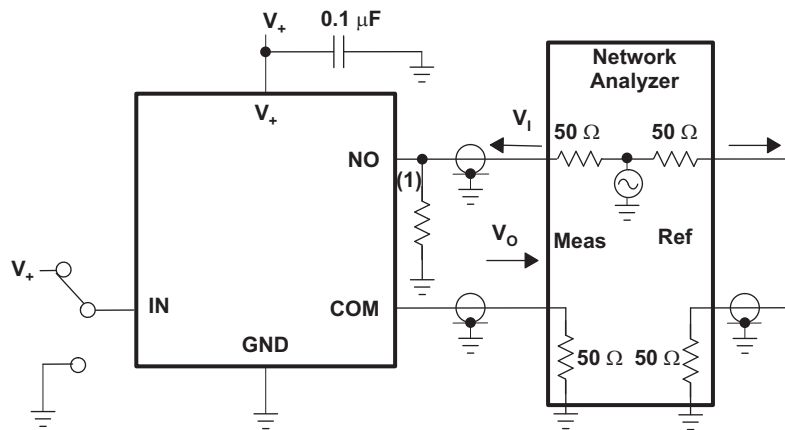
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

OFF isolation = 20 log V_O/V_I

[1]Add 50-Ω termination for OFF isolation

Figure 17. OFF Isolation, Bandwidth, and Crosstalk

Product Folder Link(s): *TS3A4751*
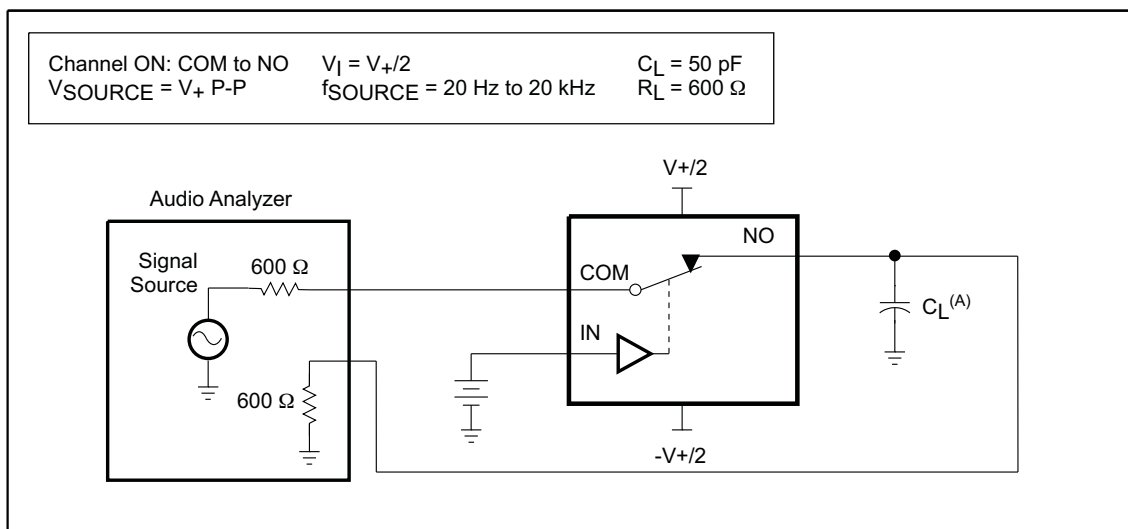
A. C_L includes probe and jig capacitance.

Figure 18. Total Harmonic Distortion (THD)

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS3A4751PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A4751PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A4751RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A4751RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A4751RUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
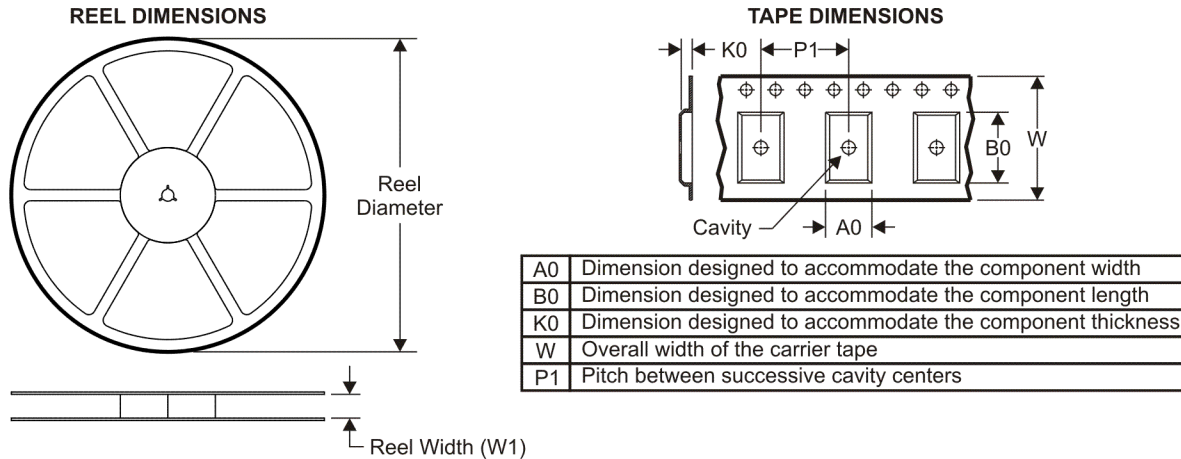
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

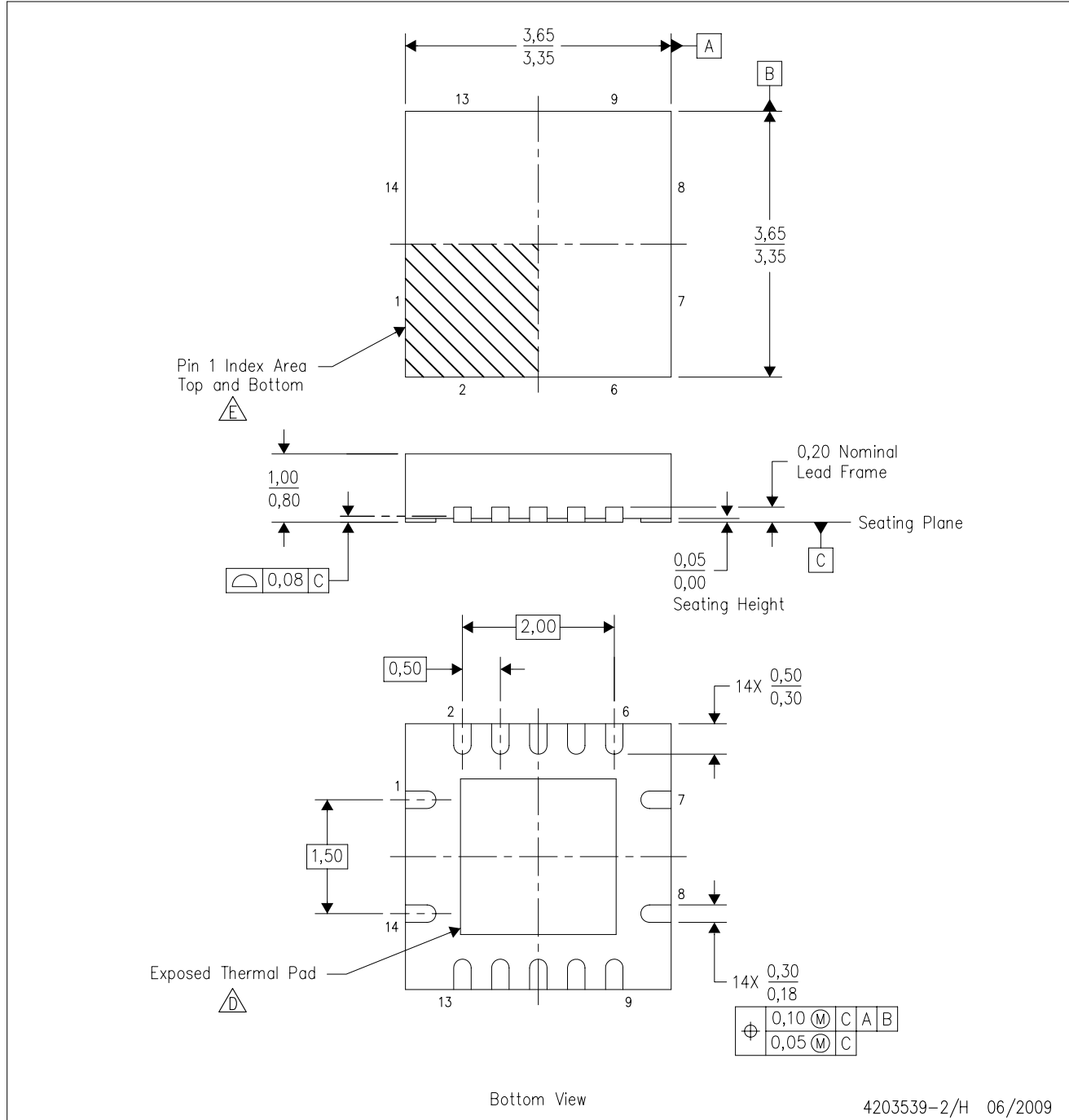| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TS3A4751RGYR	VQFN	RGY	14	3000	346.0	346.0	29.0

RGY (S−PVQFN−N14) PLASTIC QUAD FLATPACK NO−LEAD

3,65 / 3,35 A

B

13   9

14   8

3,65 / 3,35

1   7

2   6

Pin 1 Index Area
Top and Bottom
E

0,20 Nominal
Lead Frame

1,00 / 0,80

Seating Plane

0,08 C

0,05 / 0,00
Seating Height

C

2,00

0,50

14X 0,50 / 0,30

2   6

1   7

1,50

8

14

Exposed Thermal Pad
D

13   9

14X 0,30 / 0,18

⊕ 0,10 Ⓜ C A B
0,05 Ⓜ C

Bottom View

4203539−2/H 06/2009

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
            See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
        E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
            The Pin 1 identifiers are either a molded, marked, or metal feature.
        F. Package complies to JEDEC MO−241 variation BA.

TEXAS
INSTRUMENTS
www.ti.com

RGY (S−PVQFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View
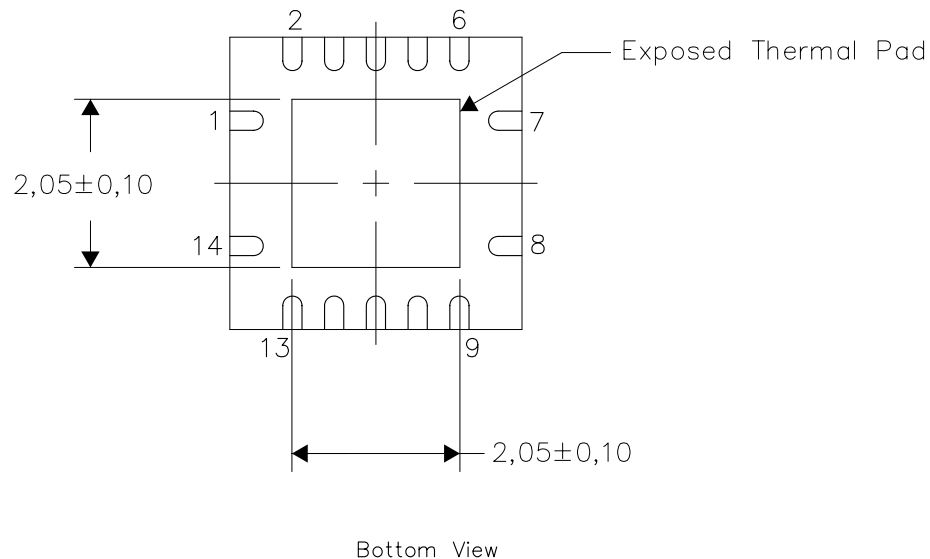
NOTES: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353−2/L 08/10

Texas
Instruments
www.ti.com

RGY (S–PVQFN–N14)   PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

4,30

4,30
2,60
1,50
2,05
2,05

Note D

8x0,50   0.28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25

4,25
2,65
1,50

0,82 SQ

0,30

0,80 x 14 PL.

8x0,50   0,23 x 14 PL.

64% solder coverage by printed
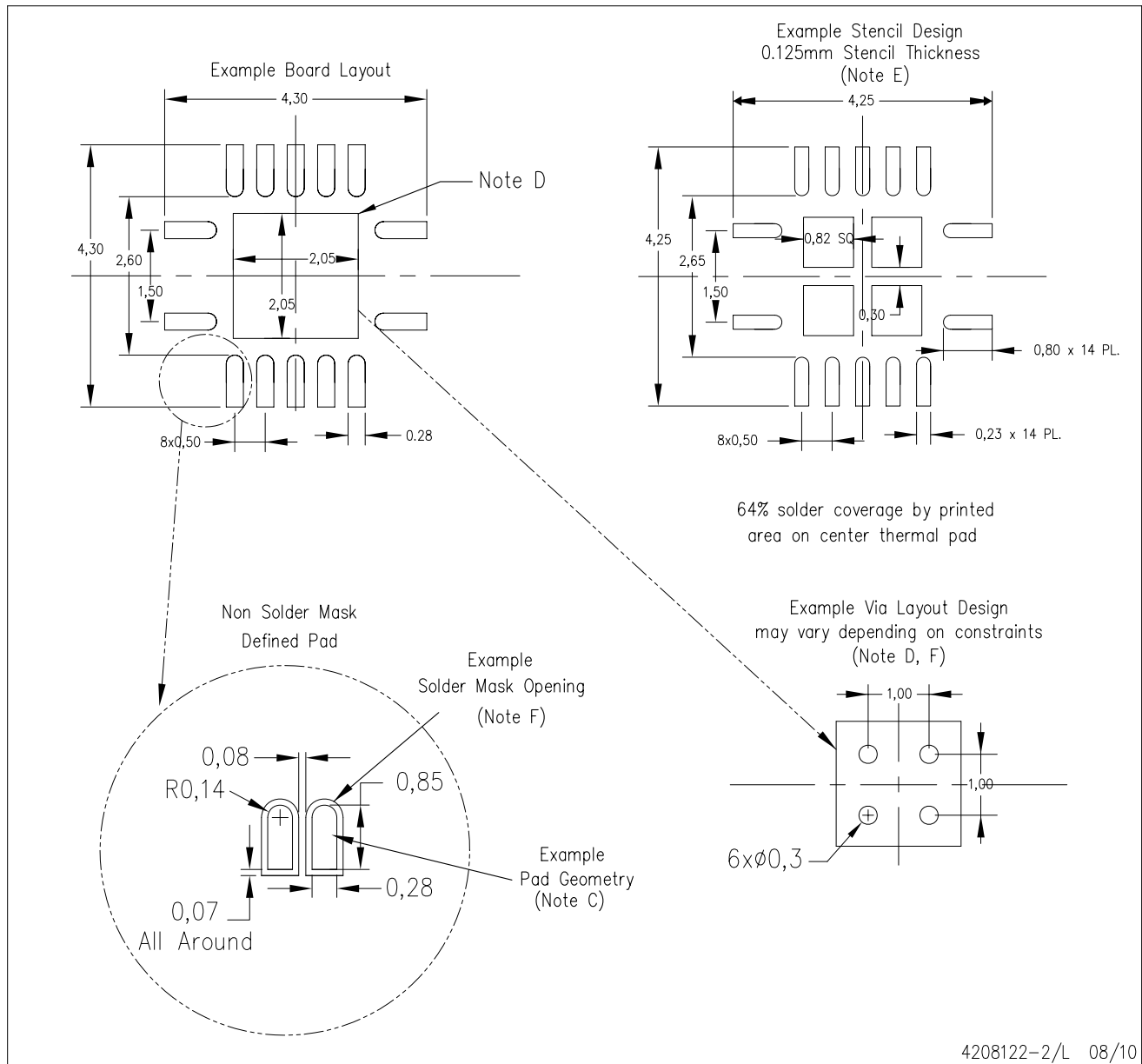area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14   0,85

0,07   0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6x⌀0,3

4208122–2/L 08/10

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

Texas
Instruments
www.ti.com

RUC (S−PX2QFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{2,05}{1,95}$

A

B

12 11 10   9   8

13   7

14   6

$\frac{2,05}{1,95}$

1   2   3   4   5

Pin 1 Index Area

$\frac{0,40}{0,34}$

⌒ 0,05 C

$\frac{0,05}{0,00}$
Seating Height

Seating Plane

C

1,60

1   2   3   4   5

14X $\frac{0,45}{0,35}$

Pin 1 Identifier
0,10 X 45°

14

13

6

7

0,40

0,20

12 11 10   9   8

14X $\frac{0,25}{0,15}$

⊕	0,07 Ⓜ	C	A	B
	0,05 Ⓜ	C		
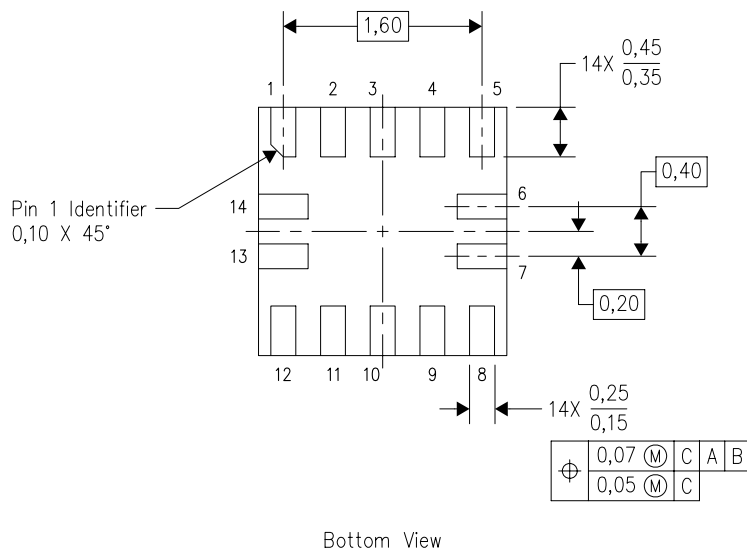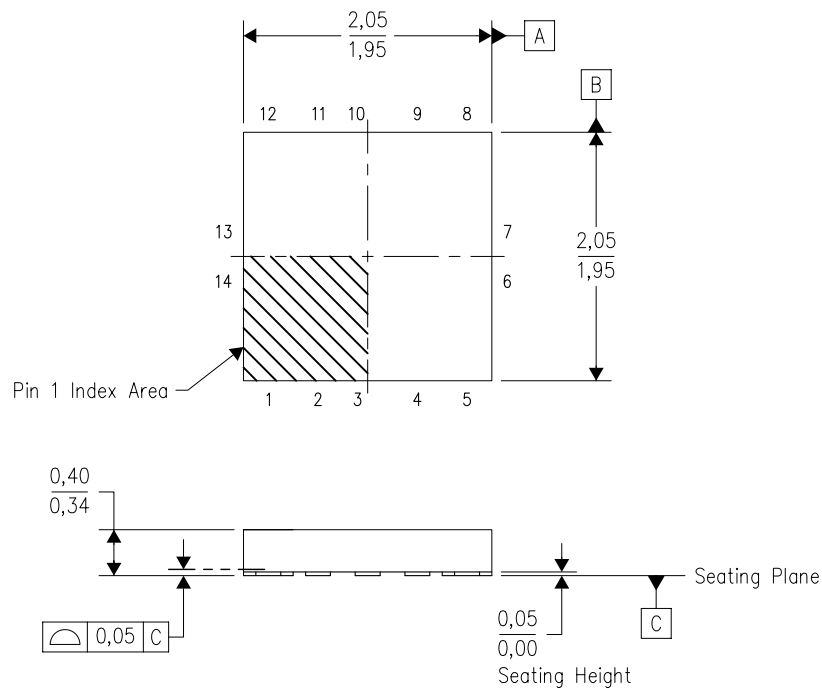
Bottom View

4208447/C   08/2008

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−lead) package configuration.
         D.   This package complies to JEDEC MO−288 variation X2GFE.

RUC (S−PX2QFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout   Example Stencil Design
                                              (Note E)

1,60   1,60

0,68 14X   0,68 14X

0,20 14X   0,20 14X

2,45   1,10   0,40 10X   2,45   1,10   0,40 10X

1,10   1,10

2,45   2,45

0,05 Solder Mask Clearance for all pads   Note D

0,05

4211124/A 06/10

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
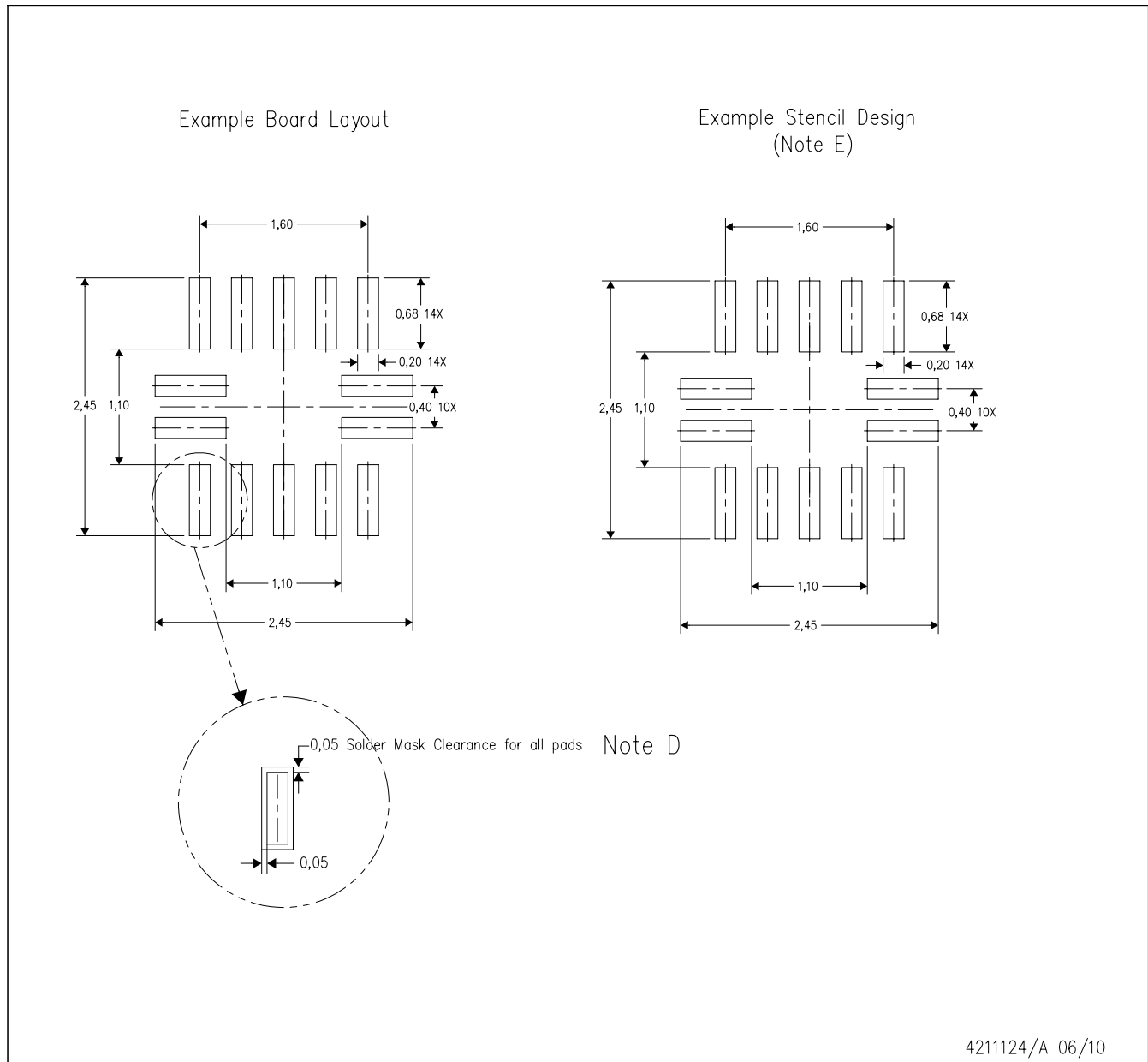   E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
            if stencil manufacturing process allows for sufficient release at smaller opening.

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

4,50
4,30

6,60
6,20

1   7

A

0,15 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◯ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps