High-Voltage Ultralow-Iq Low-Dropout Regulator

Check for Samples: TPS7A6601-Q1, TPS7A6633-Q1, TPS7A6650-Q1, TPS7A6933-Q1, TPS7A6950-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- 4-V to 40-V Wide Vin Input Voltage Range With up to 45-V Transient
- Output Current 150 mA
- Low Quiescent Current Iq:
  - 2 µA when EN = Low (Shutdown Mode)
  - 12 µA Typical at Light Loads
- Low ESR Ceramic Output Stability Capacitor (2.2 µF–100 µF)
- 300-mV Dropout Voltage at 150 mA (Typical, V_{IN} = 4 V)
- Fixed (3.3-V and 5-V) and Adjustable (1.5-V to 5-V) Output Voltages (Adjustable for TPS7A66xx-Q1 Only)
- Low Input Voltage Tracking
- Integrated Power-On Reset
  - Programmable Reset-Pulse Delay
  - Open-Drain Reset Output
- Integrated Fault Protection
  - Thermal Shutdown
  - Short-Circuit Protection
- Input Voltage Sense Comparator (TPS7A69xx-Q1 Only)
- Packages
  - 8-Pin SOIC-D for TPS7A69xxQ1
  - 8-Pin MSOP-DGN for TPS7A66xx-Q1

APPLICATIONS

- Qualified for Automotive Applications
- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

DESCRIPTION

The TPS7A66xx and TPS7A69xx are low-dropout linear regulators designed for up to 40-V Vin operations. With only 12-µA quiescent current at no load, they are quite suitable for standby micro control unit systems, especially in automotive applications.

The devices feature integrated short-circuit and overcurrent protection. The devices implement reset delay on power up to indicate the output voltage is stable and in regulation. One can program the delay with an external capacitor. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

The devices operate in the –40°C to 125°C temperature range. These features suit the devices well for power supplies in various automotive applications.

TYPICAL APPLICATION SCHEMATIC

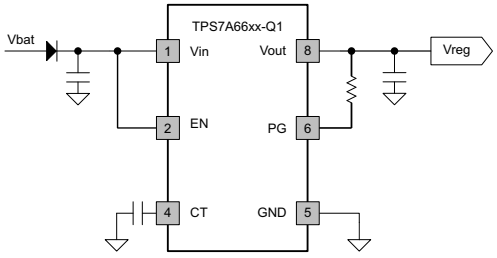


Figure 1. Hardware-Enable Option

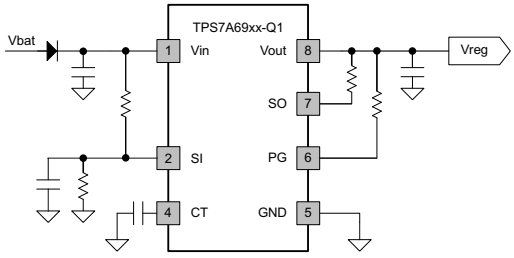


Figure 2. Input-Voltage-Sensing Option

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		MAX	UNITS
Vin, EN	Unregulated input (2) (3)(4)	45	V
Vout	Regulated output	7	V
SI	See (2) (3)	Vin	V
CT		25	V
FB, SO, PG		Vout	V
ESD	Electrostatic Discharge (5)	4	kV
T_J	Operating ambient temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND
(3) Absolute negative voltage on these pins not to go below –0.3 V
(4) Absolute maximum voltage, withstand 45 V for 200 ms
(5) The human-body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS7A66xx-Q1	TPS7A69xx-Q1	UNITS
		MSOP (8 PINS)	SOIC (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	63.4	113.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.0	59.6	
θ_{JB}	Junction-to-board thermal resistance (2)	37.4	23.4	
ψ_{JT}	Junction-to-top characterization parameter	3.7	12.8	
ψ_{JB}	Junction-to-board characterization parameter	37.1	52.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	13.5	NA	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
Vin	Unregulated input	4	40	V
EN, SI		0	40	V
CT		0	20	V
Vout		1.5	5.5	V
PG, SO, FB	Low voltage (I/O)	0	5.5	V
T_J	Operating junction temperature range	–40	150	°C

ELECTRICAL CHARACTERISTICS

Vin = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT(Vin)						
Vin	Input voltage	Fixed 5-V output, I_{OUT} = 1 mA	5.5		40	V
		Fixed 3.3-V output, I_{OUT} = 1 mA	4		40	V
$I_{quiescent}$	Quiescent current	V_{IN} = 5.5 V to 40 V, EN = ON, I_{OUT} = 0.2 mA		12	20	µA
I_{Sleep}	Input sleep current	No load current and EN = OFF			4	µA
I_{EN}	EN pin current	EN = 40 V			1.0	µA
Vbg	Band gap	Reference voltage for FB	–2%	1.223	2%	V
Vin_{UVLO}	Undervoltage detection	Ramp Vin down until output turns OFF			2.6	V
$UVLO_{Hys}$				1		V
ENABLE INPUT (EN)						
V_{IL}	Logic input low level		0		0.4	V
V_{IH}	Logic input high level		1.7			V
REGULATED OUTPUT (Vout)						
Vout	Regulated output	I_{OUT} = 1 mA, T_J = 25°C	–1%		1%	
		V_{IN} = 6 V to 40 V, I_{OUT} = 1 mA to 150 mA(1)	–2%		2%	
$V_{line-reg}$	Line regulation	V_{IN} = 5.5 V to 40 V, ΔV_{OUT}, Iout = 50 mA			5	mV
$V_{load-reg}$	Load regulation	I_{OUT} = 1 mA to 150 mA, ΔV_{OUT}			20	mV
$V_{dropout}$	Dropout voltage	V_{IN} – V_{OUT}, I_{OUT} = 80 mA		180	240	mV
		V_{IN} – V_{OUT}, I_{OUT} = 150 mA		300	450	
		V_{IN} = 3 V, V_{IN} – V_{OUT}, I_{OUT} = 5 mA	12	27.5	58	
		V_{IN} = 3 V, V_{IN} – V_{OUT}, I_{OUT} = 30 mA	44	80	145	
Iout	Output current	V_{OUT} in regulation	0		150	mA
$I_{lreg-CL}$	Output current limit	V_{OUT} short to ground		500	800	mA
PSRR	Power supply ripple rejection(2)	V_{IN} = 12 V, I_{Load} = 10 mA, C_{OUT} = 2.2 µF				
		Freq = 100 Hz		60		dB
		Freq = 100 kHz		40		dB
VOLTAGE SENSING PRE-WARNING						
V_{SIth}	Sense low threshold	V_{SI} decreasing	1.089	1.123	1.157	V
$V_{SIth,hys}$	Sense threshold hysteresis		50	100	150	mV
V_{SOL}	Sense output low voltage	(V_{SI} ≤ 1.06 V, Vin ≥ 4 V, R_{SO} = 10 kΩ to V_{OUT})			0.4	V
I_{SOH}	Sense output leakage	(V_{SO} = 5 V, V_{SI} ≥ 1.5 V)			1	µA
I_{SI}	Sense input current		–1	0.1	1	µA
RESET (PG)						
V_{OL}	Reset pulled low	I_{OL} = 0.5 mA			0.4	V
I_{OH}	Reset pulled Vout through 10-kΩ resistor	Leakage current			1	µA
$V_{TH-(POR)}$	Power-on-reset threshold	Vout power up set tolerance	89.6	91.6	93.6	% of Vout
V_{Thres}	Hysteresis	Vout power down set tolerance		2		% of Vout
RESET DELAY (CT)						
I_{Chg}	Delay-capacitor charging current	Rdelay = 0 V		1.4		µA
V_{th}	Threshold to release nRST high			1		V
TIMING FOR RESET (PG)						
t_{POR}	Power-on-reset delay	Where C = Delay capacitor value Capacitance C = 100 nF(3)	50	100	180	ms
$t_{POR-fixed}$		No capacitor on pin	100	290	650	µs
$t_{Deglitch}$	Reset deglitch time		20	250		µs
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{shutdown}$	Junction shutdown temperature			175		°C

(1) Adjustable version with precision external feedback resistor with tolerance of less than ±1%.
(2) Design information – Not tested, specified by characterization.
(3) This information only will NOT be tested in production and equation will be based as; (C × 1) / 1 × 10^{-6} = t_{Delay} (delay time). Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

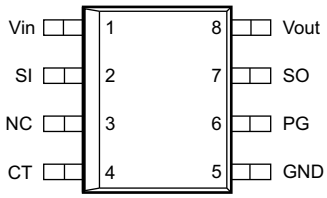
ELECTRICAL CHARACTERISTICS (continued)

Vin = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150°C (unless otherwise noted)

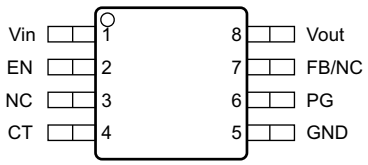
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
T_{Hyst}	Hysteresis of thermal shutdown			20		°C

DEVICE INFORMATION

SOIC 8 (TPS7A69xx-Q1)
D Package
(Top View)



MSOP 8 (TPS7A66xx-Q1)
DGN Package
(Top View)



Pin Functions

PIN NAME	PIN NO.		TYPE	DESCRIPTION
	SOIC-D	MSOP - DGN		
CT	4	4	O	Reset-pulse delay adjustment. Connecting this pin via a capacitor to GND
EN		2	I	Enable pin. Standby state when enable pin becomes lower than threshold
FB/NC		7	I	Feedback pin when using external resistor divider or NC pin when using internal resistor divider
GND	5	5	G	Ground reference
NC	3	3		Not connected pins
PG	6	6	O	Output ready. This open-drain pin must connect to Vout via an external resistor. The output voltage going below threshold pulls it down.
SI	2		I	Sense input pin to supervise input voltage. Connect via an external voltage divider connected to Vs and GND
SO	7		O	Sense output. This open-drain pin must connect to Vout via an external resistor. The SI voltage becoming lower than the threshold pulls it down.
Vin	1	1	P	Input power-supply voltage
Vout	8	8	P	Output voltage
		—		Thermal pad for MSOP-DGN package

FUNCTIONAL BLOCK DIAGRAMS

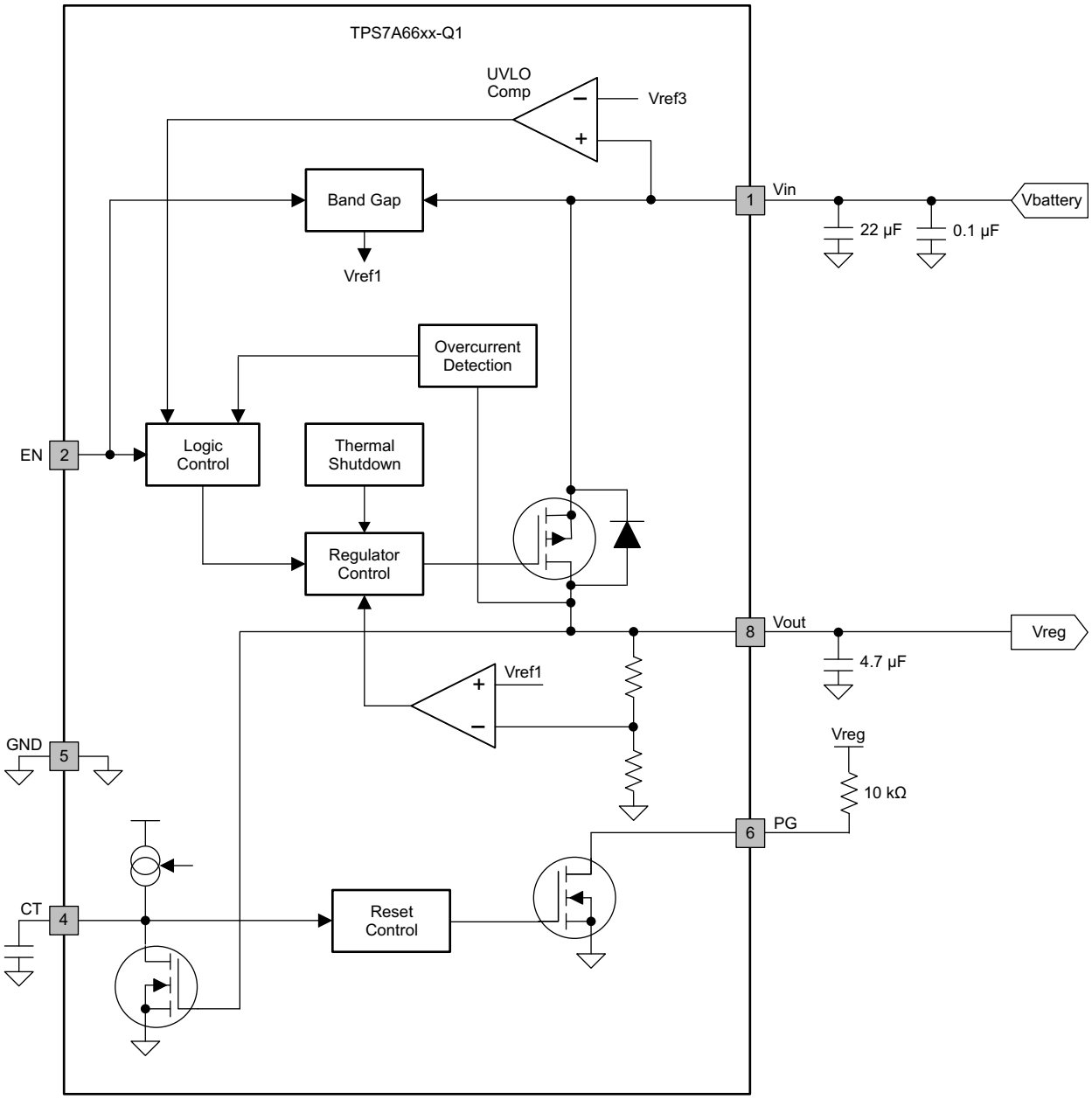


Figure 3. TPS7A66xx Functional Block Diagram

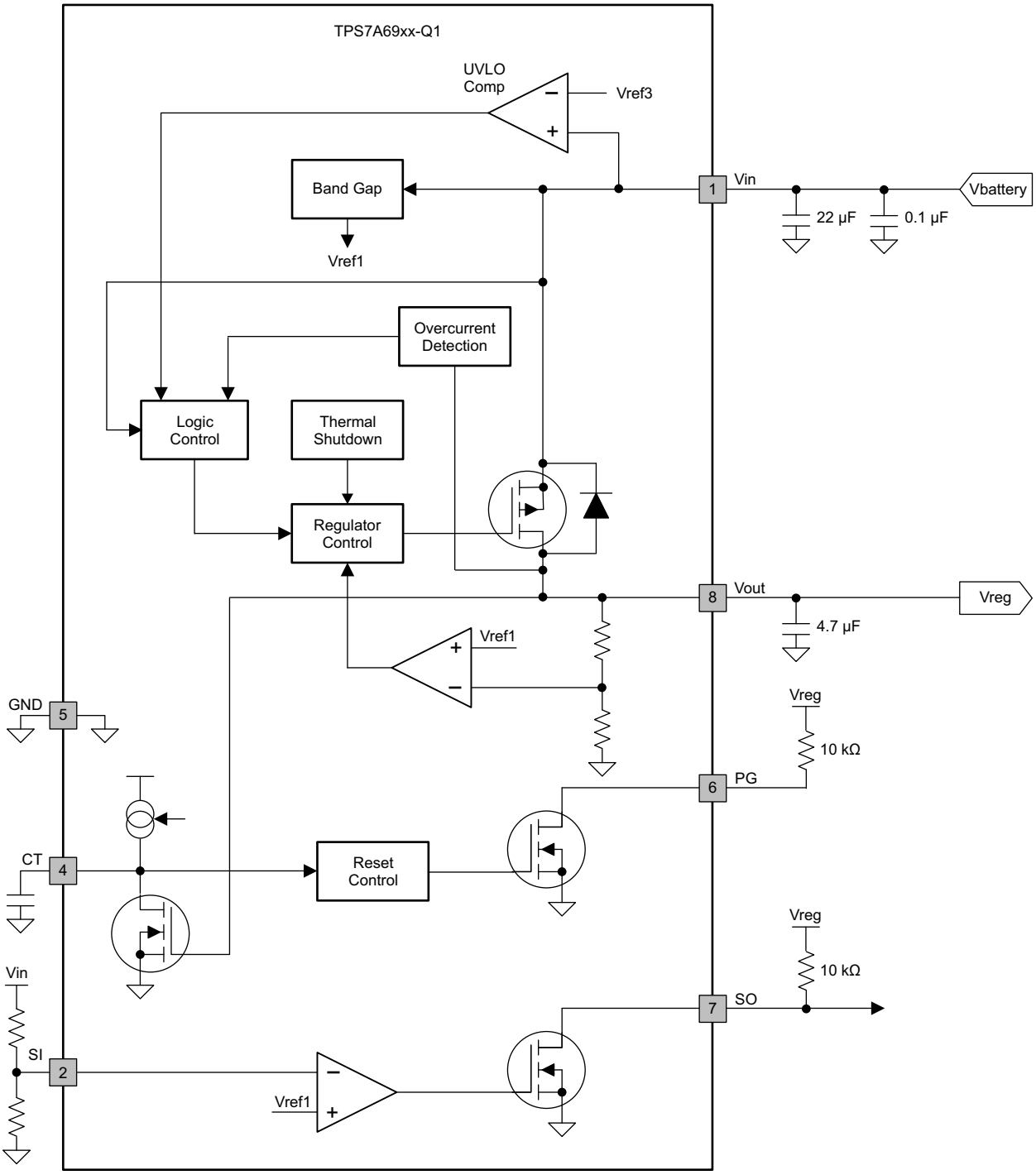


Figure 4. TPS7A69xx Functional Block Diagram

TYPICAL CHARACTERISTICS

POWER-GOOD THRESHOLD VOLTAGE vs TEMPERATURE (Vin=14 V, NO LOAD)

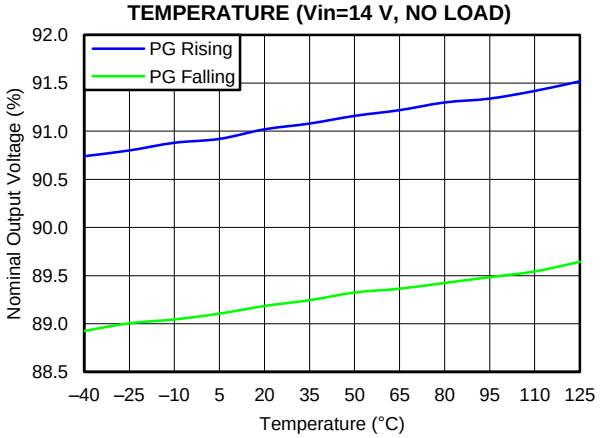


Figure 5.

LINE REGULATION (Vin = 14 V, Iload = 1 mA)

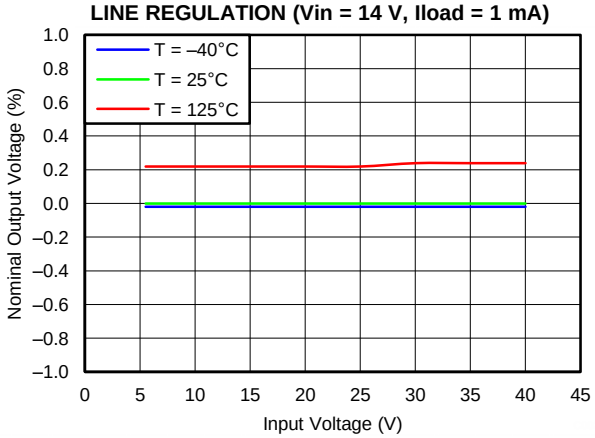


Figure 6.

GROUND CURRENT vs OUTPUT CURRENT (Vin = 14V)

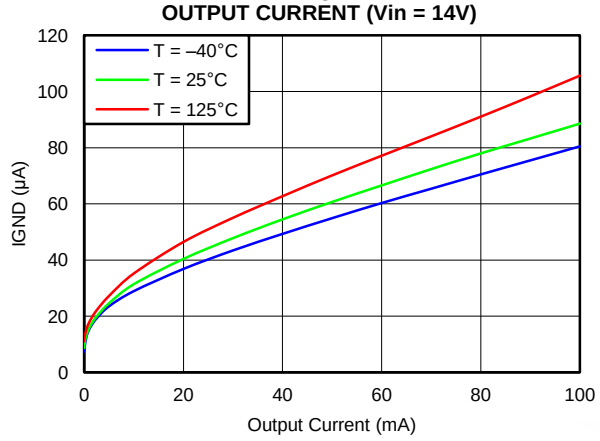


Figure 7.

QUIESCENT CURRENT vs INPUT VOLTAGE (Iload = 0)

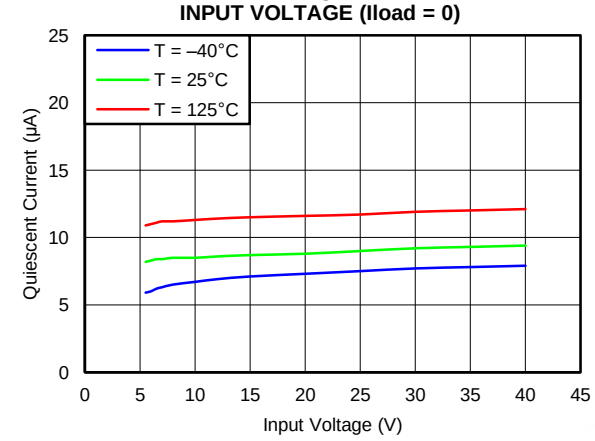


Figure 8.

**LOAD REGULATION (Vin= 14 V) **

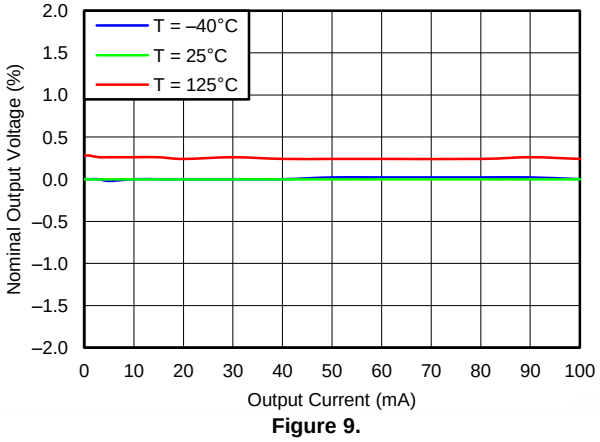


Figure 9.

DROPOUT VOLTAGE vs OUTPUT CURRENT (Vin = 4 V)

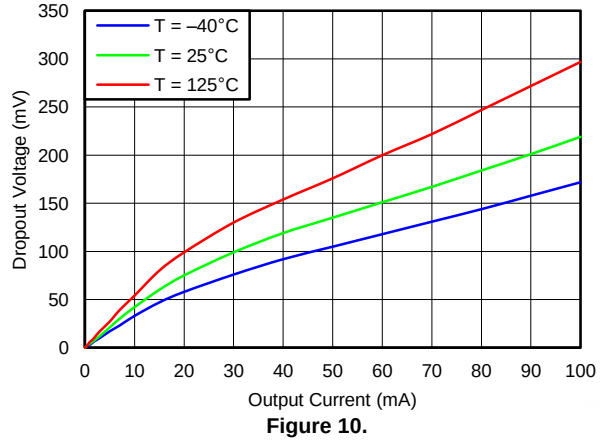


Figure 10.

TYPICAL CHARACTERISTICS (continued)

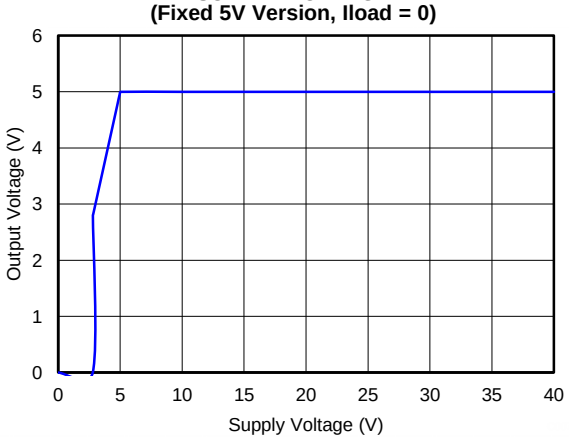


Figure 11.

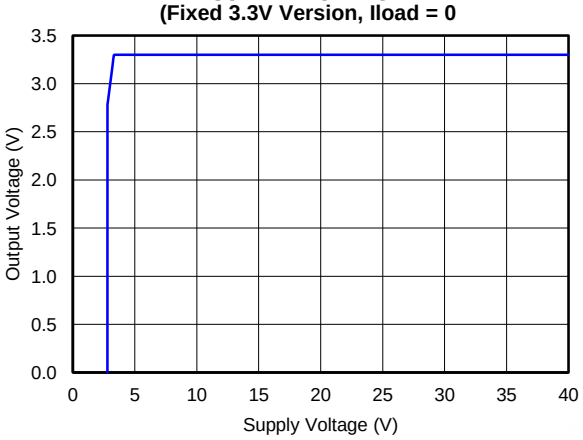


Figure 12.

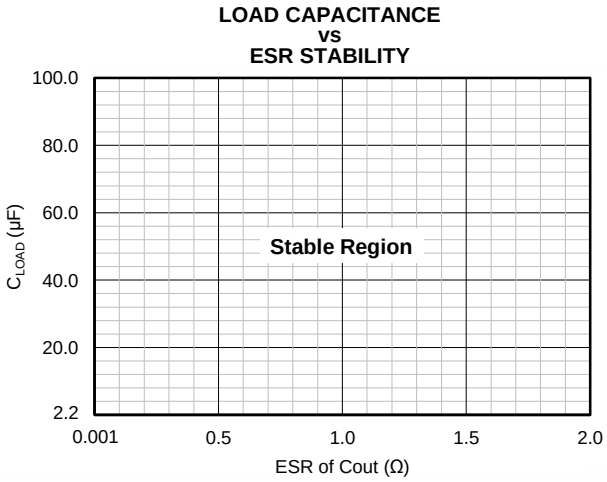


Figure 13.

All oscilloscope waveforms were taken at room temperature.

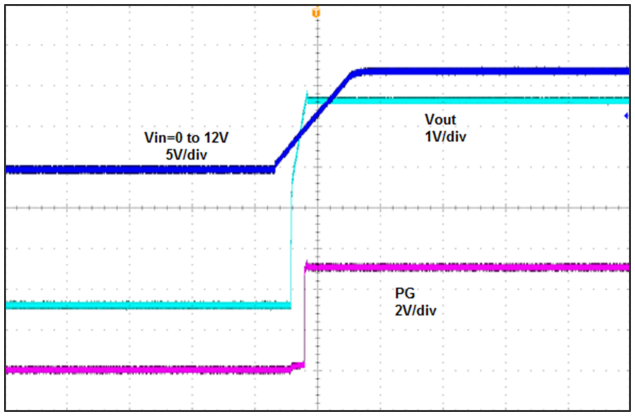


Figure 14. Power Up (5 V), 20 ms/div, Iload = 20 mA

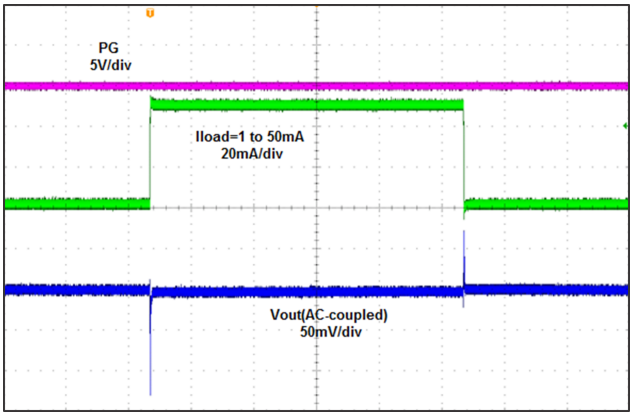


Figure 15. Load Transient Response, 10 ms/div

TYPICAL CHARACTERISTICS (continued)

All oscilloscope waveforms were taken at room temperature.

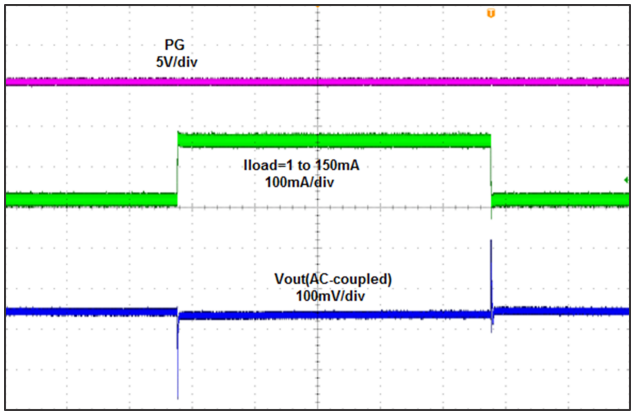


Figure 16. Load Transient Response, 10 ms/div

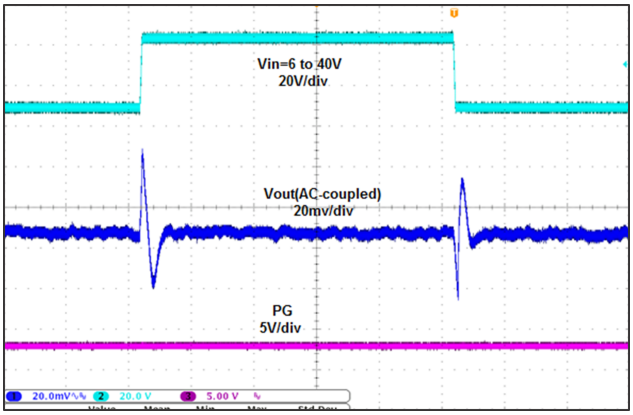


Figure 17. Line Transient Response, Iload = 1 mA, 1 V/µs

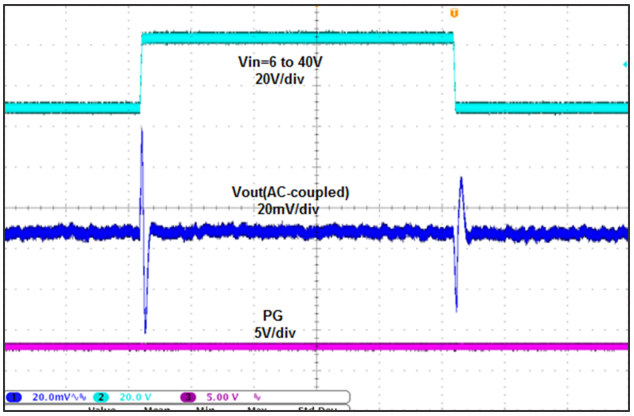


Figure 18. Line Transient Response, Iload = 10 mA, 1 V/µs

DETAILED DESCRIPTION

This product is a combination of a low-dropout linear regulator with reset function. The power-on-reset initializes once the output Vout exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the Rdelay pin before releasing the RST terminal high.

Enable (EN):

This is a high-voltage-tolerant terminal; high input actives the device and turns the regulator ON. One can connect this input to the Vin terminal for self-bias applications.

Regulated Output (Vout):

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

Power-On-Reset (PG):

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated Vout has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 50 µs (typical).

Reset Delay Timer (CT):

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 150 µs (typ). After releasing the nRST pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approx 0.2 V for the next power-on-reset delay-timer function.

An external capacitor CT defines the reset-pulse delay time, t_{CT}, with the charge time of :

$$t_{CT} = \frac{C_{CT} \times 1V}{1\mu A} \quad (1)$$

The power-on-reset initializes once the output Vout exceeds 90% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG terminal high.

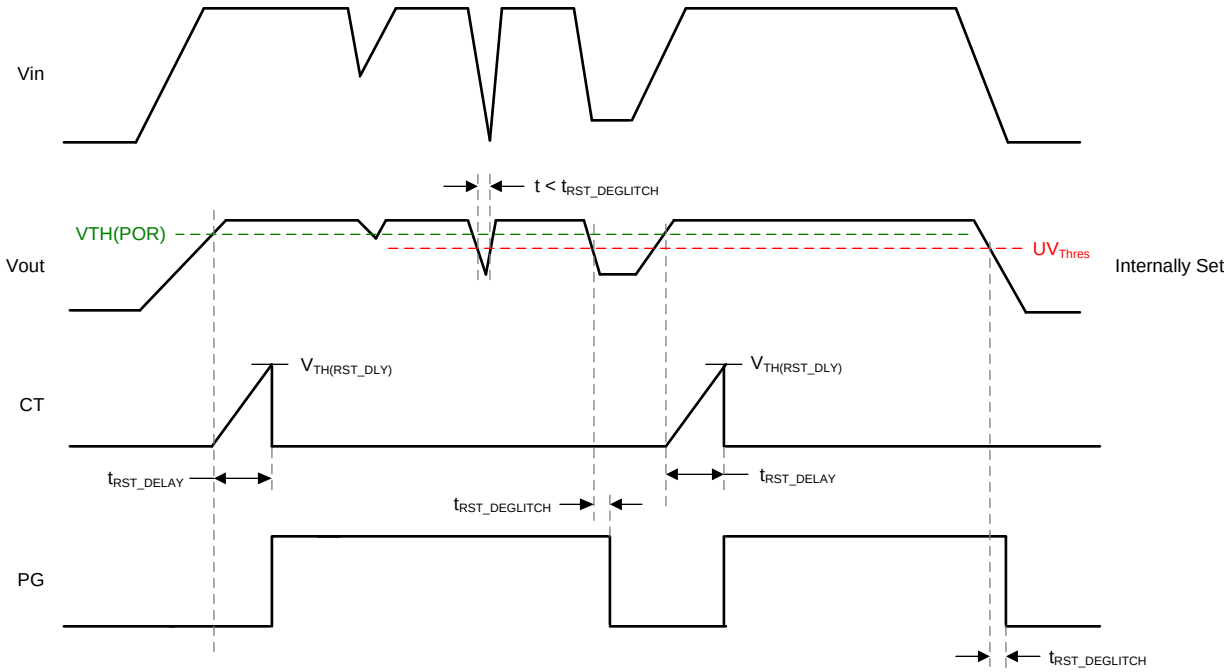


Figure 19. Conditions for Activation of Reset

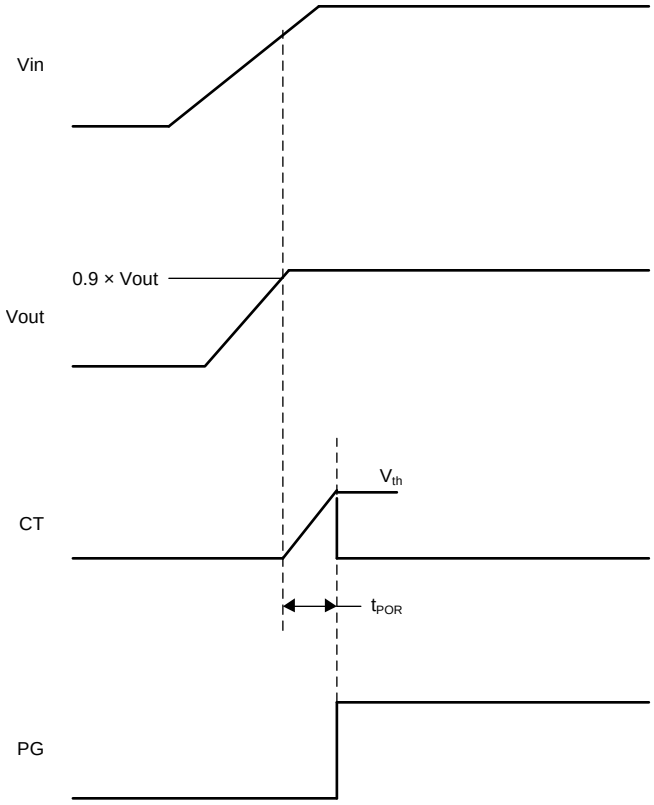


Figure 20. External Programmable Reset Delay

Sense Comparator (SI and SO for TPS7A69xx)

The sense comparator compares an input signal with an internal voltage reference of 1.223 V for rising and 1.123 V for falling threshold. The use of an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and give additional information to the microprocessor, like low-voltage warnings.

The regulator operates in low-power mode when the output load is below 2 mA (typical, 1-mA to 10-mA range). In this mode, the regulator output tolerance is approximately Vout ± 1%.

Adjustable Output Voltage (FB for TPS7A6601)

One can select an output voltage between 1.5 V and 5.5 V by using the external resistor dividers. Calculate the output voltage using the following equation, where V_{FB}= 1.223 V.

$$Vout = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

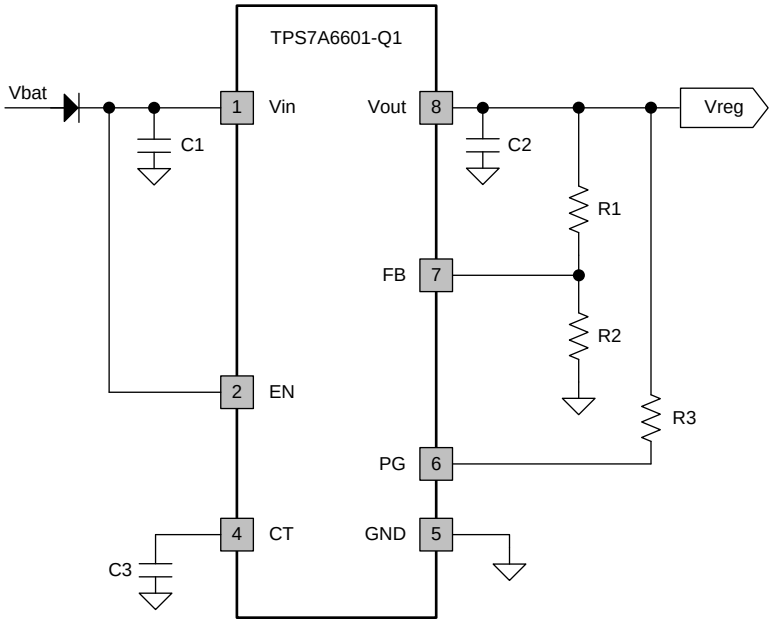


Figure 21. External Feedback Resistor Divider

Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on Vin drops below Vin_{UVLO}. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up like a normal power-up sequence once the input voltage is above the required levels.

Low-Voltage Tracking

At low input voltages the regulator drops out of regulation, the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

APPLICATION INFORMATION

Figure 22 and Figure 23 show typical application circuits for the TPS7A66xx and TPS7A69xx, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor may uring fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

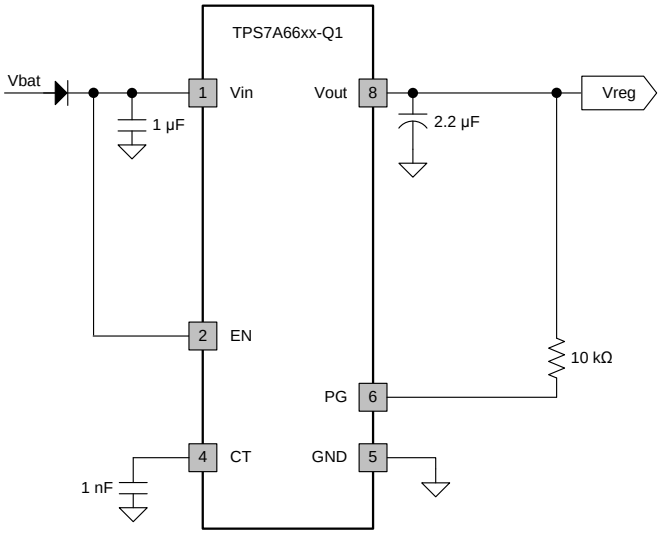


Figure 22. Typical Application Schematic for TPS7A66xx

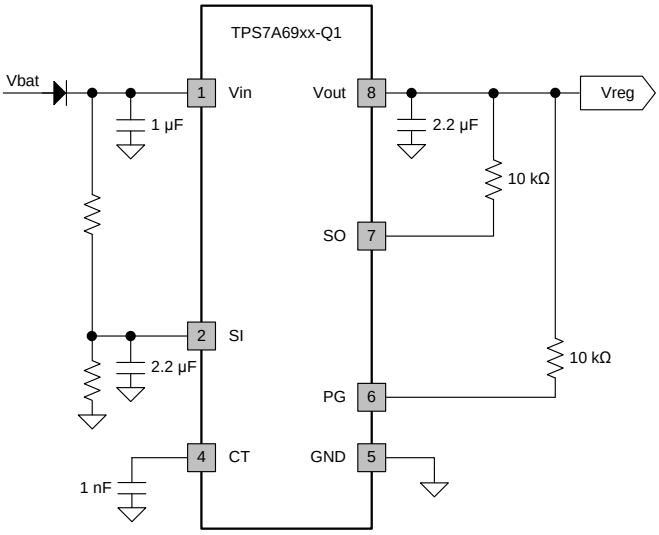


Figure 23. Typical Application Schematic for TPS7A69xx

Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using Equation 3.

$$P_D = I_{out} \times (V_{in} - V_{out}) + I_{quiescent} \times V_{in} \quad (3)$$

Where:

P_D = continuous power dissipation
I_{out} = output current
V_{in} = input voltage
V_{out} = output voltage

As $I_{quiescent} << I_{out}$, therefore ignore the term $I_{quiescent} \times V_{in}$ in Equation 3.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 4.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (4)$$

where:

θ_{JA} = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (5)$$

LAYOUT INFORMATION

Package Mounting

Solder pad footprint recommendations for the TPS7A66xx-Q1 and TPS7A69xx-Q1 are available at the end of this product data sheet and at www.ti.com.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for Vin and Vout, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A66xx-Q1 and TPS7A69xx-Q1 evaluation board, available at www.ti.com.

Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitive-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends the use of a fixed-voltage version of the TPS7A66xx-Q1, or isolation of the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. Cooling of the junction temperature to approximately 150°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, junction temperature should be limited to a maximum of 125°C at the worst-case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The purpose of the design of the internal protection circuitry of the TPS7A66/69xx-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A66xx-Q1 or TPS7A69xx-Q1 into thermal shutdown degrades device reliability.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Added two conditions to Vdropout in the Electrical Characteristics table	3

Changes from Original (December 2012) to Revision A **Page**

- Deleted the ORDERING INFORMATION table 2
- Changed From: T_A Operating ambient temperature range –40 to 125°C To: T_J Operating junction temperature range –40 to 150°C 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6601QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q	Samples
TPS7A6633QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q	Samples
TPS7A6650QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q	Samples
TPS7A6933QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6933	Samples
TPS7A6950QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

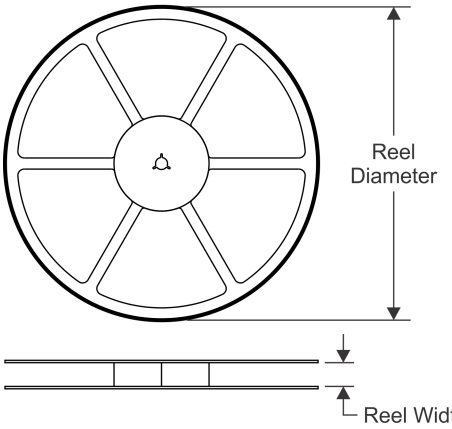
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

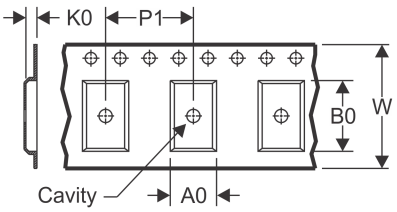
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

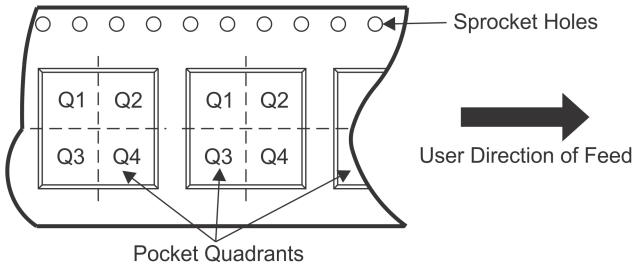


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

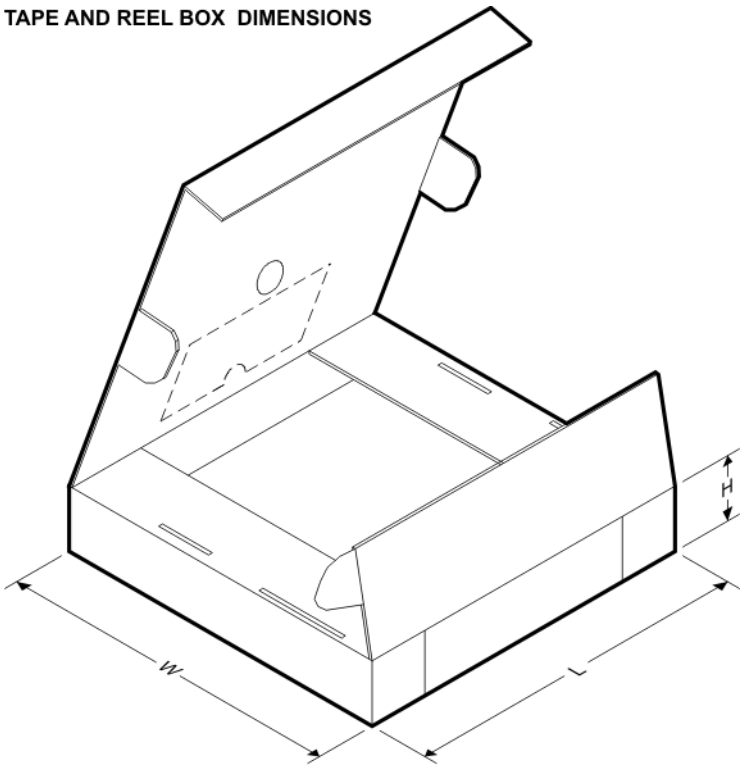
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6601QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6633QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6650QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6950QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

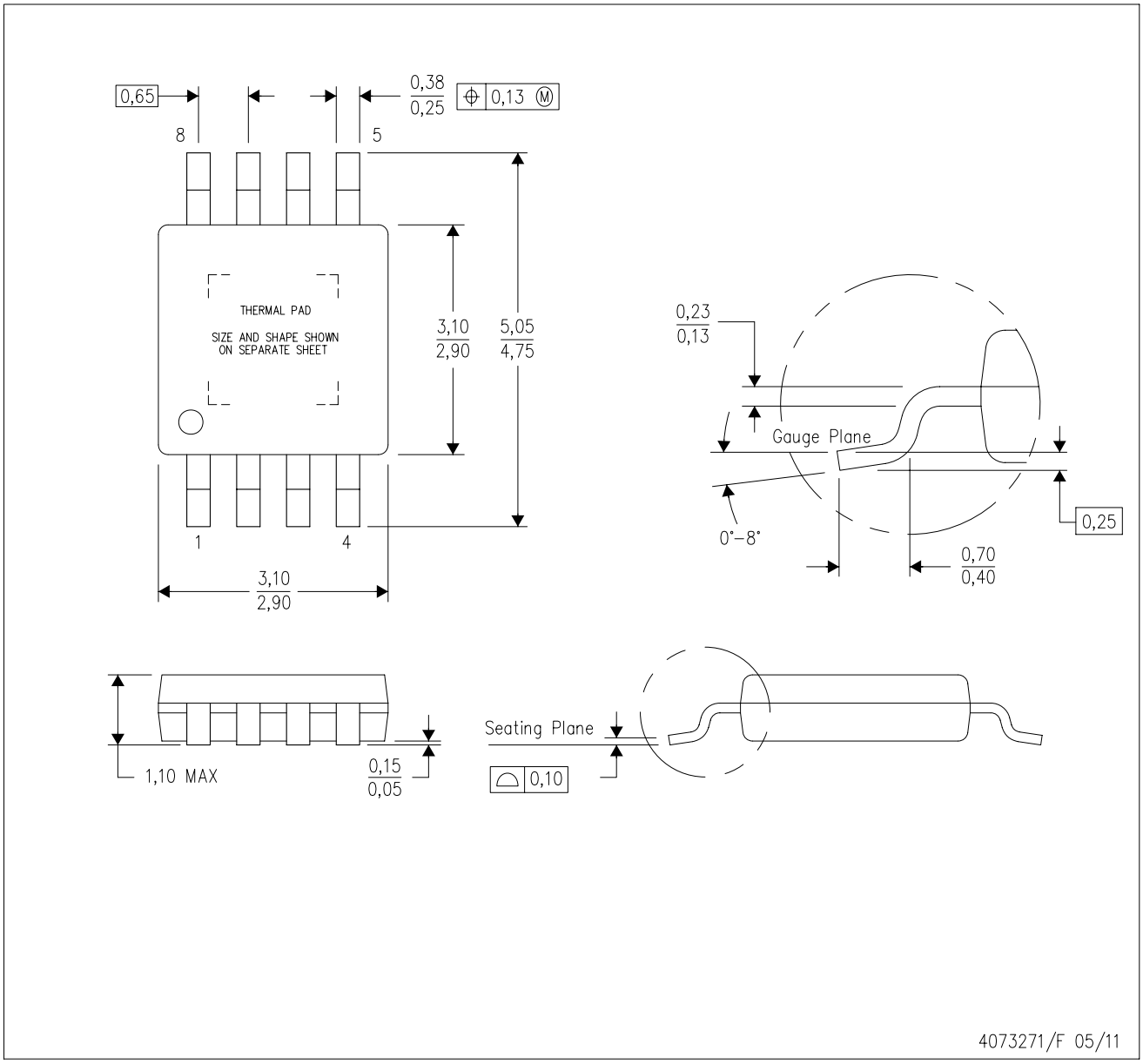
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6601QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6633QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6650QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6950QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

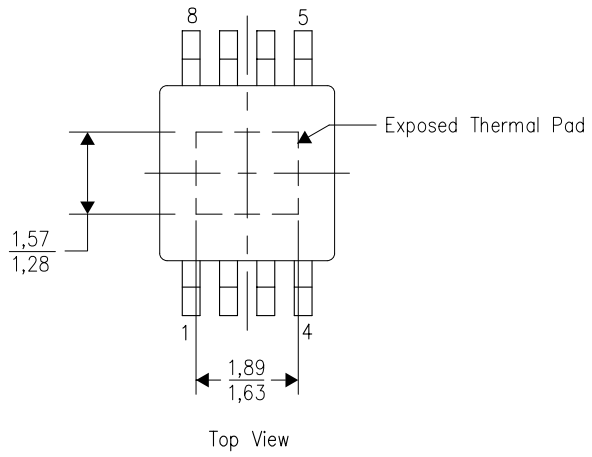
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

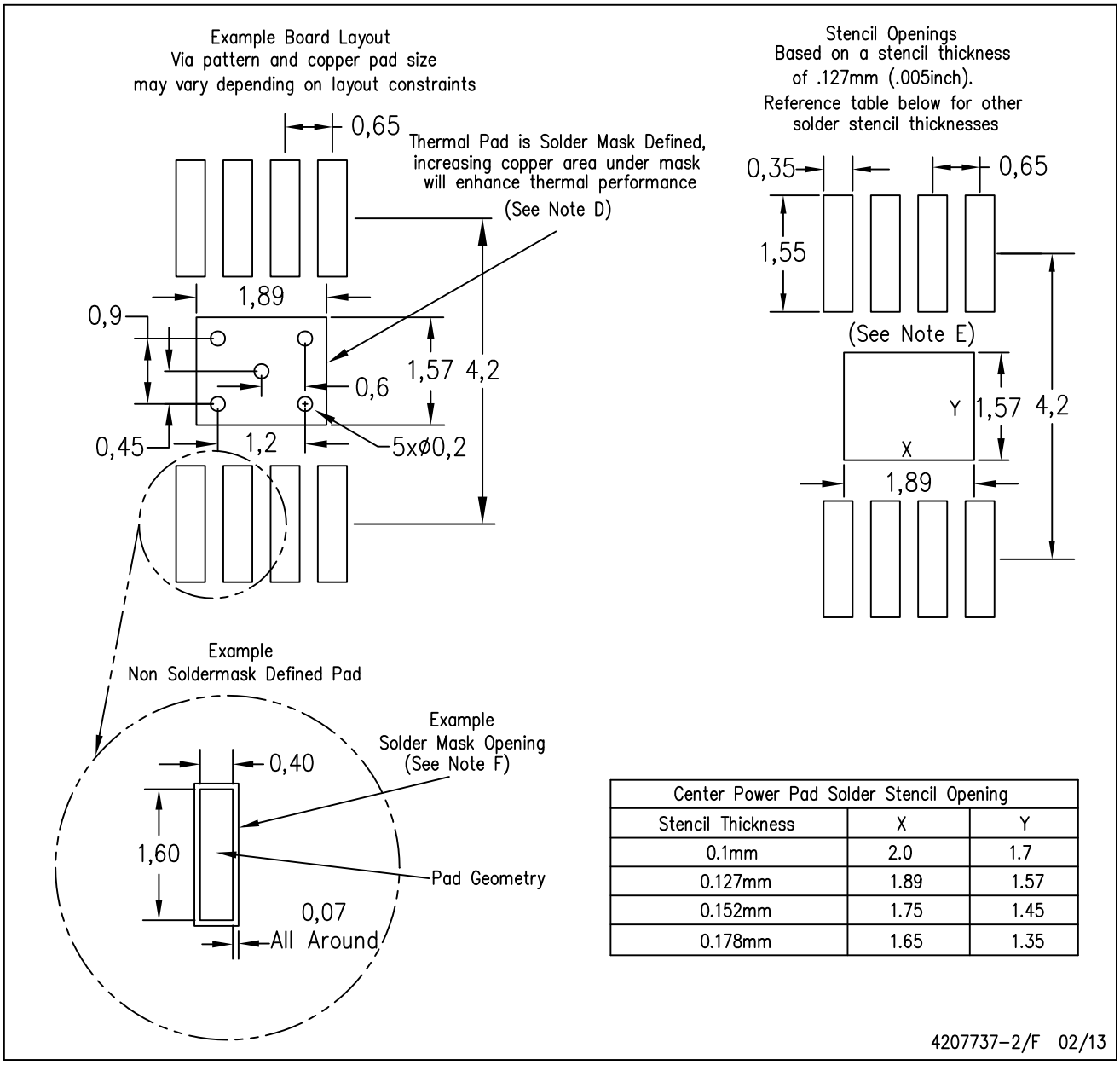
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

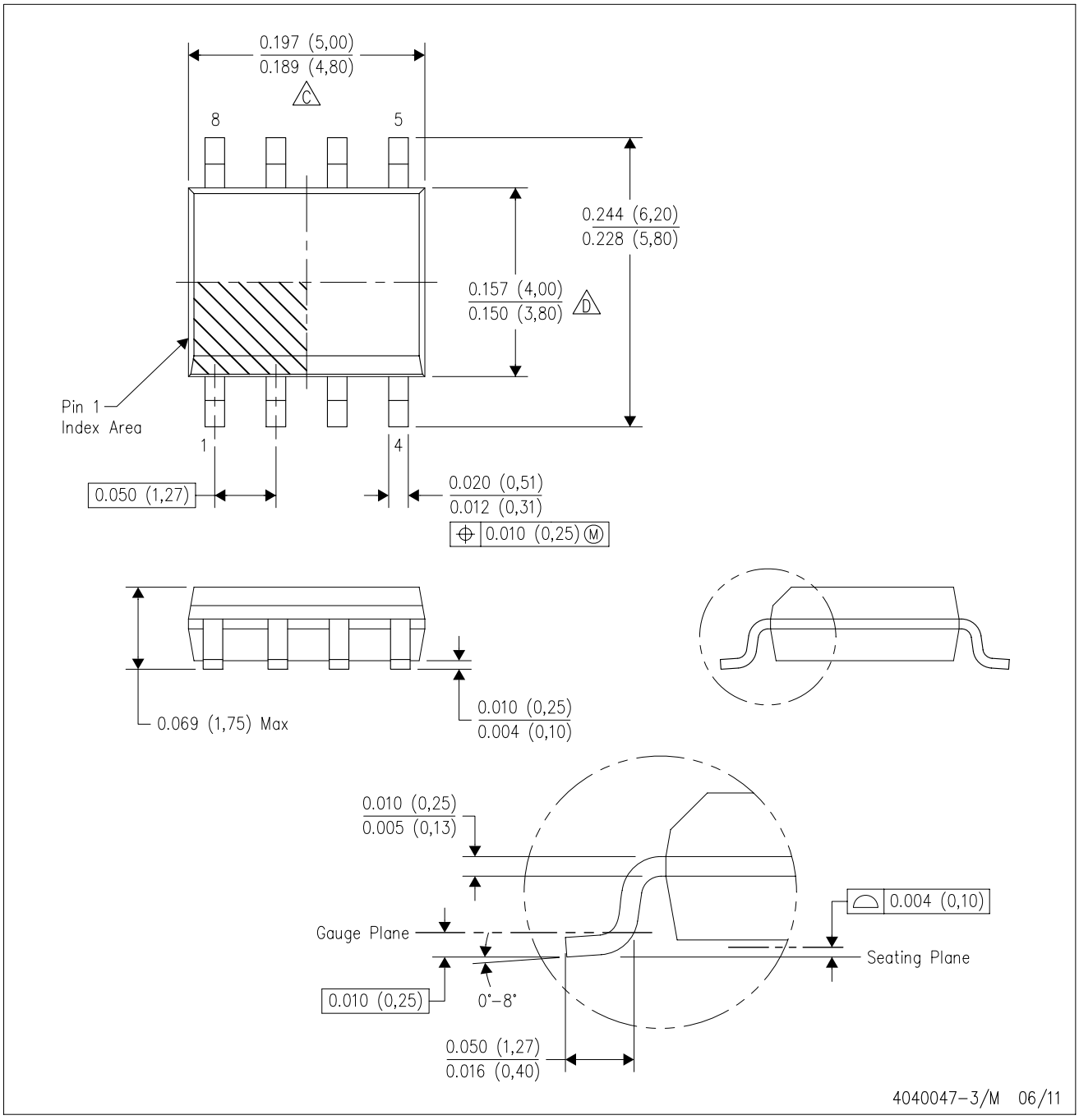


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

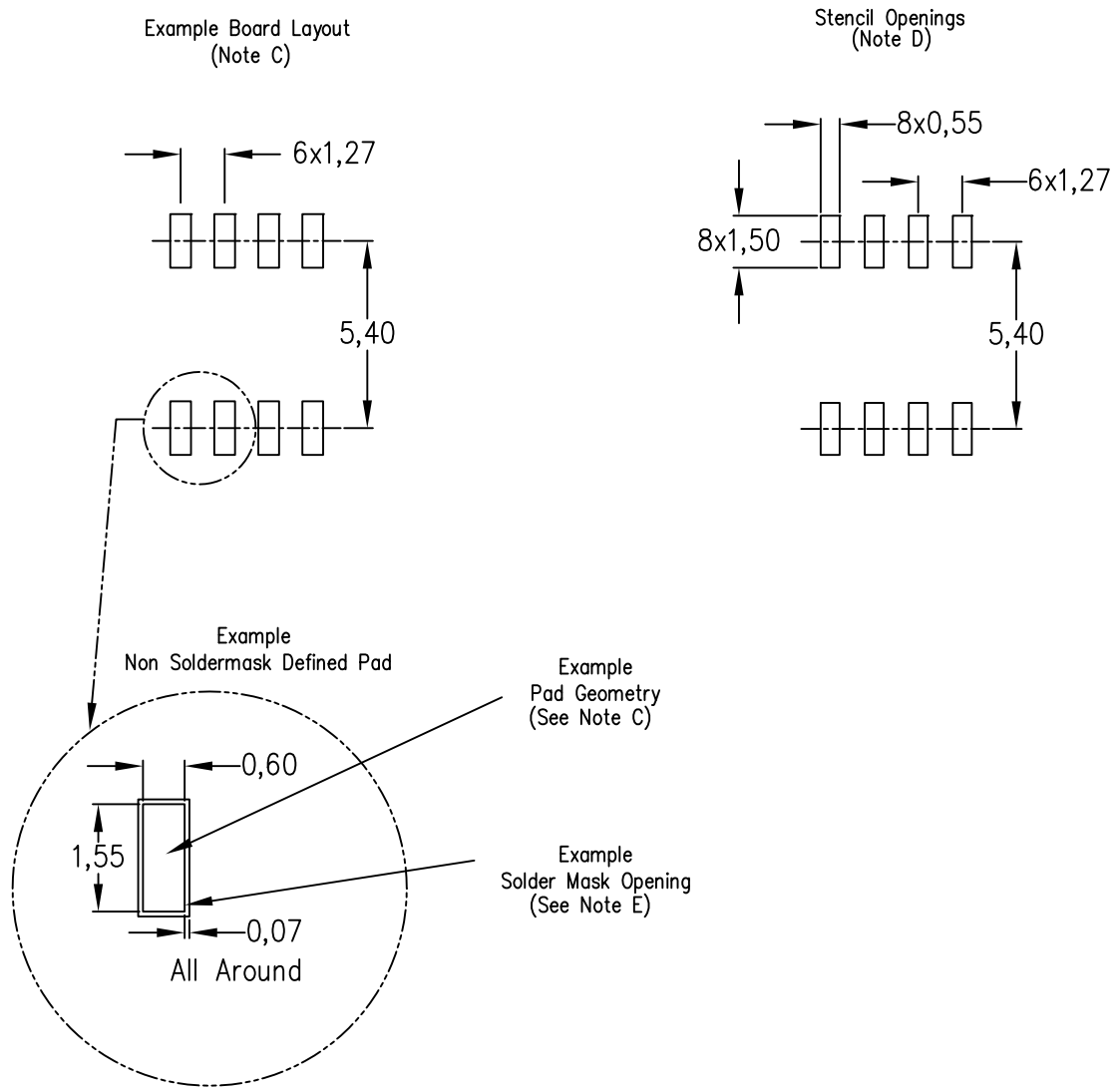
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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