High PSRR, Low-Noise, 1-A Power Filter

Check for Samples: TPS7A3501

FEATURES

- Regulates Input-to-Output Voltage:
  - User-Programmable Input-to-Output Voltage Regulation Range: 200 mV to 500 mV
- Power-Supply Rejection Ratio:
  - 42 dB at 1 MHz
  - ≥ 32 dB (360 kHz to 3.9 MHz)
- Low-Noise Output:
  - 3.8 μV_{RMS} (10 Hz to 100 kHz)
- Output Current: Up to 1 A
- Output Voltage Range: 1.21 V to 4.5 V
- Excellent Load Transient Response
- Stable with Ceramic Capacitors as Low as 10 µF
- Current Limit and Thermal Shutdown for Fault Protection
- Available in a Low Thermal Resistance Package: 2-mm × 2-mm SON-6
- Operating Temperature Range: –40°C to +125°C

APPLICATIONS

- Post DC/DC Converter Ripple Filtering
- Base Stations and Telecom Infrastructure
- Professional Audio
- Communications
- Imaging
- Test and Measurement
- Passive Filter Replacement

DESCRIPTION

The TPS7A3501 is a positive voltage, low-noise (3.8 μV_{RMS}) power filter capable of sourcing a 1-A load suitable for quiet supply solutions. Power filters, such as the TPS7A3501, provide voltage regulation across the input and output terminals with high efficiency (low insertion loss), and power-supply rejection. The device is ideally-suited as a noise filter for 3.3-V, 2.5-V, and 1.8-V supplies at up to 1 A.

The input-to-output voltage regulation is also user-programmable, from 200 mV to 500 mV, with a single external resistor. If no resistor is used, the TPS7A3501 provides 330 mV of input-to-output voltage regulation. The device is stable with 10-µF input and output ceramic capacitors and a 10-nF noise-reduction ceramic capacitor.

The TPS7A3501 is fully specified over a wide temperature of –40°C to +125°C. The device is offered in a low thermal resistance, 2-mm × 2-mm, SON-6 package. Unlike passive filters, the TPS7A3501 provides thermal and current protection for itself and surrounding circuitry.

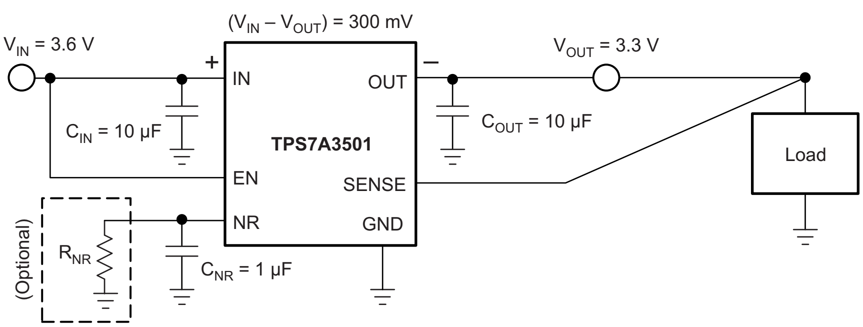


Figure 1. TPS7A3501 Typical Application Circuit

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Voltage	IN, NR, EN	–0.3	7	V
	OUT SENSE	–0.3	V_{IN} + 0.3(2)	V
Current	OUT	Internally limited		
Temperature range	Operating junction, T_J	–40	+125	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		1	kV
	Charged device model (CDM)		250	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum rating is V_{IN} + 0.3 V or +7.0 V, whichever is smaller.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A3501 DRV (SON) 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	66.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	86.5	
θ_{JB}	Junction-to-board thermal resistance	36.4	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	36.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

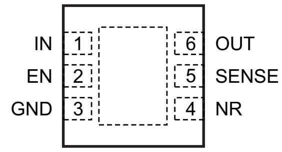
At T_J = –40°C to +125°C, V_{IN} = 3.6 V, R_{NR} = ∞ (not connected), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.71		5.0	V
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} increasing	1.5		1.7	V
		V_{IN} hysteresis		200		mV
V_{OUT}	Output voltage range		1.21		4.5	V
	V_{IN} – V_{OUT} voltage range		200		500	mV
		$V_{OUT(NOM)}$ = V_{IN} – 330mV, I_{OUT} ≤ 1 A, 1.71 V ≤ V_{IN} ≤ 4.83 V	297	330	363	mV
		$R_{NR\_INTERNAL}$ (1)	110	170	210	kΩ
		$I_{NR\_INTERNAL}$ (2)	1.4	1.8	2.4	µA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	10 mA ≤ I_{OUT} ≤ 1 A		10		µV/mA
I_{CL}	Output current limit	V_{OUT} = 0.85 × $V_{OUT(nom)}$	1.1			A
I_{GND}	GND pin current			2.25	5	mA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.3 V		0.01	3	µA
PSRR	Power-supply rejection ratio	f = 10 kHz, C_{NR} = 1.0 µF, I_{OUT} = 0.5 A		55		dB
		f = 100 kHz, C_{NR} = 1.0 µF, I_{OUT} = 0.5 A		40		dB
		f = 1 MHz, C_{NR} = 1.0 µF, I_{OUT} = 0.5 A		42		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, C_{NR} = 1 µF, I_{OUT} = 1 A		3.8		μV_{RMS}
		BW = 100 Hz to 100 kHz, C_{NR} = 1 µF, I_{OUT} = 1 A		3.62		μV_{RMS}
		BW = 10 Hz to 1 MHz, C_{NR} = 1 µF, I_{OUT} = 1 A		12.1		μV_{RMS}
I_{EN}	EN pin input current	V_{EN} = V_{IN}		1	50	nA
V_{IL_EN}	EN pin input low (disable)				0.4	V
V_{IH_EN}	EN pin input high (enable)		1.1			V
T_{SD}	Thermal shutdown junction temperature	Shutdown, temperature increasing		+165		°C
		Shutdown, temperature hysteresis		+20		°C

(1) $R_{NR\_INTERNAL}$ refers to the internal resistor used to set (V_{IN} – V_{OUT}) for the device when no external R_{NR} is used. See the *Application Information* section and Figure 1 for details.
(2) $I_{NR\_INTERNAL}$ refers to the internal current source used to set (V_{IN} – V_{OUT}) for the device when no external R_{NR} is used. See the *Application Information* section and Figure 1 for details.

PIN CONFIGURATION

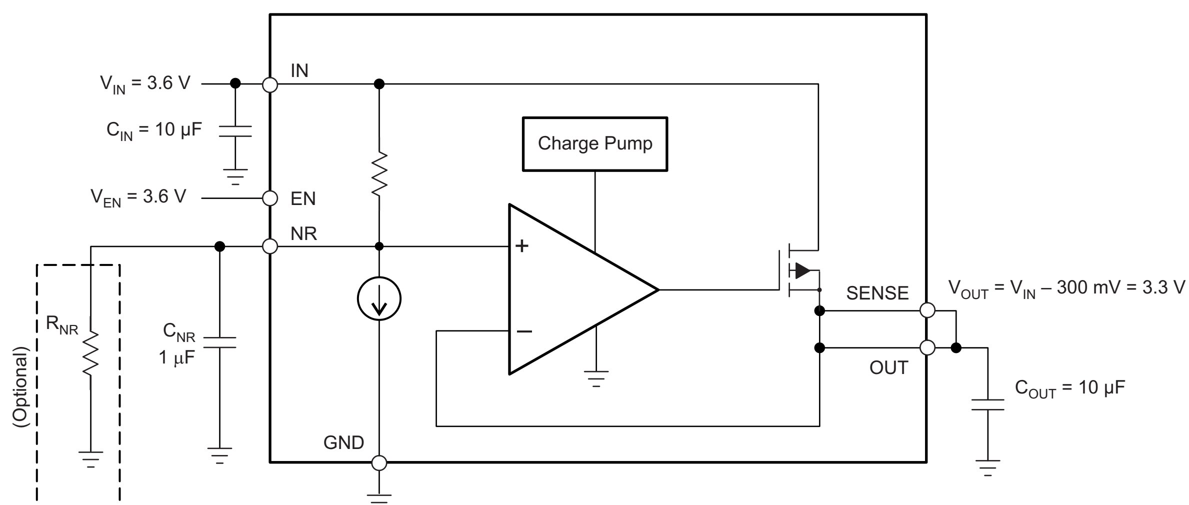
DRV PACKAGE
2-mm × 2-mm SON-6
(Top View)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
EN	2	Enable pin. Driving EN high turns on the device (if driven low, EN turns off the device). EN must not be left floating and can be connected to IN if not used.
GND	3	Ground
IN	1	Input supply. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. This configuration is especially important when long input traces or high source impedances are encountered. Using X5R- or X7R-type dielectrics is recommended in order to minimize the temperature variations inherent to capacitors.
NR	4	Noise-reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1-µF capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise. Using X5R- or X7R-type dielectrics is recommended in order to minimize the temperature variations inherent to capacitors. In addition, when a resistor is connected from this pin to GND or IN, the device input-to-output voltage can be programmed; see the *Application Information* section for details.
OUT	6	Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. Using X5R- or X7R-type dielectrics is recommended in order to minimize the temperature variations inherent to capacitors.
PowerPAD	—	Connect the PowerPAD™ to the ground plane for improved thermal performance.
SENSE	5	Control-loop error amplifier input. This pin must be connected to OUT. SENSE is recommended to be connected at the point of load to maximize accuracy.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At V_{IN} = 3.6 V, R_{NR} = ∞ (not connected), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 10.0 µF, C_{IN} = 10 µF, and C_{NR} = 0.1 µF, unless otherwise noted.

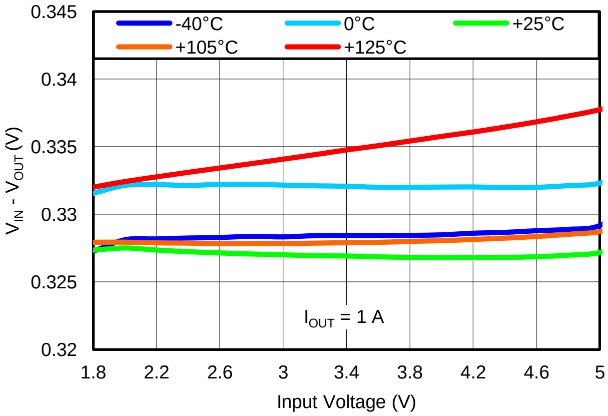


Figure 2. LINE REGULATION

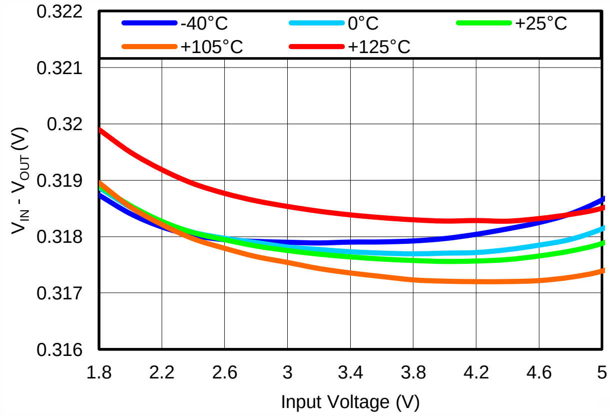


Figure 3. LINE REGULATION

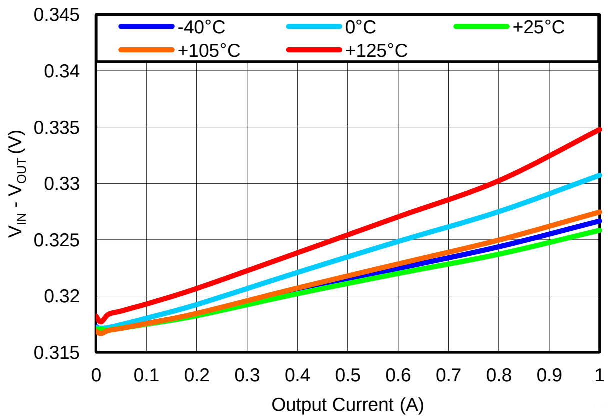


Figure 4. LOAD REGULATION

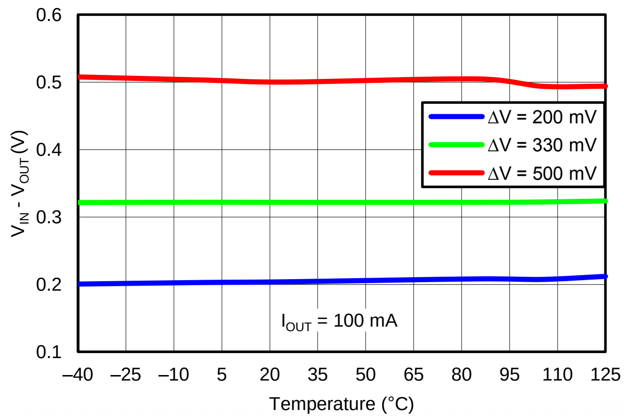


Figure 5. V_{DELTA} vs TEMPERATURE

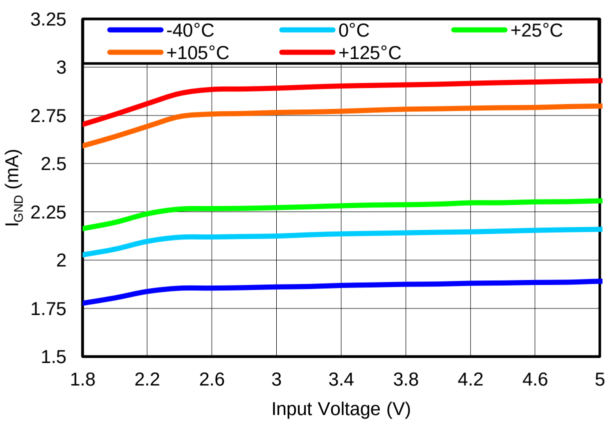


Figure 6. GROUND CURRENT vs INPUT VOLTAGE

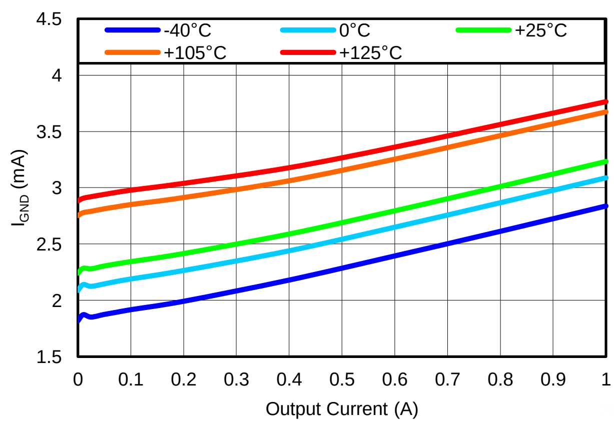


Figure 7. GROUND CURRENT vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 3.6 V, R_{NR} = ∞ (not connected), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 10.0 µF, C_{IN} = 10 µF, and C_{NR} = 0.1 µF, unless otherwise noted.

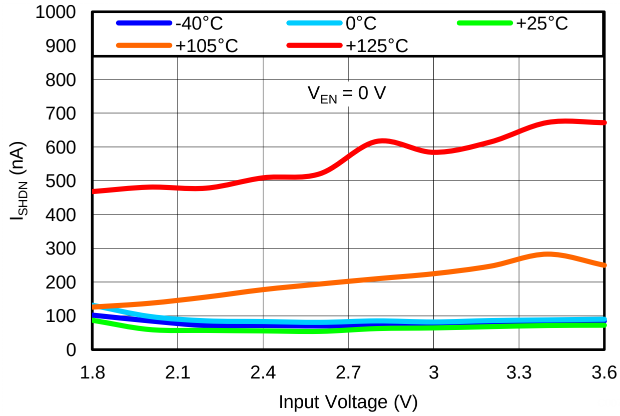


Figure 8. SHUTDOWN CURRENT vs INPUT VOLTAGE

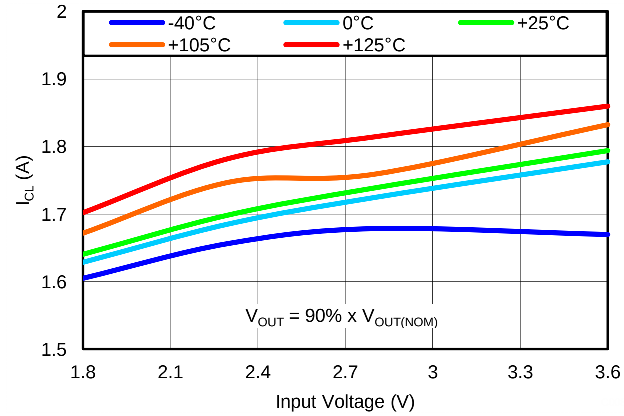


Figure 9. CURRENT LIMIT vs INPUT VOLTAGE

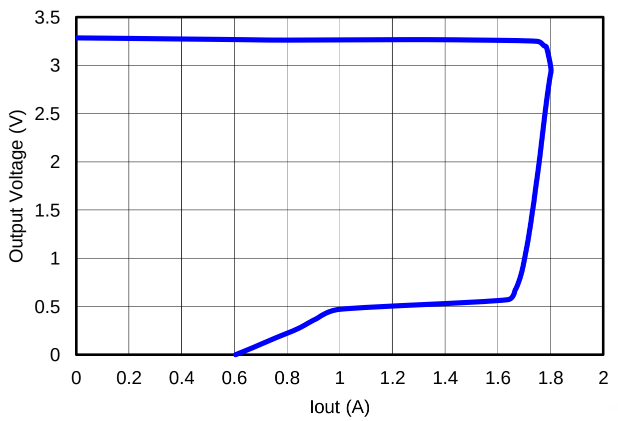


Figure 10. FOLDBACK CURRENT LIMIT

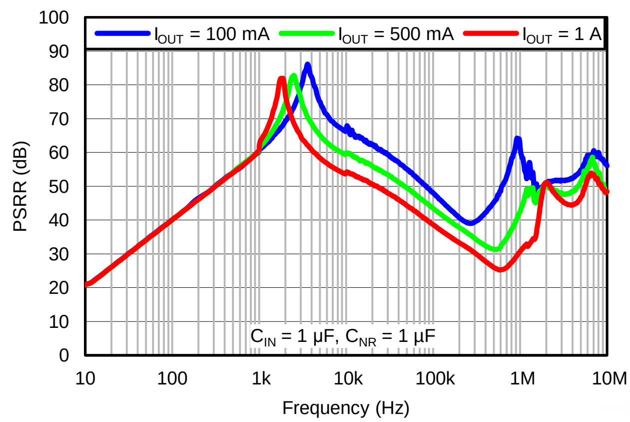


Figure 11. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

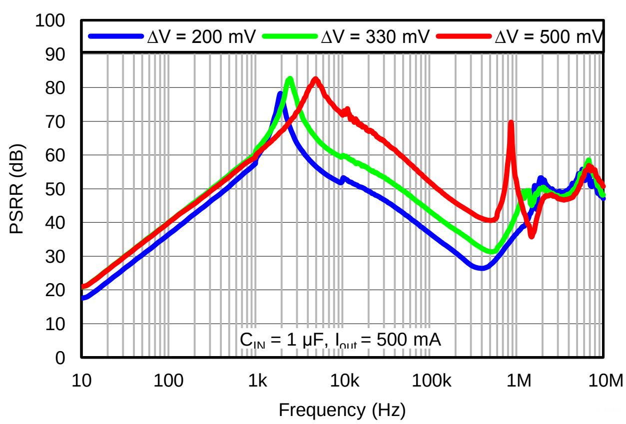


Figure 12. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

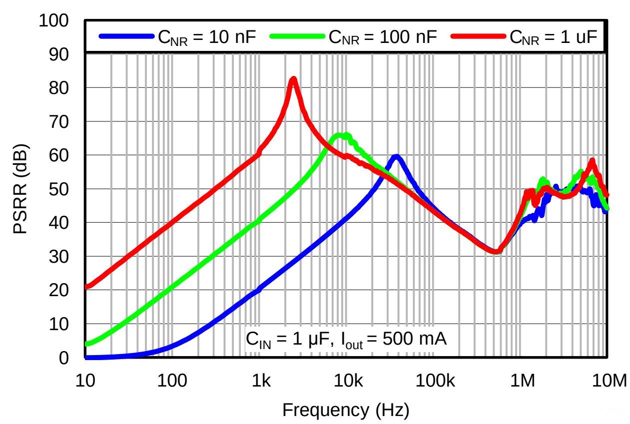


Figure 13. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 3.6 V, R_{NR} = ∞ (not connected), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 10.0 µF, C_{IN} = 10 µF, and C_{NR} = 0.1 µF, unless otherwise noted.

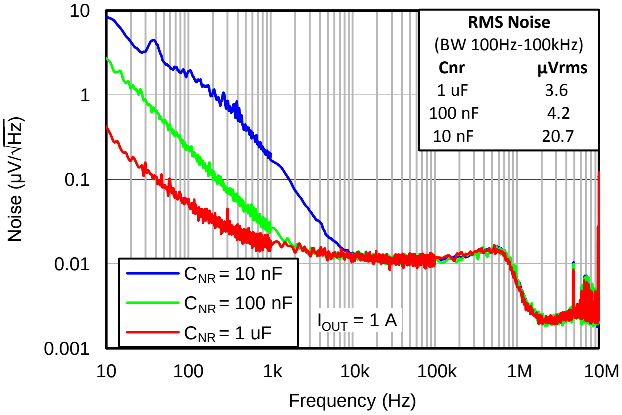


Figure 14. SPECTRAL NOISE DENSITY vs FREQUENCY

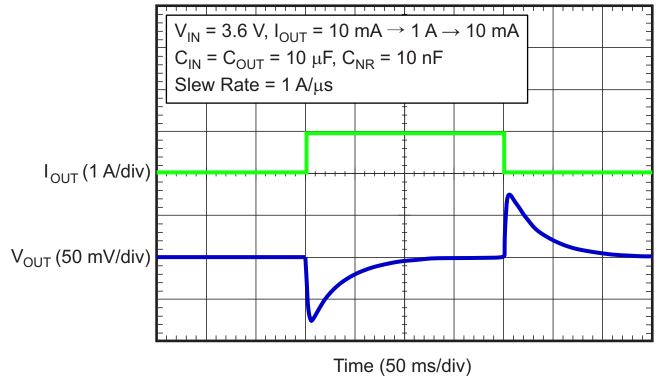


Figure 15. LOAD TRANSIENT RESPONSE

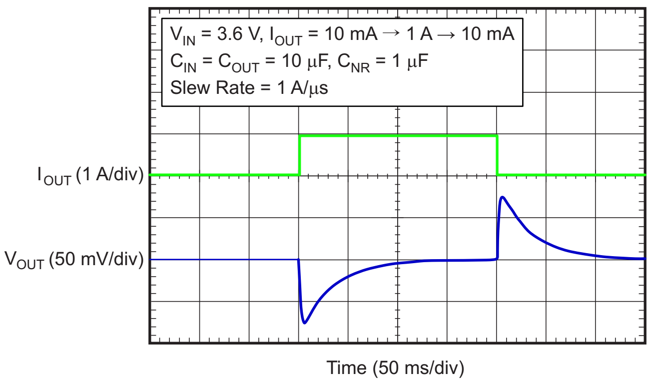


Figure 16. LOAD TRANSIENT RESPONSE

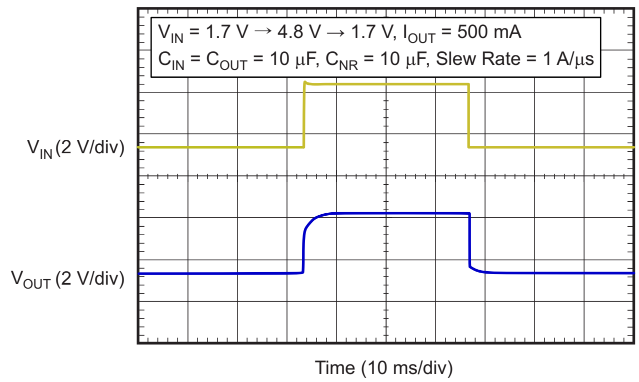


Figure 17. LINE TRANSIENT RESPONSE

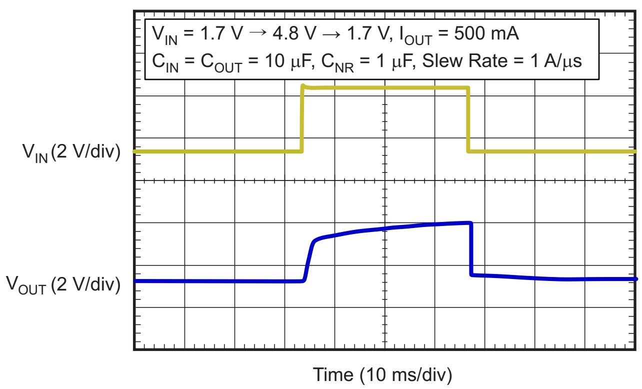


Figure 18. LINE TRANSIENT RESPONSE

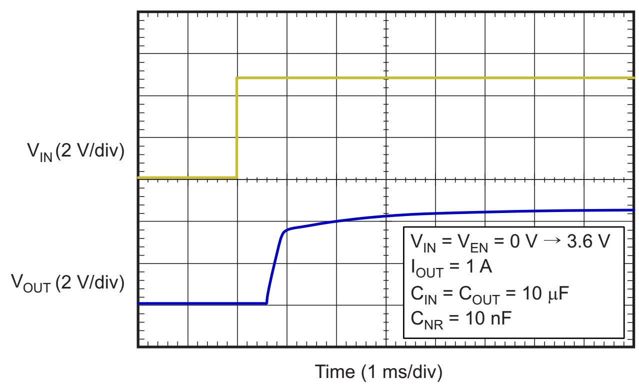


Figure 19. STARTUP

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 3.6 V, R_{NR} = ∞ (not connected), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 10.0 µF, C_{IN} = 10 µF, and C_{NR} = 0.1 µF, unless otherwise noted.

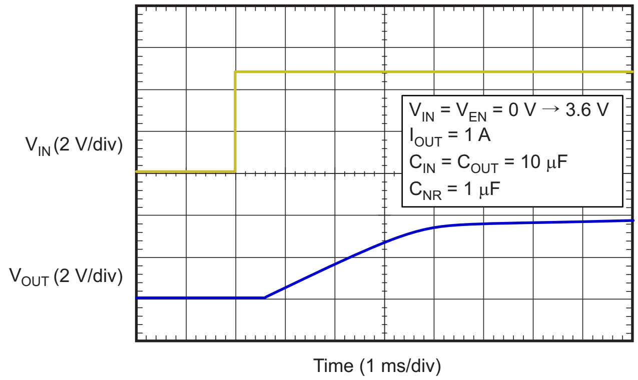


Figure 20. STARTUP

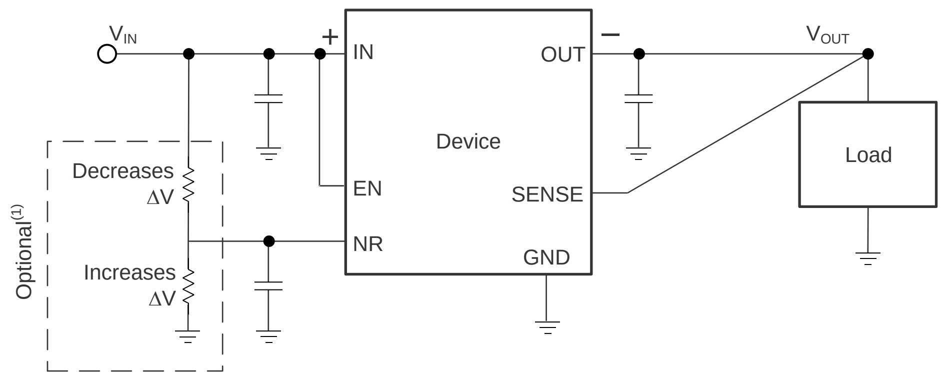
APPLICATION INFORMATION

The TPS7A3501 is a positive-voltage, low-noise (3.8-µV_{RMS}) power filter capable of sourcing a 1-A load. Power filters, such as the TPS7A3501, provide voltage regulation across the input and output terminals with high accuracy and power-supply rejection ratio. The device is ideally-suited as a noise filter for 4.5-V, 3.3-V, and 1.8-V supplies up to 1-A loads.

The input-to-output voltage drop is also user-programmable, from 200 mV up to 500 mV, with an external resistor. If no resistor is used, the TPS7A3501 provides 330 mV of input-to-output voltage regulation.

The TPS7A3501 is stable with 10-µF ceramic input and output capacitors and a 10-nF ceramic noise-reduction capacitor. The device is fully specified over a wide temperature range of –40°C to +125°C and is offered in a low thermal resistance, 2-mm × 2-mm, SON-6 package.

Figure 21 shows the basic circuit connections for the TPS7A3501. The IN pin should be connected to a well-regulated power source, typically a switching power supply.



(1) Refer to Table 2.

Figure 21. Basic Circuit Connections

POWER FILTER OPERATION

A power filter is very similar to a low-dropout (LDO) regulator, except that instead of regulating output voltage relative to ground, the power filter regulates output voltage relative to V_{IN}. In other words, a power filter maintains a fixed ΔV from input to output. The device is optimized for high PSRR with a low V_{IN}-to-V_{OUT} delta, leading to a lower power dissipation than standard LDOs. Unlike a standard LDO, the band gap and noise associated with the device are never gained up, resulting in low output noise regardless of V_{OUT}. The external noise capacitor on the power filter allows the user to set the frequency at which the power filter starts rejecting noise from the input. Table 1 summarizes the differences between a power filter and a high-performance LDO.

Table 1. Power Filter vs LDO Characteristics

PARAMETER	POWER FILTER	LDO
Voltage regulation	Regulates input-to-output delta. Voltage delta can be set from 0.2 V to 0.5 V. Relies on the upstream power rail to set the output voltage.	Regulates the output voltage referenced to ground. Outputs any output voltage within the output voltage range (limited by power dissipation).
PSRR	High PSRR at typical switching frequencies of dc/dc converters with lower power dissipation. Lower PSRR at low frequencies.	High PSRR over broad bandwidth. Effective rejection of low-frequency noise and switching noise from dc/dc.
Noise	Lower noise, 3.8 µV. Noise is not gained up when V_{OUT} increases.	Low noise (typically in the range of 5 µV_{RMS} to 20 µV_{RMS}). Noise is gained up when V_{OUT} increases.
Power dissipation	High PSRR can be achieved with only 330 mV from V_{IN} to V_{OUT}.	Typically requires 750 mV to 1 V of V_{IN}-to-V_{OUT} delta to achieve high PSRR.

ADJUSTABLE VOLTAGE DROP

In the TPS7A3501, the nominal voltage drop (ΔV) from IN to OUT is 330 mV. ΔV can be adjusted from this nominal setting with an external resistor. By connecting a resistor from the NR pin to IN, ΔV can be decreased to as low as 200 mV. By connecting a resistor from the NR pin to GND, ΔV can be increased to as high as 500 mV. The ability to change ΔV allows for the creation of standard voltage rails from higher voltage rails (for example, 2.5 V from 3.0 V, 1.5 V from 1.8 V, and so forth).

By connecting a resistor from the NR pin to IN, ΔV can be decreased to as low as 200 mV. Use Equation 1 to determine the size of the resister required to set ΔV.

$$R = \Delta V / (0.33 - \Delta V) \times 150{,}000\ \Omega \quad (1)$$

By connecting a resistor from the NR pin to GND, ΔV can be increased to as high as 500 mV. Use Equation 2 to determine the size of the resister required to set ΔV.

$$R = V_{OUT} / (\Delta V - 0.33) \times 150{,}000\ \Omega \quad (2)$$

Table 2 lists the standard external resistor values required for different input-to-output voltage drops.

Table 2. Common Input-to-Output Voltage Drops

ΔV (mV)	V_{OUT}	R TO V_{IN}	R TO GND
200	Any	240 kΩ	Do not install
330	Any	Do not install	Do not install
400	3.3 V	Do not install	6.8 MΩ
	2.5 V	Do not install	5.1 MΩ
	1.8 V	Do not install	3.9 MΩ
500	3.3 V	Do not install	3 MΩ
	2.5 V	Do not install	2.2 MΩ
	1.8 V	Do not install	1.6 MΩ

CAPACITOR SELECTION AND RESPONSE

Input and Output Capacitor Requirements

Ceramic 10-µF or larger input and output capacitors are required to assure proper device operation. This capacitor counteracts reactive source impedances, improving supply transient response and decreasing input ripple. Higher-value capacitors may be used if large, fast slew rate load transients are anticipated, or if the device is located several inches away from the power source. To assure correct device operation, there should be no more than 100 µF of capacitance on the output of the device, including capacitance from downstream bypass capacitors.

X5R- and X7R-type ceramic capacitors are recommended because these types of capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Other types of capacitors, such as electrolytic or tantalum, can make the device unstable.

NR Capacitor Effects

Output Noise

A 10-nF, or higher, noise-reduction capacitor is required to assure stability. Using a 1-µF ceramic capacitor minimizes output noise (see Figure 14). To assure correct device operation, a maximum capacitor of 2.2 µF can be connected to NR.

Power-Supply Rejection Ratio (PSRR)

Unlike standard LDOs, the TPS7A3501 PSRR is significantly affected by the noise-reduction capacitor. The larger the noise-reduction capacitor, the higher the PSRR is for frequencies below 10 kHz. Using a 1-µF ceramic capacitor maximizes PSRR.

One of the most compelling features of the TPS7A3501 is its high PSRR capabilities. The rejection ratio for this device is lower than standard LDOs at frequencies below 1 kHz but becomes higher at higher frequencies. For better low-frequency PSRR performance, a larger noise-reduction capacitor can be used. Connecting a 1-µF ceramic capacitor to NR is recommended to maximize PSRR (see Figure 13). A higher input-to-output voltage difference also increases the device rejection ratio. Although the device maximizes rejection ratio at 500 mV, high rejection ratio can still be achieved with as little as a 330-mV input-to-output voltage differential, unlike most standard LDOs.

Startup

Because adding a noise-reduction capacitor leads to the formation of an RC filter, startup time and the rate at which the device tracks V_{IN} are increased. Thus, consider the tradeoff between startup time, noise, and PSRR when selecting a noise-reduction capacitor to use with the TPS7A3501. Use Equation 3 to calculate the typical startup time.

$$T\_startup = 250{,}000 \times C_{NR}\ (s) \tag{3}$$

Table 3 shows the effect of various noise-reduction capacitors on RMS noise (with a 100-Hz to 100-kHz bandwidth), PSRR (at 1 kHz), and startup time.

Table 3. Effect of Various Filter Capacitors

FILTER CAPACITOR	RMS NOISE (BW 100 kHz to 100 kHz)	PSRR (at 1 kHz)	START-UP TIME (EN to 90% of V_{OUT})
1 µF	3.62 µV	60 dB	250 ms
100 nF	4.21 µV	40 dB	25 ms
10 nF	20.70 µV	20 dB	3 ms

Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude during transients; however this size increase also slows the recovery from these transients.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. All components are recommended to be on the same side of the printed circuit board (PCB) as the device. Using long, thin traces or vias to connect the device to external components is highly discouraged because this practice leads to parasitic inductances, which in turn degrade noise, PSRR, and transient response. For an example layout, refer to the *TPS7A3501EVM-547 Evaluation Module User Guide* (SLVU921).

Minimum Load

The device is stable without an output load.

Shutdown

The enable pin (EN) is active high and compatible with standard and low-voltage TTL-CMOS levels. The enable pin voltage level is independent of input voltage and can be biased to a higher value than V_{IN} as long as EN is within the maximum specification. When shutdown capability is not required, EN can be connected to IN.

Internal Current Limit

The device has an internal foldback current limit that helps protect the power filter during fault conditions. The current supplied by the device is gradually reduced when the output voltage decreases. When the output is shorted to GND, the LDO supplies a typical current of 550 mA. When in current limit, the output voltage is not regulated and $V_{OUT} = I_{OUT} \times R_{LOAD}$. For reliable operation, the device should not be operated in current limit for extended periods of time.

Because of the nature of the foldback current limit circuitry, if OUT is forced below 0 V before EN goes high, the device may not start up. To ensure proper startup in applications that have both a positive and negative voltage rail, extra care must be taken to ensure that OUT is greater than or equal to 0 V. There are several ways to help ensure proper start-up for dual-rail applications:

- Enable the device before the negative rail and disable the device after the negative rail.
- Delaying the EN voltage with respect to IN voltage allows the internal pull-down resistor to discharge any residual voltage at OUT.
- If a faster discharge rate is required, or if EN is tied directly to IN, an external resistor from OUT to GND can be used.

Reverse Current

The TPS7A3501 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not internally limited, so if reverse voltage conditions are anticipated, external limiting may be required.

If there are potential situations where reverse current is expected, place a diode from OUT to IN, as shown in Figure 22.

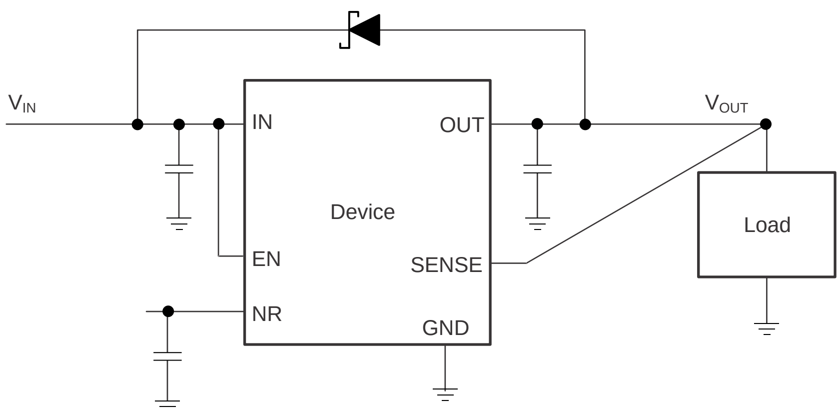


Figure 22. Reverse Current Protection Schematic

Undervoltage Lockout (UVLO)

The device uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly, thus ensuring a well-controlled startup.

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits device power dissipation, thus protecting the device from damage resulting from overheating.

Any activation of the thermal protection circuit indicates excessive power dissipation or inadequate thermal dissipation on the PCB. For reliable operation, limit junction temperature to +125°C (maximum). To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered using worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the application. This configuration produces a worst-case junction temperature of +125°C at the highest-expected ambient temperature and worst-case load.

The device internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat-sinking or thermal dissipation on the PCB. Continuously running the device into thermal shutdown degrades device reliability.

Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation. Device power dissipation depends on input voltage and load conditions and can be calculated with Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest available voltage drop option of 200 mV. However, an important note to keep in mind is that higher voltage drops result in better PSRR performance.

On the SON (DRV) package, the primary conduction path for heat is through the exposed power pad to the printed circuit board (PCB). To ensure the device does not overheat, connect the pad to ground with an appropriate amount of copper PCB area through vias.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 5:

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (5)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the Thermal Information table is determined by the JEDEC standard for PCB and copper-spreading area and is to be used only as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper.

Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the power filter on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the Thermal Information table and are used in accordance with Equation 6.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 4,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (6)

Typical Application

The TPS7A3501 is well-suited for use as a filter for switching power supplies. The high PSRR of the device significantly reduces the ripple caused by the switching frequency as well as the subsequent harmonic frequencies. Figure 23 shows a schematic for filtering the output of a switching regulator using the TPS7A3501 to power an ADC.

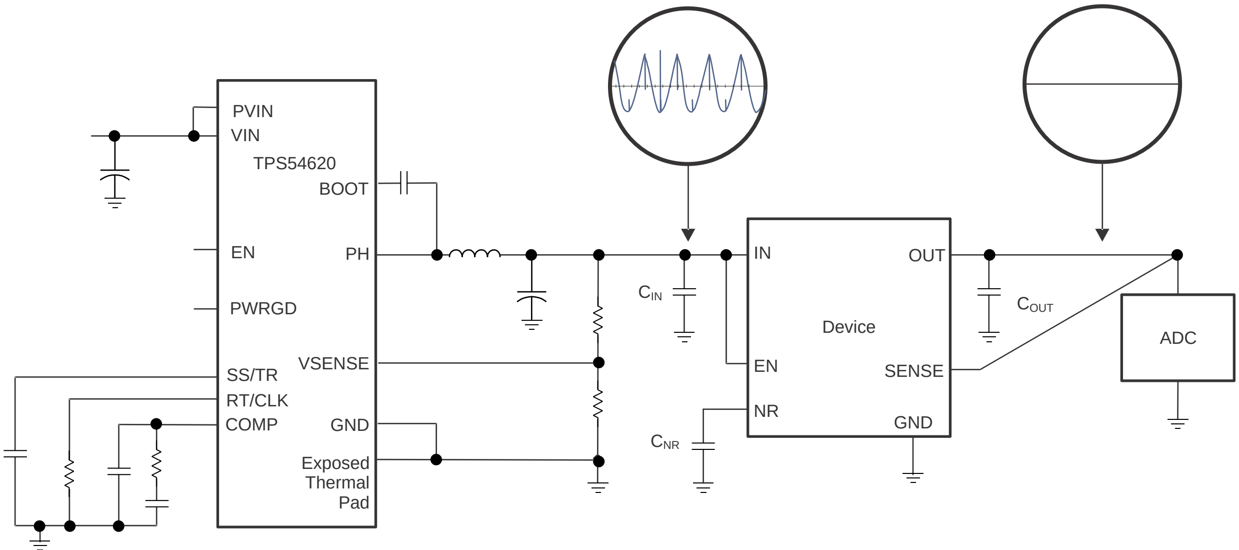


Figure 23. Typical Application Schematic

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2013) to Revision A — **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3501DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIQ	Samples
TPS7A3501DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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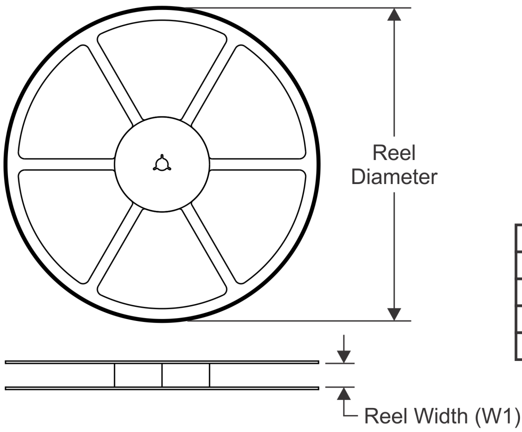
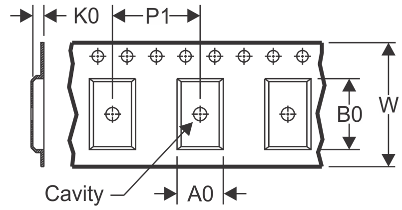
TAPE AND REEL INFORMATION

REEL DIMENSIONS

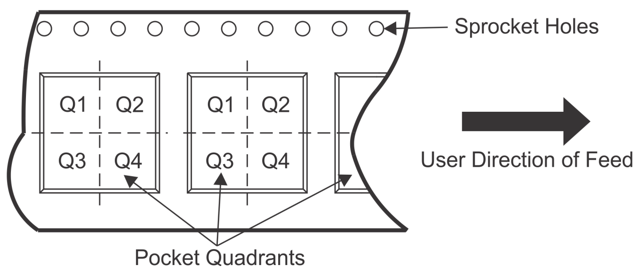


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

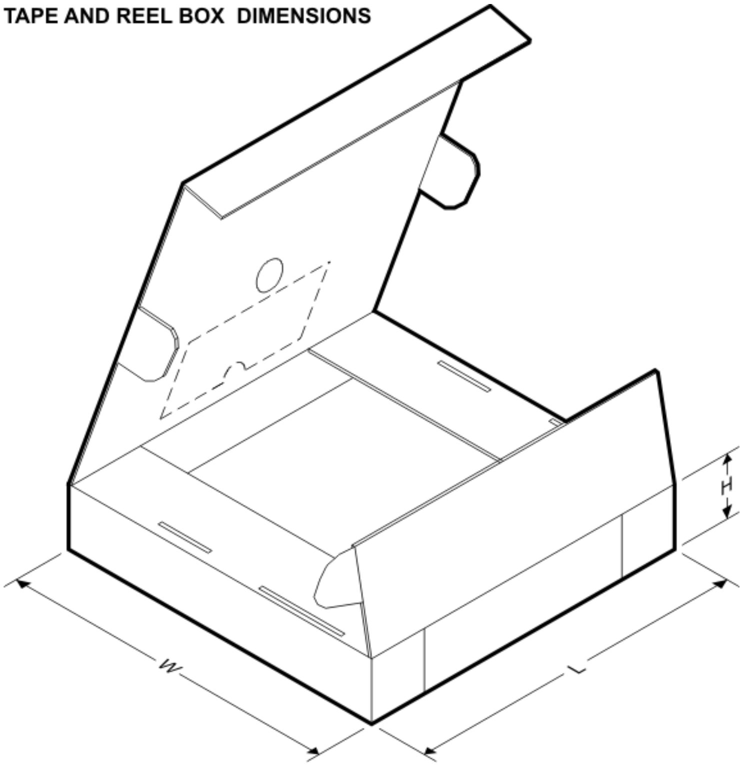
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3501DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A3501DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

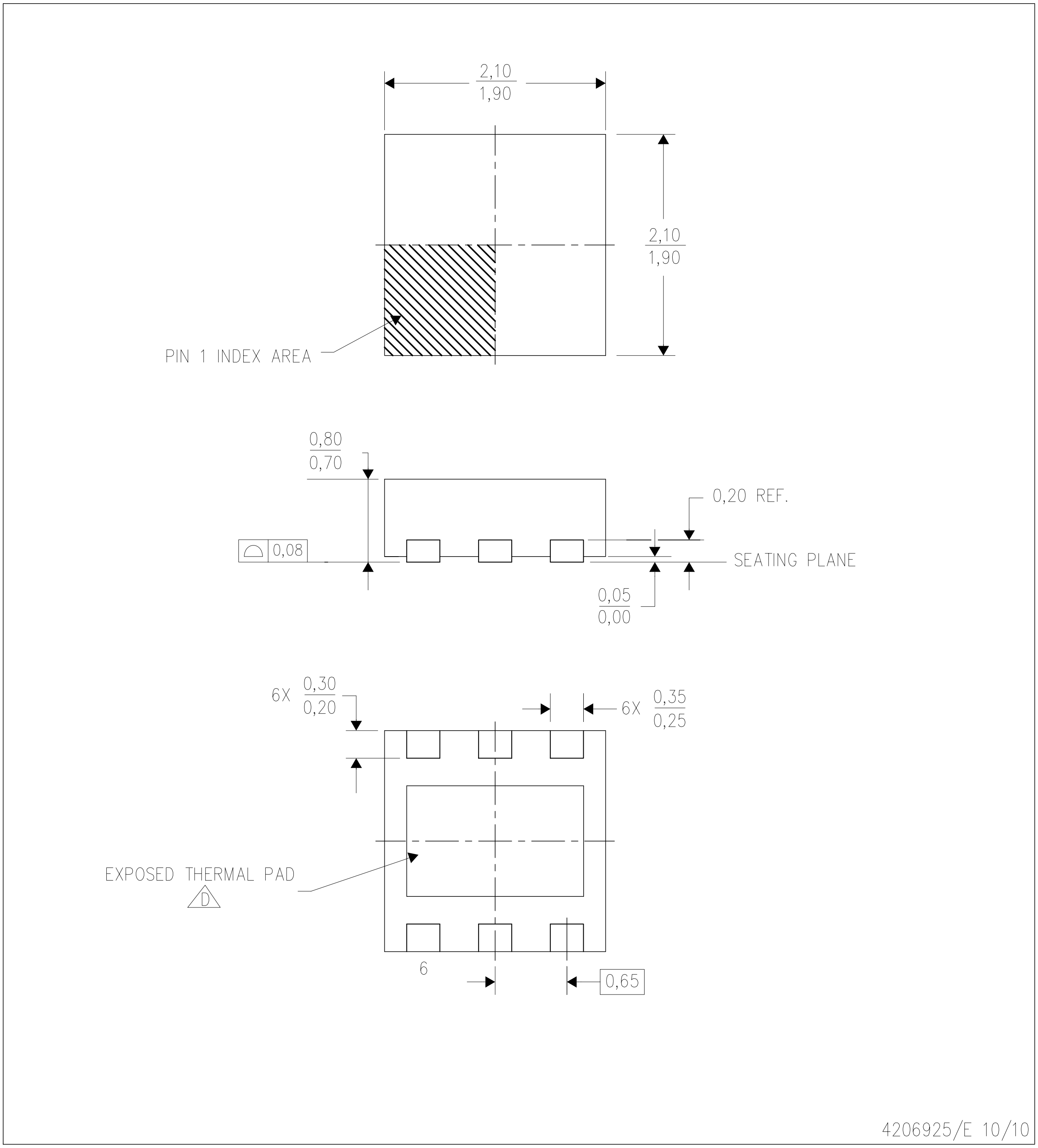
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3501DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS7A3501DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

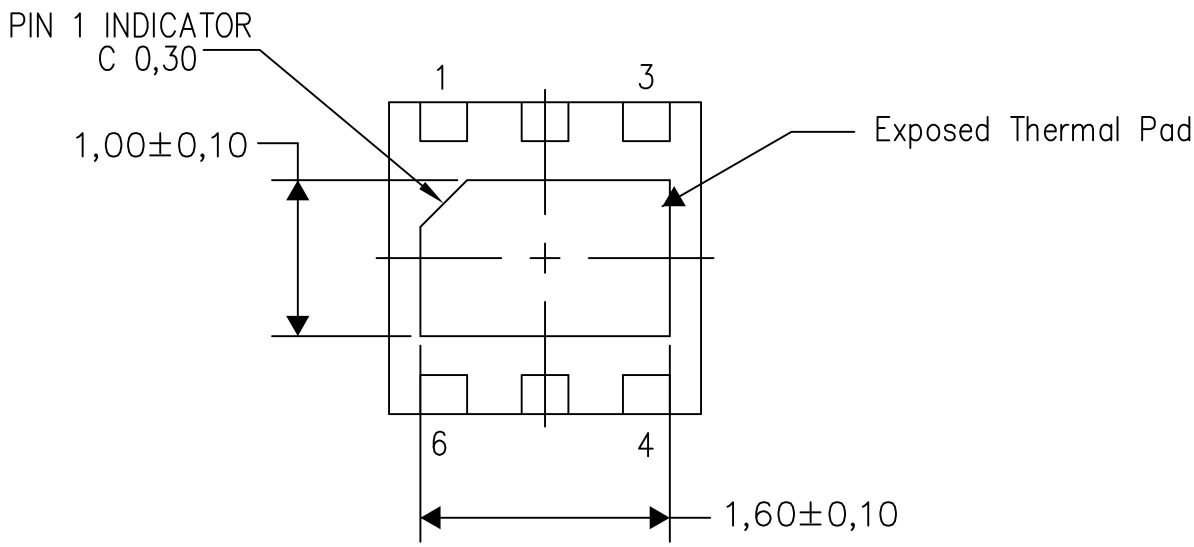
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



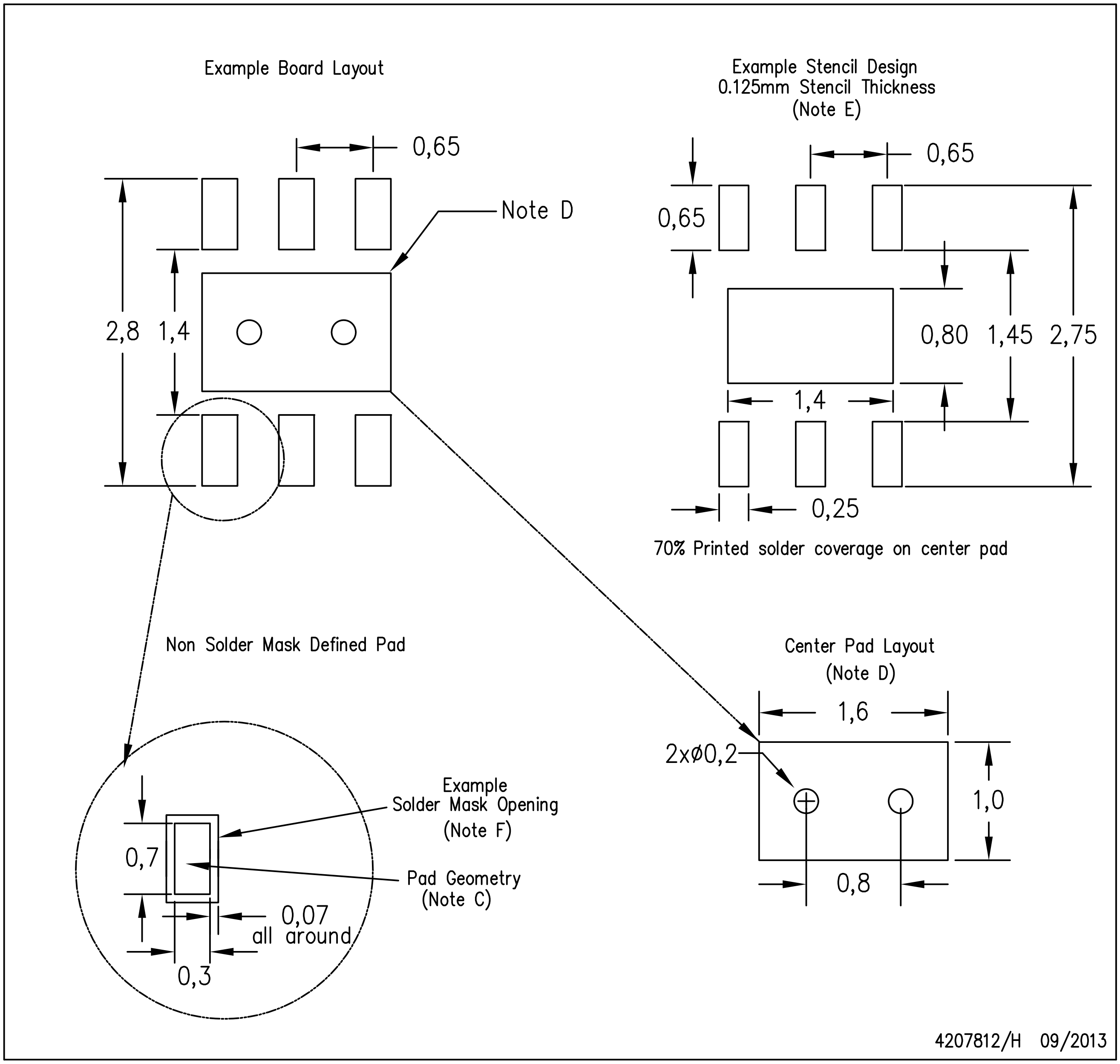
Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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