

## TPS7A16A-Q1

### 60-V, 5- $\mu$ A $I_Q$ , 100-mA, low-dropout voltage regulator with enable and power-good

#### 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C3B
- Wide input voltage range: 3 V to 60 V
- Ultralow quiescent current: 5  $\mu\text{A}$
- Quiescent current at shutdown: 1  $\mu\text{A}$
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed output voltage: 3.3 V, 5 V
  - Adjustable version from approximately 1.2 to 18.5 V
- Power-good with programable delay
- Current-limit and thermal shutdown protections
- Stable with ceramic output capacitors:  $\geq 2.2 \mu\text{F}$
- Package: high-thermal-performance HVSSOP-8 PowerPAD™

#### 2 Applications

- High cell-count battery packs for power tools and other battery-powered microprocessor and microcontroller systems
- Car audio, navigation, infotainment, and other automotive systems
- Power supplies for notebook PCs, digital TVs, and private LAN systems
- Smoke or  $\text{CO}_2$  detectors and battery-powered alarm or security systems

#### 3 Description

The TPS7A16A-Q1 ultralow-power, low-dropout (LDO) voltage regulators offer the benefits of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A-Q1 is designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A16A-Q1 offer an enable pin (EN) compatible with standard CMOS logic and an integrated open-drain active-high power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

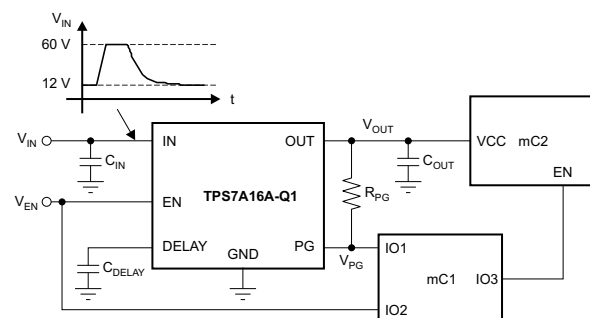
In addition, the TPS7A16A-Q1 is ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count power-tool packs to automotive applications; not only can these devices supply a well-regulated voltage rail, but they can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A16A-Q1	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Typical Application Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>11</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>11</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Applications .....	<b>11</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Power Supply Recommendations</b> .....	<b>17</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Layout</b> .....	<b>17</b>
6.1 Absolute Maximum Ratings .....	4	10.1 Layout Guidelines .....	17
6.2 ESD Ratings.....	4	10.2 Layout Examples.....	18
6.3 Recommended Operating Conditions .....	4	<b>11 Device and Documentation Support</b> .....	<b>20</b>
6.4 Thermal Information .....	4	11.1 Receiving Notification of Documentation Updates	20
6.5 Electrical Characteristics.....	5	11.2 Community Resources.....	20
6.6 Typical Characteristics.....	6	11.3 Trademarks .....	20
<b>7 Detailed Description</b> .....	<b>9</b>	11.4 Electrostatic Discharge Caution.....	20
7.1 Overview .....	9	11.5 Glossary .....	20
7.2 Functional Block Diagram .....	9	<b>12 Mechanical, Packaging, and Orderable</b>	
7.3 Feature Description.....	9	<b>Information</b> .....	<b>20</b>

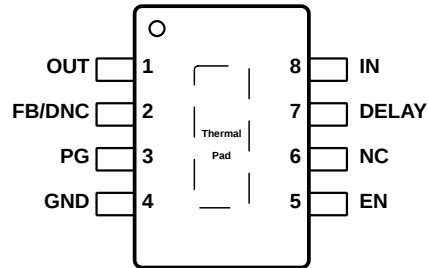
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2019	*	Initial release.

## 5 Pin Configuration and Functions

**DGN Package**  
**8-Pin HVSSOP With Exposed Thermal Pad**  
**Top View**



NC – No internal connection

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ , the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$ , the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	I	For the adjustable version (TPS7A16A-Q1), the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed voltage versions: <b>Do not connect</b> to this pin. Do not route this pin to any electrical net, not even GND or IN.
GND	4	—	Ground pin
IN	8	I	Regulator input supply pin. A capacitor > 0.1 $\mu$ F must be tied from this pin to ground to assure stability. It is recommended to connect a 10- $\mu$ F ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	---	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor > 2.2 $\mu$ F must be tied from this pin to ground to assure stability. It is recommended to connect a 10- $\mu$ F ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	O	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad		---	Solder to printed circuit board (PCB) to enhance thermal performance. Although it can be left floating, it is highly recommended to connect the thermal pad to the GND plane.

**ADVANCE INFORMATION**

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	-0.3	62	V
	OUT pin to GND pin	-0.3	20	
	OUT pin to IN pin	-62	0.3	
	FB pin to GND pin	-0.3	3	
	FB pin to IN pin	-62	0.3	
	EN pin to IN pin	-62	0.3	
	EN pin to GND pin	-0.3	62	
	PG pin to GND pin	-0.3	5.5	
	DELAY pin to GND pin	-0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T <sub>J</sub> , absolute maximum range <sup>(2)</sup>	-40	150	°C
	Storage temperature range	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	Corner pins (OUT, GND, IN, and EN)		±750
			Other pins		±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Unregulated input	3		60	V
V <sub>OUT</sub>	Regulated output	1.2		18.5	V
EN	Voltage	0		V <sub>IN</sub>	V
	Slew rate, voltage ramp-up			1.5	V/μs
DELAY		0		5	V
PG		0		5	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7A16A	UNIT
		DGN (HVSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	66.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	45.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	34.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	34.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	14.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 500\text{ mV}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\text{ }\mu\text{A}$ ,  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range		3		60	V
$V_{REF}$	Internal reference	$T_A = 25^\circ\text{C}$ , $V_{FB} = V_{REF}$ , $V_{IN} = 3\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$	1.169	1.193	1.217	V
$V_{UVLO}$	Undervoltage lockout threshold			2		V
$V_{OUT}$	Output voltage range	$V_{IN} \geq V_{OUT(NOM)} + 0.5\text{ V}$	$V_{REF}$		18.5	V
	Overall $V_{OUT}$ accuracy	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 60\text{ V}^{(1)}$ $10\text{ }\mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$	-2%		2%	
$\Delta V_{O(\Delta V)}$	Line regulation	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$		$\pm 1$		% $V_{OUT}$
$\Delta V_{O(\Delta I)}$	Load regulation	$10\text{ }\mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$		$\pm 1$		% $V_{OUT}$
$V_{DO}$	Dropout voltage	$V_{IN} = 0.95 \cdot V_{OUT(NOM)}$ , $I_{OUT} = 20\text{ mA}$		60		mV
		$V_{IN} = 0.95 \cdot V_{OUT(NOM)}$ , $I_{OUT} = 100\text{ mA}$		265	500	
$I_{LIM}$	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$ , $V_{IN} = V_{OUT(NOM)} + 1\text{ V}^{(2)}$	101	225	400	mA
		$V_{OUT} = 90\% V_{OUT(NOM)}$ , $V_{IN} = 3\text{ V}^{(3)}$	101	225	400	
$I_{GND}$	Ground current	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$		5	15	$\mu\text{A}$
		$I_{OUT} = 100\text{ mA}$ , $V_{OUT} = 1.2\text{ V}$		60		
$I_{SHDN}$	Shutdown supply current	$V_{EN} = 0.4\text{ V}$ , $V_{IN} = 12\text{ V}$		0.59	5.0	$\mu\text{A}$
$I_{FB}$	Feedback current <sup>(4)</sup>		-1	0.0	1	$\mu\text{A}$
$I_{EN}$	Enable current	$3\text{ V} \leq V_{IN} \leq 12\text{ V}$ , $V_{IN} = V_{EN}$	-1	0.01	1	$\mu\text{A}$
$V_{EN\_HI}$	Enable high-level voltage		1.2			V
$V_{EN\_LO}$	Enable low-level voltage				0.3	V
$V_{IT}$	PG trip threshold	OUT pin floating, $V_{FB}$ increasing, $V_{IN} \geq V_{IN\_MIN}$	85		95	% $V_{OUT}$
		OUT pin floating, $V_{FB}$ decreasing, $V_{IN} \geq V_{IN\_MIN}$	83		93	
$V_{HYS}$	PG trip hysteresis			2.3		% $V_{OUT}$
$V_{PG\_LO}$	PG output low voltage	OUT pin floating, $V_{FB} = 80\% V_{REF}$ , $I_{PG} = 100\text{ }\mu\text{A}$			0.4	V
$I_{PG\_LKG}$	PG leakage current	$V_{PG} = V_{OUT(NOM)}$	-1		1	$\mu\text{A}$
$I_{DELAY}$	DELAY pin current			1	2	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 3\text{ V}$ , $V_{OUT(NOM)} = V_{REF}$ , $C_{OUT} = 10\text{ }\mu\text{F}$ , $f = 100\text{ Hz}$		50		dB
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		175		$^\circ\text{C}$
		Reset, temperature decreasing		155		

- (1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ( $P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$ ). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
- (2) For fixed output voltages only
- (3) For adjustable output only, where  $V_{OUT} = 1.2\text{ V}$
- (4)  $I_{FB} > 0$  flows out of the device.

### 6.6 Typical Characteristics

at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

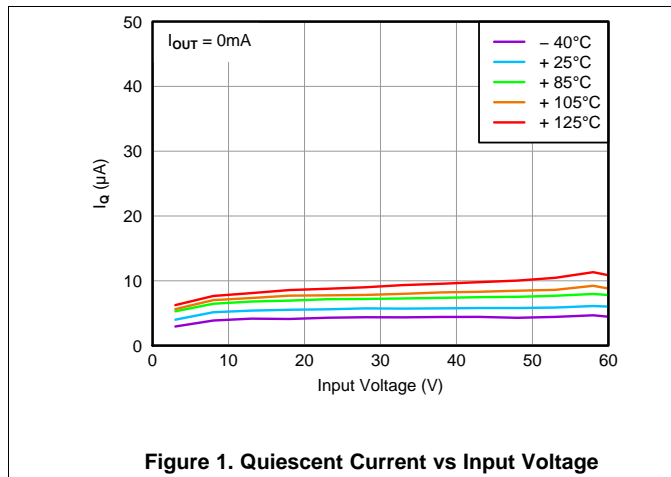


Figure 1. Quiescent Current vs Input Voltage

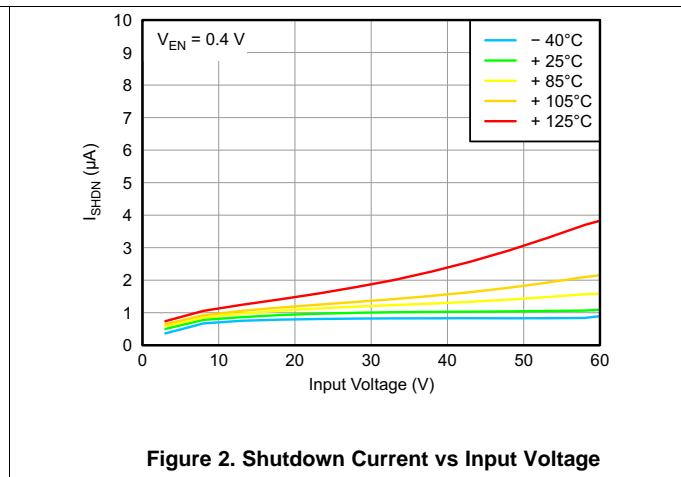


Figure 2. Shutdown Current vs Input Voltage

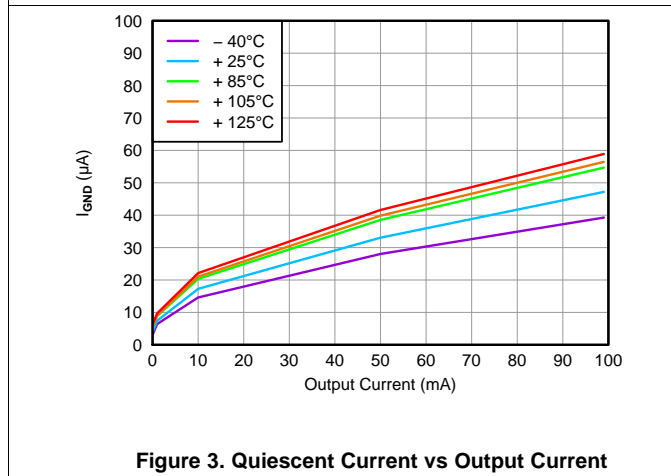


Figure 3. Quiescent Current vs Output Current

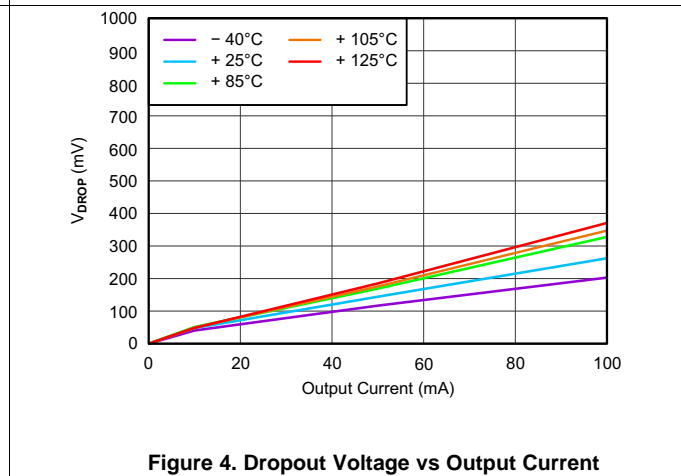


Figure 4. Dropout Voltage vs Output Current

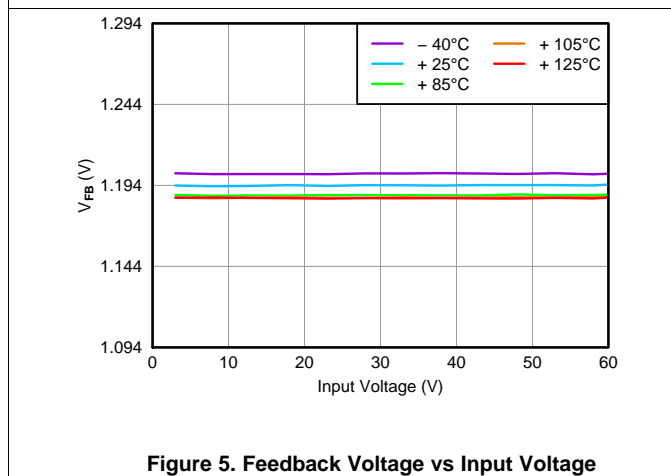


Figure 5. Feedback Voltage vs Input Voltage

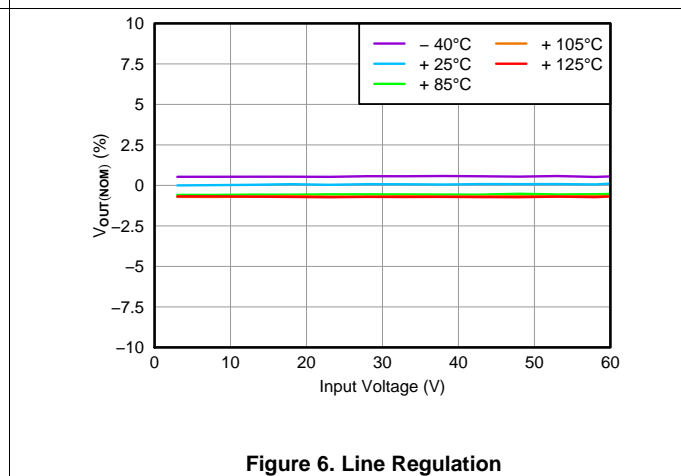


Figure 6. Line Regulation

ADVANCE INFORMATION

Typical Characteristics (continued)

at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

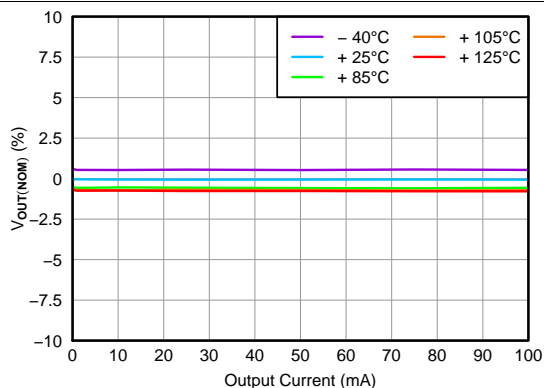


Figure 7. Load Regulation

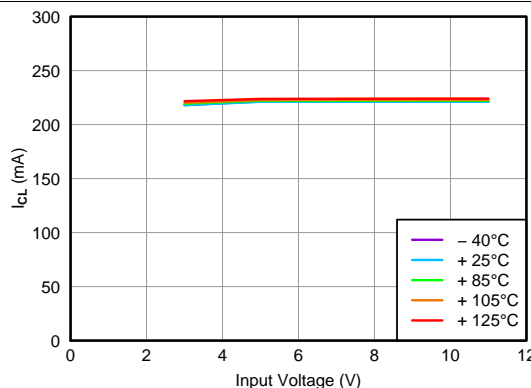


Figure 8. Current Limit vs Input Voltage

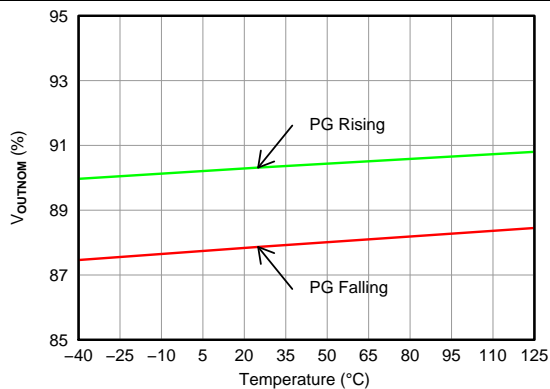


Figure 9. Power-Good Threshold Voltage vs Temperature

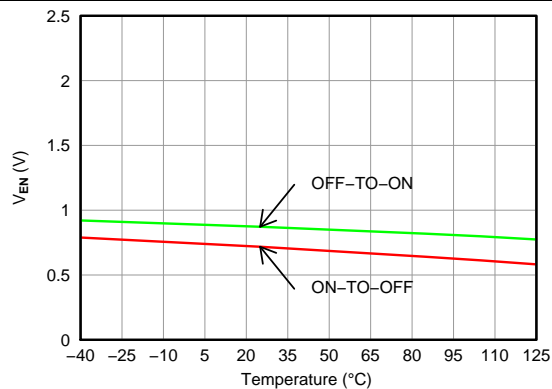


Figure 10. Enable Threshold Voltage vs Temperature

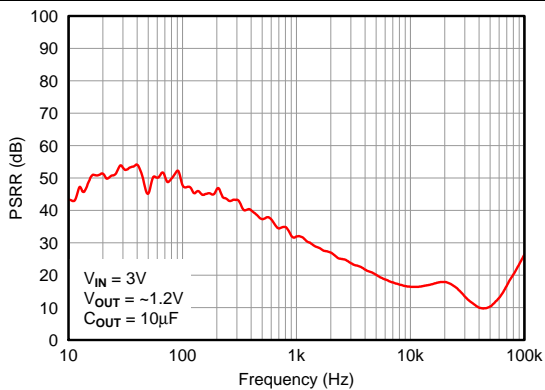


Figure 11. Power-Supply Rejection Ratio

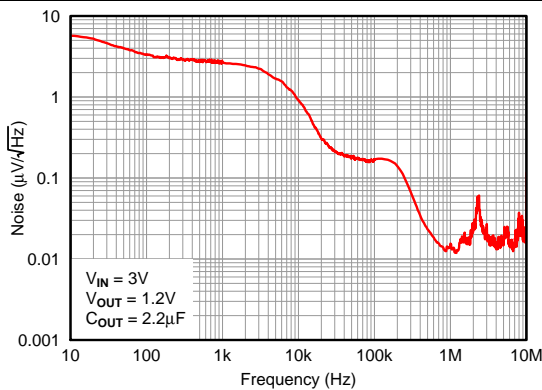
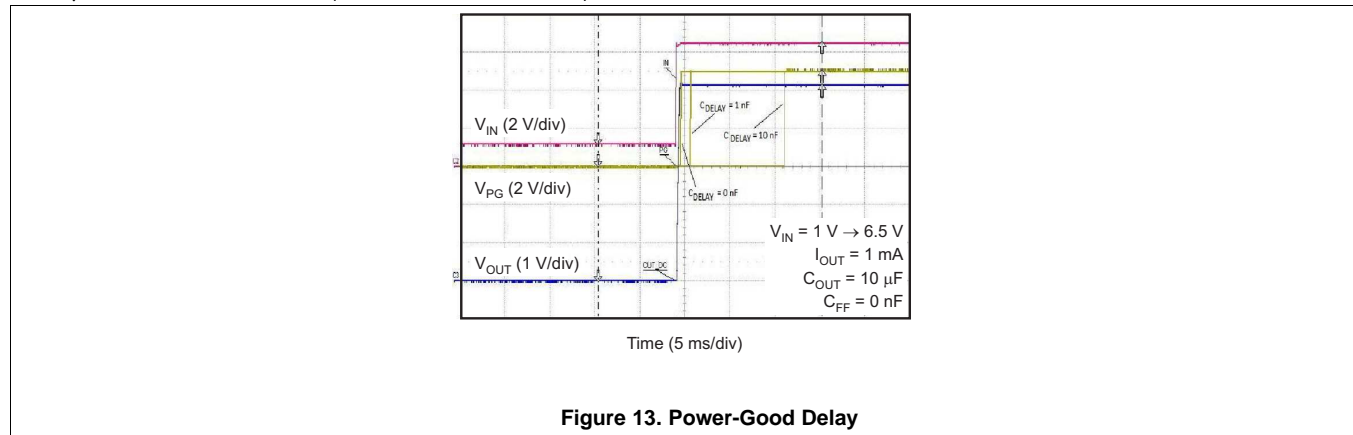


Figure 12. Output Spectral Noise Density

ADVANCE INFORMATION

**Typical Characteristics (continued)**

at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)



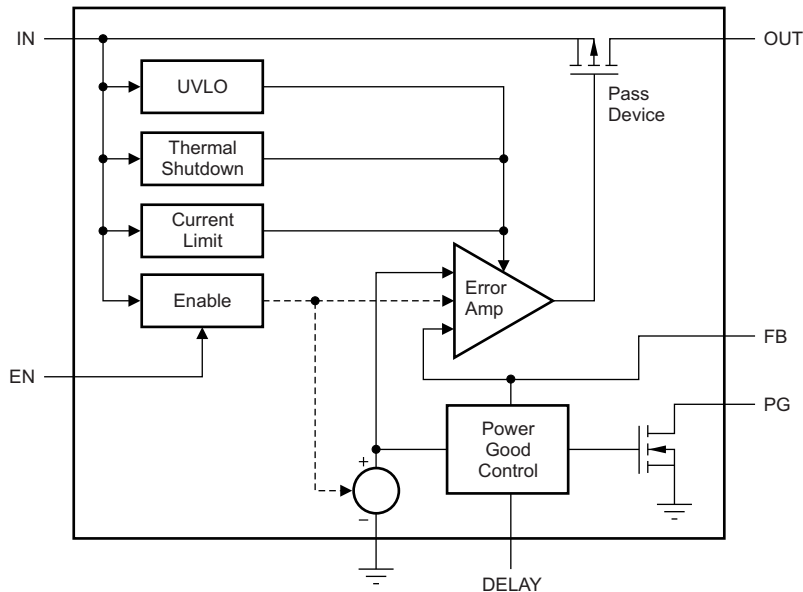


## 7 Detailed Description

### 7.1 Overview

The TPS7A16A-Q1 device is ultra low power, low-dropout (LDO) voltage regulators that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. TPS7A16A-Q1 also offers an enable pin (EN) and integrated open-drain active-high power-good output (PG) with a user-programmable delay.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Enable (EN)

The enable terminal is a high-voltage-tolerant terminal. A high input on EN activates the device and turns on the regulator. For self-bias applications, connect this input to the  $V_{IN}$  terminal. Ensure that  $V_{EN} \leq V_{IN}$  at all times.

When the enable signal is PWM pulses, the slew rate of the rising and falling edges must be less than  $1.5 \text{ V}/\mu\text{s}$ . Adding a  $0.1\text{-}\mu\text{F}$  capacitor from the EN pin to GND is recommended.

#### 7.3.2 Regulated Output ( $V_{OUT}$ )

The  $V_{OUT}$  terminal is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

#### 7.3.3 PG Delay Timer (DELAY)

The power-good delay time ( $t_{DELAY}$ ) is defined as the time period from when  $V_{OUT}$  exceeds the PG trip threshold voltage ( $V_{IT}$ ) to when the PG output is high. This power-good delay time is set by an external capacitor ( $C_{DELAY}$ ) connected from the DELAY pin to GND; this capacitor is charged from  $0 \text{ V}$  to  $\sim 1.8 \text{ V}$  by the DELAY pin current ( $I_{DELAY}$ ) once  $V_{OUT}$  exceeds the PG trip threshold ( $V_{IT}$ ).

## 7.4 Device Functional Modes

### 7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no  $C_{\text{DELAY}}$  is used, the PG output is high-impedance when  $V_{\text{OUT}}$  is greater than the PG trip threshold ( $V_{\text{IT}}$ ). If  $V_{\text{OUT}}$  drops below  $V_{\text{IT}}$ , the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain  $V_{\text{IN}} \geq 3 \text{ V}$  ( $V_{\text{IN\_MIN}}$ ).

#### 7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time ( $t_{\text{DELAY}}$ ) is defined as the time period from when  $V_{\text{OUT}}$  exceeds the PG trip threshold voltage ( $V_{\text{IT}}$ ) to when the PG output is high. This power-good delay time is set by an external capacitor ( $C_{\text{DELAY}}$ ) connected from the DELAY pin to GND; this capacitor is charged from 0 V to up to 1.8 V by the DELAY pin current ( $I_{\text{DELAY}}$ ) once  $V_{\text{OUT}}$  exceeds the PG trip threshold ( $V_{\text{IT}}$ ).

When  $C_{\text{DELAY}}$  is used, the PG output is high-impedance when  $V_{\text{OUT}}$  exceeds  $V_{\text{IT}}$ , and  $V_{\text{DELAY}}$  exceeds  $V_{\text{REF}}$ .

The power-good delay time can be calculated using:  $t_{\text{DELAY}} = (C_{\text{DELAY}} \times V_{\text{REF}}) / I_{\text{DELAY}}$ . For example, when  $C_{\text{DELAY}} = 10 \text{ nF}$ , the PG delay time is approximately 12 ms; that is,  $(10 \text{ nF} \times 1.193 \text{ V}) / 1 \mu\text{A} = 11.93 \text{ ms}$ .

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7A16A-Q1 of ultralow-power voltage regulators offers the benefit of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A-Q1 is designed for continuous or sporadic (power backup) battery-operated applications where ultralow quiescent current is critical to extending system battery life.

### 8.2 Typical Applications

#### 8.2.1 TPS7A16A-Q1 Circuit as an Adjustable Regulator

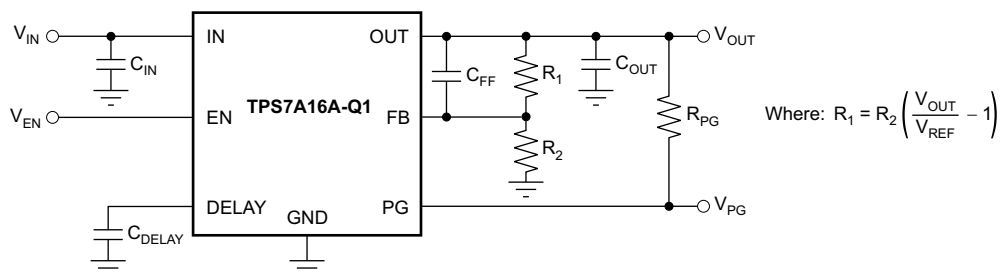


Figure 14. TPS7A16A-Q1 Circuit as an Adjustable Regulator Schematic

#### 8.2.1.1 Design Requirements

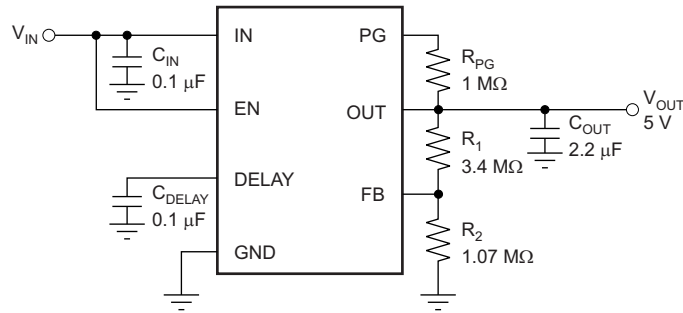
Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Delay capacitor range	100 pF to 100 nF

#### 8.2.1.2 Detailed Design Procedure

##### 8.2.1.2.1 Adjustable Voltage Operation

The TPS7A16A-Q1 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in [Figure 15](#):


**Figure 15. Adjustable Operation**

$R_1$  and  $R_2$  can be calculated for any output voltage range using the formula shown in [Equation 1](#):

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

#### 8.2.1.2.1 Resistor Selection

It is recommended to use resistors in the order of  $M\Omega$  to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

[Table 2](#) shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in [Equation 1](#).

**Table 2. Selected Resistor Combinations**

$V_{OUT}$	$R_1$	$R_2$	$V_{OUT}/(R_1 + R_2) \ll I_Q$	NOMINAL ACCURACY
1.194 V	0 $\Omega$	$\infty$	0 $\mu A$	$\pm 2\%$
1.8 V	1.18 $M\Omega$	2.32 $M\Omega$	514 nA	$\pm(2\% + 0.14\%)$
2.5 V	1.5 $M\Omega$	1.37 $M\Omega$	871 nA	$\pm(2\% + 0.16\%)$
3.3 V	2 $M\Omega$	1.13 $M\Omega$	1056 nA	$\pm(2\% + 0.35\%)$
5 V	3.4 $M\Omega$	1.07 $M\Omega$	1115 nA	$\pm(2\% + 0.39\%)$
10 V	7.87 $M\Omega$	1.07 $M\Omega$	1115 nA	$\pm(2\% + 0.42\%)$
12 V	14.3 $M\Omega$	1.58 $M\Omega$	755 nA	$\pm(2\% + 0.18\%)$
15 V	42.2 $M\Omega$	3.65 $M\Omega$	327 nA	$\pm(2\% + 0.19\%)$
18 V	16.2 $M\Omega$	1.15 $M\Omega$	1038 nA	$\pm(2\% + 0.26\%)$

Close attention must be paid to board contamination when using high-value resistors; board contaminants may significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16A-Q1 or using resistors in the order of hundreds or tens of  $k\Omega$ .

#### 8.2.1.2.2 Capacitor Recommendations

Low equivalent-series-resistance (ESR) capacitors should be used for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high-ESR capacitors may degrade PSRR.

### 8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16A-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1  $\mu\text{F}$  and output capacitance of 2.2  $\mu\text{F}$ ; however, it is recommended to use a 10- $\mu\text{F}$  ceramic capacitor to maximize ac performance.

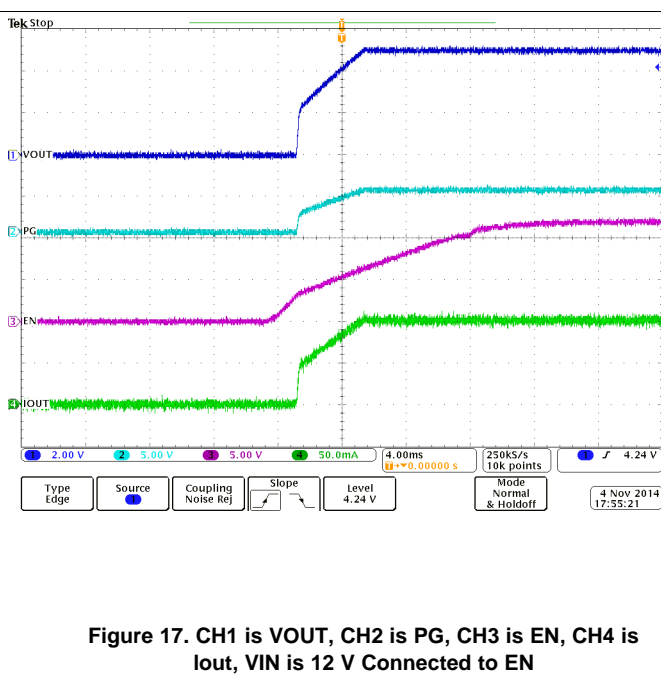
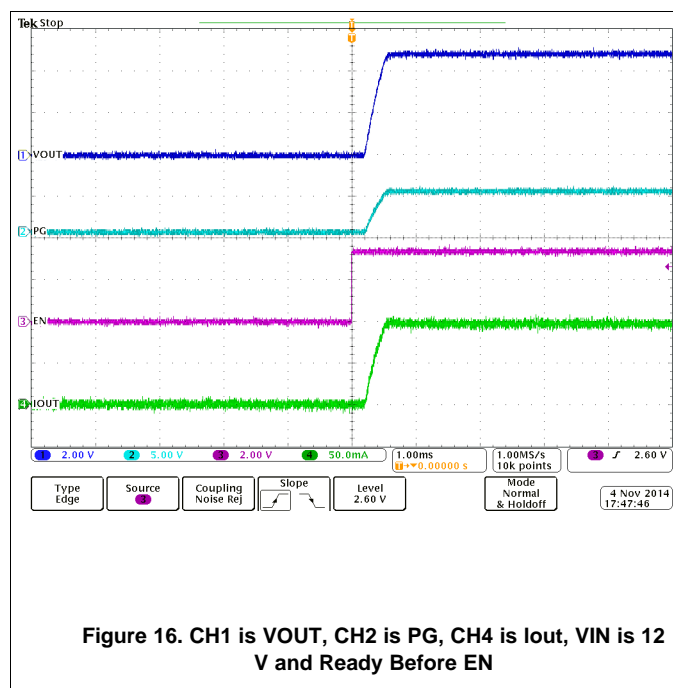
### 8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor ( $C_{FF}$ ) from OUT to FB is not needed to achieve stability, it is recommended to use a 0.01- $\mu\text{F}$  feed-forward capacitor to maximize ac performance.

### 8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases the duration of the transient response.

### 8.2.1.3 Application Curves



ADVANCE INFORMATION

### 8.2.2 Automotive Applications

The TPS7A16A-Q1 maximum input voltage of 60 V makes it ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) may cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16A-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

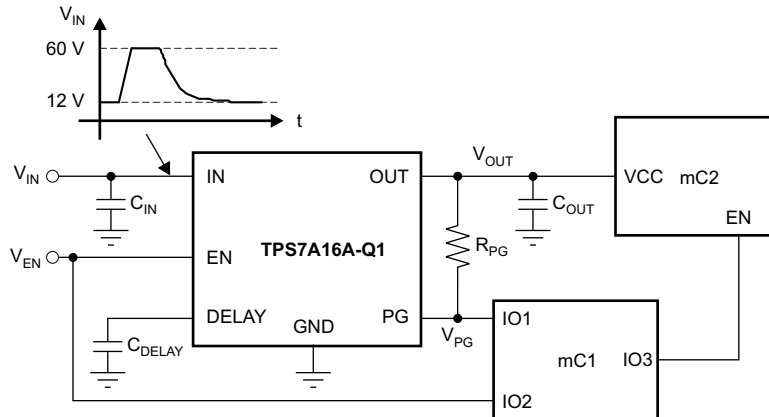


Figure 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

#### 8.2.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Delay capacitor range	100 pF to 100 nF

#### 8.2.2.2 Detailed Design Procedure

See [Capacitor Recommendations](#) and [Input and Output Capacitor Requirements](#).

##### 8.2.2.2.1 Device Recommendations

The output is fixed, so choose TPS7A16A-Q1.

##### 8.2.2.3 Application Curves

See [Figure 16](#) and [Figure 17](#).

### 8.2.3 Multicell Battery Packs

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, may have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that may degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI's MSP430™. See the overview for microcontrollers (MCU) for more information.

The microcontroller continuously monitors the battery itself, whether the battery is in use or not. Although this microcontroller could be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack itself, degrading its life or adding cost to implement more complex cell balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

TPS7A16A-Q1 is the ideal regulator for this application because it can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

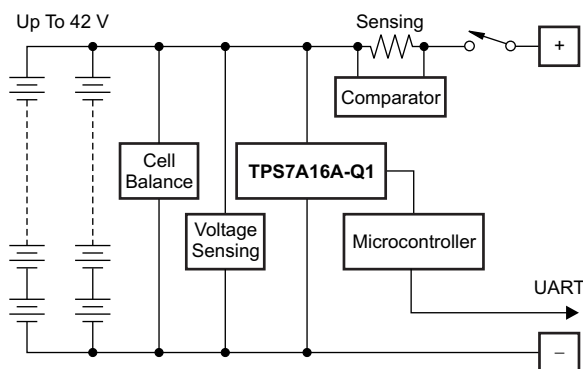


Figure 19. Protection Based on Low-Power Microcontroller Power From Multicell Battery Packs

#### 8.2.3.1 Design Requirements

Table 4. Device Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 55 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Delay capacitor range	100 pF to 100 nF

#### 8.2.3.2 Detailed Design Procedure

See [Device Recommendations](#), [Capacitor Recommendations](#), and [Input and Output Capacitor Requirements](#).

#### 8.2.3.3 Application Curves

See [Figure 16](#) and [Figure 17](#).

### 8.2.4 Battery-Operated Power Tools

High-voltage multicell battery packs support high-power applications, such as power tools, with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients because of the motor inductance.

The TPS7A16A-Q1 can be used to power the motor-controlled microcontroller or microprocessor; its low quiescent current maximizes battery shelf life, and its very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

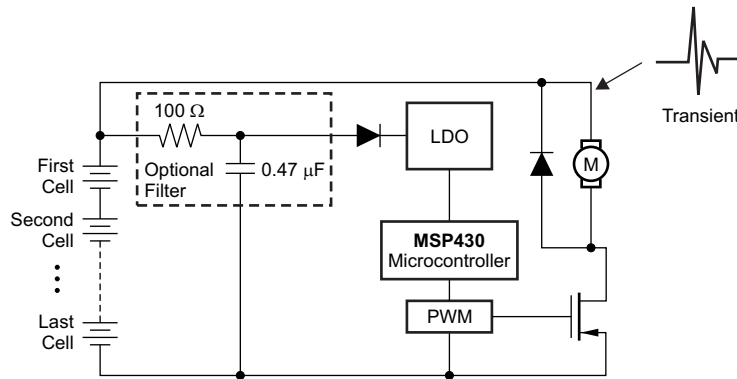


Figure 20. Low Power Microcontroller Power From Multi-Cell Battery Packs in Power Tools

#### 8.2.4.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 μF to 100 μF
Delay capacitor range	100 pF to 100 nF

#### 8.2.4.2 Detailed Design Procedure

See [Device Recommendations](#), [Capacitor Recommendations](#), and [Input and Output Capacitor Requirements](#).

#### 8.2.4.3 Application Curves

See [Figure 16](#) and [Figure 17](#).



## 9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. TPS7A16A-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1  $\mu\text{F}$  and output capacitance of 2.2  $\mu\text{F}$ ; however, it is recommended to use a 10- $\mu\text{F}$  ceramic capacitor to maximize AC performance.

## 10 Layout

### 10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A16A-Q1 evaluation board, available at [www.ti.com](http://www.ti.com).

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

[Figure 21](#) shows the schematic for the suggested layout. [Figure 22](#) and [Figure 23](#) show the top and bottom printed circuit board (PCB) layers for the suggested layout.

#### 10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, it is recommended to use a fixed-voltage version of the TPS7A16A-Q1, or to isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

#### 10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

## Layout Guidelines (continued)

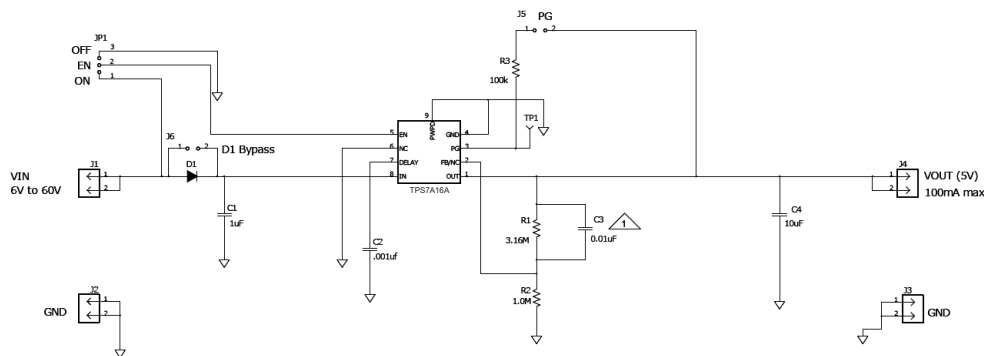
### 10.1.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, junction temperature should be limited to a maximum of 125°C at the worst case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16A-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A16A-Q1 into thermal shutdown degrades device reliability.

### 10.2 Layout Examples



**Figure 21. Schematic for Suggested Layout**

Layout Examples (continued)

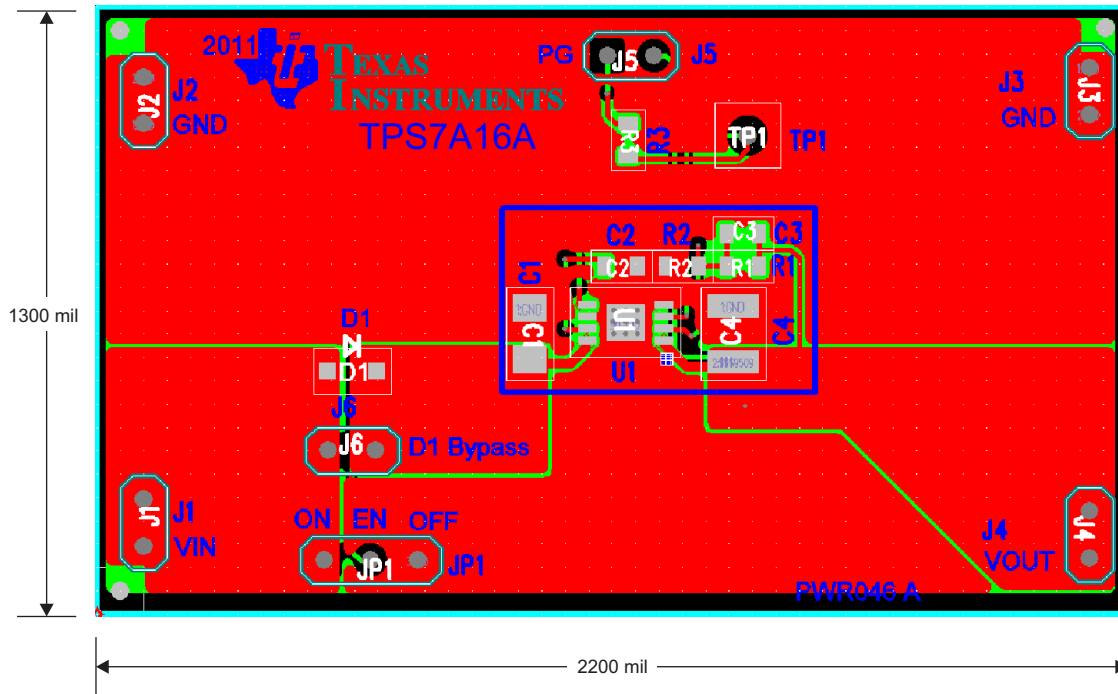


Figure 22. Suggested Layout: Top Layer

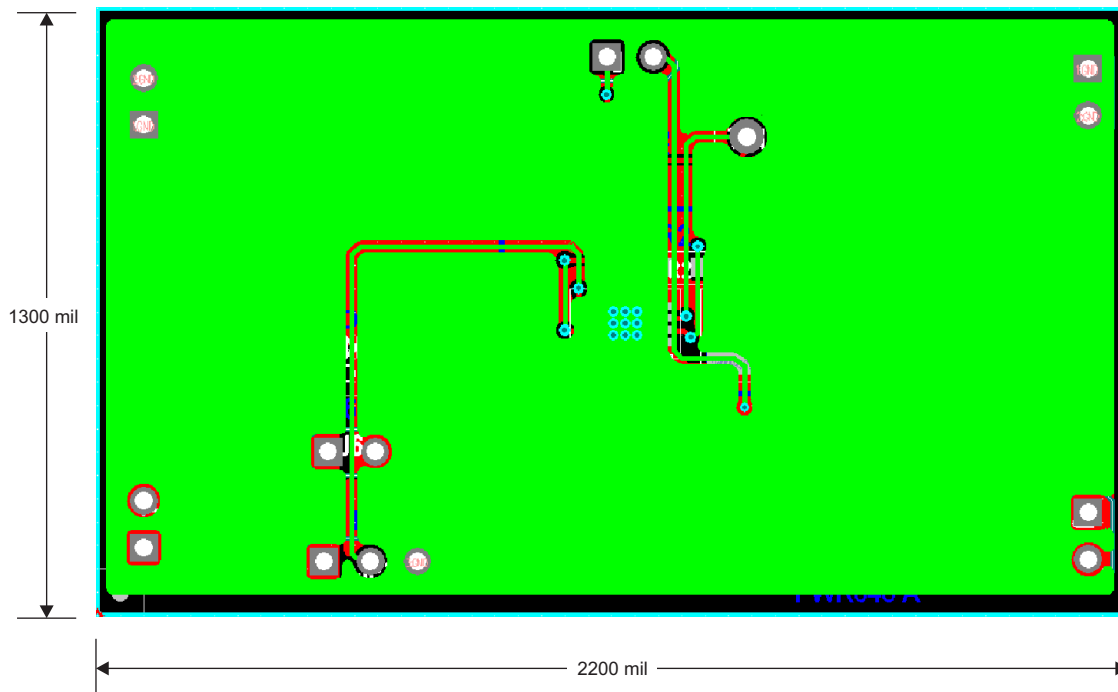


Figure 23. Suggested Layout: Bottom Layer

ADVANCE INFORMATION

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

PowerPAD, MSP430, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A1601AQDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
PTPS7A1633AQDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
PTPS7A1650AQDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TPS7A1601AQDGNRQ1	PREVIEW	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		
TPS7A1633AQDGNRQ1	PREVIEW	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		
TPS7A1650AQDGNRQ1	PREVIEW	MSOP-PowerPAD	DGN	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated