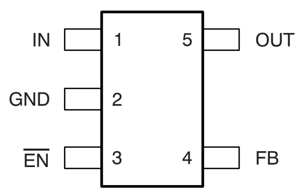
Low Output, Adjustable, Ultralow-Power, 100-mA Low-Dropout Linear Regulator

Check for Samples: TPS76201-Q1

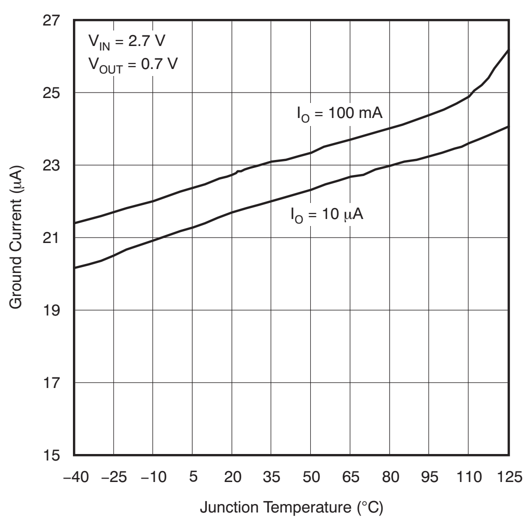
FEATURES

- **Qualified for Automotive Applications**
- **100-mA Low-Dropout Regulator**
- **Adjustable Output Voltage: 0.7 V to 5.5 V**
- **Only 27-μA Quiescent Current at 100 mA**
- **1-μA Quiescent Current in Standby Mode**
- **Overcurrent Limitation**
- **–40°C to +125°C Operating Ambient Temperature Range**
- **Available in 5-Pin SOT-23 (DBV) Package**

DBV PACKAGE (TOP VIEW)



GROUND CURRENT vs JUNCTION TEMPERATURE



DESCRIPTION

The TPS76201-Q1 low-dropout (LDO) voltage regulator features an adjustable output voltage as low as 0.7 V. It is an ideal regulator for sub 1.2-V DSP core voltage supplies and is equally suited for similar applications with other low-voltage processors and controllers. SOT-23 packaging and the high-efficiency that results from the ultralow power regulator operation make the TPS76201-Q1 especially useful in handheld and portable battery applications. This regulator features low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a five-terminal, small outline integrated circuit (SOT-23) package, the TPS76201-Q1 is ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (30 μA maximum) and is stable over the entire range of output load current (10 μA to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-power operation results in a significant increase in the system battery operating life.

The TPS76201-Q1 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at T_J = +25°C. The TPS76201-Q1 is offered in an adjustable version (programmable over the range of 0.7 V to 5.5 V).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

VOLTAGE(2)	T_A	PACKAGE	PART NUMBER	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
Variable 0.7 V to 5.5 V	−40°C to +125°C	SOT-23 (DBV)	TPS76201QDBVRQ1	PUEQ	Tape and reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Contact the factory for availability of fixed output options.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TPS76201-Q1	UNIT
Input voltage range, V_{IN}(2)	–0.3 to +13.5	V
Voltage range at $\overline{EN}$	–0.3 to V_{IN} +0.3	V
Voltage on OUT, FB	7	V
Peak output current, I_{OUT}	Internally limited	
Operating ambient temperature range, T_A	–40 to +150	°C
Storage temperature range, T_{STG}	–65 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied..
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS76201-Q1 DBV 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	183.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	69.9	
θ_{JB}	Junction-to-board thermal resistance	41.6	
ψ_{JT}	Junction-to-top characterization parameter	2.4	
ψ_{JB}	Junction-to-board characterization parameter	40.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
Input voltage range, V_{IN} [(1)]	2.7		10	V
Output voltage range, V_{OUT} [(2)]	0.7		5.5	V
Continuous output current, I_{OUT} [(2)]	0.01		100	mA
Operating ambient temperature range, T_A [(2)]	–40		+125	°C

(1) To calculate the minimum input voltage for the desired maximum output current, use the following formula: $V_{INmin} = V_{OUTmax} + V_{DO}$ (max load)
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range; $V_{IN} = V_{OUT(Typ)} + 1$ V; $I_{OUT} = 100$ mA, $\overline{EN} = 0$ V, and $C_{OUT} = 4.7$ µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	10-µA to 100-mA load [(1)]	0.7 V ≤ V_{OUT} ≤ 5.5 V, T_J = +25°C		V_{OUT}		V
		0.7 V ≤ V_{OUT} ≤ 5.5 V, T_J = −40°C to +125°C	0.97 × V_{OUT}		1.03 × V_{OUT}	V
I_Q	GND current [(1)(2)]	$\overline{EN}$ = 0 V, 10 µA < I_{OUT} < 100 mA, T_J = +25°C		27		µA
		$\overline{EN}$ = 0 V, 10 µA < I_{OUT} < 100 mA, T_J = −40°C to +125°C			35	µA
	Load regulation	$\overline{EN}$ = 0 V, 10 µA < I_{OUT} < 100 mA, T_J = +25°C		12		mV
$\Delta V_O/V_{OUT}$	Line regulation, output voltage [(2)]	2.7 V < V_{IN} ≤ 10 V, T_J = +25°C, see [(1)]		0.04		%/V
		2.7 V < V_{IN} ≤ 10 V, T_J = −40°C to +125°C, see [(1)]			0.1	%/V
V_N	Output noise voltage	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF, V_{OUT} = 0.7 V, T_J = +25°C		60		μV_{RMS}
I_{CL}	Output current limit	V_{OUT} = 0 V, see [(1)]		350	750	mA
I_{STBY}	Standby current	$\overline{EN}$ = V_{IN}, 2.7 V < V_{IN} ≤ 10 V		1		µA
		T_J = −40°C to +125°C			2	µA
$V_{EN(HI)}$	High-level enable input voltage	2.7 V < V_{IN} ≤ 10 V	1.7			V
$V_{EN(LO)}$	Low-level enable input voltage	2.7 V < V_{IN} ≤ 10 V			0.8	V
PSRR	Power-supply rejection ratio	f = 1 kHz, C_{OUT} = 10 µF, T_J = +25°C, see [(1)]		60		dB
I_{EN}	Enable pin current	$\overline{EN}$ = 0 V	–1	0	1	µA
		$\overline{EN}$ = V_{IN}	–1		1	µA

(1) Minimum IN operating voltage is 2.7 V or V_{OUT}(typ) + 1 V, whichever is greater. Maximum IN voltage = 10 V, minimum output current = 10 µA, and maximum output current = 100 mA.
(2) If V_{OUT} ≤ 1.8 V, then V_{INmin} = 2.7 V, V_{INmax} = 10 V: $\text{Line Reg. (mV)} = (\%/V) \times \frac{V_{OUT}(V_{Imax} - 2.7\ V)}{100} \times 1000$

If V_{OUT} ≥ 2.5 V, then V_{INmin} = V_{OUT} + 1 V, V_{INmax} = 10 V: $\text{Line Reg. (mV)} = (\%/V) \times \frac{V_{OUT}[V_{Imax} - (V_{OUT} + 1\ V)]}{100} \times 1000$

FUNCTIONAL BLOCK DIAGRAM

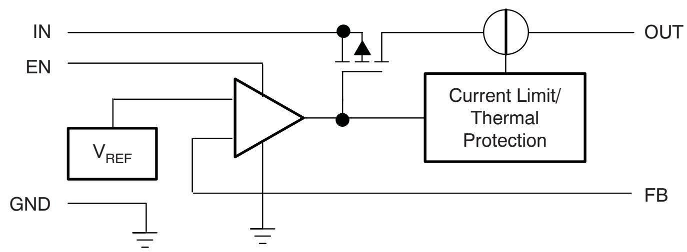
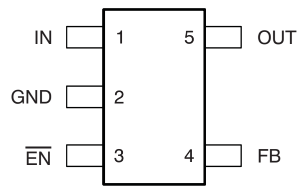


Figure 1. TPS76201-Q1

PIN CONFIGURATION

DBV PACKAGE
SOT-23
(TOP VIEW)



PIN DESCRIPTIONS

NAME	SOT-23 DBV	I/O	DESCRIPTION
IN	1	I	Input supply voltage
GND	2	—	Ground pin
$\overline{EN}$	3	I	Enable input
OUT	4	I	Regulated output voltage
FB	5	O	Feedback voltage

TYPICAL CHARACTERISTICS

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT VOLTAGE vs OUTPUT CURRENT

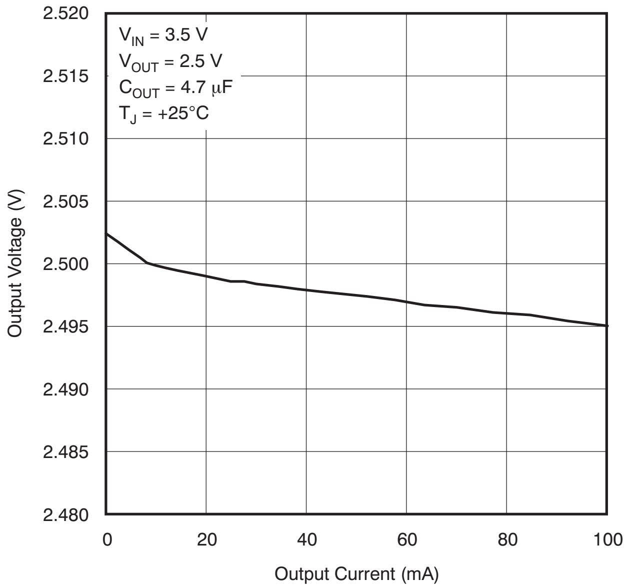


Figure 2.

OUTPUT VOLTAGE vs OUTPUT CURRENT

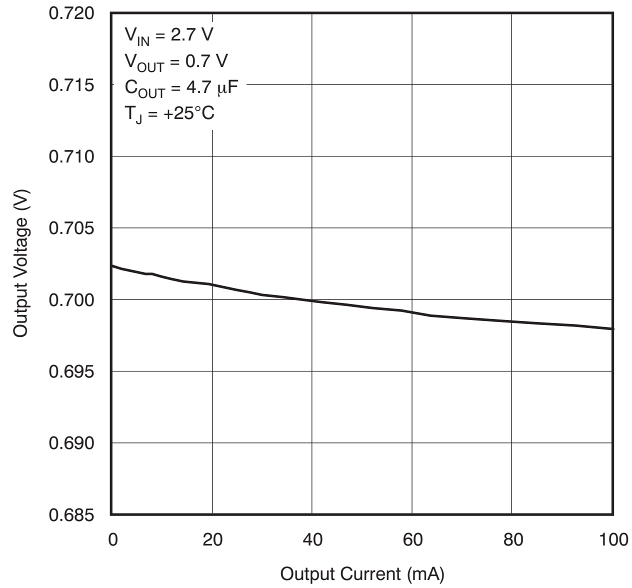


Figure 3.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

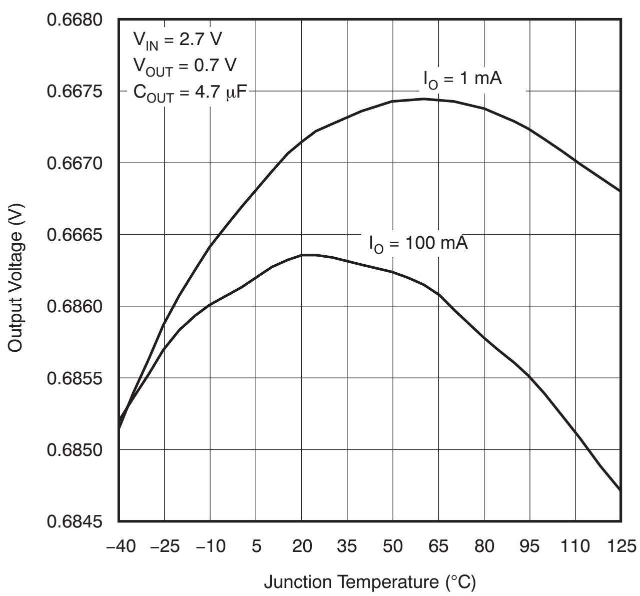


Figure 4.

GROUND CURRENT vs JUNCTION TEMPERATURE

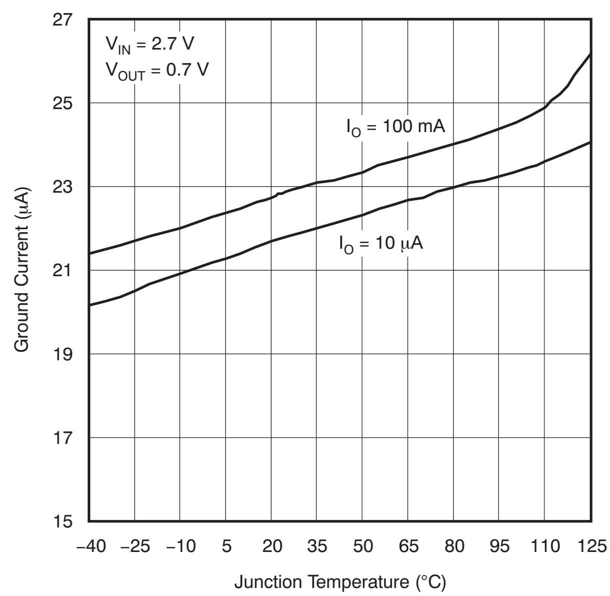


Figure 5.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

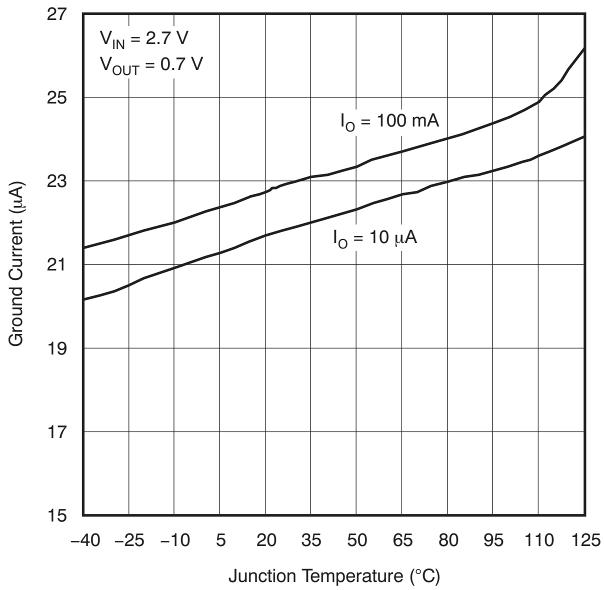


Figure 6.

OUTPUT IMPEDANCE vs FREQUENCY

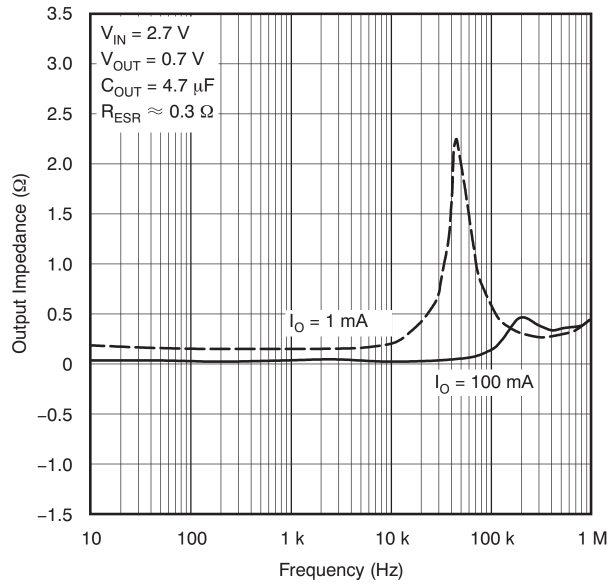


Figure 7.

DROPOUT VOLTAGE vs INPUT VOLTAGE

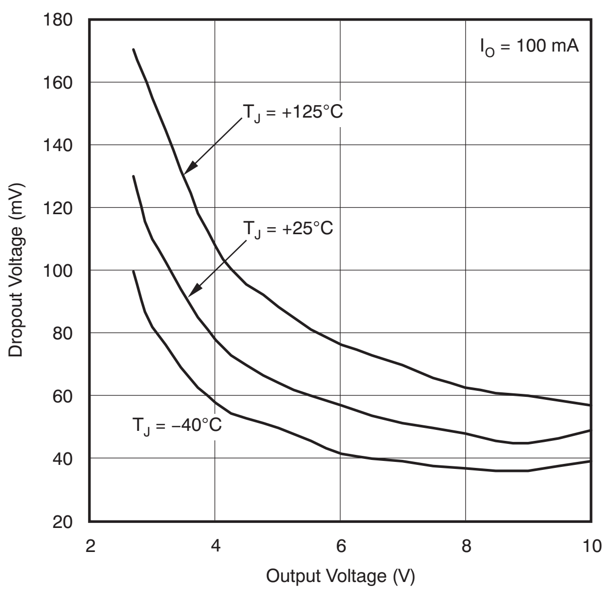


Figure 8.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

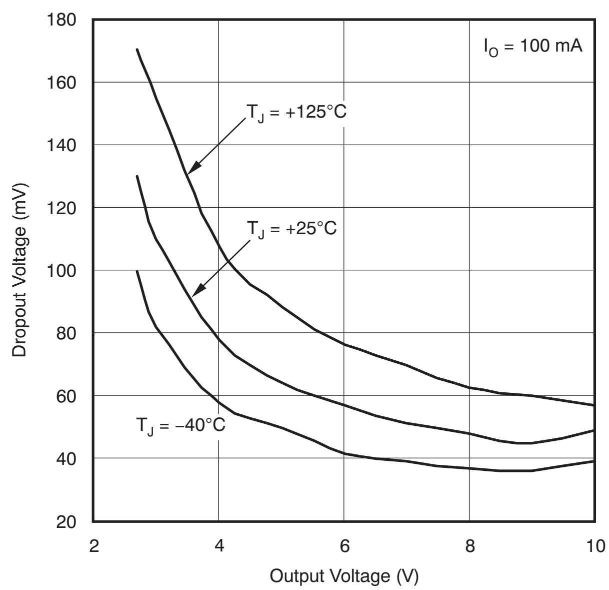


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C.

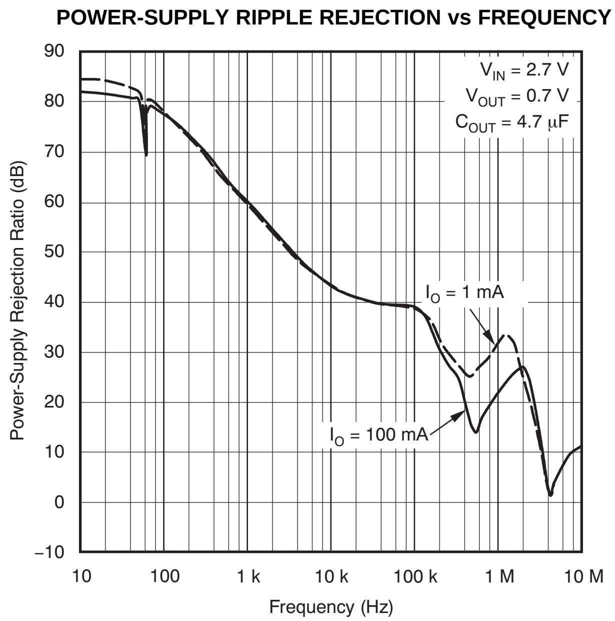


Figure 10.

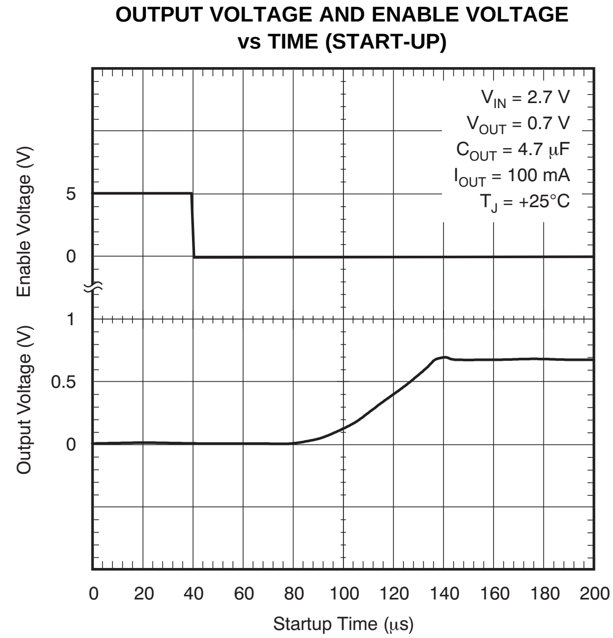


Figure 11.

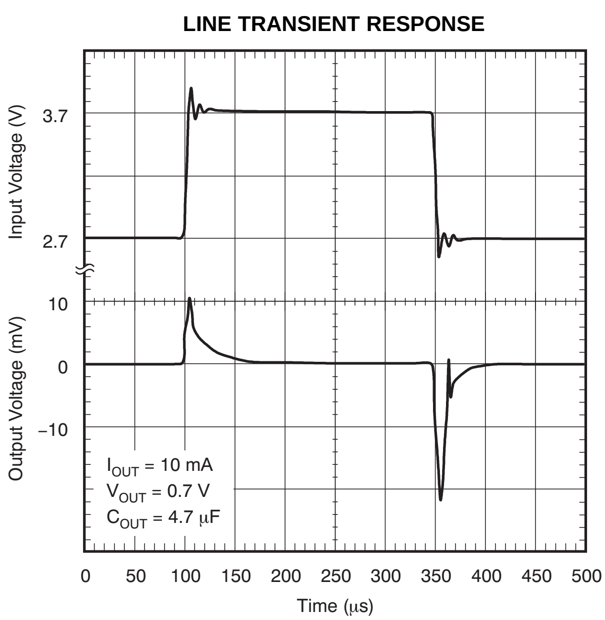


Figure 12.

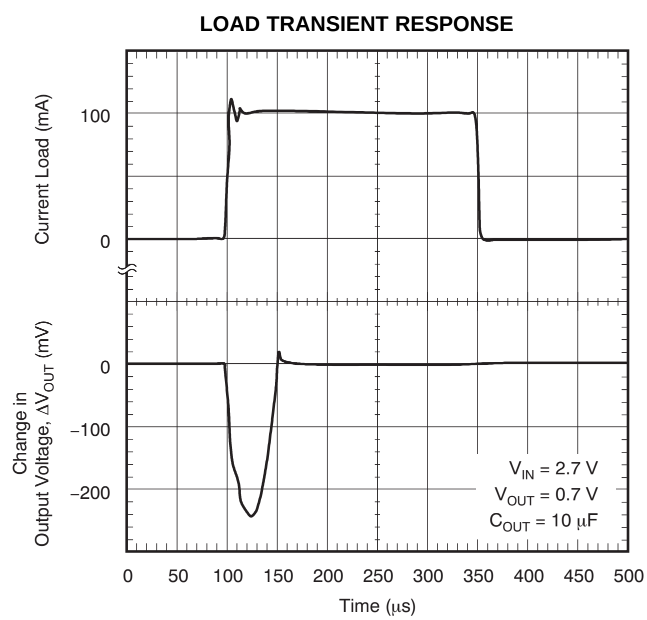


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE TRANSIENT RESPONSE

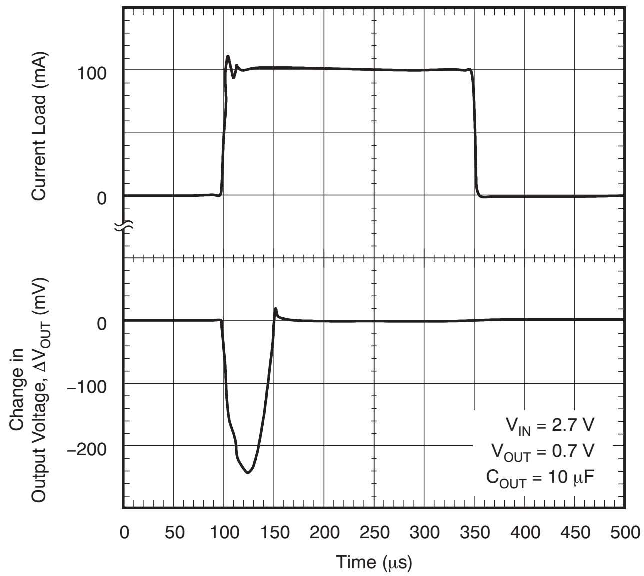


Figure 14.

LOAD TRANSIENT RESPONSE

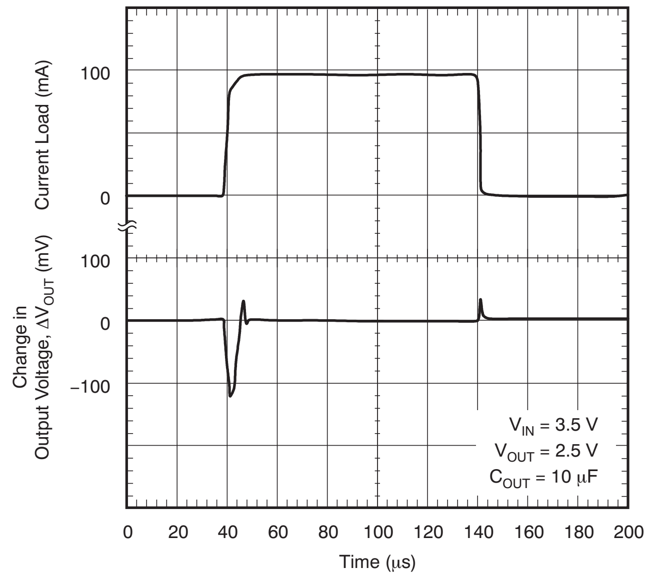


Figure 15.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

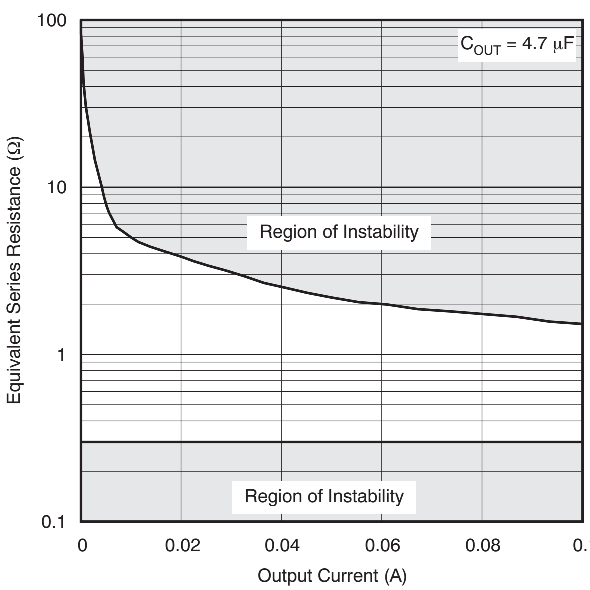


Figure 16.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

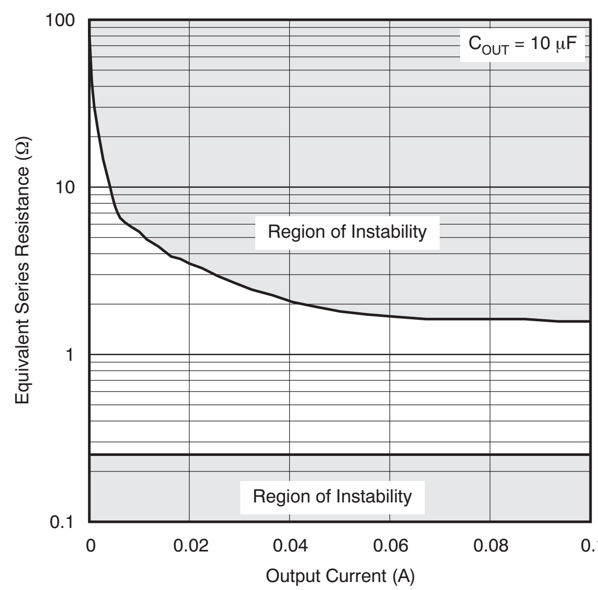


Figure 17.

APPLICATION INFORMATION

The TPS76201-Q1 low-dropout (LDO) regulator has been optimized for use in battery-operated equipment including, but not limited to, the sub 1.2-V DSP core voltage supplies. It features low quiescent current (23 μA nominally) and enable inputs to reduce supply currents to 1 μA when the regulators are turned off. A typical application circuit is shown in Figure 18.

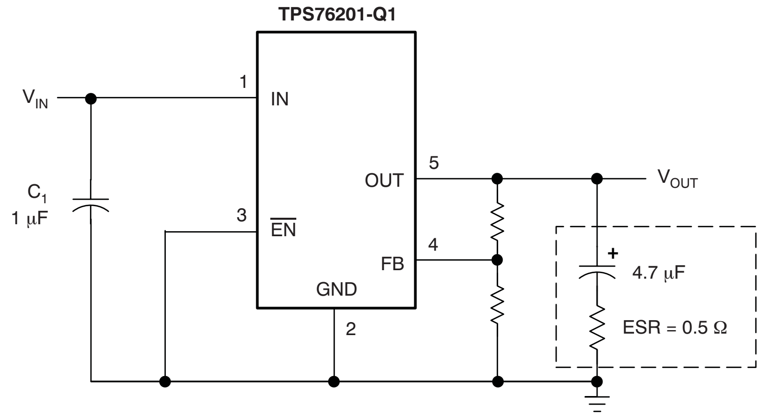


Figure 18. Typical Application Circuit

External Capacitor Requirements

Although not required, a 0.047-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS76201-Q1, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS76201-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μF. The equivalent series resistance (ESR) of the capacitor should be between 0.3 Ω and 1.5 Ω. to ensure stability. Capacitor values larger than 4.7 μF are acceptable, and allow the use of smaller ESR values. Capacitors less than 4.7 μF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7-μF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet these ESR requirements. Multilayer ceramic capacitors may have very small equivalent series resistances and therefore may require the addition of a low-value series resistor to ensure stability. Table 1 summarizes the capacitor selection recommendations.

Table 1. Capacitor Selection

PART NO.	MFR	VALUE	MAX ESR(1)	SIZE (H × L × W)(2)
T494B475K016AS	KEMET	4.7 μF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 μF	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 μF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 μF	0.6 Ω	2.6 × 6.0 × 3.2

(1) ESR is maximum resistance in Ohms at 100 kHz and T_A = +25°C. Contact manufacturer for minimum ESR values.
(2) Size is shown in mm.

Output Voltage Programming

The output voltage of the TPS76201-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 19. The output voltage is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{REF} = 0.6663 V, typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided because leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 66.5 kΩ to set the divider current at 10 µA and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (2)$$

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)[1]	
	R1	R2
0.7	3.36	66.5
0.9	23.2	66.5
1.2	53.6	66.5
1.5	83.5	66.5
1.8	113	66.5
2.5	182	66.5
3.3	246	66.5
3.6	294	66.5
4	332	66.5
5	432	66.5

(1) 1% values shown.

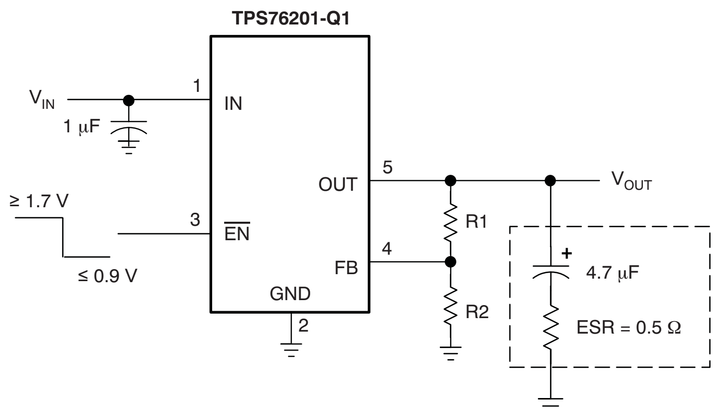


Figure 19. TPS76201-Q1 Adjustable LDO Regulator Programming

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +150°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 3:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

T_{Jmax} is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; see the *Thermal Information* table.

T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Regulator Protection

The TPS76201-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS76201-Q1 features internal current limiting and thermal protection. During normal operation, the TPS76201-Q1 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal protection circuitry shuts it down. Once the device has cooled to below approximately +140°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS76201QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS76201-Q1 :

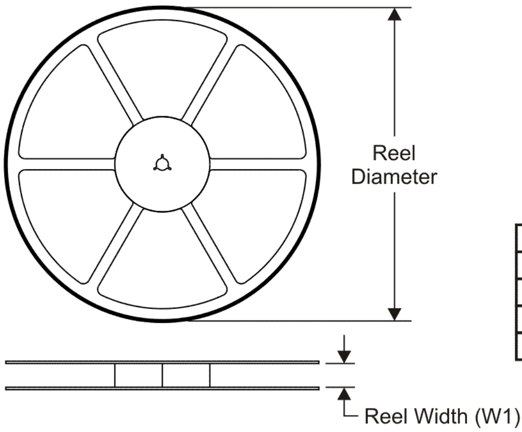
- Catalog: TPS76201

NOTE: Qualified Version Definitions:

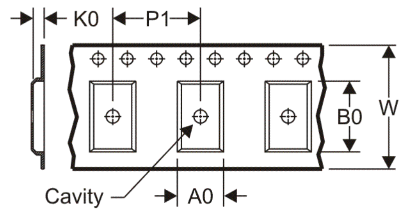
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

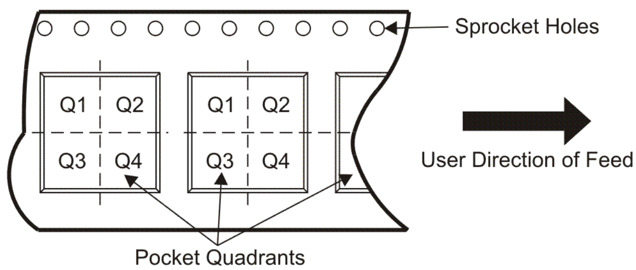


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

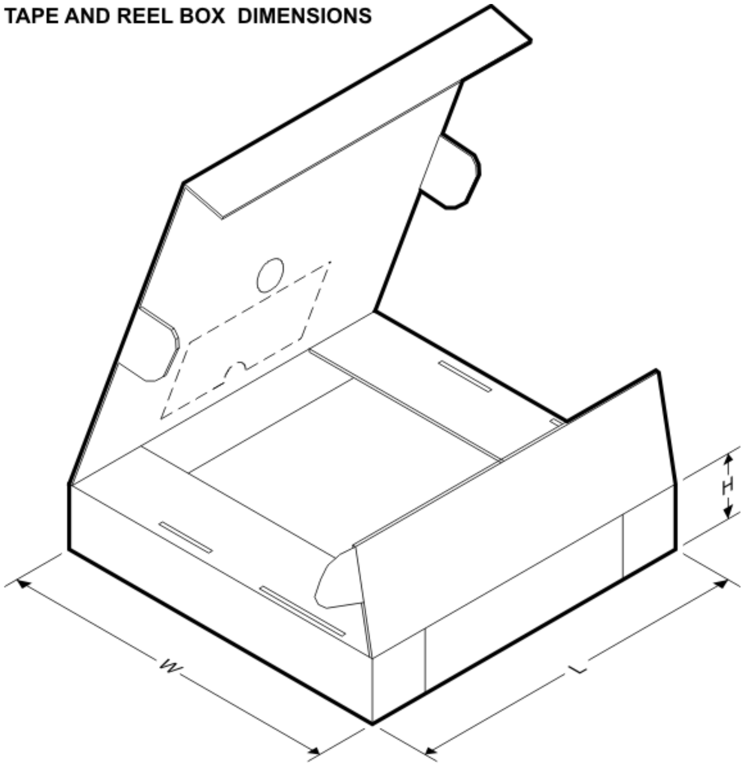
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76201QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

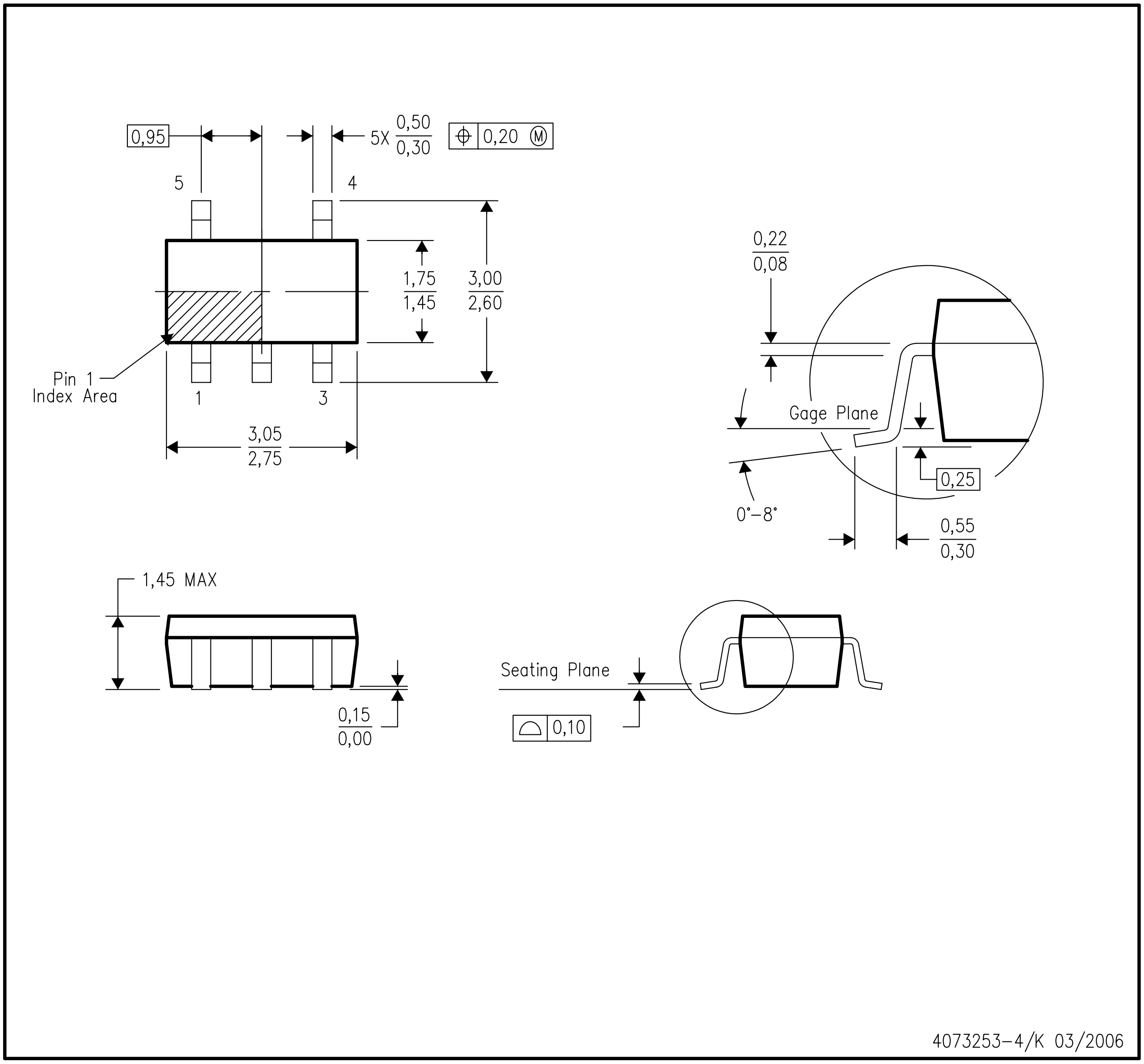
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

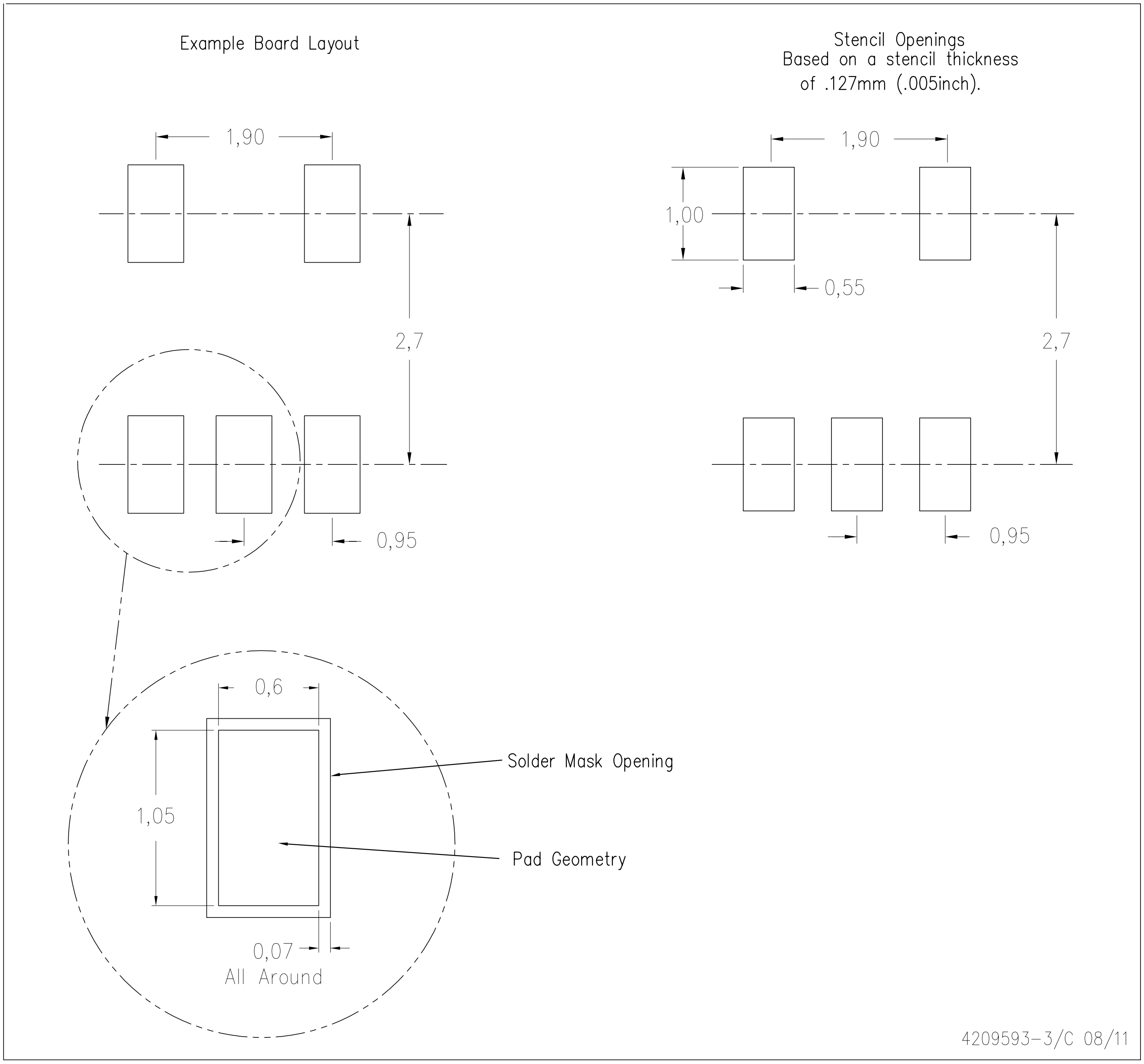
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76201QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
		TI E2E Community Home Page	e2e.ti.com

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