Triple-Supply Power Management IC for Powering FPGAs and DSPs

Check for Samples: TPS75003-EP

FEATURES

- **Two 95% Efficient, 3-A Buck Controllers and One 300-mA LDO**
- **Tested and Endorsed by Xilinx for Powering the Spartan™-3, Spartan-3E, and Spartan-3L FPGAs**
- **Adjustable (1.2 V to 6.5 V for Bucks, 1 V to 6.5 V for LDO) Output Voltages on All Channels**
- **Input Voltage Range: 2.2 V to 6.5 V**
- **Independent Soft-Start for Each Supply**
- **Independent Enable for Each Supply for Flexible Sequencing**
- **LDO Stable with 2.2-µF Ceramic Output Capicitor**
- **Small, Low-Profile 4,5 mm x 3,5 mm x 0,9 mm QFN Package**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

APPLICATIONS

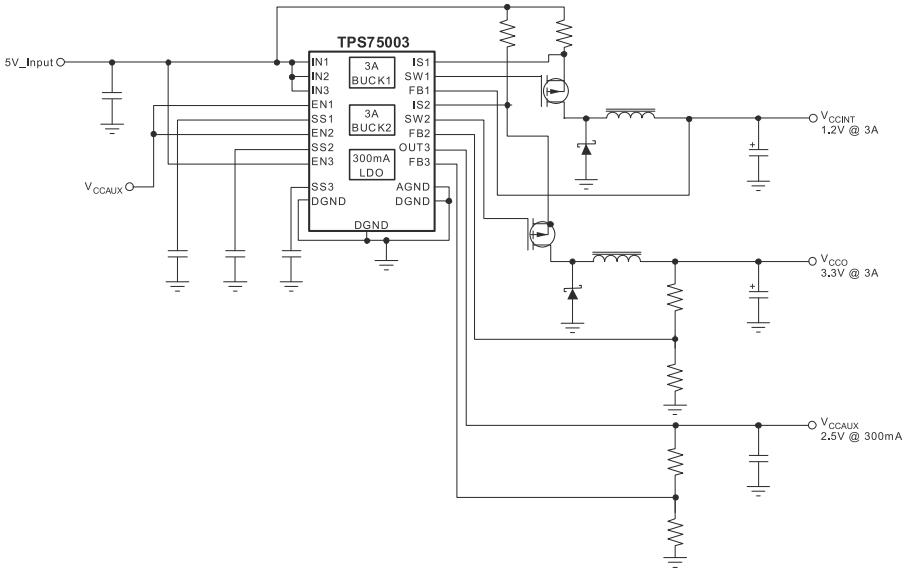
- **FPGA/DSP/ASIC Supplies**
- **Set-Top Boxes**
- **DSL Modems**
- **Plasma TV Display Panels**

DESCRIPTION

The TPS75003 is a complete power management solution for FPGA, DSP and other multi-supply applications. The device has been tested with and meets all of the Xilinx Spartan-3, Spartan-3E, and Spartan-3L start-up profile requirements, including monotonic voltage ramp and minimum voltage rail rise time. Independent Enables for each output allow sequencing to minimize demand on the power supply at start-up. Soft-start on each supply limits inrush current during start-up. Two integrated buck controllers allow efficient, cost-effective voltage conversion for both low and high current supplies such as core and I/O. A 300-mA LDO is integrated to provide an auxiliary rail such as V_{CCAUX} on the Xilinx Spartan-3 FPGA. All three supply voltages are offered in user-programmable options for maximum flexibility.

The TPS75003 is fully specified from –55°C to +125°C and is offered in a QFN package, yielding a highly compact total solution size with high power dissipation capability.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS75003MRHLREP	Buck1: Adjustable Buck2: Adjustable LDO: Adjustable

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this document or see the Texas Instruments website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS75003	UNIT
V_{INX} range (IN1, IN2, IN3)	-0.3 to +7	V
V_{ENX} range (EN1, EN2, EN3)	-0.3 to V_{INX} + 0.3	V
V_{SWX} range (SW1, SW2, SW3)	-0.3 to V_{INX} + 0.3	V
V_{ISX} range (IS1, IS2, IS3)	-0.3 to V_{INX} + 0.3	V
V_{OUT3} range	-0.3 to +7	V
V_{SSX} range (SS1, SS2, SS3)	-0.3 to V_{INX} + 0.3	V
V_{FBX} range (FB1, FB2, FB3)	-0.3 to +3.3	V
Peak LDO output current (I_{OUT3})	Internally limited	—
Continuous total power dissipation	See the Thermal Information Table	—
Junction temperature range, T_J	-55 to +150	°C
Storage temperature range	-65 to +150	°C
ESD rating, HBM	1	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

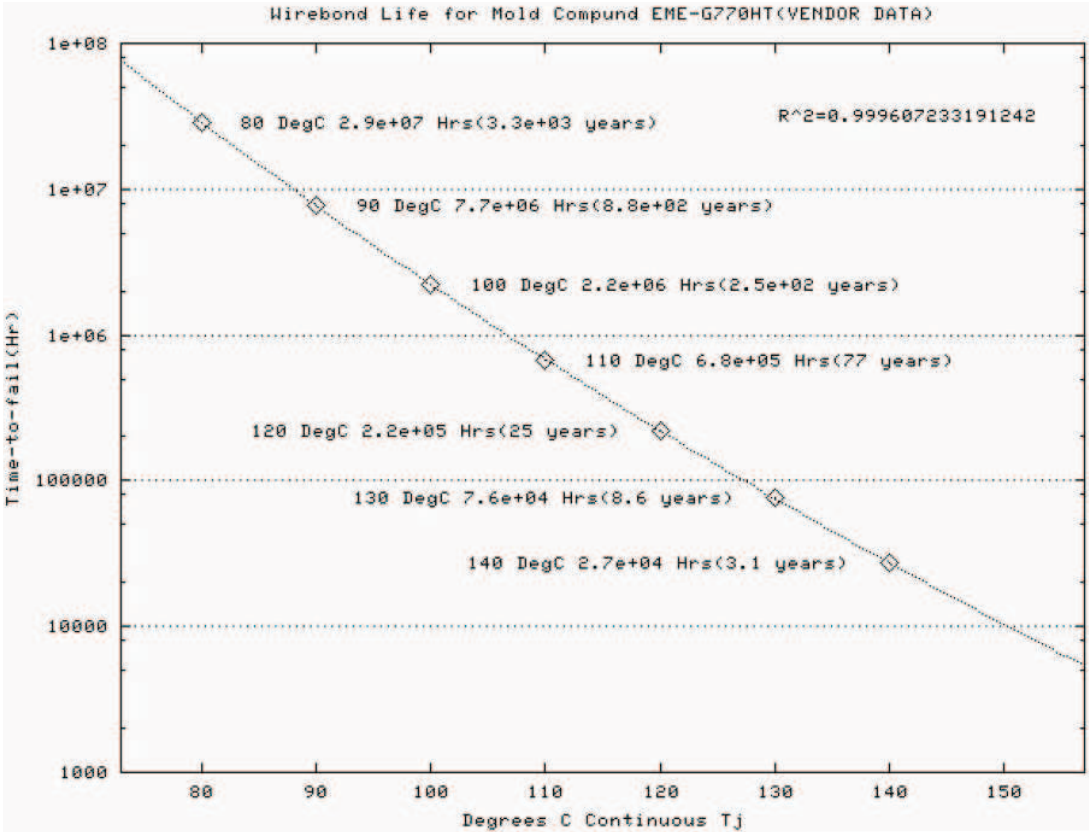


Figure 1. Wirebond Plot

THERMAL INFORMATION

THERMAL METRIC[1]		TPS75003-EP RHL (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	42.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.8	
θ_{JB}	Junction-to-board thermal resistance	39.5	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	14.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2$ V, $V_{IN3} = 3$ V, $V_{OUT3} = 2.5$V, $C_{OUT1} = C_{OUT2} = 47$ µF, $C_{OUT3} = 2.2$ µF, $T_A = -55°C$ to 125°C, unless otherwise noted. Typical values are at $T_A = 25°C$.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply and Logic						
V_{INX}	Input voltage range (IN1, IN2, IN3)(1)		2.2		6.5	V
I_Q	Quiescent current, $I_Q = I_{DGND} + I_{AGND}$	$I_{OUT1} = I_{OUT2} = I_{OUT3} = 0$ mA		75	150	µA
I_{SHDN}	Shutdown supply current	$V_{EN1} = V_{EN2} = V_{EN3} = 0$ V		0.05	3	µA
$V_{IH1, 2}$	Enable high, enabled (EN1, EN2)	$T_A = 25°C$	1.4			V
		T_A = Full Range	1.45			
V_{IH3}	Enable High, enabled (EN3)	$T_A = 25°C$	1.14			V
		T_A = Full Range	1.2			
V_{ILX}	Enable low, shutdown (EN1, EN2, EN3)		0		0.3	V
I_{ENX}	Enable pin current (EN1, EN2, EN3)			0.01	0.5	µA
Buck Controllers 1 and 2						
$V_{OUT1,2}$	Adjustable output voltage Range(2)		V_{FBX}		V_{INX}	V
$V_{FB1,2}$	Feedback voltage (FB1, FB2)			1.22		V
	Feedback voltage accuracy(1) (FB1, FB2)			±2%		
$I_{FB1,2}$	Current into FB1, FB2 pins			0.01	0.5	µA
$V_{IS1,2}$	Reference voltage for current sense	$T_A = 25°C$	80	100	120	mV
		T_A = Full Range	75		125	
$I_{IS1,2}$	Current into IS1, IS2 pins			0.01	0.5	µA
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line regulation(1)	Measured with the circuit in Figure 2, $V_{OUT} + 0.5$ V ≤ V_{IN} ≤ 6.5 V		0.1		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load regulation	Measured with the circuit in Figure 2, 30 mA ≤ I_{OUT} ≤ 2 A		0.6		% / A
$n_{1,2}$	Efficiency(3)	Measured with the circuit in Figure 2, $I_{OUT} = 1$ A		94%		
$t_{STR1,2}$	Startup time(3)	Measured with the circuit in Figure 2, $R_L = 6$ Ω, $C_{OUT} = 100$ µF, $C_{SS} = 2.2$ nF		5		ms
$R_{DS,ON1,2}$	Gate driver P-Channel and N-Channel MOSFET on-resistance	$V_{IN1,2} > 2.5$ V		4		Ω
		$V_{IN1,2} = 2.2$ V		6		
$I_{SW1,2}$	Gate Driver P-Channel and N-Channel MOSFET drive current			100		mA
t_{ON}	Minimum on time		1.36	1.55	1.84	µs
t_{OFF}	Minimum off time		0.44	0.65	0.86	µs

(1) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2 V, whichever is greater.
(2) Maximum V_{OUT} is dependent on external components and will be less than V_{IN}. Parameter is not production tested.
(3) Depends on external components.

ELECTRICAL CHARACTERISTICS (continued)

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2$ V, $V_{IN3} = 3$ V, $V_{OUT3} = 2.5$V, $C_{OUT1} = C_{OUT2} = 47$ µF, $C_{OUT3} = 2.2$ µF, $T_A = -55°C$ to 125°C, unless otherwise noted. Typical values are at $T_A = 25°C$.

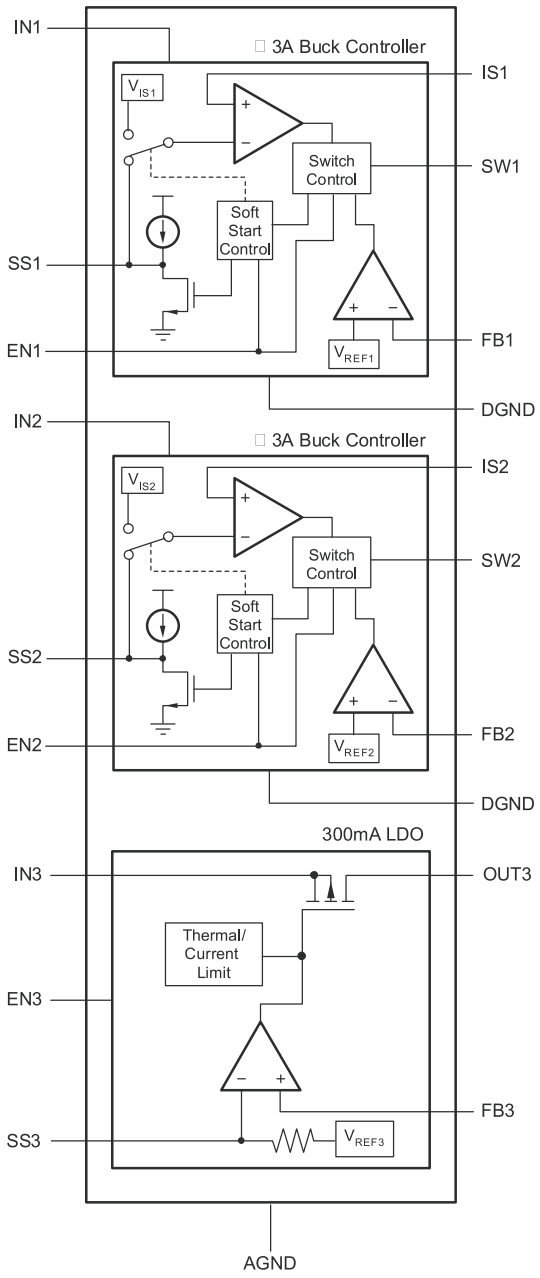
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
LDO						
V_{OUT3}	Output voltage range (4)		1		6.5 - V_{DO}	V
V_{FB3}	Feedback pin voltage			0.507		V
	Feedback pin voltage accuracy(5)	2.95 V ≤ V_{IN3} ≤ 6.5 V 1 mA ≤ I_{OUT3} ≤ 300 mA		±4%		
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line regulation(5)	V_{OUT3} + 0.5V ≤ V_{IN3} ≤ 6.5 V		0.075		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load regulation	10 mA ≤ I_{OUT3} ≤ 300 mA		0.01		% / mA
V_{DO}	Dropout voltage ($V_{IN} = V_{OUT(NOM)}$ - 0.1)(6)	I_{OUT3} = 300 mA		250	350	mV
I_{CL3}	Current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$	375	600	1000	mA
I_{FB3}	Current into FB3 pin			0.03	0.1	µA
V_n	Output noise	BW = 100 Hz - 100 kHz, I_{OUT3} = 300 mA		400		μV_{RMS}
t_{SD}	Thermal shutdown temperature for LDO	Shutdown, temperature increasing		175		°C
		Reset, temperature decreasing		160		
UVLO	Undervoltage lockout threshold	V_{IN} rising		1.8		V
	Undervoltage lockout hysteresis	V_{IN} falling		100		mV

(4) Maximum V_{OUT} is dependent on external components and will be less than V_{IN}. Parameter is not production tested.
(5) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2 V, whichever is greater.
(6) V_{DO} does not apply when $V_{OUT} + V_{DO} < 2.2$ V.

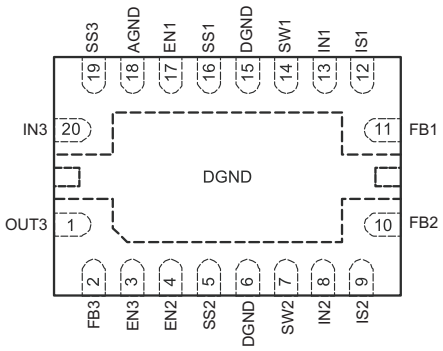
DEVICE INFORMATION

Functional Block Diagram

TPS75003



RHL PACKAGE
4.5mm x 3.5mm QFN
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	RHL	
DGND	6, 15, PAD	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the *PCB Layout* section of this data sheet.
AGND	18	Ground connection for LDO
IN1	13	Input supply to BUCK1
IN2	8	Input supply to BUCK2
IN3	20	Input supply to LDO
EN1	17	Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.
EN2	4	Same as EN1 but for BUCK2 controller
EN3	3	Same as EN1 but for LDO
SS1	16	Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important. See the *Typical Characteristics, Applications*, and *PCB Layout* sections for details.
SS2	5	Same as SS1 but for BUCK2 regulator.
SS3	19	Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, therby slowing output voltage ramp-up. See the *Applications* section for details.
IS1	12	Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required. See the *Applications* section for details.
IS2	9	Same as IS1, but compared to IN2 and used for BUCK2 controller
SW1	14	Gate drive pin for external BUCK1 P-channel MOSFET
SW2	7	Same as SW1, but for BUCK2 controller
FB1	11	Feedback pin. Used to set the output voltage of BUCK1 regulator
FB2	10	Same as FB1, but for BUCK2 controller
FB3	2	Same as FB1, but for LDO
OUT3	1	Regulated LDO output. A small ceramic capacitor (≥ 2.2 μF) is needed from this pin to ground to ensure stability.

Typical Application Circuit for Powering the Xilinx Spartan-3 FPGA

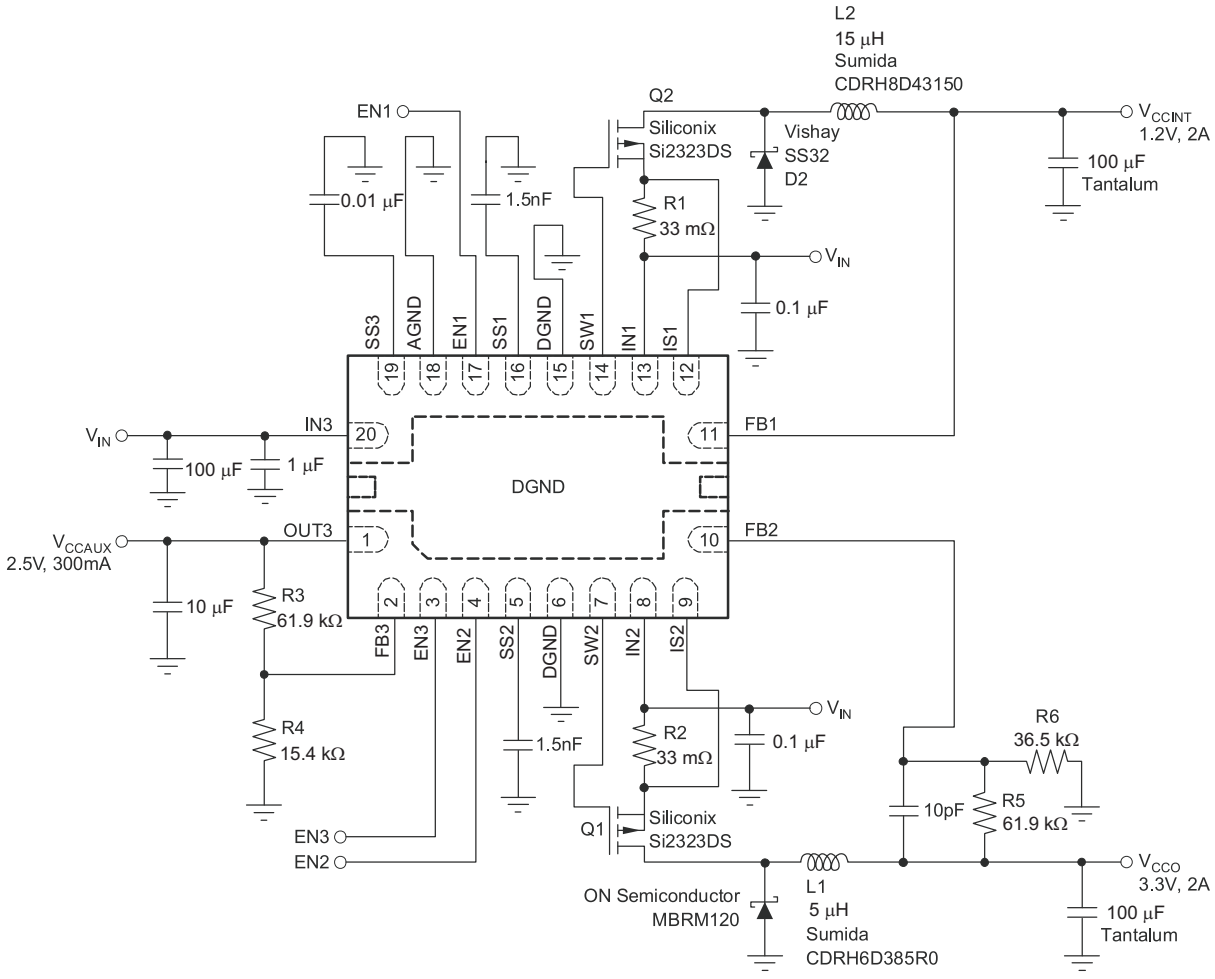


Figure 2.

TYPICAL CHARACTERISTICS

Measured using circuit in Figure 2

Buck Converter

BUCK LOAD REGULATION

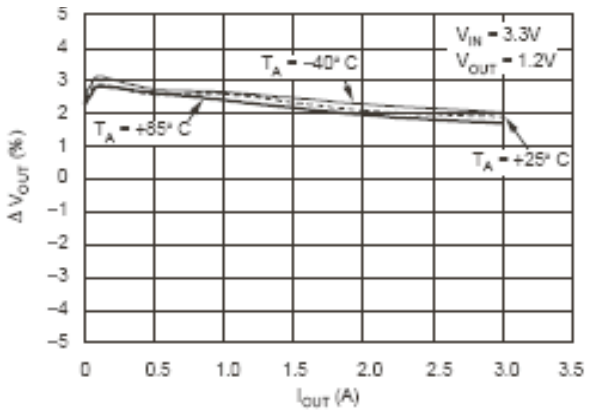


Figure 3.

BUCK LOAD REGULATION

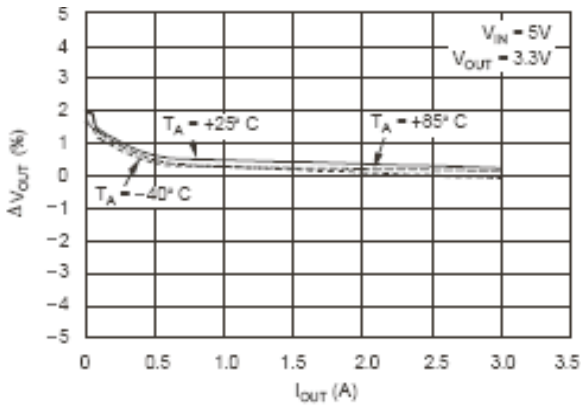


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 2

BUCK LINE REGULATION

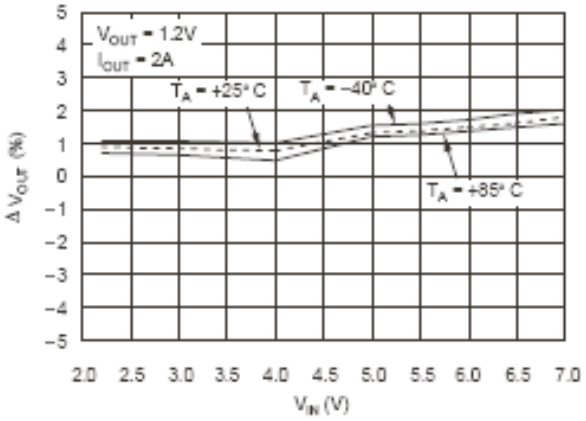


Figure 5.

BUCK LINE REGULATION

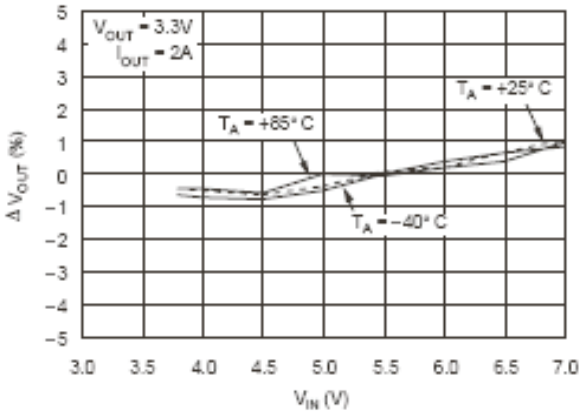


Figure 6.

BUCK SWITCHING FREQUENCY vs I_{OUT}, T_A

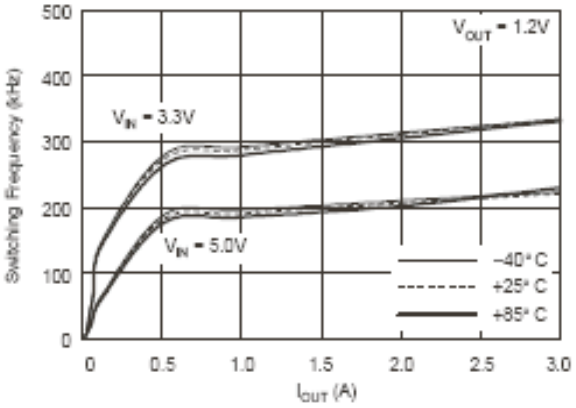


Figure 7.

BUCK SWITCHING FREQUENCY vs I_{OUT}

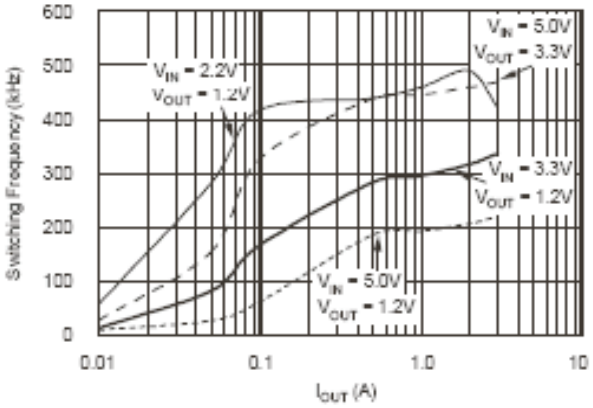


Figure 8.

BUCK OUTPUT VOLTAGE RIPPLE

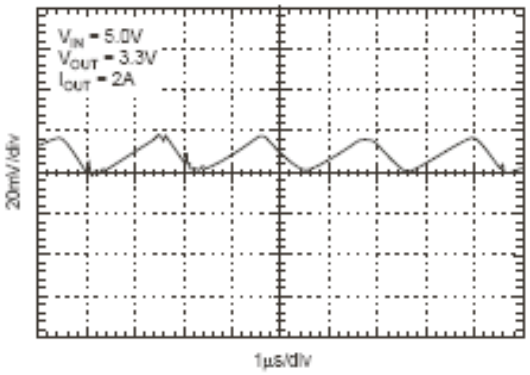


Figure 9.

EFFICIENCY vs I_{OUT}

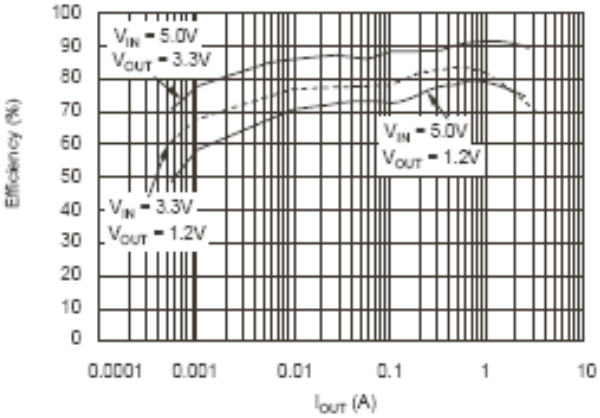


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 2

BUCK START-UP vs V_{IN} and I_{OUT}

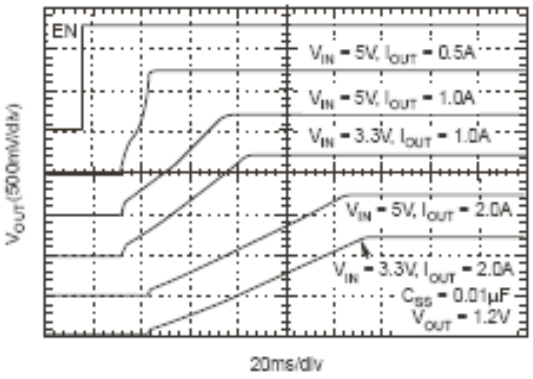


Figure 11.

BUCK START-UP vs V_{IN} and C_{OUT}

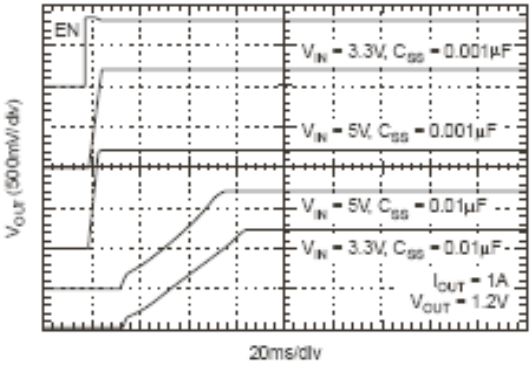


Figure 12.

BUCK START-UP vs V_{IN} and C_{SS}

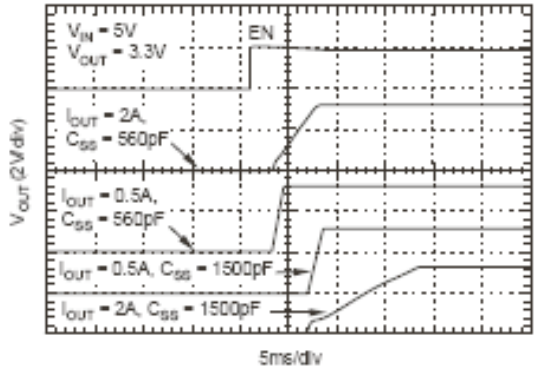


Figure 13.

BUCK START-UP vs I_{OUT} and C_{SS}

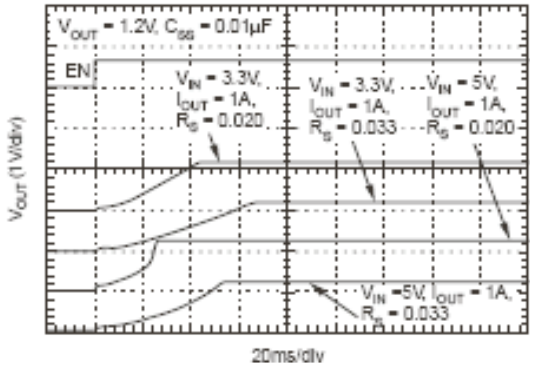


Figure 14.

LDO Converter

LDO LOAD REGULATION

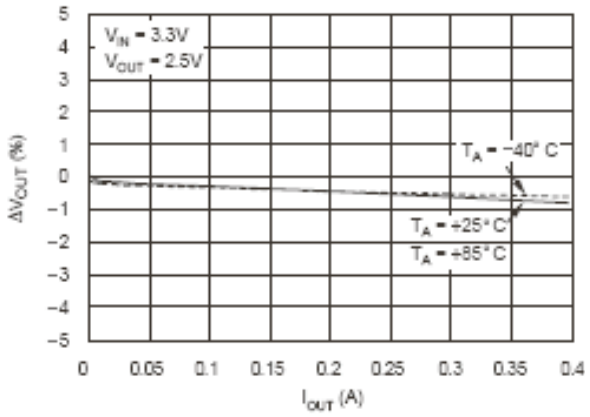


Figure 15.

LDO LINE REGULATION

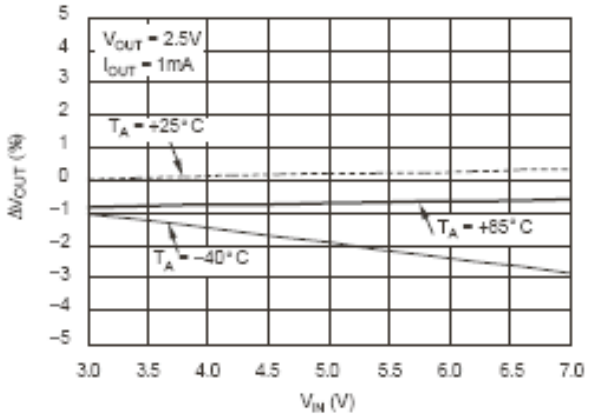


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 2

LDO DROPOUT vs I_{OUT}

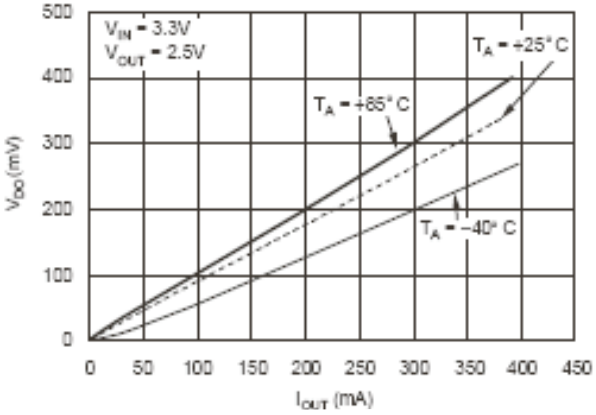


Figure 17.

LDO DROPOUT vs T_A

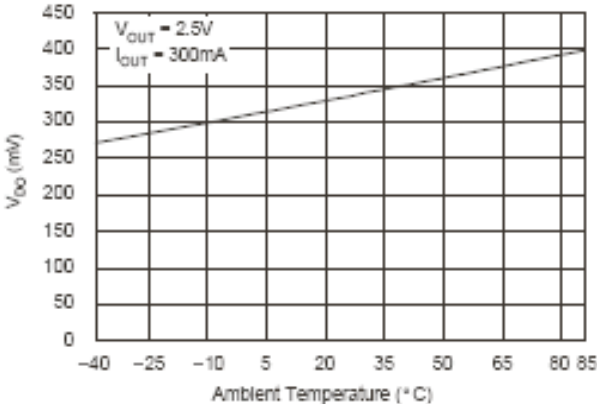


Figure 18.

$R_{DS,ON}$ PMOS vs V_{IN}

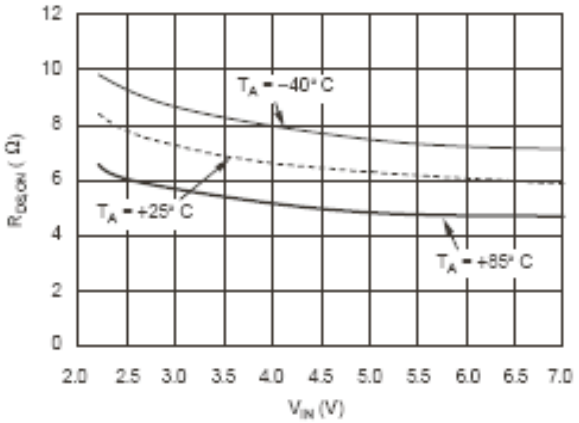


Figure 19.

$R_{DS,ON}$ NMOS vs V_{IN}

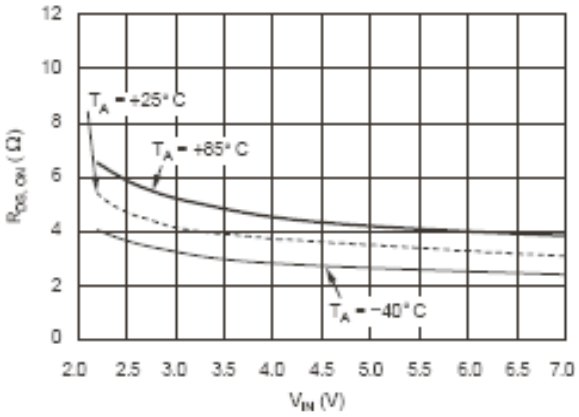


Figure 20.

LDO V_{OUT} vs T_A

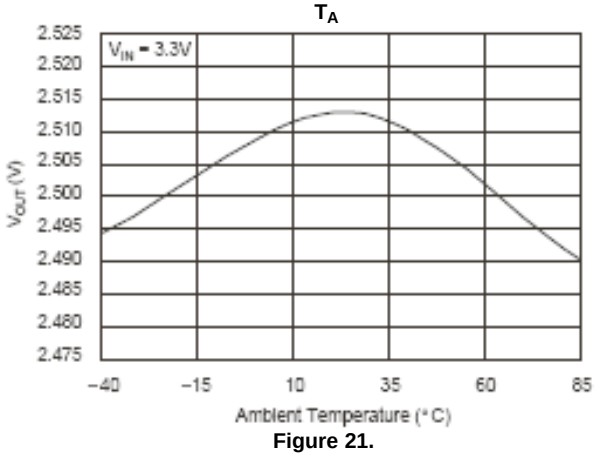


Figure 21.

APPLICATION INFORMATION

The TPS75003 is an integrated power management IC designed specifically to power DSPs and FPGAs such as the Xilinx Spartan-3, Spartan-3E and Spartan-3L. Two non-synchronous buck controllers can be configured to supply up to 3 A for both CORE and I/O rails. A low dropout linear regulator powers auxiliary rails up to 300 mA. All channels have independent enable and soft-start, allowing control of inrush current and output voltage ramp time as required by the application.

Figure 2 shows a typical application circuit for powering the Xilinx Spartan-3 FPGA. Table 1 through Table 4 show component values that have been tested for use with 2-A and 3-A load currents. Other similar external components can be substituted as desired; however, in all cases the circuits that are used should be tested for compliance to application requirements.

Table 1. Inductors Tested with the TPS75003

PART NUMBER	MANUFACTURER	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
SLF7032T−100M1R4	TDK	10 µH ±20%	53 mΩ ±20%	1.4 A
SLF6025−150MR88	TDK	15 µH ±20%	85 mΩ ±20%	0.88 A
CDRH6D28−5R0	Sumida	5 µH	23 mΩ	2.4 A
CDRH6D38-5R0	Sumida	5 µH	18 mΩ	2.9 A
CDRH103R−100	Sumida	10 µH	45 mΩ	2.4 A
CDRH4D28−100	Sumida	10 µH	96 mΩ	1 A
CDRH8D43-150	Sumida	15 µH	42 mΩ	2.9 A
CDRH5D18−6R2	Sumida	6.2 µH	71 mΩ	1.4 A
DO3316P−472	Coilcraft	4.7 µH	18 mΩ	5.4 A
DT3316P−153	Coilcraft	15 µH	60 mΩ	1.8 A
DT3316P−223	Coilcraft	22 µH	84 mΩ	1.5 A
744052006	Wurth	6.2 µH	80 mΩ	1.45 A
74451115	Wurth	15 µH	90 mΩ	0.8 A

Table 2. PMOS Transistors Tested with the TPS75003

PART NUMBER	MANUFACTURER	$R_{DS,ON}$ (TYP)	V_{DS}	I_D	PACKAGE
Si5447DC	Vishay Siliconix	0.11 Ω at VGS = −2.5 V	−20 V	−3.5 A at +25°C	1206
Si5475DC	Vishay Siliconix	0.041 Ω at VGS = −2.5 V	−12 V	−6.6 A at +25°C	1206
Si2323DS	Vishay Siliconix	0.052 Ω at VGS = −2.5 V	−20 V	−4.1 A at +25°C	SOT23
Si2301ADS	Vishay Siliconix	0.19 Ω at VGS = −2.5 V	−20 V	−1.4 A at +25°C	SOT23
Si2323DS	Vishay Siliconix	0.41 Ω at VGS = −2.5 V	−20 V	−4.1 A at +25°C	SOT23
FDG326P	Fairchild	0.17 Ω at VGS = −2.5 V	−20 V	−1.5 A	SC70

Table 3. Diodes Tested with the TPS75003

PART NUMBER	MANUFACTURER	V_R	I_F	PACKAGE
MBRM120LT3	ON Semiconductor	20 V	1 A	DO216AA
MBR0530T1	ON Semiconductor	30 V	1.5 A	SOD123
ZHCS2000TA	Zetex	40 V	2 A	SOT23−6
B320	Diodes Inc.	20 V	3 A	SMA
SS32	Fairchild	20 V	3 A	DO214AB

Table 4. Capacitors Tested with the TPS75003

PART NUMBER	MANUFACTURER	CAPACITANCE	ESR	VOLTAGE RATING
6TPB47M (PosCap)	Sanyo	47 µF	0.1 Ω	6.3 V
T491D476M010AS	Kemet	47 µF	0.8 Ω	10 V
B45197A	Epco	47 µF	0.175 Ω	16 V
B45294−R1107−M40	Epco	100 µF	0.045 Ω	6.3 V
594D476X0016C2	Vishay	47 µF	0.11 Ω	16 V
594D127X96R3C2	Vishay	120 µF	0.085 Ω	6.3 V
TPSC107K006R0150	AVX	100 µF	0.15 Ω	6.3 V
6TPS100MC	Sanyo	100 µF	0.45 Ω	6.3 V

OPERATION (BUCK CONTROLLERS)

Channels 1 and 2 contain two identical non-synchronous buck controllers that use minimum on-time/minimum off-time hysteretic control. (See Figure 2.) For clarity, BUCK1 is used throughout the discussion of device operation. When V_{OUT1} is below its target, an external PMOS (Q1) is turned on for at least the minimum on-time, increasing current through the inductor (L1) until V_{OUT1} reaches its target value or the current limit (set by R1) is reached. Once either of these conditions is met, the PMOS is switched off for at least the minimum off-time of the device. After the minimum off-time has passed, the output voltage is monitored and the switch is turned on again when necessary.

When output current is low, the buck controllers operate in discontinuous mode. In this mode, each switching cycle begins at zero inductor current, rises to a maximum value, then falls back to zero current. When current reaches zero on the falling edge, ringing occurs at the resonant frequency of the inductor and stray switch node capacitance. This is normal operation; it does not affect circuit performance, and can be minimized if desired by using an RC snubber and/or a resistor in series with the gate of the PMOS, as shown in Figure 22.

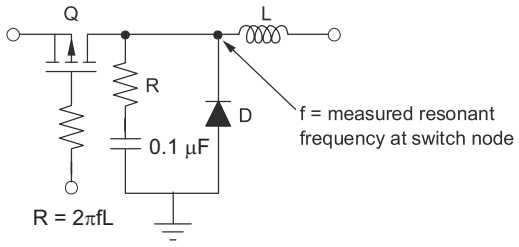


Figure 22. RC Snubber and Series Gate Resistor Used to Minimize Ringing

At higher output currents, the TPS75003 operates in continuous mode. In continuous mode, there is no ringing at the switch node and V_{OUT} is equal to V_{IN} times the duty cycle of the switching waveform.

When V_{IN} approaches or falls below V_{OUT}, the buck controllers operate in 100% duty cycle mode, fully turning on the external PMOS to allow regulation at lower dropout than would otherwise be possible.

Enable (Buck Controllers)

The enable pins (EN1 and EN2) for the buck controllers are active high. When the enable pin is driven low and input voltage is present at IN1 or IN2, an on-chip FET is turned on to discharge the soft-start pin SS1 or SS2, respectively. If the soft-start feature is being used, enable should be driven high at least 10µs after V_{IN} is applied to ensure this discharge cycle occurs.

UVLO (Buck Controllers)

An under-voltage lockout circuit is present to prevent turning on the external PMOS (Q1 or Q2) until a reliable operating voltage is reached on the appropriate regulator (IN1 or IN2). This prevents the buck controllers from mis-operation at low input voltages.

Current Limit (Buck Controllers)

An external resistor (R1 or R2) is used to set the current limit for the external PMOS transistor (Q1 or Q2). These resistors are connected between IN1 and IS1 (or IN2 and IS2) to provide a reference voltage across these pins that is proportional to the current flowing through the PMOS transistor. This reference voltage is compared to an internal reference to determine if an over-current condition exists. When current limit is exceeded, the external PMOS is turned off for the minimum off-time. Current limit detection is disabled for 10 ns any time the PMOS is turned on to avoid triggering on switching noise. In 100% duty cycle mode, current limit is always enabled. Current limit is calculated using the V_{IS1} or V_{IS2} specification in the *Electrical Characteristics* section, shown in Equation 1.

$$I_{LIMIT} = \frac{V_{IS1,2}}{R_{1,2}} \tag{1}$$

The current limit resistor must be appropriately rated for the dissipated power determined by its RMS current calculated by Equation 2.

$$I_{RMS} = I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

$$P_{DISS} = (I_{RMS})^2 \times R \tag{2}$$

For low-cost applications the $I_{S1,2}$ pin can be connected to the drain of the PMOS, using $R_{DS,ON}$ instead of R1 or R2 to set current limit. Variations in the PMOS $R_{DS,ON}$ must be taken into account to ensure that current limit will protect external components such as the inductor, the diode, and the switch itself from damage as a result of overcurrent.

Short-Circuit Protection (Buck Controllers)

In an overload condition, the current rating of the external components (PMOS, diode, and inductor) can be exceeded. To help guard against this, the TPS75003 increases its minimum off-time when the voltage at the feedback pin is lower than the reference voltage. When the output is shorted (V_{FB} is zero), minimum off-time is increased to approximately 4 µs. The increase in off-time is proportional to the difference between the voltage at the feedback pin and the internal reference.

Soft-Start (Buck Controllers)

The buck controllers each have independent soft-start capability to limit inrush during start-up and to meet timing requirements of the Xilinx Spartan-3 FPGA. Limiting inrush current by using soft-start, or by staggering the turn-on of power rails, also guards against voltage drops at the input source due to its output impedance. See the soft-start circuitry shown in Figure 23 and the soft-start timing diagram shown in Figure 24. BUCK 1 will be discussed in this section; it is identical to BUCK2. Note that pins SS1 and SS2 are high-impedance and cannot be probed using a typical oscilloscope setup. When input voltage is applied at IN1 and EN1 is driven low, any charge on the SS pin is discharged by an on-chip pulldown transistor. When EN1 is driven high, an on-chip current source starts charging the external soft-start capacitor C_{SS1}. The voltage on the capacitor is compared to the voltage across the current sense resistor R1 to determine if an over-current condition exists. If the voltage drop across the sense resistor goes above the reference voltage, then the external PMOS is shut off for the minimum off-time. This implementation provides a cycle-by-cycle current limit and allows the user to program the soft-start time over a wide range for most applications. For detailed information on choosing C_{SS1} and C_{SS2}, see the section, *Selecting the Soft-Start Cap.*

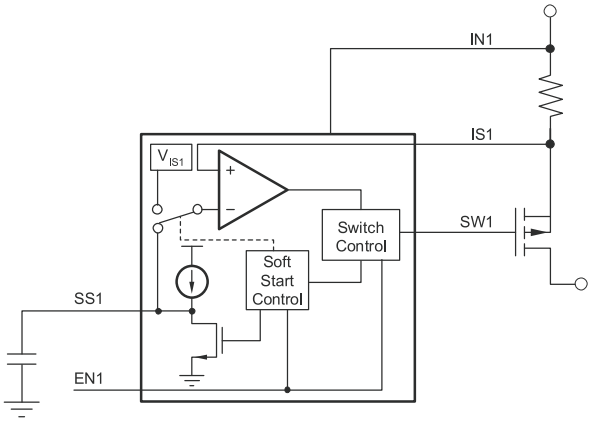


Figure 23. Soft-Start Circuitry

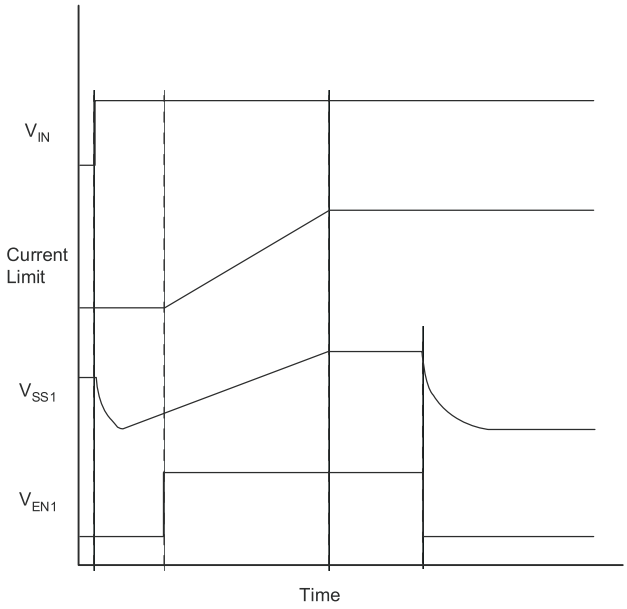


Figure 24. Soft-Start Timing Diagram

Input Capacitor C_{IN1}, C_{IN2} Selection (Buck Controllers)

It is good analog design practice to place input capacitors near the inputs of the device in order to ensure a low impedance input supply. A capacitance of 10 µF to 22 µF for each buck converter is adequate for most applications, and should be placed within 100 mils (0.001 in) of the IN1 and IN2 pins to minimize the effects of pulsed current switching noise on the soft-start circuitry during the first ~1 V of output voltage ramp. Low ESR capacitors also help to minimize noise on the supply line. The minimum value of capacitance can be estimated using Equation 3.

$$C_{IN},\ MIN = \frac{(1/2)L \times (\Delta I_L)^2}{V_{RIPPLE} \times V_{IN}} \approx \frac{(1/2)L \times (0.3 \times I_{OUT})^2}{V_{(RIPPLE)} \times V_{IN}} \quad (3)$$

Note that the capacitors must be able to handle the RMS current in continuous conduction mode, which can be calculated using Equation 4.

$$I_{C,IN(RMS)} \approx \sqrt{\left(\frac{V_{OUT}}{V_{IN},MIN}\right)} \quad (4)$$

Inductor Value Selection (Buck Controllers)

The inductor is chosen based on inductance value and maximum current rating. Larger inductors reduce current ripple (and therefore, output voltage ripple) but are physically larger and more expensive. Inductors with lower DC resistance typically improve efficiency, but also have higher cost and larger physical size. The buck converters work well with inductor values between 4.7 µH and 47 µH in most applications. When selecting an inductor, the current rating should exceed the current limit set by R_{IS} or $R_{DS,ON}$ (see *Current Limit* section). To determine the minimum inductor size, first determine if the device will operate in minimum on-time or minimum off-time mode. The device will operate in minimum on-time mode if Equation 5 is satisfied.

$$V_{IN} - V_{OUT} - IOUT \times r_{DS(on)} - R_L \times I_{OUT} \geq \frac{t_{(OFF,min)} \times \left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT}\right)}{t_{ON},MIN} \quad (5)$$

where R_L = the inductor's DC resistance.

Minimum inductor size needed when operating in minimum on-time mode is given by Equation 6.

$$L_{MIN} = \frac{\left(V_{IN} - V_{OUT} - I_{OUT} \times r_{DS(on)} - R_L \times I_{OUT}\right) \times t_{ON},MIN}{\Delta I} \quad (6)$$

Minimum inductor size needed when operating in minimum off-time mode is given by Equation 7.

$$L_{MIN} = \frac{\left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT}\right) \times t_{OFF},MIN}{\Delta I} \quad (7)$$

External PMOS Transistor Selection (Buck Controllers)

The external PMOS transistor is selected based on threshold voltage (V_T), on-resistance ($R_{DS,ON}$), gate capacitance (C_G) and voltage rating. The PMOS V_T magnitude must be much lower than the lowest voltage at IN1 or IN2 that will be used. A V_T magnitude that is 0.5 V less than the lowest input voltage is normally sufficient. The PMOS gate will see voltages from 0 V to the maximum input voltage, so gate-to-source breakdown should be a few volts higher than the maximum input supply. The drain-to-source of the device will also see this full voltage swing, and should therefore be a few volts higher than the maximum input supply. The RMS current in the PMOS can be estimated by using Equation 8.

$$I_{PMOS(RMS)} \approx I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}} \quad (8)$$

The power dissipated in the PMOS is comprised of both conduction and switching losses. Switching losses are typically insignificant. The conduction losses are a function of the RMS current and the $R_{DS,ON}$ of the PMOS, and are calculated by Equation 9.

$$P_{(cond)} = \left(I_{OUT}\sqrt{D}\right)^2 \times r_{DS(on)} \times \left(1 + TC \times \left[T_J - 25°C\right]\right) \approx \left(I_{OUT}\sqrt{D}\right) \times r_{DS(on)} \quad (9)$$

Diode Selection (Buck Controllers)

The diode is off when the PMOS is on, and on when the PMOS is off. Since it will be turned on and off at a relatively high frequency, a Schottky diode is recommended for good performance. The peak current rating of the diode should exceed the peak current limit set by the sense resistor $R_{IS1,2}$. A diode with low reverse leakage current and low forward voltage at operating current will optimize efficiency. Equation 10 calculates the estimated average power dissipation.

$$I_{(diode)(RMS)} \approx I_{OUT}(1 - D) = I_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

Output Capacitor Selection (Buck Controllers)

The output capacitor is selected based on output voltage ripple and transient response requirements. As a result of the nature of the hysteretic control loop, a minimum ESR of a few tens of mΩ should be maintained for good operation unless a feed-forward resistor is used. Low ESR bulk tantalum or PosCap capacitors work best in most applications. A 1-µF ceramic capacitor can be used in parallel with this capacitor to filter higher frequency spikes. The output voltage ripple can be estimated by Equation 11.

$$\Delta V_{PP} = \Delta I \times \left[ESR + \left(\frac{1}{8 \times COUT \times f}\right)\right] \approx 1.1\Delta I \times ESR \quad (11)$$

To calculate the capacitance needed to achieve a given voltage ripple as a result of a load transient from zero output to full current, use Equation 12.

$$C_{OUT} = \frac{L \times \Delta I_{OUT}^2}{(V_{IN} - V_{OUT}) \times \Delta V} \quad (12)$$

If only ceramic or other very low ESR output capacitor configurations are desired, additional voltage ripple must be passed to the feedback pin. See Application Note, Using Ceramic Output Capacitors with the TPS6420x Buck Controllers (SLVA210), for detailed application information.

Output Voltage Ripple Effect on V_{OUT} (Buck Controllers)

Output voltage ripple causes V_{OUT} to be higher or lower than the target value by half of the peak-to-peak voltage ripple. For minimum on-time, the ripple adds to the voltage; for minimum off-time, it subtracts from the voltage.

Soft-Start Capacitor Selection (Buck Controllers)

BUCK1 is discussed in this section; it is identical to BUCK2. Soft-start is implemented on the buck controllers by ramping current limit from 0 to its target value (set by R1) over a user-defined time. This time is set by the external soft-start cap connected to pin SS1. If SS1 is left open, a small on-chip capacitor will provide a current limit ramp time of approximately 250 µs. Figure 25 shows the effects of R1 and SS1 on the current limit start-up ramp.

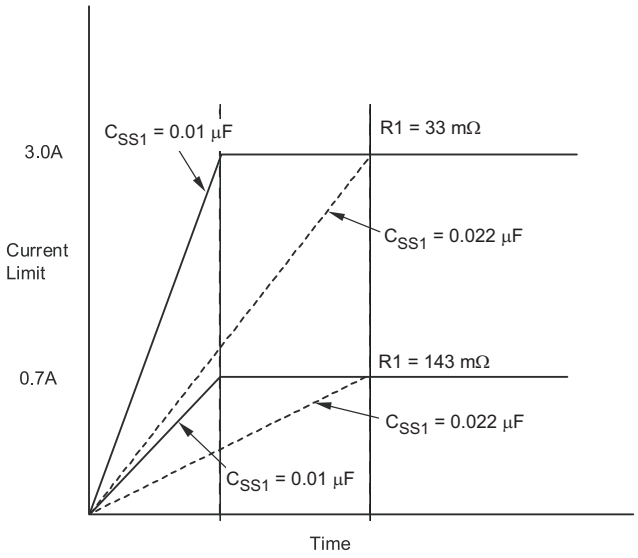


Figure 25. Effects of C_{SS1} and R_1 on Current Ramp Limit

This soft-start current limit ramo can be used to provide inrush current control or output voltage ramp control. While the current limit ramp can be easily understood by looking at Figure 25, the output voltage ramp is a complex function of many variables. The dominant variables in this process are V_{OUT1}, C_{SS1}, I_{OUT1}, and R_1. Less important variables are V_{IN1} and L_1.

The best way to set a target start-up time is through bench measurement under target conditions, adjusting C_{SS1} to get the desired startup profile. To stay above a minimum start-up time, set the nominal start-up time to approximately five times the minimum. To stay below a maximum time, set the nominal start-up time at one-fifth of the maximum. Fastest start-up times occur at maximum V_{IN1}, with minimum V_{OUT1}, L_1, C_{OUT1}, C_{SS1}, and I_{OUT1}. Slowest start-up times occur under opposite conditions.

See Figure 11 to Figure 14 for characterization curves showing how the start-up profile is affected by these critical parameters.

Output Voltage Setting Selection (Buck Controllers)

Output voltage is set using two resistors as shown for Buck2 in Figure 2. Output voltage is then calculated using Equation 13.

$$V_{OUT} = V_{FB}\left(\frac{R_5}{R_6}+1\right) \quad (13)$$

where V_{FB} = 1.24V.

LDO OPERATION

The TPS75003 LDO uses a PMOS pass element and is offered in an adjustable version for ease of programming to any output voltage. When used to power $V_{CC,AUX}$ it is set to 2.5 V; it can optionally be set to other output voltages to power other circuitry. The LDO has integrated soft-start, independent enable, and short-circuit and thermal protection. The LDO can be used to power $V_{CC,AUX}$ on the Xilinx Spartan-3 FPGA when 3.3-V JTAG signals are used as described in Application Note SLVA159 (available for download from www.ti.com).

Input Capacitor Selection (LDO)

Although an input capacitor is not required, it is good analog design practice to connect a 0.1-µF to 10-µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, stability, and ripple rejection. A higher value capacitor may be needed if large, fast rise-time load transients are anticipated, or if the device is located far from its power source.

Output Capacitor Selection (LDO)

A 2.2 µF or greater capacitor is required near the output of the device to ensure stability. The LDO is stable with any capacitor type, including ceramic. If improved transient response or ripple rejection is required, larger and/or lower ESR output capacitors can be used.

Soft-Start (LDO)

The LDO uses an external soft-start capacitor, C_{SS3}, to provide an RC-ramped reference voltage to the control loop. (See the Functional Block Diagram.) This is a voltage-controlled soft-start, as compared to the current-controlled soft-start used by the buck controllers.

Setting Output Voltage (LDO)

Output voltage is set using two resistors as shown in Figure 2. Output voltage is then calculated using Equation 14.

$$V_{OUT} = V_{FB}\left(\frac{R_3}{R_4} + 1\right) \tag{14}$$

where V_{FB} = 0.507 V.

Internal Current Limit (LDO)

The internal current limit of the LDO helps protect the regulator during fault conditions. When an over-current condition is detected, the output voltage will be reduced until the current falls to a level that will not damage the device. For good device reliability, the LDO should not operate at current limit.

Enable Pin (LDO)

The active high enable pin (EN3) can be used to put the device into shutdown mode. If shutdown and soft-start capability are not required, EN3 can be tied to IN3.

Dropout Voltage (LDO)

The LDO uses a PMOS transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the pass device is in its linear region of operation, and the input-output resistance is the $R_{DS,ON}$ of the pass transistor. In this region, the regulator is said to be out of regulation; ripple rejection, line regulation, and load regulation degrade as (V_{IN} – V_{OUT}) falls much below 0.5 V.

Transient Response (LDO)

The LDO does not have an on-chip pulldown circuit for output is over-voltage conditions. This feature permits applications that connect higher voltage sources such as an alternate power supply to the output. This design also results in an output overshoot of several percent if the load current quickly drops to zero. The amplitude of overshoot can be reduced by increasing C_{OUT}; the duration of overshoot can be reduced by adding a load resistor.

Thermal Protection (LDO)

Thermal protection disables the output when the junction temperature, T_J, reaches unsafe levels. When the junction cools, the output is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage. For good long term reliability, the device should not be continuously operated at or near thermal shutdown.

Power Dissipation (LDO)

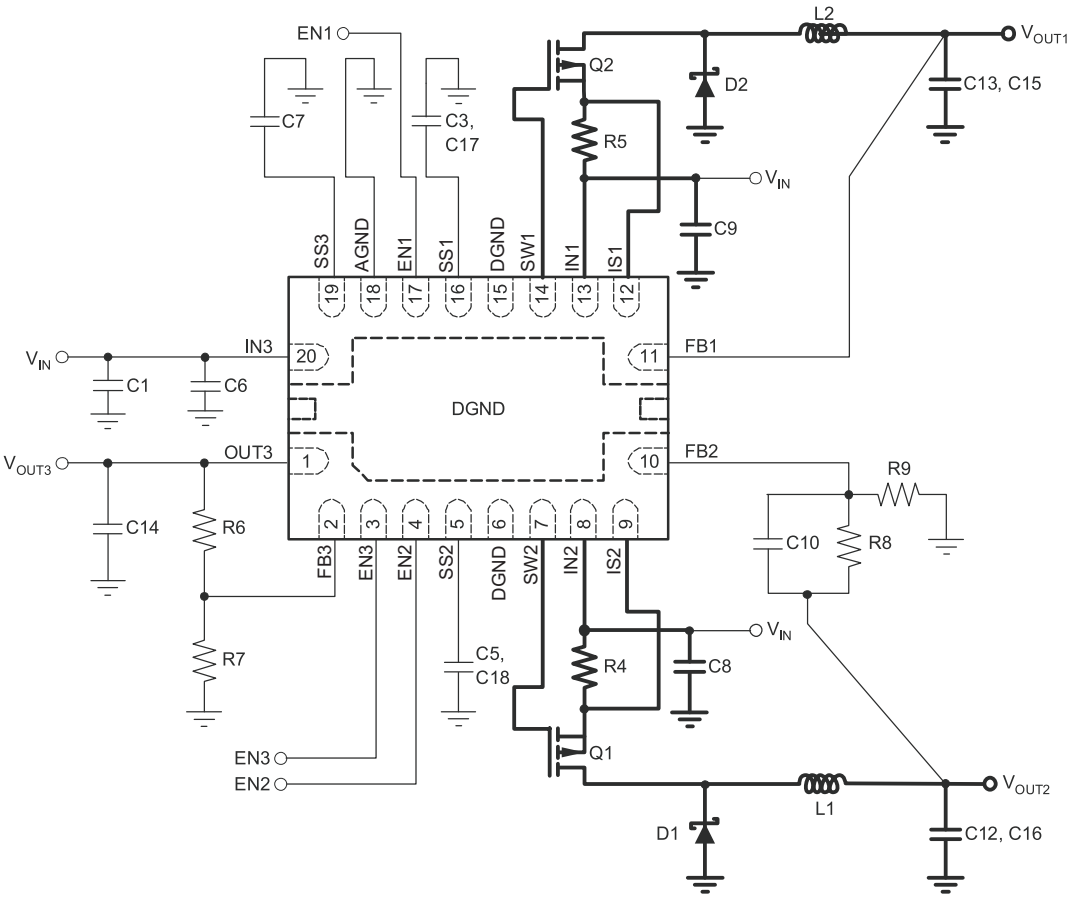
The TPS75003 comes in a QFN-style package with an exposed lead frame on the package underside. The exposed lead frame is the primary path for removing heat and should be soldered to a PC board that is configured to remove the amount of power dissipated by the LDO, as calculated by Equation 15.

$$P_D = (V_{IN3} - V_{OUT3}) \times I_{OUT3} \quad (15)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage. The two buck converters do not contribute a significant amount of dissipated power. Using heavier copper increases the overall effectiveness of removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

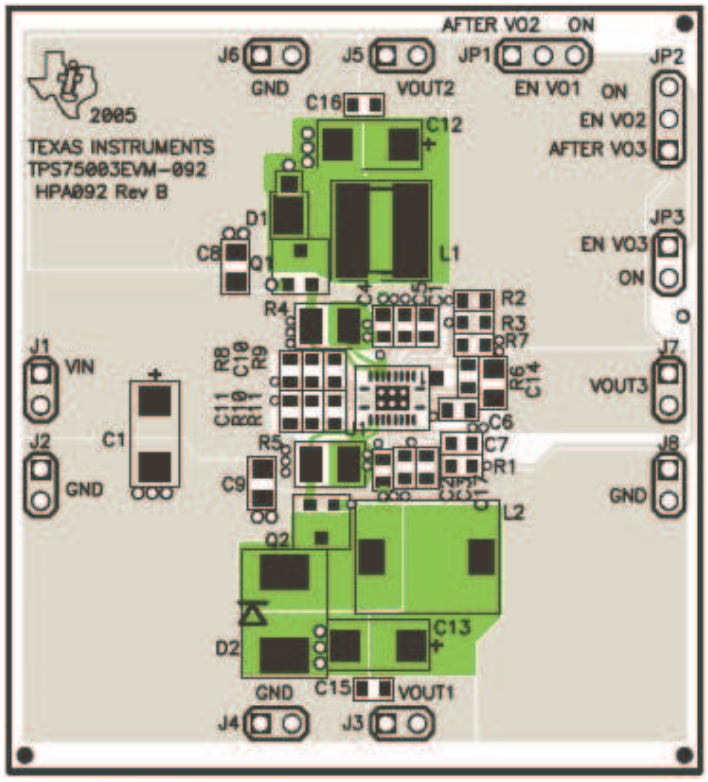
PCB Layout Considerations

As with any switching regulators, careful attention must be paid to board layout. A typical application circuit and corresponding recommended printed circuit board (PCB) layout with emphasis on the most sensitive areas are shown in Figure 26 through Figure 28.



Note: Most sensitive areas are highlighted by bold lines.

Figure 26. Typical Application Circuit



Note: Most sensitive areas are highlighted in green.

Figure 27. Recommended PCB Layout, Component Side, Top View

Note: Most sensitive areas are highlighted in green.

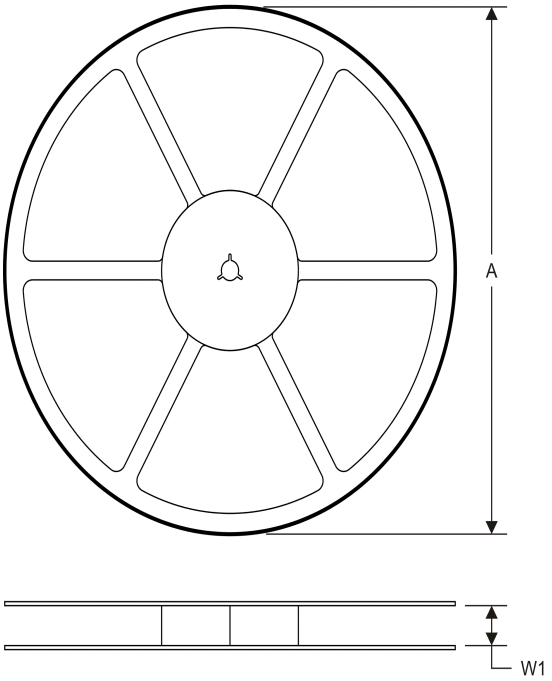
Figure 28. Recommended PCB Layout, Bottom Side, Top View

REVISION HISTORY

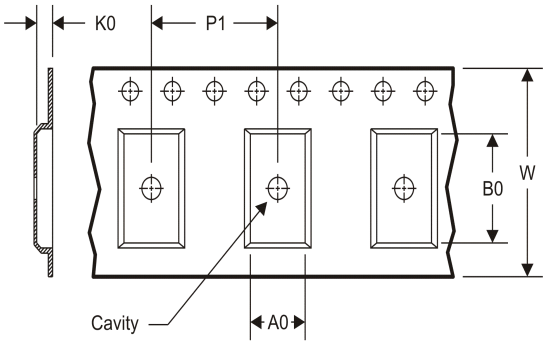
Changes from Original (December 2006) to Revision A	Page
• Replaced the DISSIPATION RATINGS table with the Thermal Information Table	3

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



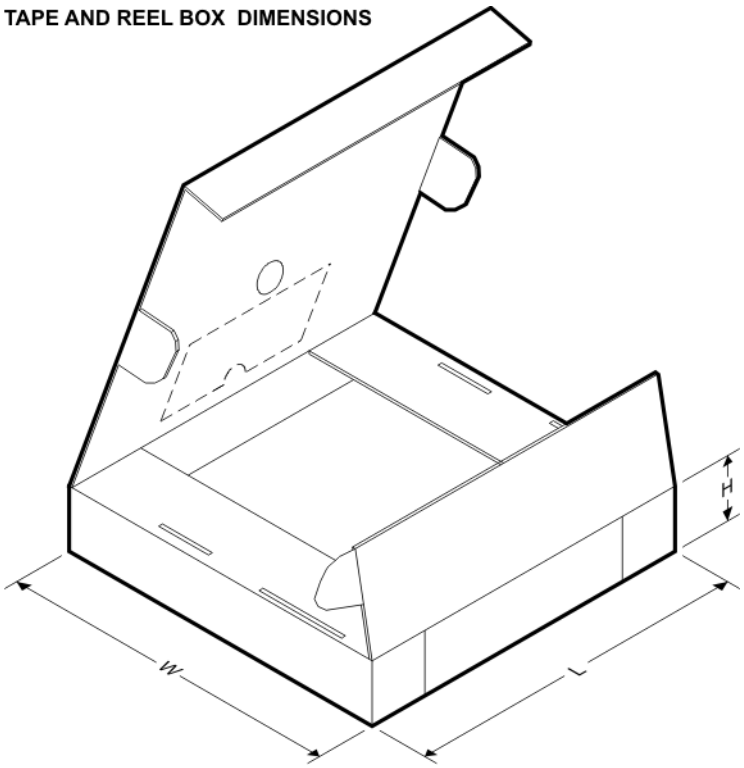
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75003MRHLREP	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

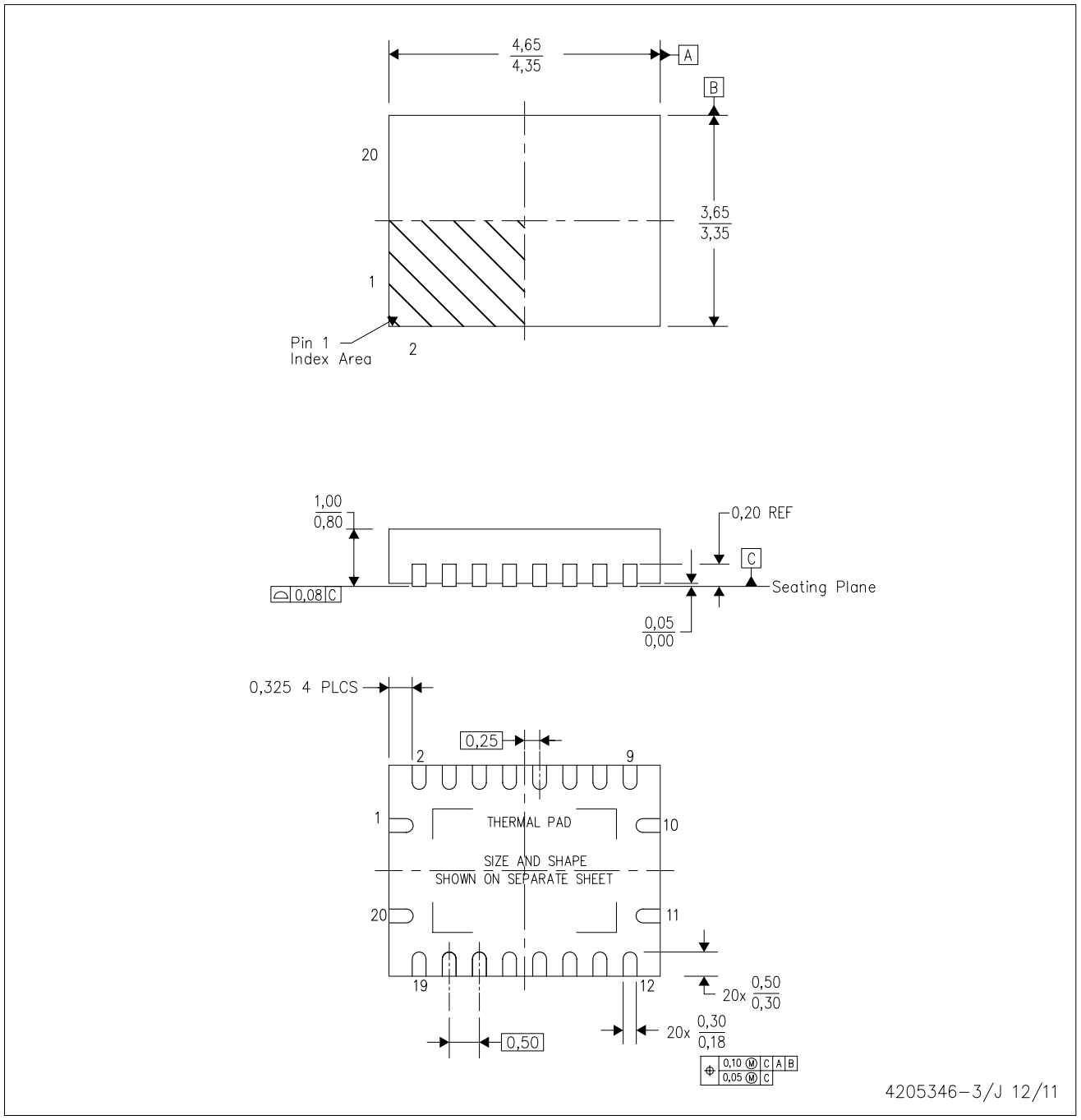
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75003MRHLREP	QFN	RHL	20	3000	367.0	367.0	35.0

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

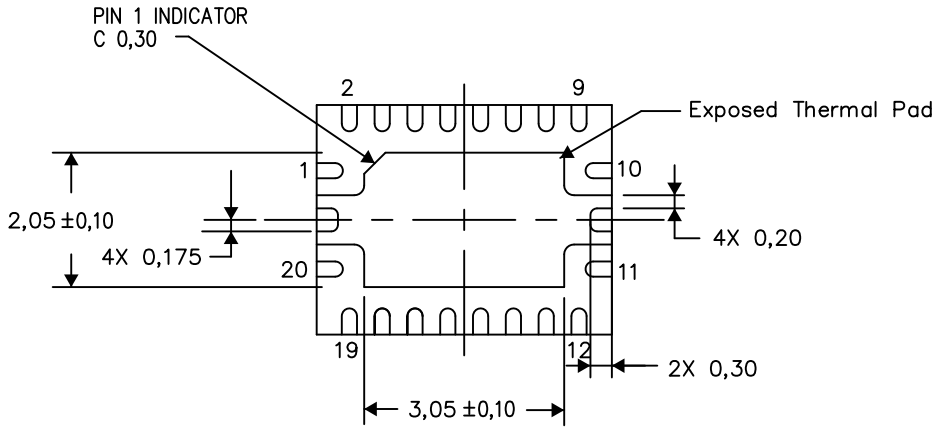
RHL (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



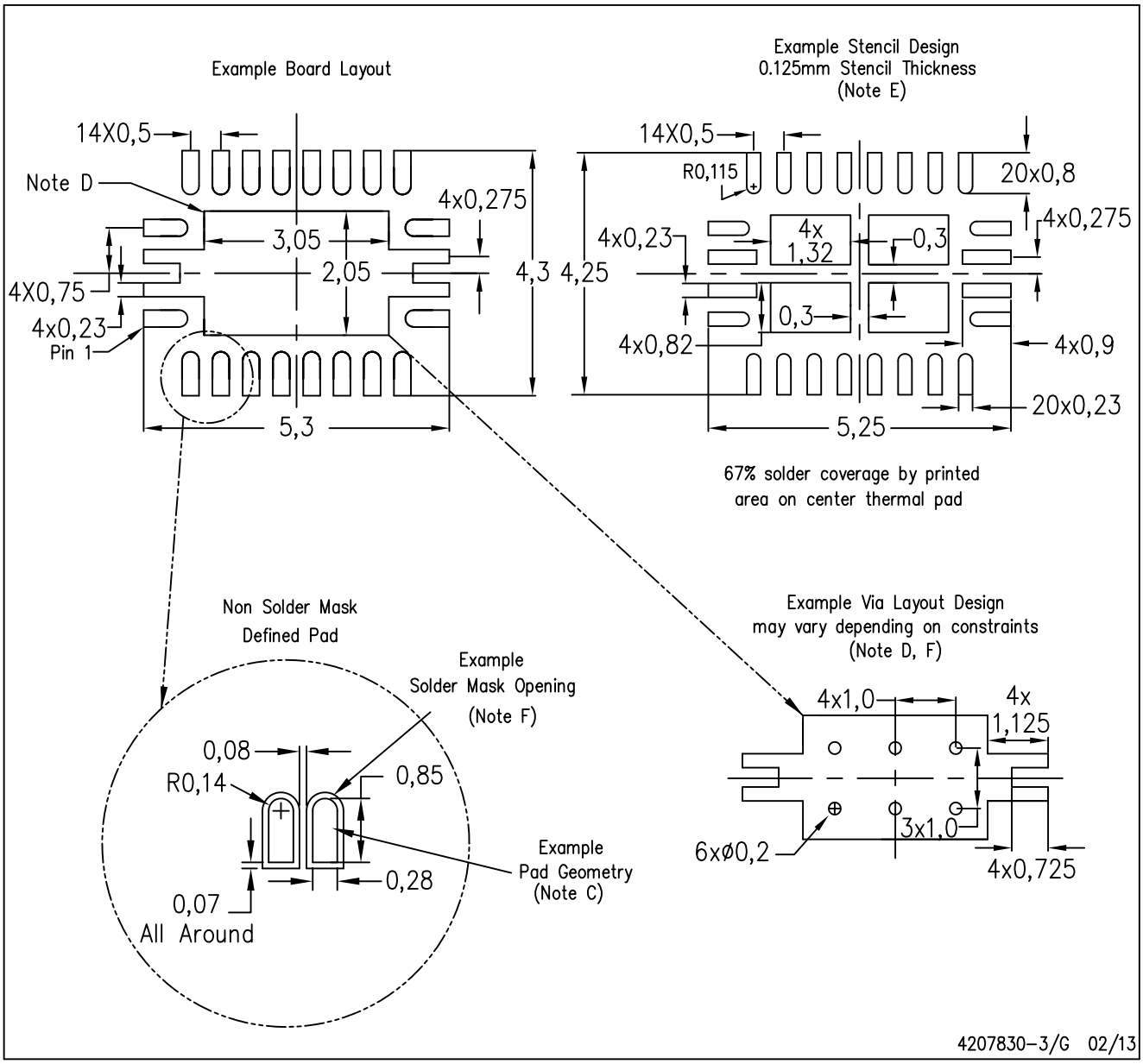
Bottom View

Exposed Thermal Pad Dimensions

4206363–3/M 08/12

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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