Application Report
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Simple Power Solution Using LDOs

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ABSTRACT

This reference design helps those desiring to design-in the TMS320C6742, TMS320C6746, TMS320C6748, and OMAP-L138. This design, employing sequenced power supplies, describes a system with an input voltage of 3.3 V, and uses LDOs for a small, simple system.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. This application report addresses these topics and suggests solutions for output voltage sequencing.

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1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bidirectional bus during power up. Bus contention also may affect I/O reliability. Power supply designers must check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in Table 1. No specific voltage ramp rate is required for any of the supplies as long as the 3.3-V rail never exceeds the 1.8-V rail by more than 2 volts.

2 Power Requirements

The power requirements are as specified in the following table.

Table 1. Power Requirements

	PIN NAME	VOLTAGE (1) (2) (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1(3)	
Core	CVDD(4)	1.0 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90(5)	±5%	4 / 5	

(1) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1)

(2) No specific voltage ramp rate is required for any of the supplies as long asa LVCMOS33 (USB0_VDDA33, USB1_VDDA33) never exceeds STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) by more than 2 volts.

(3) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(4) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail is 1/3 the above maximum power.

3 Features

The design uses the LDOs.

INPUT VOLTAGE	~3.3 V
	Simple (no DVFS)
COMBINE RTC AND STATIC 1.2	
Core 1.2 V at 600 mA	TPS74801
Static 1.2 V + VRTC at 251 mA	TPS74701
Static 1.8 V at 230 mA	TPS71718
Static 3.3 V at 115 mA	TPS74801

Here VRTC is included in the STATIC12 (fixed 1.2V) group.

TPS74801 and TPS74701

- VOUT Range: 0.8 V to 3.6 V
- 2% Accuracy Over Line/Load/Temperature
- Programmable Soft-Start Provides Linear Voltage Startup
- Stable with Any Output Capacitor ≥ 2.2 μF
- Available in a Small 3-mm × 3-mm × 1-mm SON-10 and 5 × 5 QFN-20 Packages

TPS71718

- 150-mA Low-Dropout Regulator with Enable
- Low Noise: 30 μV typical (100 Hz to 100 kHz)
- Excellent Load/Line Transient Response
- Small SC70-5, 2-mm × 2-mm SON-6, and 1,5-mm × 1,5-mm SON-6 Packages

More information on the devices can be found from the data sheets.

- TPS74801, http://focus.ti.com/lit/ds/symlink/tps74801.pdf
- TPS74701, http://focus.ti.com/lit/ds/symlink/tps74701.pdf
- TPS71718, http://focus.ti.com/lit/ds/symlink/tps71718.pdf

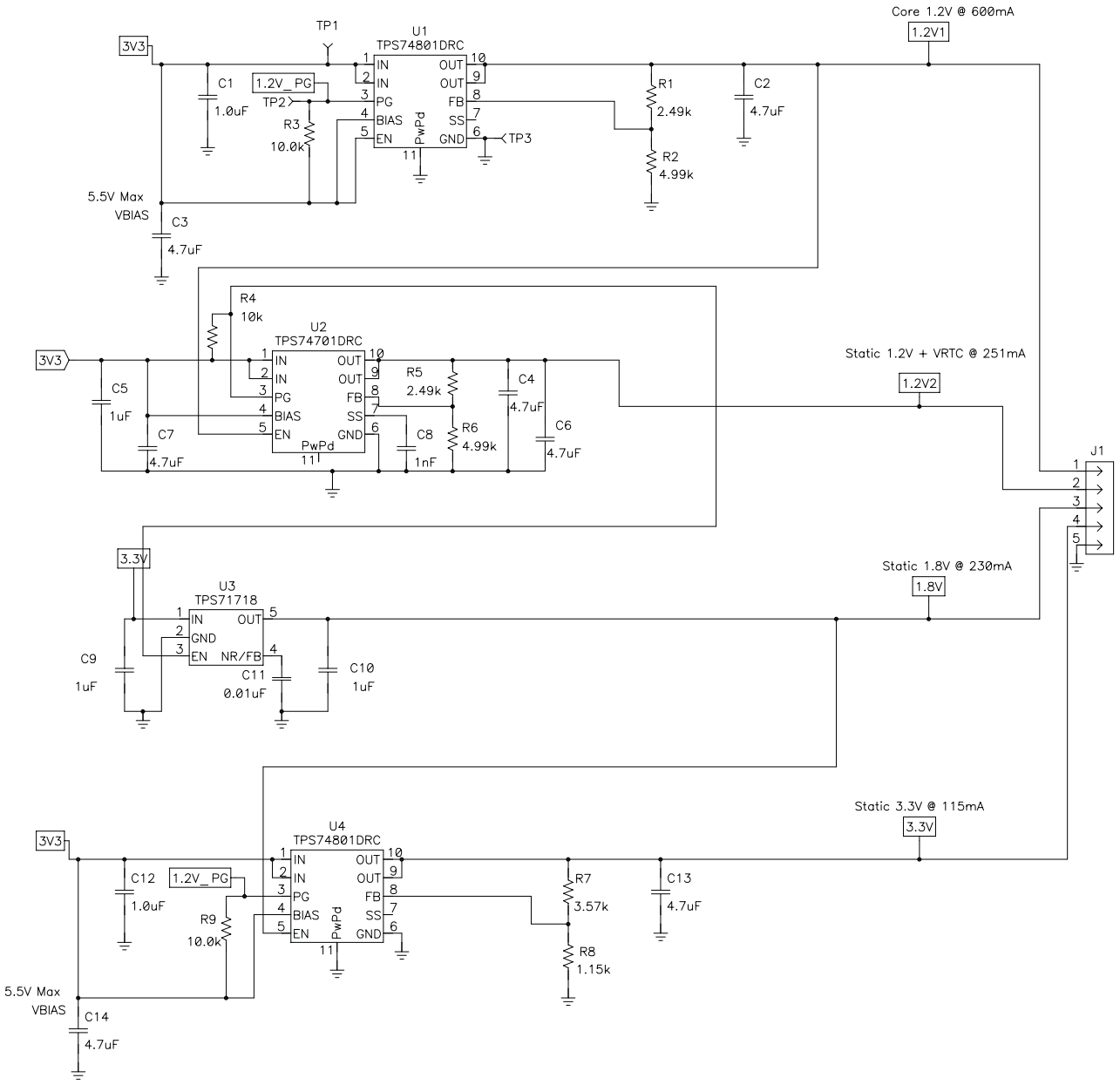
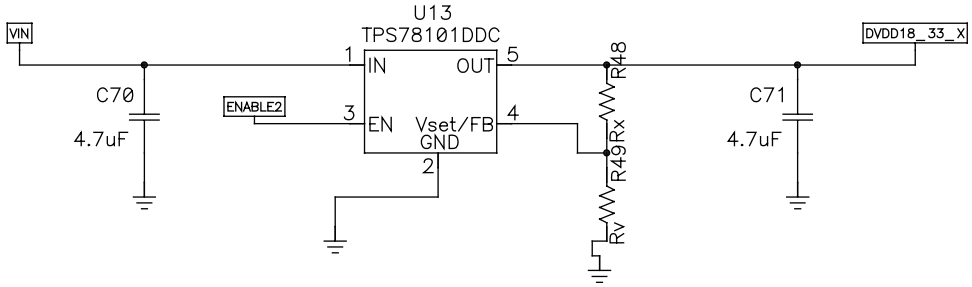


Figure 1. PMP4980 Reference Design Schematic

Proper sequencing is ensured in the design with the use of enable pins. As required, Core 1.2 V at 600 mA comes first, followed by Static 1.2 V + VRTC at 251 mA, Static 1.8 V at 230 mA which in turn enable the LDO and hence at last Static 3.3 V at 115 mA comes up.



(1) Use three such LDOs to power up DVDDA, DVDDB, DVDDC (It can either be 1.8 V or 3.3 V)

(2) Rx = 0.499 MΩ, Ry = 1 MΩ for Vout = 1.8 V

(3) Rx = 1.8 MΩ, Ry = 1 MΩ for Vout = 3.3 V

(4) For proper sequencing of output, enable of the LDOs are fed either from 1.2-V output from TPS74701 if DVDDX is 1.8 V or from 1.8-V output from TPS71718 if DVDDX is 3.3 V.

Figure 2. Optional Circuit for DVDD_A, DVDD_B, and DVDD_C

4 List of Material

Table 2. PMP4980 List of Material

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	1.0uF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK	5650
2	C2	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J106M	TDK	5650
2	C3	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J475K	TDK	5650
3	C4	4.7uF	Capacitor, Ceramic,4.7uF, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
1	C5	1uF	Capacitor, Ceramic,1uF, 16V, X5R	0603	C1608X5R1C105K	TDK	5650
	C6	4.7uF	Capacitor, Ceramic,4.7uF, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
	C7	4.7uF	Capacitor, Ceramic,4.7uF, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
1	C8	1nF	Capacitor, Ceramic, 1000pF, 50V, X7R, 10%	0603	C1608X7R1H102K	TDK	5650
2	C9	1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650
	C10	1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650
1	C11	0.01uF	Capacitor, Ceramic, 50V, COG, 10%	0402	Std	Std	2800
1	C12	1.0uF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK	5650
	C13	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J106M	TDK	5650
	C14	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J475K	TDK	5650
1	J1	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch × 5	PEC36SAAN	Sullins	60000
1	R1	2.49k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R2	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
2	R3	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R4	10k	Resistor, Chip, 10k-Ohms 1/16W, 5%	0603	Std	Std	5,650
1	R5	2.49k	Resistor, Chip, 2k49-Ohms, 1/16W, 5%	0603	Std	Std	5,650
1	R6	4.99k	Resistor, Chip, 4k99-Ohms, 1/16W, 5%	0603	Std	Std	5,650
1	R7	3.57k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R8	1.15k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R9	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
2	TP1	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keyston e	10
	TP2	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keyston e	10
1	TP3	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keyston e	10
2	U1	TPS74801DRC	IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74801DRC	TI	30400
1	U2	TPS74701DRC	IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74701DRC	TI	30400
1	U3	TPS71718	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71718	TI	18600
	U4	TPS74801DRC	IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74801DRC	TI	30400

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of unclean flux is unacceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Results

The start-up waveform is shown in Figure 3, which specifies the sequencing order that is required.

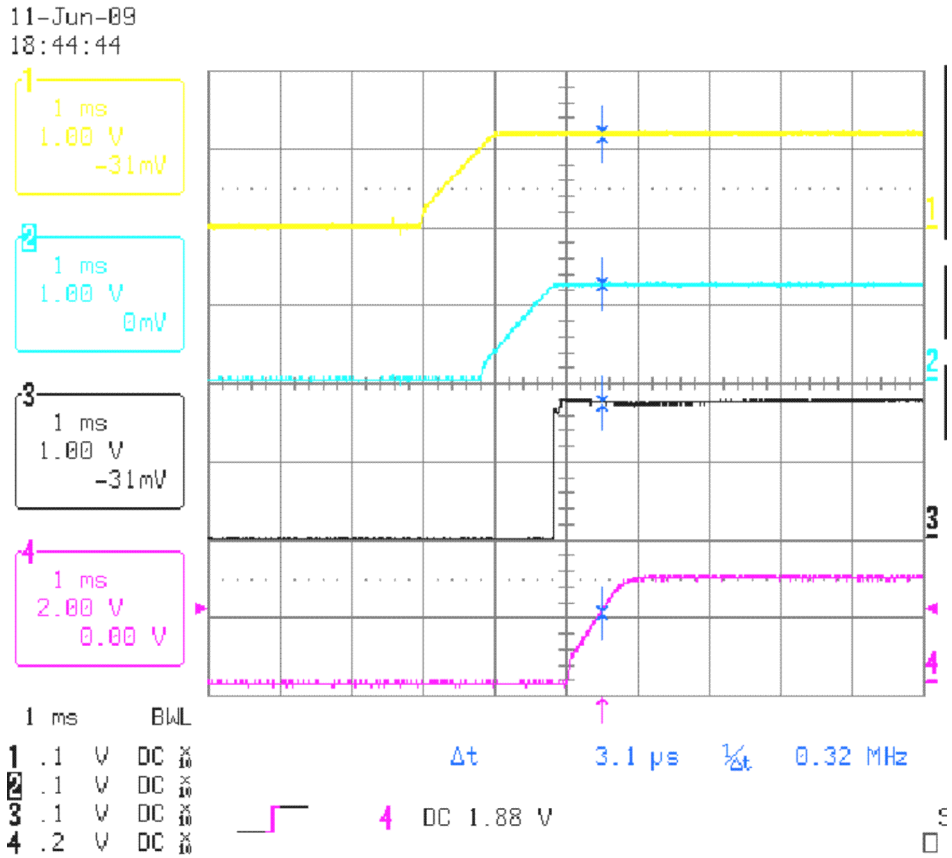


Figure 3. Sequencing in Start-Up Waveform

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