TPS746 1-A LDO With Power-Good in a Small 2-mm × 2-mm WSON Package

1 Features

- Input Voltage Range: 1.5 V to 6.0 V
- Adjustable Output Voltage:
  - 0.55 V to 5.5 V
- Very Low Dropout:
  - 250 mV (max) at 1 A (3.3 V_{OUT})
- Open-Drain Power-Good Output
- I_Q: 25 µA (Typical)
- Output Accuracy: 1% (Maximum)
- Built-In Soft-Start With Monotonic V_{OUT} Rise
- Package:
  - 2-mm × 2-mm WSON-6 (DRV)
- Active Output Discharge

2 Applications

- Set-Top Boxes, Gaming Consoles
- Home Theater and Entertainment
- Desktops, Notebooks, Ultrabooks
- Printers
- Servers
- Thermostat and Lighting Control
- Electronic Point of Sale (EPOS)

3 Description

The TPS746 is an adjustable 1-A low-dropout (LDO) regulator with power-good functionality. This device is available in a small, 6-pin, 2-mm × 2-mm WSON package and consumes very low quiescent current and provides fast line and load transient performance. The TPS746 features an ultra-low dropout of 250 mV at 1 A that can help improve the power efficiency of the system.

The TPS746 is optimized for a wide variety of applications by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.55 V to 5.5 V. The low output voltage enables this LDO to power the modern microcontrollers with lower core voltages.

The TPS746 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for the sequencing multiple power sources in the system.

The TPS746 is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides a maximum accuracy of 1%. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS746 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

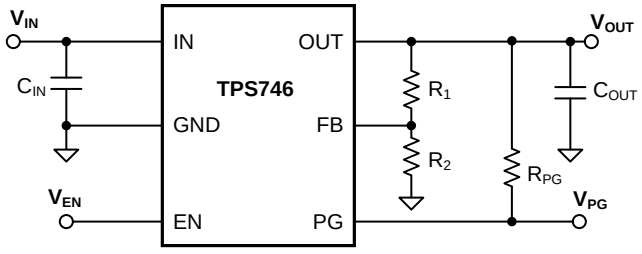
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS746	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical Application



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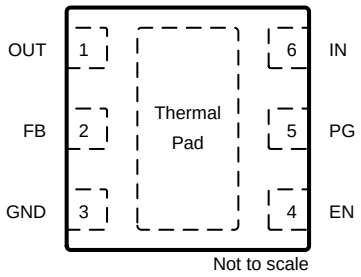
4 Revision History

DATE	REVISION	NOTES
April 2018	*	Initial release.

5 Pin Configuration and Functions

DRV Package
6-Pin Adjustable WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	WSON		
EN	4	Input	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to put the LDO into shutdown mode.
FB	2	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	—	Ground pin
IN	6	Input	Input pin. A minimum of 0.22-µF capacitance is required from this pin to ground.
OUT	1	Output	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground; see the *Input and Output Capacitor Selection* section.
PG	5	Output	Power-good output
Thermal pad	Pad	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	6.5	V
	Enable, V_{EN}	–0.3	6.5	
	Power-good, V_{PG}	–0.3	6.5	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Current	Enable, I_{EN}		TBD	µA
	Power-good, I_{PG}		±10	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{OUT}	Output voltage	0.55		5.5	V
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor	1		200	µF
V_{EN}	Enable voltage	0		6.0	V
V_{PG}	PG voltage	0		6.0	V
T_J	Junction temperature	–40		125	°C

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC[1]		TPS746 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.5		6.0	V
V_{OUT}	Output voltage			0.55		5.5	V
	Output accuracy	–40°C ≤ T_J ≤ +85°C, V_{OUT} ≥ 1.0 V		–1%		1%	
		–40°C ≤ T_J ≤ +85°C, 0.6 V ≤ V_{OUT} < 1.0 V		–10		10	mV
		V_{OUT} ≥ 1 V		–1.5%		1.5%	
		0.6 V ≤ V_{OUT} < 1 V		–15		15	mV
	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.0 V			2		mV
	Load regulation	0.1 mA ≤ I_{OUT} ≤ 1A			0.050		V/A
I_{GND}	Ground current	T_J = 25°C		14	25	33	µA
		–40°C ≤ T_J ≤ +85°C				35	
		–40°C ≤ T_J ≤ +125°C				45	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 1.5 V ≤ V_{IN} ≤ 6.0 V			0.1	1	µA
I_{FB}	Feedback pin current				0.01	0.1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 0.5 V	V_{OUT} = $V_{OUT(NOM)}$ – 0.2 V, V_{OUT} ≤ 1.5 V	1.20	1.44	1.73	A
			V_{OUT} = 0.9 V × $V_{OUT(NOM)}$, 1.5 V < V_{OUT} ≤ 5.5 V	1.20	1.44	1.73	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			770		mA
V_{DO}	Dropout voltage	I_{OUT} = 1 A, –40°C ≤ T_J ≤ +125°C	0.6 V ≤ V_{OUT} < 0.8 V		896	1050	mV
			0.8 V ≤ V_{OUT} < 1.0 V		765	910	
			1.0 V ≤ V_{OUT} < 1.2 V		600	735	
			1.2 V ≤ V_{OUT} < 1.5 V		464	580	
			1.5 V ≤ V_{OUT} < 1.8 V		332	410	
			1.8 V ≤ V_{OUT} < 2.5 V		264	340	
			2.5 V ≤ V_{OUT} < 3.3 V		193	250	
			3.3 V ≤ V_{OUT} < 5.5 V		161	205	
PSRR	Power-supply rejection ratio	f = 1 kHz			66		dB
		f = 100 kHz			45		
		f = 1 MHz			30		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 0.6 V			30		μV_{RMS}
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.27	1.33	1.42	V
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} falling			45		mV
t_{STR}	Startup time	From EN low-to-high transition to V_{OUT} = V_{OUT} × 95%			500		µs

ADVANCE INFORMATION

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HI}	EN pin high voltage (enabled)		1.0			V
V_{LO}	EN pin low voltage (enabled)				0.3	V
I_{EN}	Enable pin current	V_{IN} = EN = 6.0 V		10		nA
$R_{PULL\ DOWN}$	Pulldown resistance	V_{IN} = 6.0 V		120		Ω
PG_{HTH}	PG high threshold	V_{OUT} increasing	90	92	94	$\%V_{OUT}$
PG_{LTH}	PG low threshold	V_{OUT} decreasing	88	90	92	$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} ≥ 1.4 V, I_{SINK} = 0.2 mA			300	mV
		V_{IN} ≥ 2.5 V, I_{SINK} = 0.5 mA			300	mV
		V_{IN} ≥ 4.5 V, I_{SINK} = 1.0 mA			300	mV
$V_{OH(PG)}$	PG pin high-level output voltage	V_{IN} ≥ 1.4 V, I_{SOURCE} = 0.2 mA	0.8 × V_{OUT}			V
		V_{IN} ≥ 2.5 V, I_{SOURCE} = 0.5 mA	0.8 × V_{OUT}			V
		V_{IN} ≥ 4.5 V, I_{SOURCE} = 1.0 mA	0.8 × V_{OUT}			V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > PG_{HTH}, V_{PG} = 5.5 V			300	nA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		155		

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{PGDH}	PG delay time (rising) from V_{OUT} > PG threshold to PG toggling, overdrive = 10%	145	165	178	µs
t_{PGDL}	PG delay time (falling) from V_{OUT} < PG threshold to PG toggling, overdrive[(1)] = 10%	5	7	10	µs

(1) Overdrive = | (V_{OUT} / PG_{TH} – 1) × 100%.

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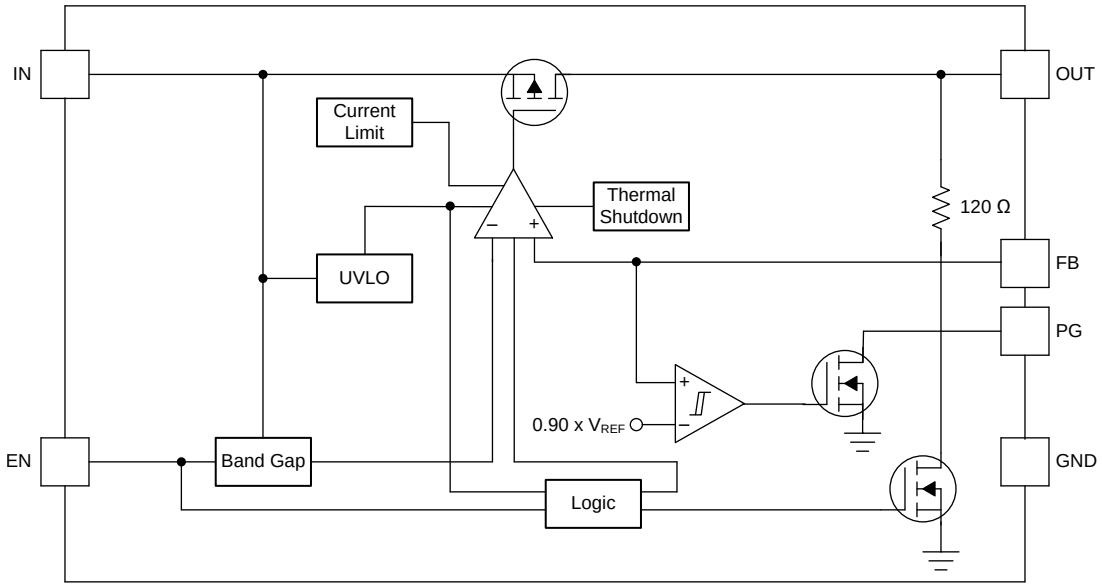
7 Detailed Description

7.1 Overview

The TPS746 belongs to a family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low dropout voltage, make this device ideal for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS746 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI} (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V (V_{LO}). If shutdown capability is not required, connect EN to IN.

The TPS746 has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. Equation 1 calculates the time constant:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

ADVANCE INFORMATION

Feature Description (continued)

7.3.3 Internal Foldback Current Limit

The TPS746 has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid brick-wall scheme until the output voltage is less than 0.4 V × $V_{OUT(NOM)}$; when the voltage drops below 0.4 V × $V_{OUT(NOM)}$, a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output is shorted, the LDO supplies a typical current of 100 mA. The output voltage is not regulated when the device is in current limit. When the device output is shorted, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{LIM}) during startup. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the load current demanded by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant-current loads, disable the output load until the TPS746 has fully risen to its nominal output voltage.

The TPS746 PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current may flow through the body diode.

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS746 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS746 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

Table 1 lists a comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout(1)	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Output

Figure 1 shows that the output voltage of the TPS746 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

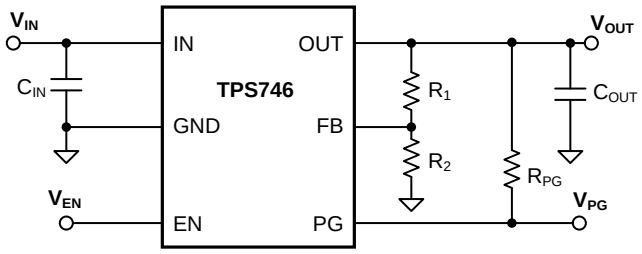


Figure 1. Adjustable Operation

Use Equation 2 to calculate R_1 and R_2 for any output voltage range.

$$R_1 = R_2 (V_{OUT} / V_{FB} – 1) \quad (2)$$

where

- V_{FB} = 0.55 V

8.1.2 Input and Output Capacitor Selection

The TPS746 requires an output capacitance of 1 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application be sure to look at the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 200 µF.

To ensure stability, place a 1-µF capacitor on the input pin of the LDO as well. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.3 Dropout Voltage

The TPS746 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

ADVANCE INFORMATION

Application Information (continued)

8.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. Equation 3 shows that P_D is equal to the product of the output current and voltage drop across the output pass element.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (3)$$

Figure 2 depicts the maximum ambient temperature versus the power dissipation of the TPS746 in the DRV package. Figure 2 assumes the device is soldered on a JEDEC standard high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to make sure the TPS746 does not operate continuously above a junction temperature of 125°C.

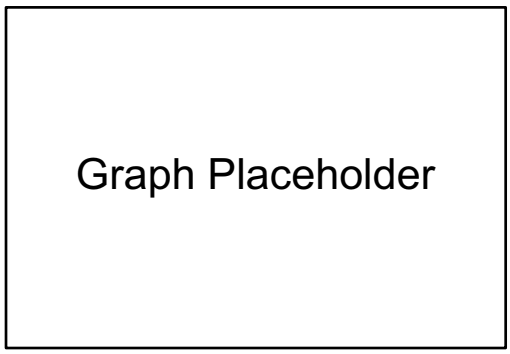


Figure 2. Maximum Ambient Temperature vs Device Power Dissipation

8.1.5 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage ($PG_{(LTH)}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $PG_{(LTH)}$ threshold by an amount greater than $PG_{(HTH)}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.

When using a feedforward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output is pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

ADVANCE INFORMATION

8.2 Typical Application

Figure 3 shows the typical application circuit for the TPS746. Input and output capacitances must be at least 1 µF.

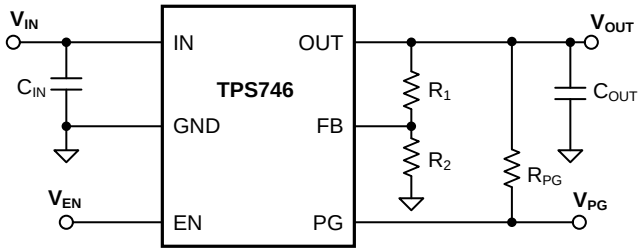


Figure 3. TPS746 Typical Application

8.2.1 Design Requirements

Use the parameters listed in Table 2 for typical linear regulator applications.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.5 V to 6 V
Output voltage	1.0 V, ±1%
Input current	0.55 V to 5.5 V
Output load	1-A dc
Maximum ambient temperature	70°C

8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 1 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

Figure 1 illustrates the output voltage of the TPS746. Set the output voltage using the resistor divider; see the *Adjustable Output* section for details.

ADVANCE INFORMATION

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TPS746.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

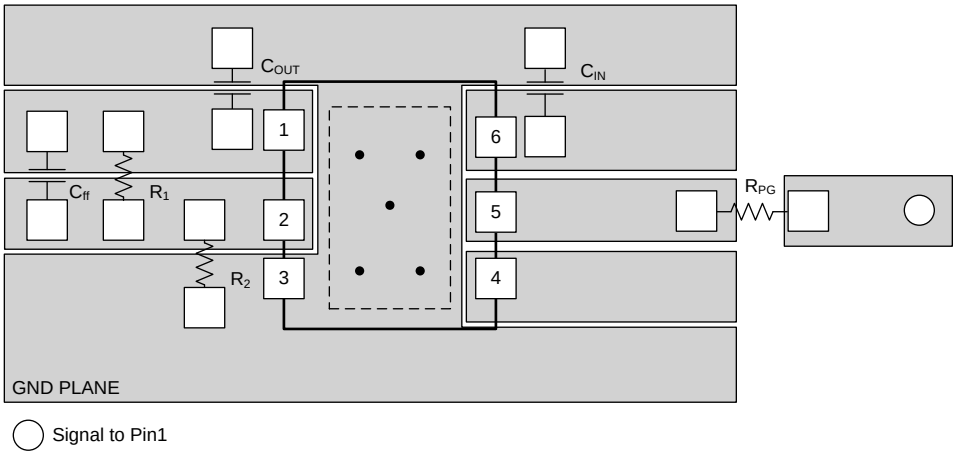


Figure 4. Layout Example for the DRV Package

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS74601PDRVR	ACTIVE	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS74601PBDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MFH	
TPS74601PBDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MFH	
TPS74601PDRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MDH	
TPS74601PDRVT	PREVIEW	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MDH	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

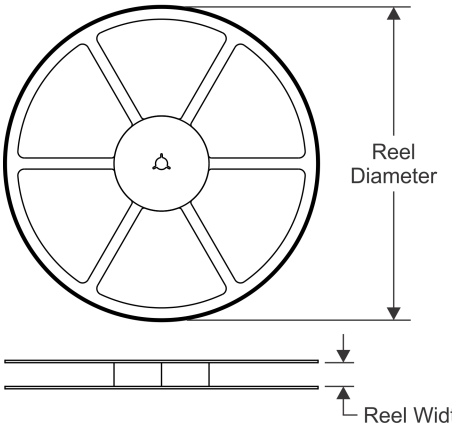
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

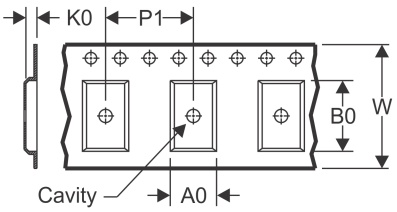
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

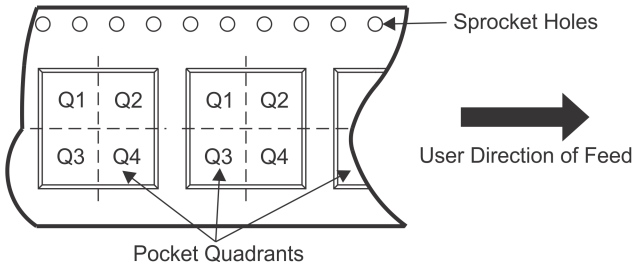


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

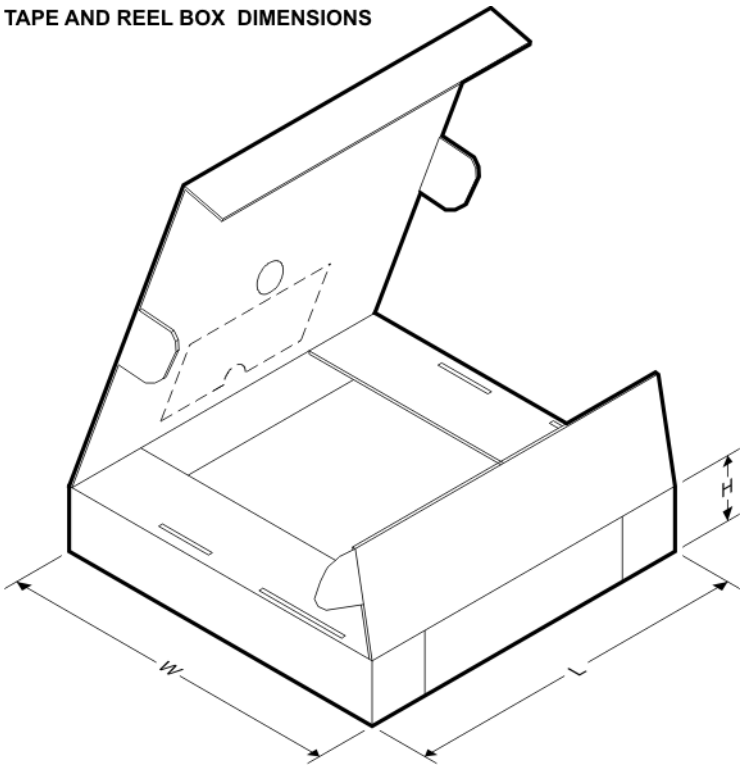
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74601PBDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS74601PBDRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS74601PBDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS74601PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS74601PDRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS74601PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

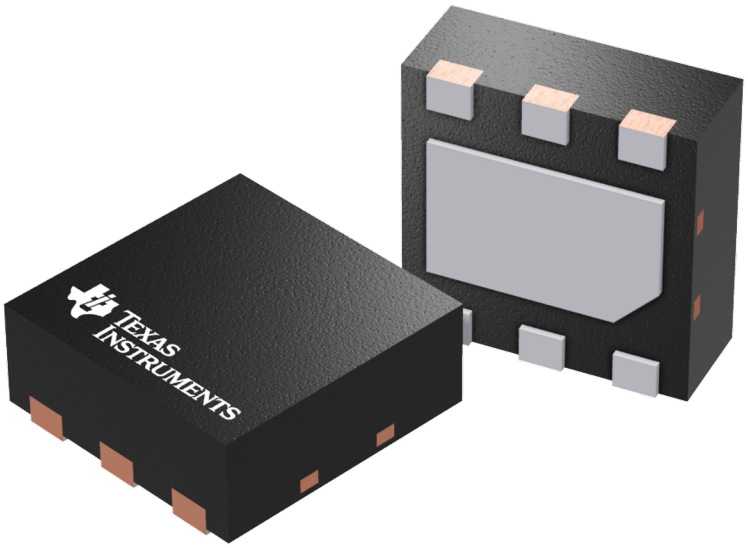


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74601PBDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS74601PBDRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS74601PBDRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS74601PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS74601PDRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS74601PDRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



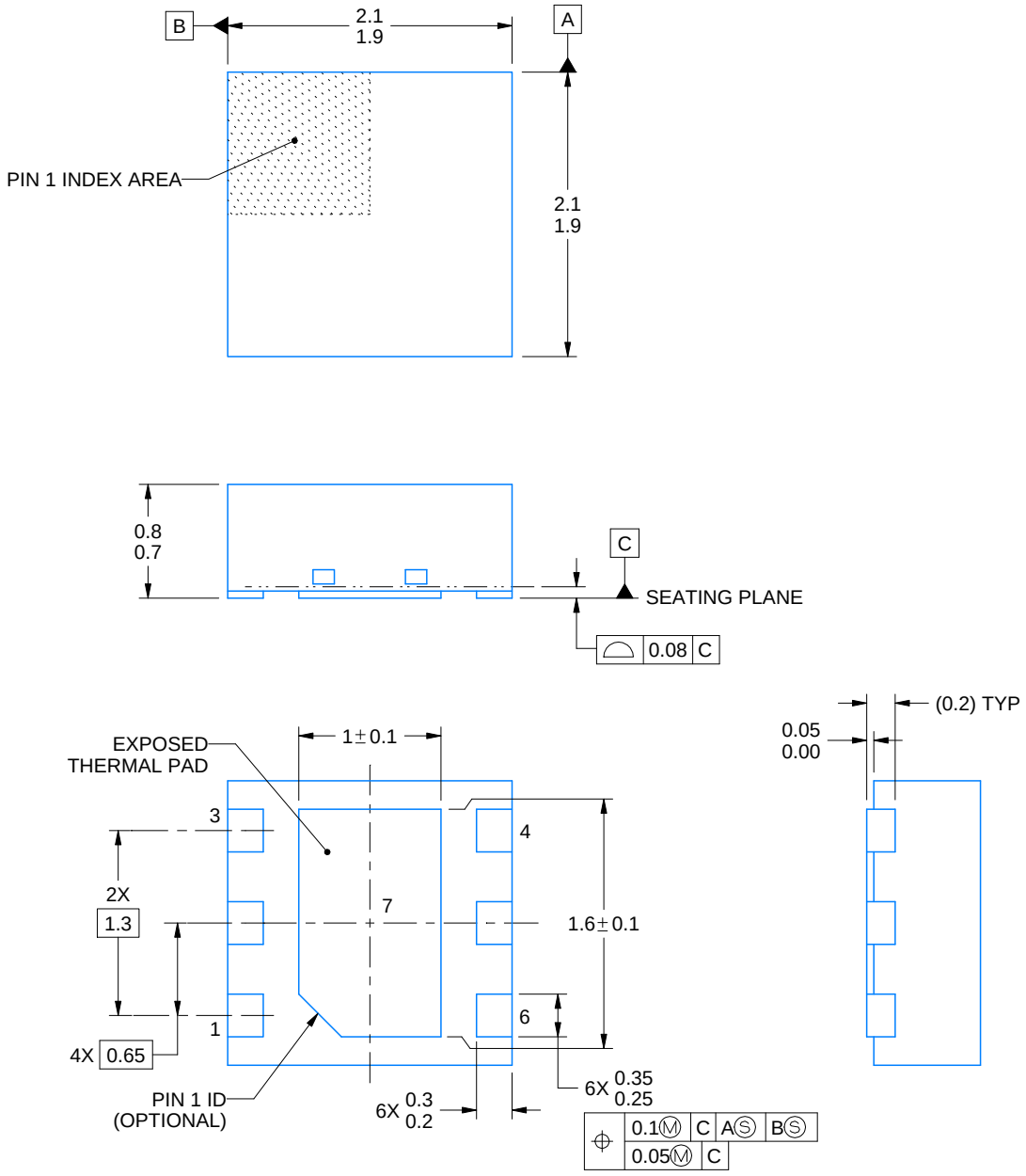
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

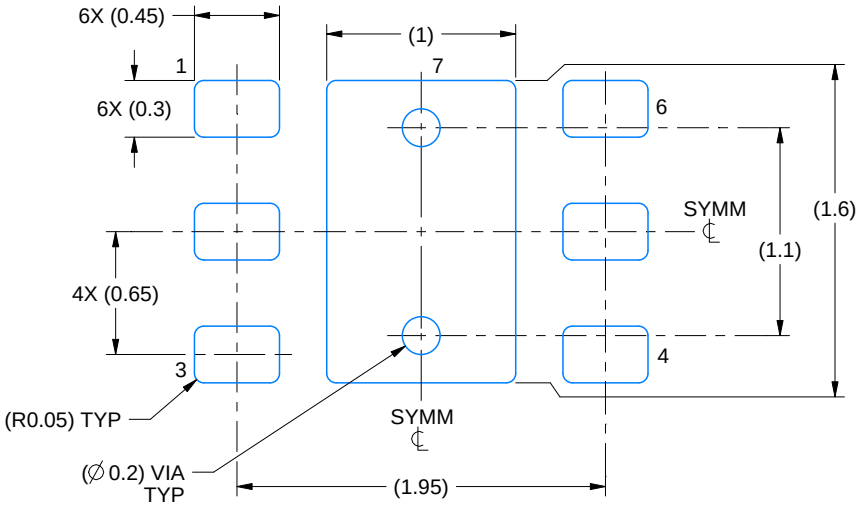
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

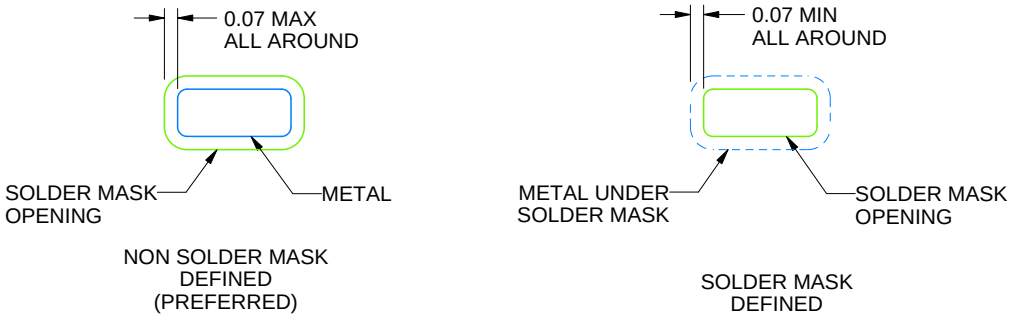


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

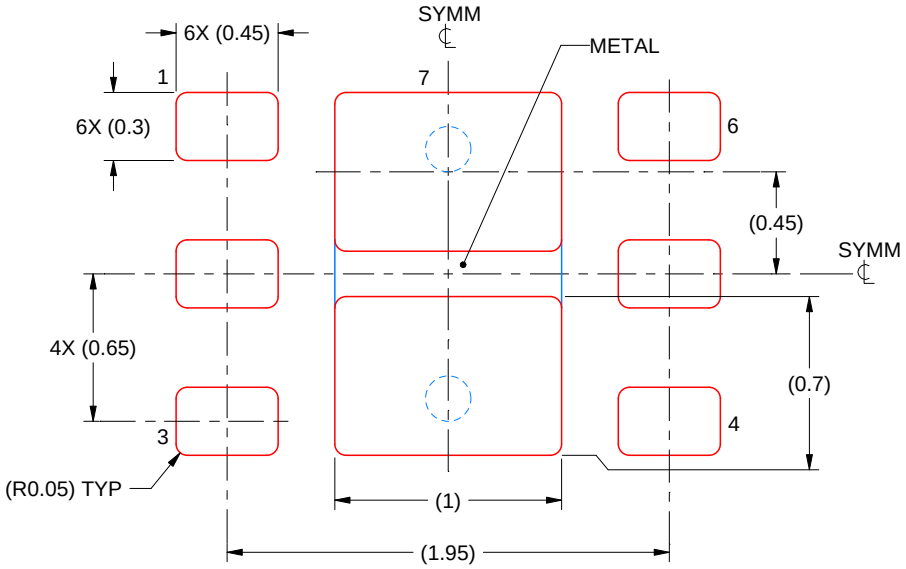
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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