TPS732xx Capacitor-Free, NMOS, 250-mA Low-Dropout Regulator With Reverse Current Protection

1 Features

- Stable with No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range: 1.7 V to 5.5 V
- Ultralow Dropout Voltage: 40 mV Typical at 250 mA
- Excellent Load Transient Response—With or Without Optional Output Capacitor
- NMOS Topology Provides Low Reverse Leakage Current
- Low Noise: 30 μV_{RMS} Typical (10 kHz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy (Line, Load, and Temperature)
- Less Than 1-µA Maximum I_Q in Shutdown Mode
- Thermal Shutdown and Specified Min and Max Current Limit Protection
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.2 V to 5 V
  - Adjustable Outputs from 1.2 V to 5.5 V
  - Custom Outputs Available

2 Applications

- Portable and Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry such as VCOs
- Point-of-Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

3 Description

The TPS732 family of low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

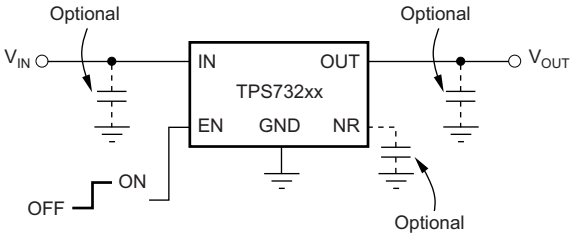
The TPS732 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS732xx	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT-223 (6)	6.50 mm × 3.50 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit for Fixed-Voltage Versions



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (August 2010) to Revision P — **Page**

- Changed *Features* bullet about NMOS topology; deleted "new" ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed first paragraph of *Description* section; deleted description of NMOS topology as "new" ... 1
- Changed Pin Configuration and Functions section; updated table format ... 3
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Changed *Thermal Information* table; updated thermal resistance values for all packages ... 5

Changes from Revision N (August, 2009) to Revision O — **Page**

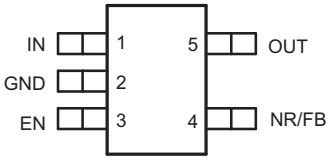
- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 6

Changes from Revision M (May, 2008) to Revision N — **Page**

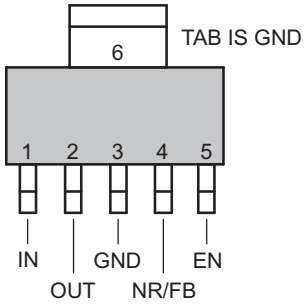
- Changed Figure 10 ... 7
- Added paragraph about recommended start-up sequence to *Internal Current Limit* section ... 14
- Added paragraph about current foldback and device start-up to *Enable Pin and Shutdown* section ... 14

5 Pin Configuration and Functions

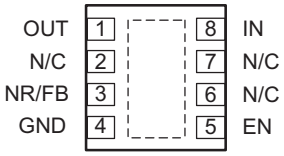
DBV Package
5-Pin SOT-23
Top View



DCQ Package
6-Pin SOT-223
Top View



DRB Package
8-Pin SON With Exposed Thermal Pad
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	SOT-23	SOT-223	SON		
IN	1	1	8	I	Input supply
GND	2	3, 6	4, Pad	—	Ground
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Feature Description* for more details. EN can be connected to IN if not used.
NR	4	4	3	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	4	3	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	6	
	V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Peak output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation		See *Power Dissipation*		
Temperature	Junction range ,T_J	–55	150	°C
	Storage range, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.7		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS732[3]			UNIT
		DRB [SON]	DCQ [SOT223]	DBV [SOT23]	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
  ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.
  iii. DBV: There is no exposed pad with the DBV package.
  (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* section of this data sheet.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73201)		T_J = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage range (TPS73201)(2)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)(3)	Nominal	T_J = 25°C	–0.5%		0.5%	
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 250 mA	–1%	±0.5%	1%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		1 mA ≤ I_{OUT} ≤ 250 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 250 mA		0.0005		%/mA
V_{DO}	Dropout voltage(4) (V_{IN} = V_{OUT} (nom) – 0.1 V)		I_{OUT} = 250 mA		40	150	mV
$Z_{O(do)}$	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	425	600	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		300		mA
I_{REV}	Reverse leakage current(5) ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 250 mA		650	950	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5, –40°C ≤ T_J ≤ 100°C		0.02	1	µA
I_{FB}	FB pin current (TPS73201)				0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 250 mA		58		dB
			f = 10 kHz, I_{OUT} = 250 mA		37		
V_n	Output noise voltage BW = 10Hz – 100kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	EN pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown Temp increasing		160		°C
			Reset Temp decreasing		140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) TPS73201 is tested at V_{OUT} = 2.5 V.
(3) Tolerance of external resistors not included in this specification.
(4) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 1.8 V because minimum V_{IN} = 1.7 V.
(5) Fixed-voltage versions only; refer to *Application Information* section for more information.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs

6.7 Typical Characteristics

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

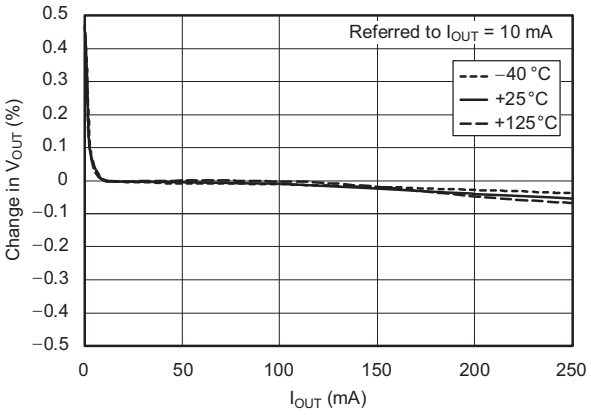


Figure 1. Load Regulation

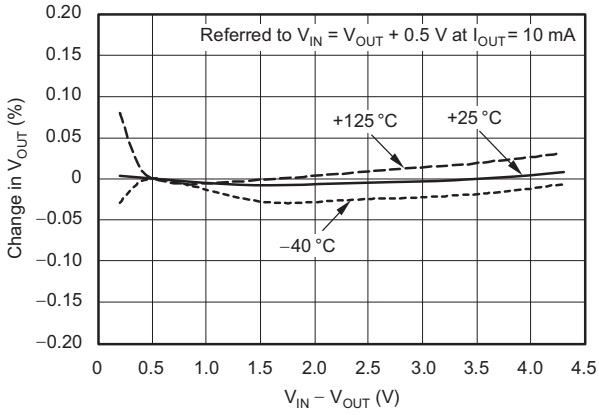


Figure 2. Line Regulation

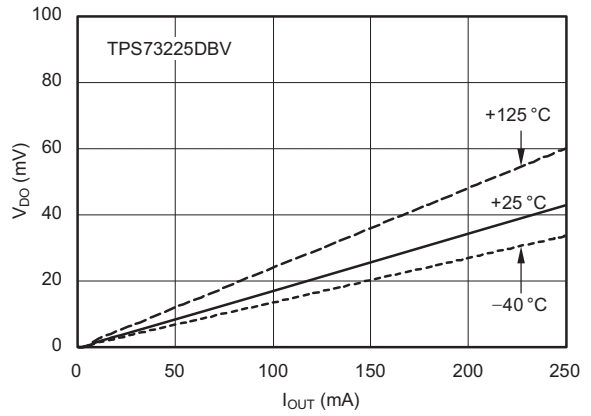


Figure 3. Dropout Voltage vs Output Current

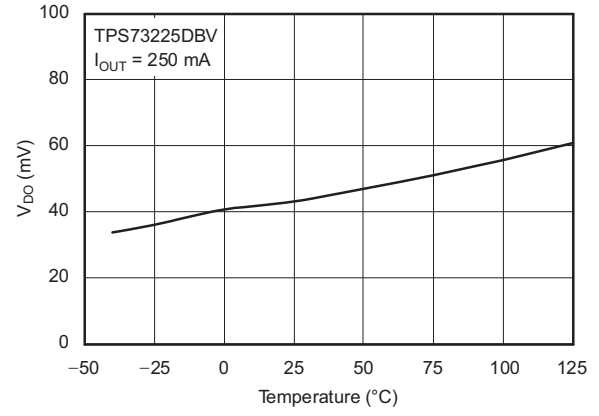


Figure 4. Dropout Voltage vs Temperature

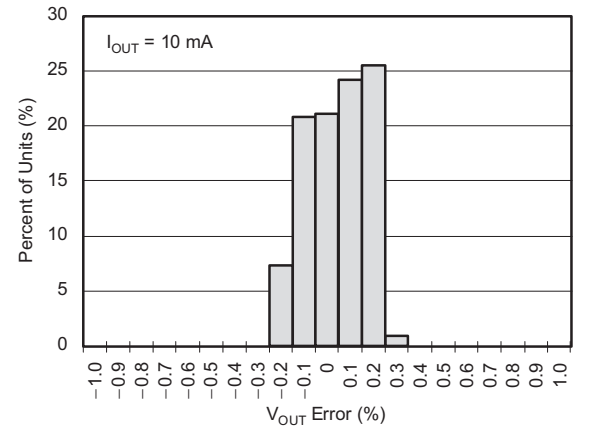


Figure 5. Output Voltage Accuracy Histogram

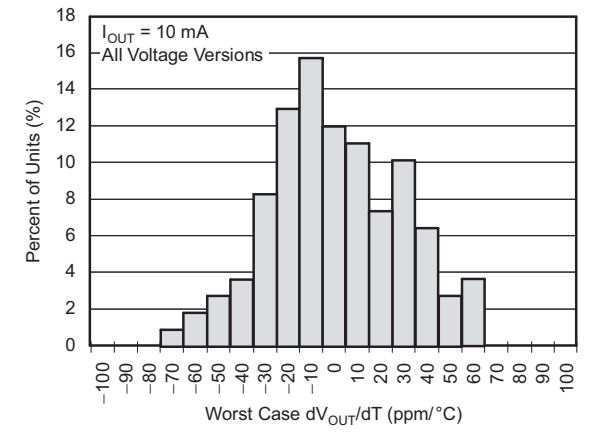


Figure 6. Output Voltage Drift Histogram

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

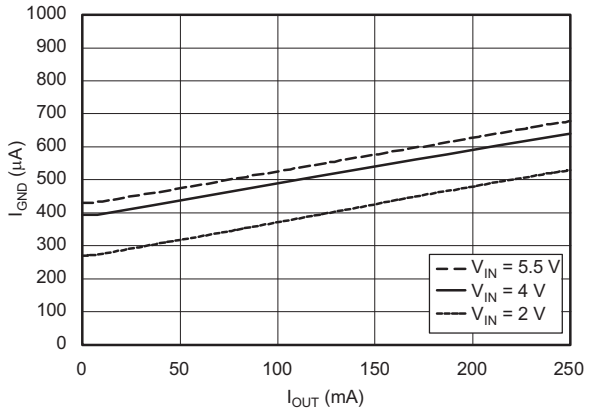


Figure 7. Ground Pin Current vs Output Current

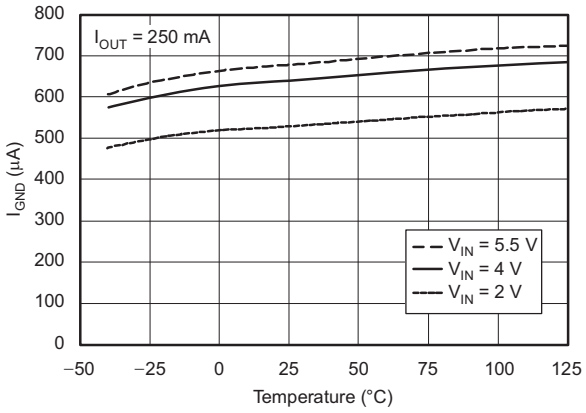


Figure 8. Ground Pin Current vs Temperature

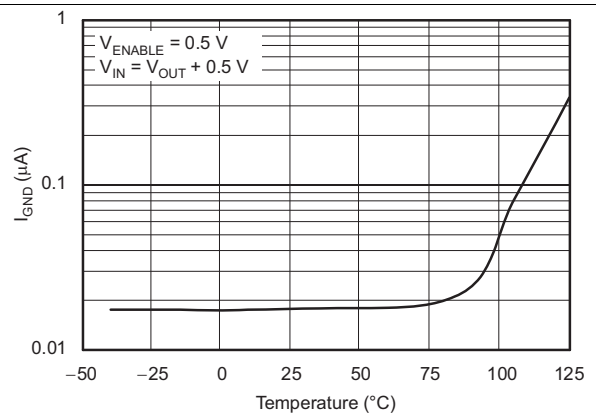


Figure 9. Ground Pin Current in Shutdown vs Temperature

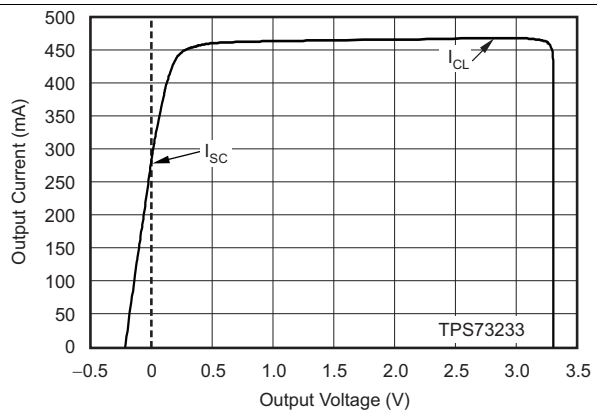


Figure 10. Current Limit vs V_{OUT} (Foldback)

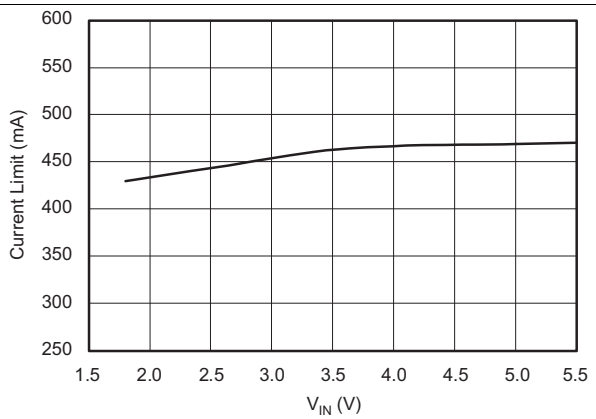


Figure 11. Current Limit vs V_{IN}

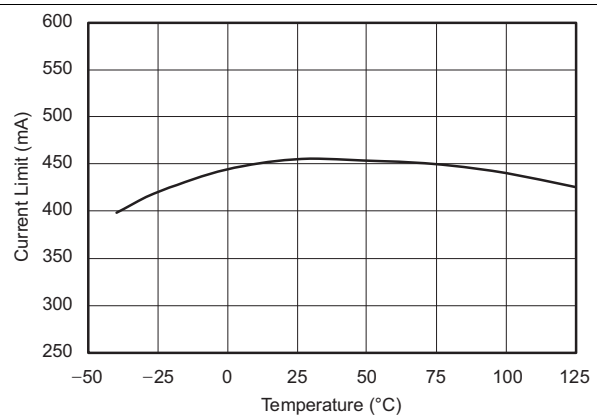


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

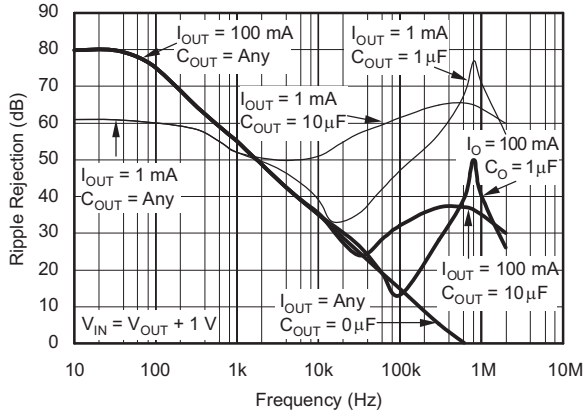


Figure 13. PSRR (Ripple Rejection) vs Frequency

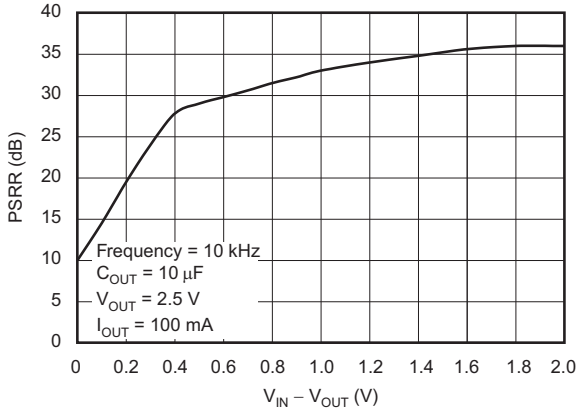


Figure 14. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})

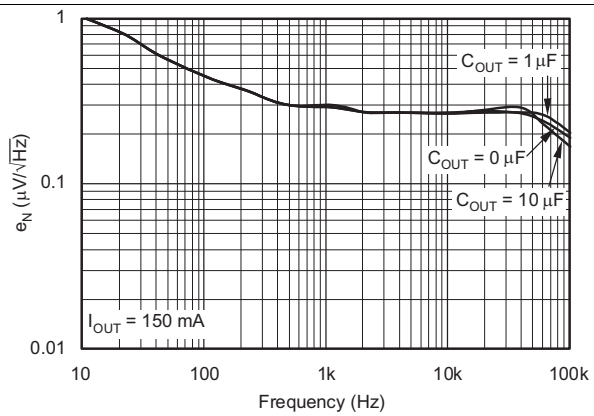


Figure 15. Noise Spectral Density C_{NR} = 0 µF

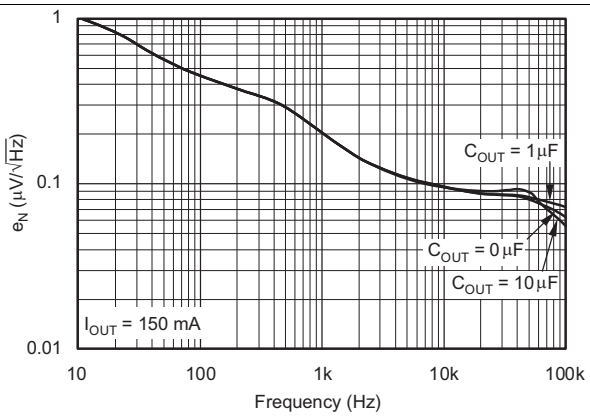


Figure 16. Noise Spectral Density C_{NR} = 0.01 µF

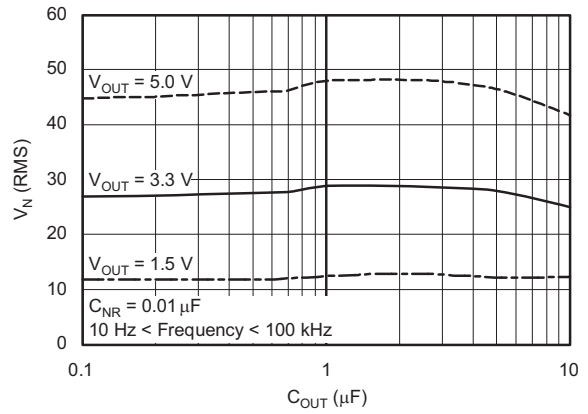


Figure 17. RMS Noise Voltage vs C_{OUT}

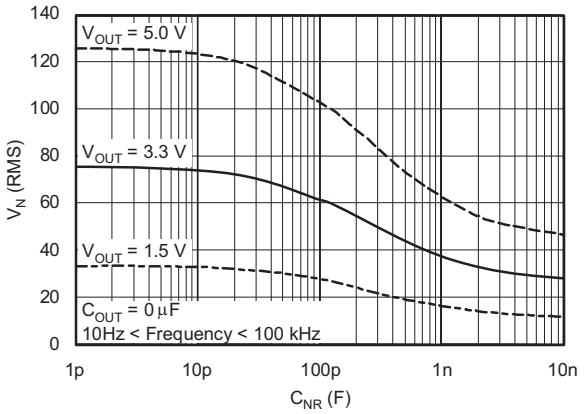


Figure 18. RMS Noise Voltage vs C_{NR}

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

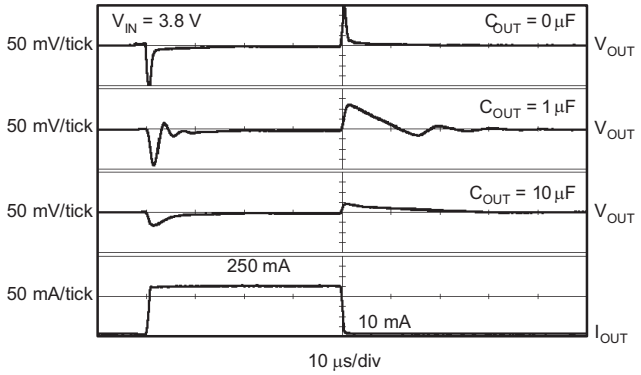


Figure 19. TPS73233 Load Transient Response

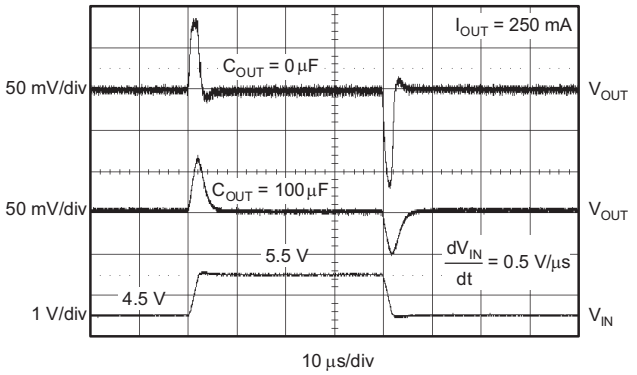


Figure 20. TPS73233 Line Transient Response

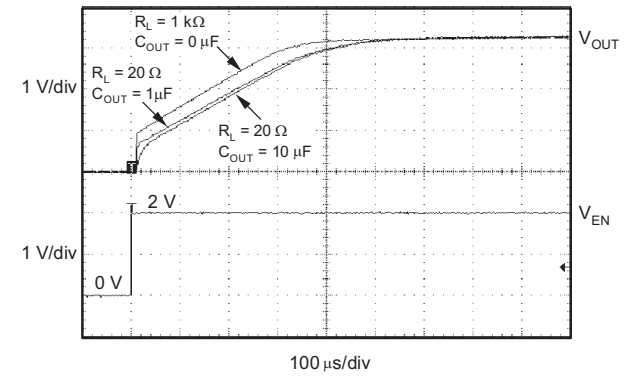


Figure 21. TPS73233 Turnon Response

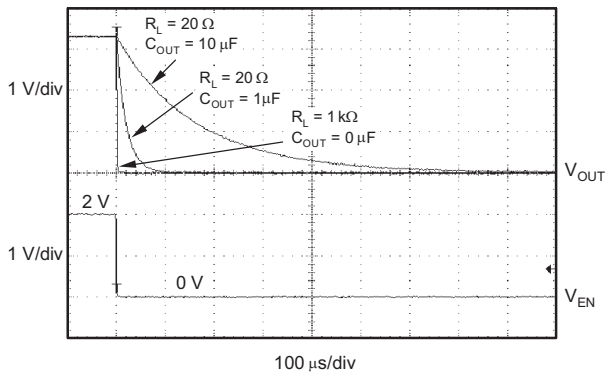


Figure 22. TPS73233 Turnoff Response

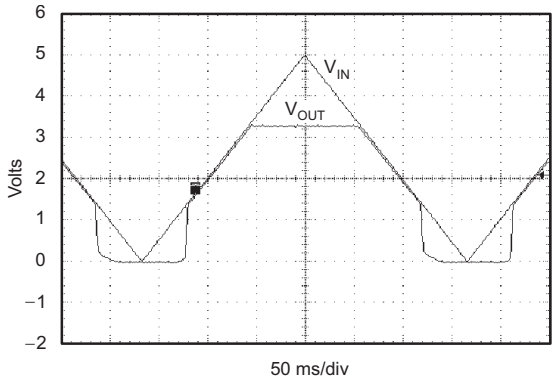


Figure 23. TPS73233 Power Up and Power Down

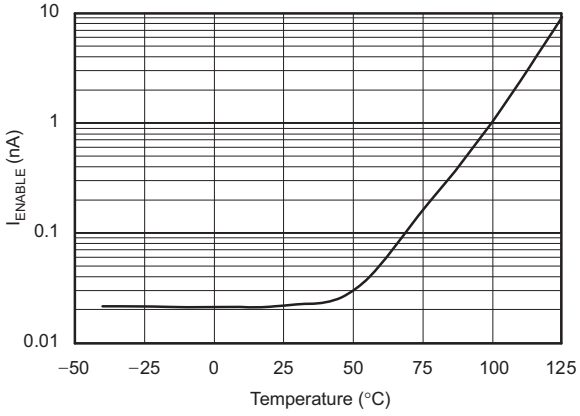


Figure 24. I_{ENABLE} vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

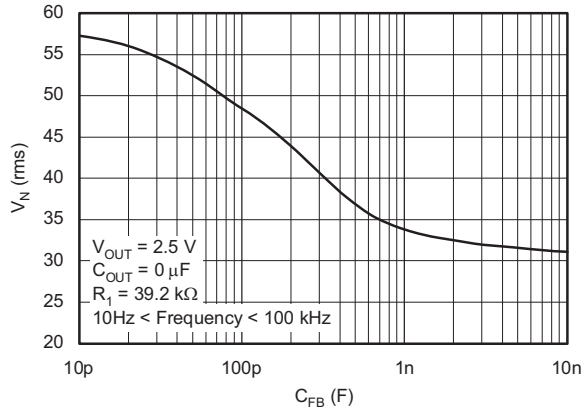


Figure 25. TPS73201 RMS Noise Voltage vs C_{FB}

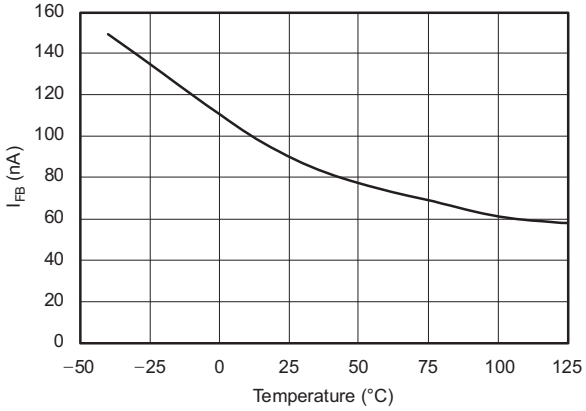


Figure 26. TPS73201 I_{FB} vs Temperature

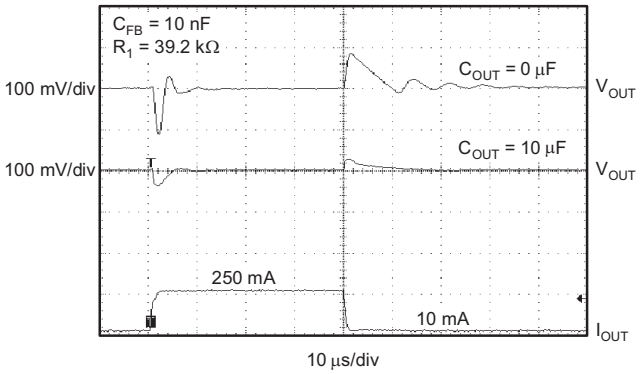


Figure 27. TPS73201 Load Transient, Adjustable Version

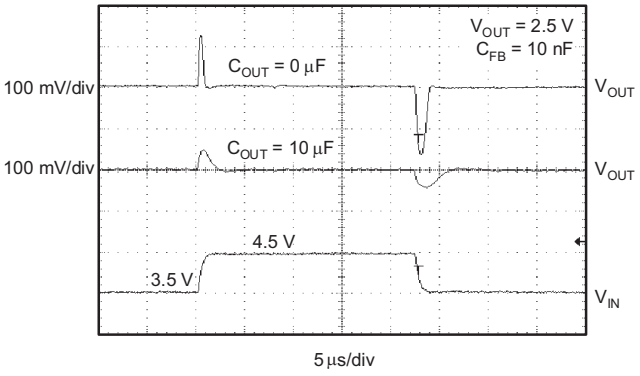


Figure 28. TPS73201 Line Transient, Adjustable Version

7 Detailed Description

7.1 Overview

The TPS732 family of low-dropout linear regulators operates down to an input voltage of 1.7 V and supports output voltages down to 1.2 V while sourcing up to 500 mA of load current. This linear regulator uses an NMOS pass element with an integrated 4-MHz charge pump to provide a dropout voltage of less than 250 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS732 family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown.

The TPS732 family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01 µF connected from the NR pin to GND, the TPS73215 output noise can be as low as 12.75 μV_{RMS}. The low noise output featured by the TPS732 family makes the device well-suited for powering VCOs or any other noise-sensitive load.

7.2 Functional Block Diagrams

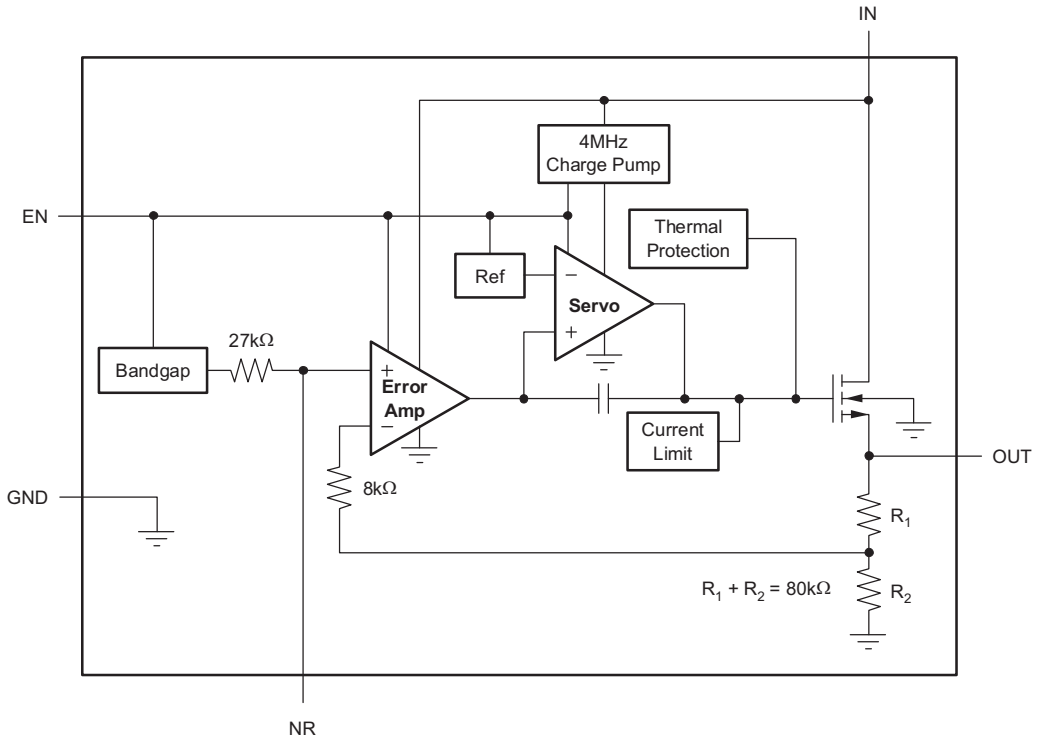


Figure 29. Fixed-Voltage Version

Functional Block Diagrams (continued)

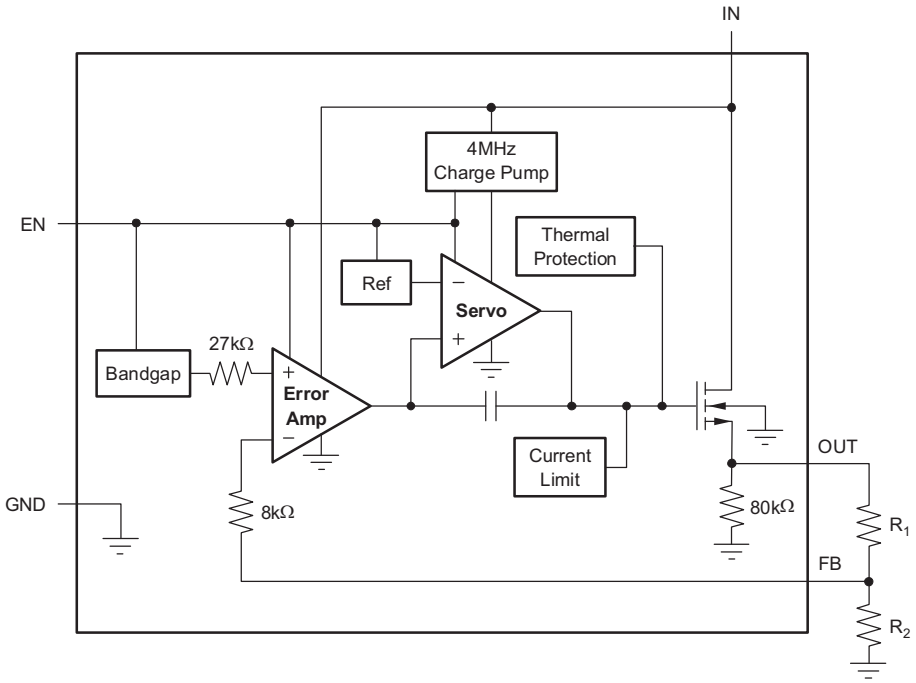


Figure 30. Adjustable-Voltage Version

Table 1. Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

7.3 Feature Description

7.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732 and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \left(\frac{R_1 + R2}{R_2} \right) = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (2)$$

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10 nF.

Feature Description (continued)

This noise reduction effect is shown as *RMS Noise Voltage vs* C_{NR} (Figure 18) in the *Typical Characteristics* section.

The TPS73201 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improve load transient performance.

The TPS732 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250 µV of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.3.2 Internal Current Limit

The TPS732 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 10 in the *Typical Characteristics* section for a graph of I_{OUT} vs V_{OUT}.

Note from Figure 10 that approximately –0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS732 should be enabled first.

7.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shut down the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 21).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section.

7.3.4 Dropout Voltage

The TPS732 uses an NMOS pass transistor to achieve extremely low dropout. When ($V_{IN} – V_{OUT}$) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass element.

For large step changes in load current, the TPS732 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of ($V_{IN} – V_{OUT}$) above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with ($V_{IN} – V_{OUT}$) close to DC dropout levels], the TPS732 can take a couple of hundred microseconds to return to the specified regulation accuracy.

Feature Description (continued)

7.3.5 Reverse Current

The NMOS pass element of the TPS732 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. Additional current will flow into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS73201, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

7.4 Device Functional Modes

7.4.1 Normal Operation With 1.7 V ≤ V_{IN} ≤ 5.5 V and V_{EN} ≥ 1.7 V

The TPS732 family requires an input voltage of at least 1.7 V to function properly and attempt to maintain regulation.

When operating the device near 5.5 V, take care to suppress any transient spikes that may exceed the 6-V absolute maximum voltage rating. The device should never operate at a DC voltage greater than 5.5 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS732 device belongs to a family of LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732 ideal for portable applications. This regulator family offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

8.2 Typical Applications

Figure 31 shows the basic circuit connections for the fixed-voltage models. Figure 32 gives the connections for the adjustable-voltage version (TPS73201).

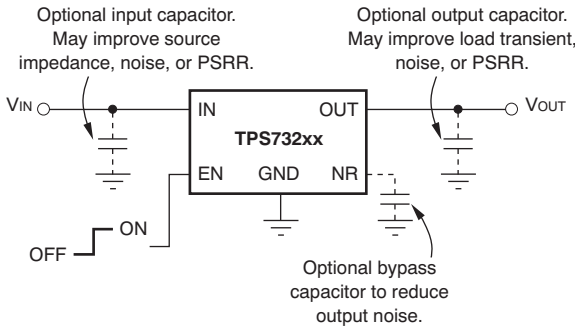


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

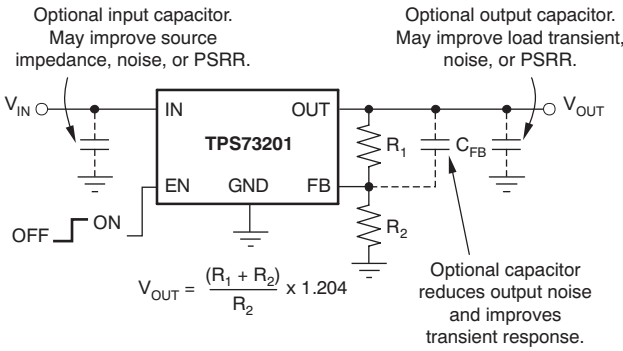


Figure 32. Typical Application Circuit for Adjustable-Voltage Version

Typical Applications (continued)

8.2.1 Design Requirements

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732 does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

8.2.2.2 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 µF) from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves the transient response.

The TPS732 does not have active pulldown when the output is overvoltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage versions)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

Typical Applications (continued)

8.2.3 Application Curves

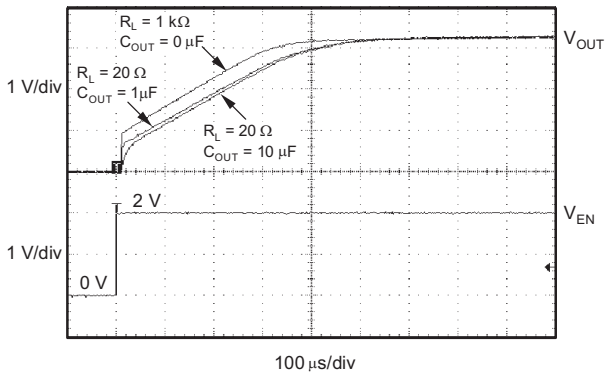


Figure 33. TPS73233 Turnon Response

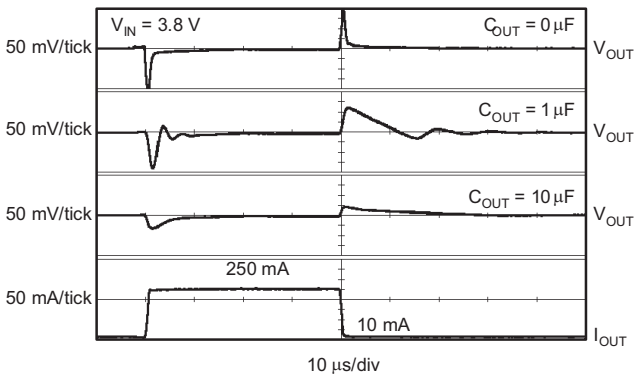


Figure 34. TPS73233 Load Transient Response

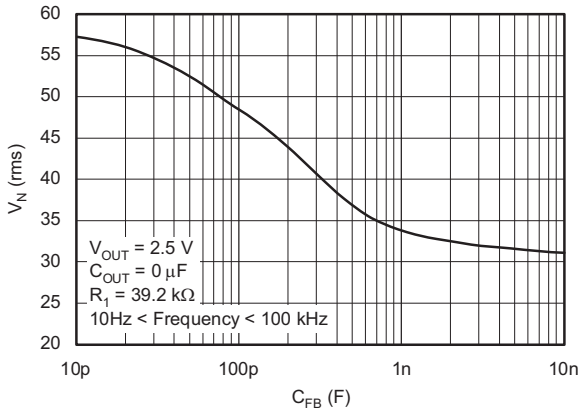


Figure 35. TPS73201 RMS Noise Voltage vs C_{FB}

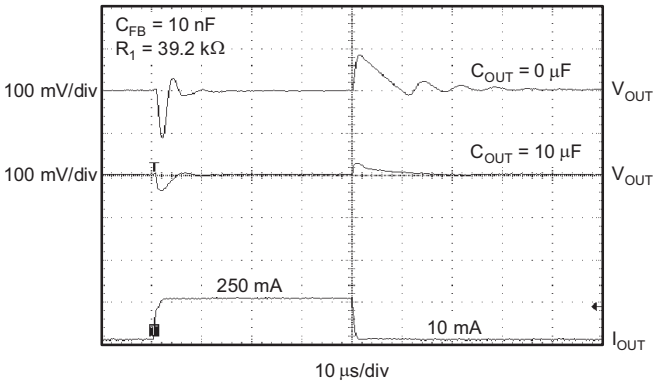


Figure 36. TPS73201 Load Transient, Adjustable Version

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.7 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the PCB with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Solder pad footprint recommendations for the TPS732 are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the TI website at www.ti.com.

10.2 Layout Examples

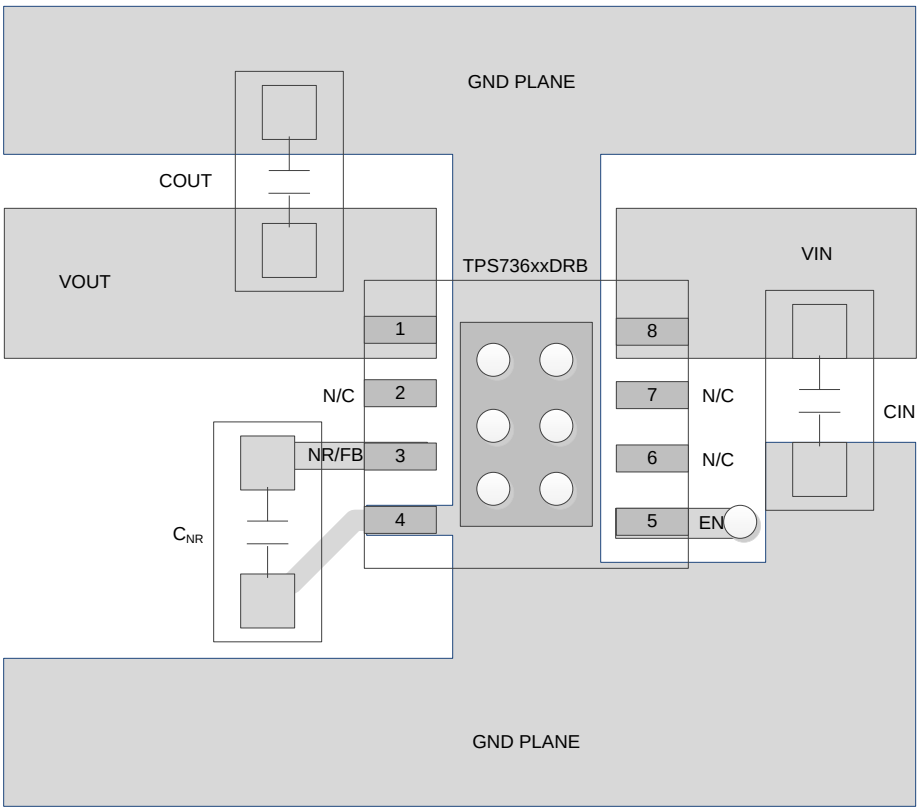


Figure 37. Fixed Output Voltage Option Layout (DRB Package)

Layout Examples (continued)

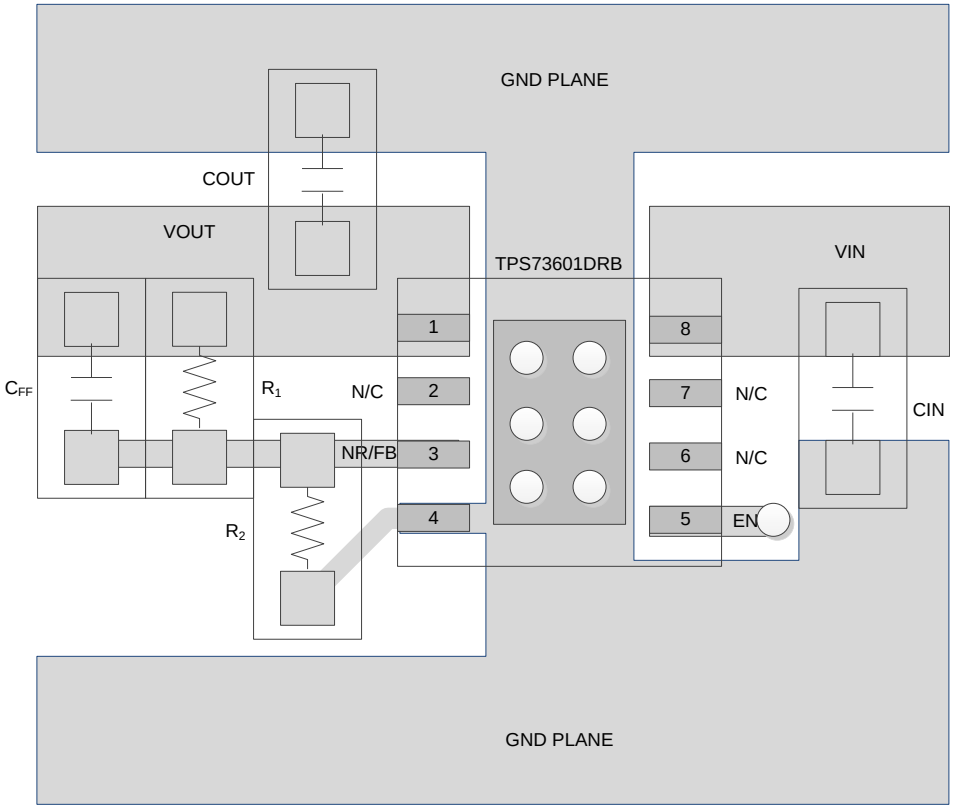


Figure 38. Adjustable Output Voltage Option Layout (DRB Package)

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732 into thermal shutdown will degrade device reliability.

Thermal Considerations (continued)

10.3.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS732. The TPS73201DRBEVM-518 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS732 is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS732**xx** ***yyy z***	**XX** is the nominal output voltage (for example, 25 = 2.5 V; 01 = Adjustable). **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- *Regulating V_{OUT} Below 1.2 V Using an External Reference*, SLVA216
- *Solder Pad Recommendations for Surface-Mount Devices*, SBFA019
- *TPS73x01DRBEVM-518 User's Guide*, SBVU014

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS73201	Click here	Click here	Click here	Click here	Click here
TPS73213	Click here	Click here	Click here	Click here	Click here
TPS73215	Click here	Click here	Click here	Click here	Click here
TPS73216	Click here	Click here	Click here	Click here	Click here
TPS73218	Click here	Click here	Click here	Click here	Click here
TPS73219	Click here	Click here	Click here	Click here	Click here
TPS73225	Click here	Click here	Click here	Click here	Click here
TPS73230	Click here	Click here	Click here	Click here	Click here
TPS73233	Click here	Click here	Click here	Click here	Click here
TPS73250	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73201DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73201	Samples
TPS73201DCQG4	ACTIVE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS73201DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS73201	Samples
TPS73201DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73213DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD	Samples
TPS73213DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD	Samples
TPS73215DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DBVTG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73215DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215	Samples
TPS73215DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215	Samples
TPS73216DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73216DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73216DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73218DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73218	Samples
TPS73218DCQG4	ACTIVE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS73218DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS73218	Samples
TPS73219DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGE	Samples
TPS73219DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGE	Samples
TPS73225DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73225DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73225DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73225DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73230DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73230	Samples
TPS73233DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73233	Samples
TPS73233DCQG4	ACTIVE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS73233DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS73233	Samples
TPS73250DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73250DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples
TPS73250DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples
TPS73250DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

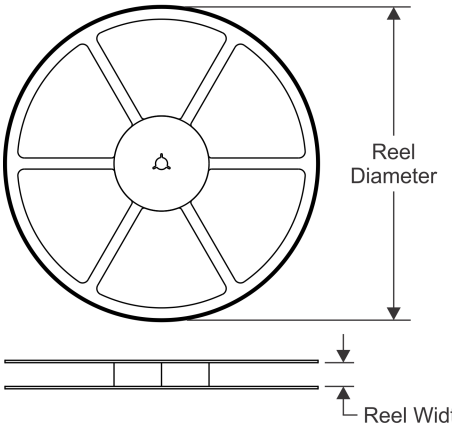
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

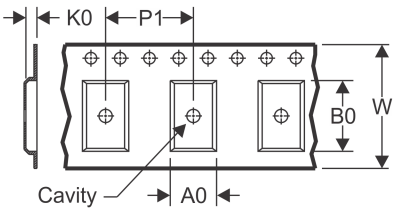
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

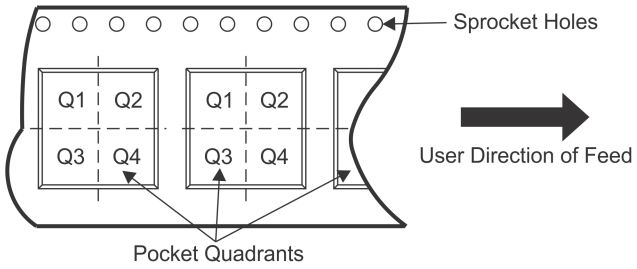


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

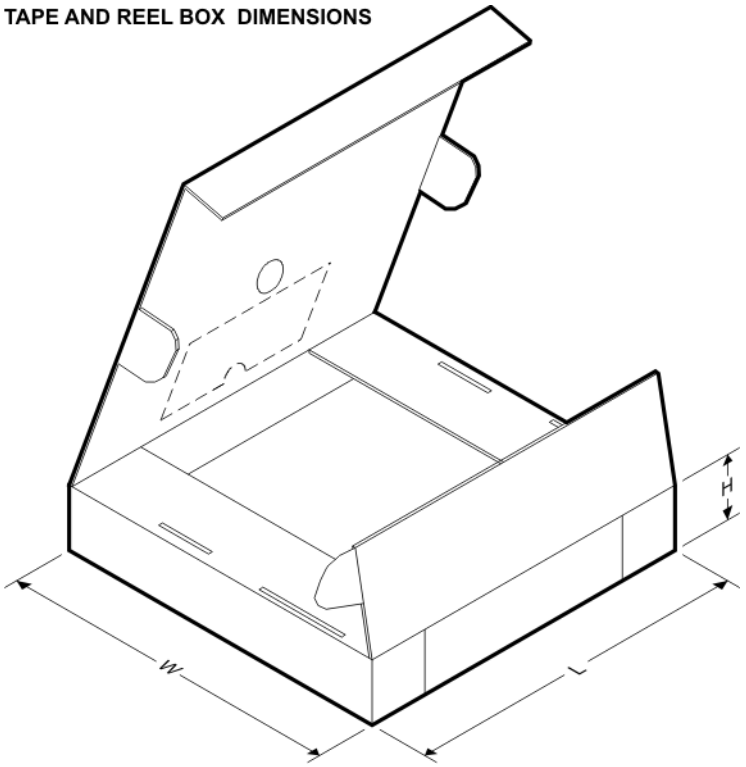


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73201DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73201DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73201DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73213DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73213DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73216DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73216DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73218DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73219DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73219DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73230DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73230DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73230DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73233DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

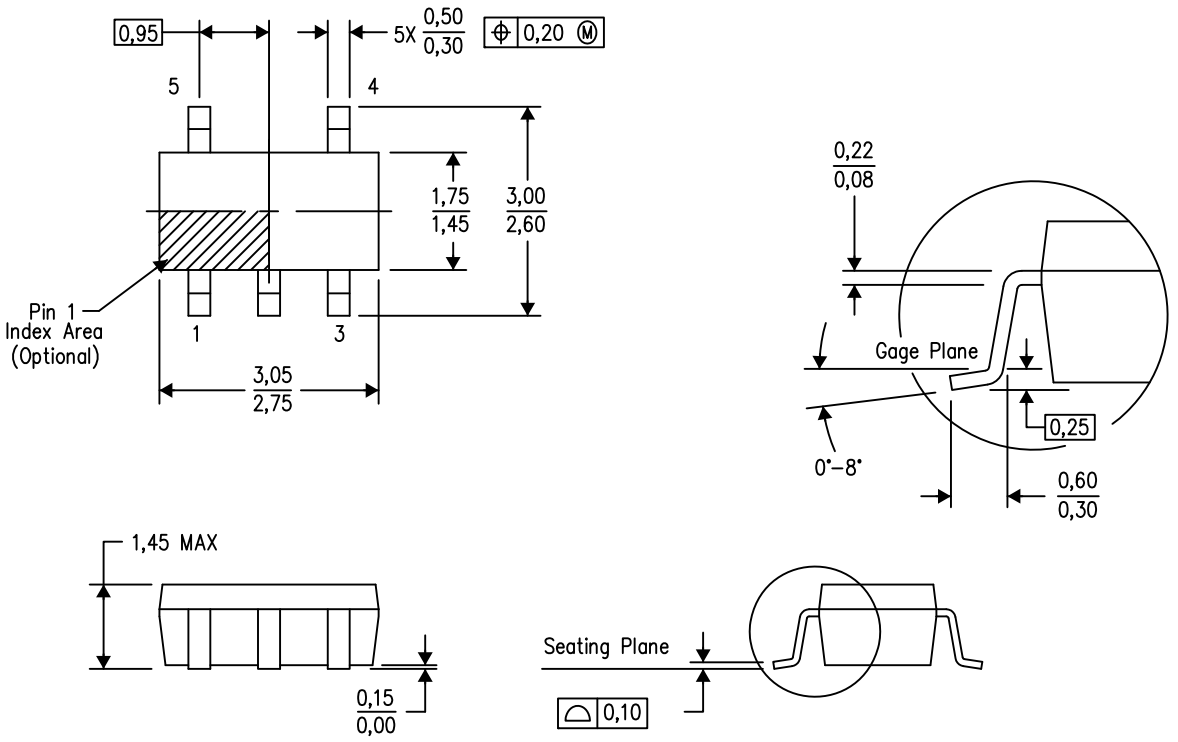


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73201DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73201DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS73201DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73201DRBR	SON	DRB	8	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS73201DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73201DRBT	SON	DRB	8	250	220.0	205.0	50.0
TPS73213DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73213DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73215DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73215DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TPS73216DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS73216DBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
TPS73218DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73218DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73219DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73219DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73225DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TPS73230DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73230DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73230DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TPS73233DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73233DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73250DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73250DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73250DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0

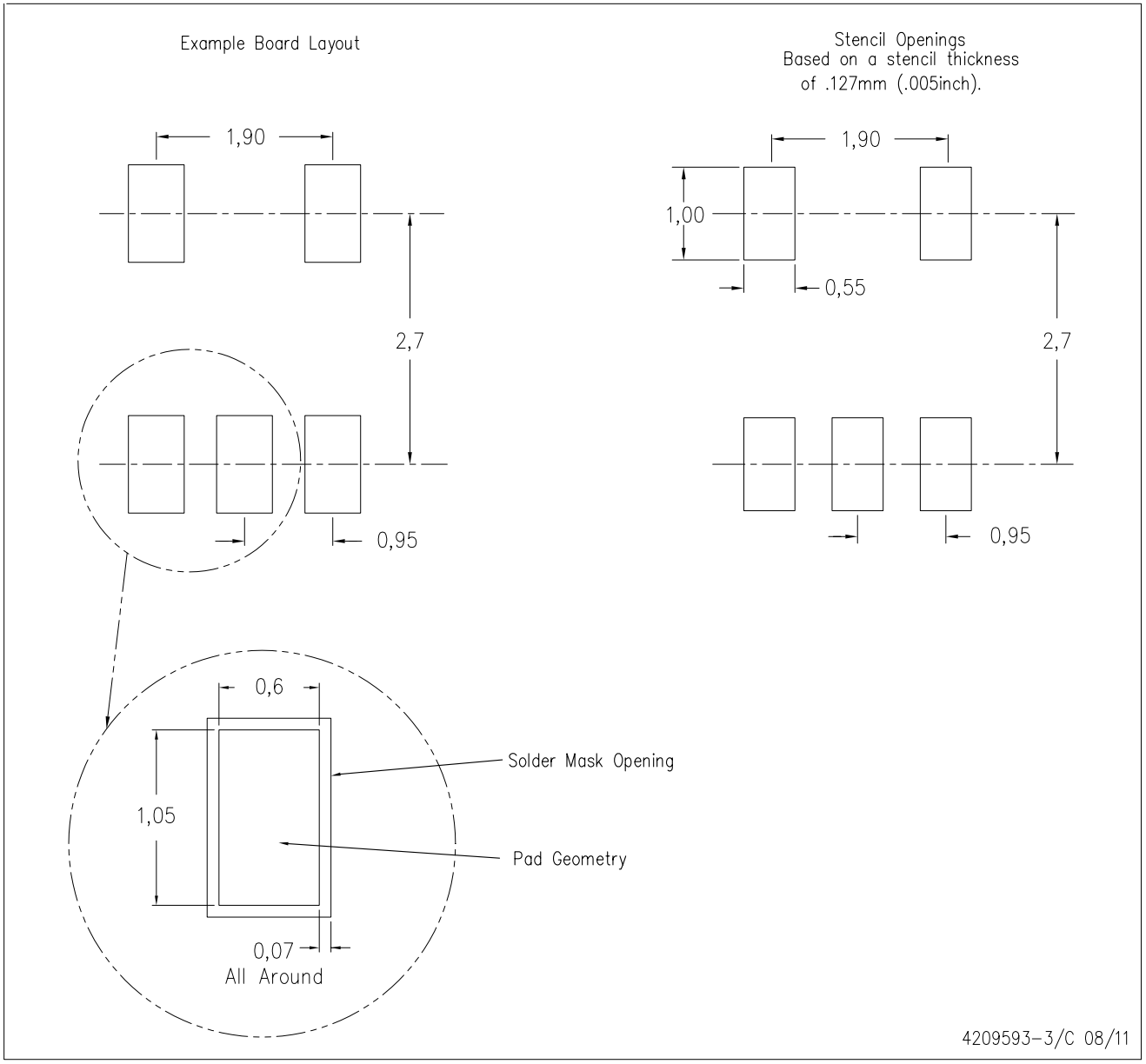
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

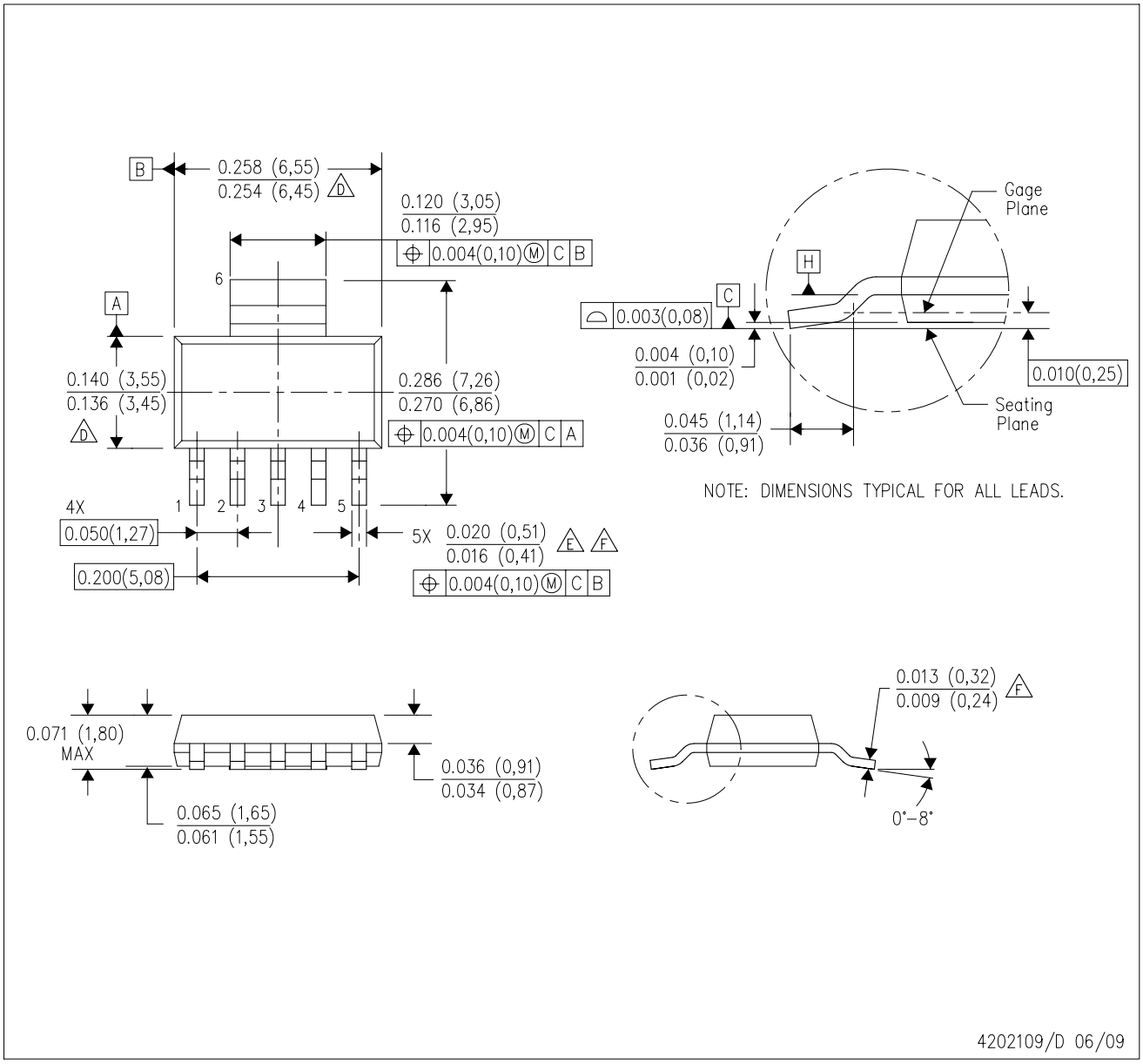
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



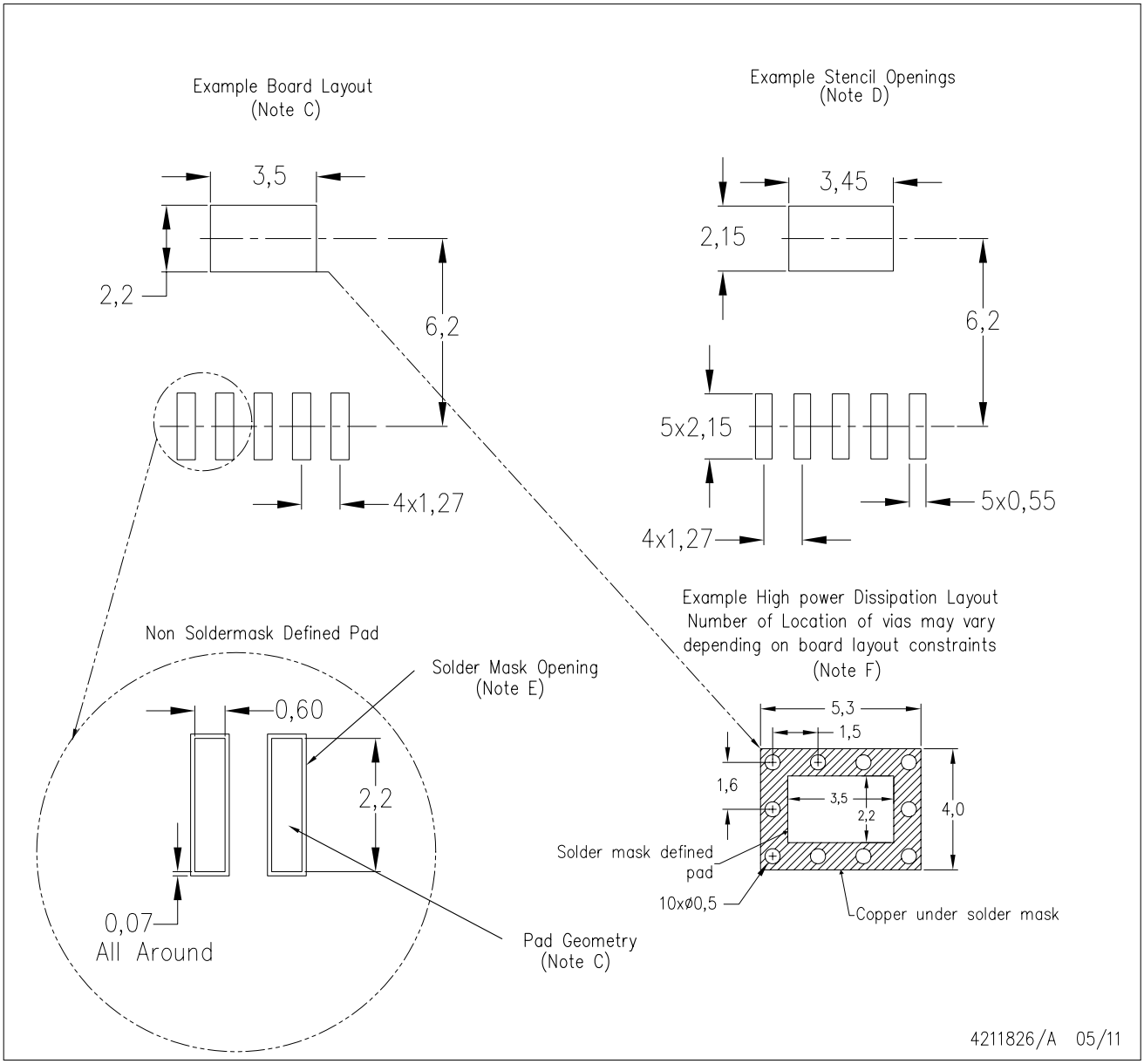
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



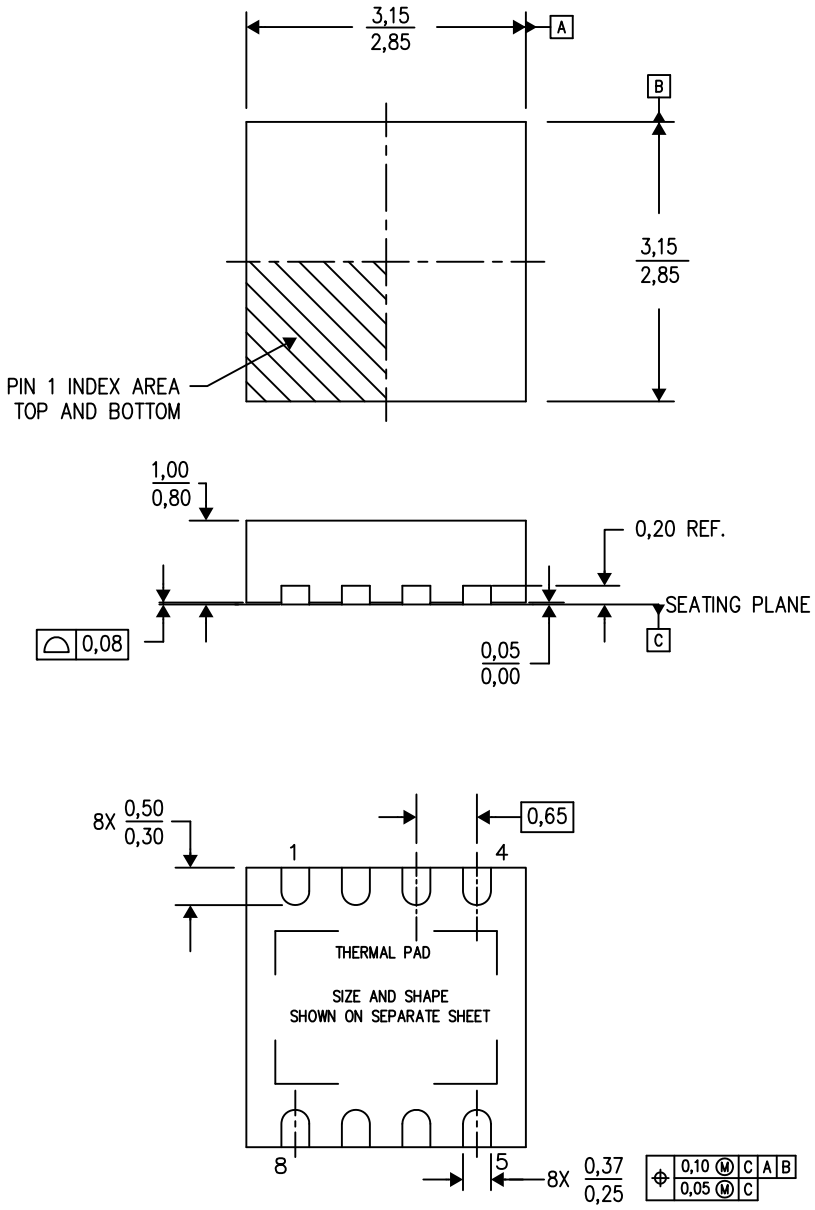
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

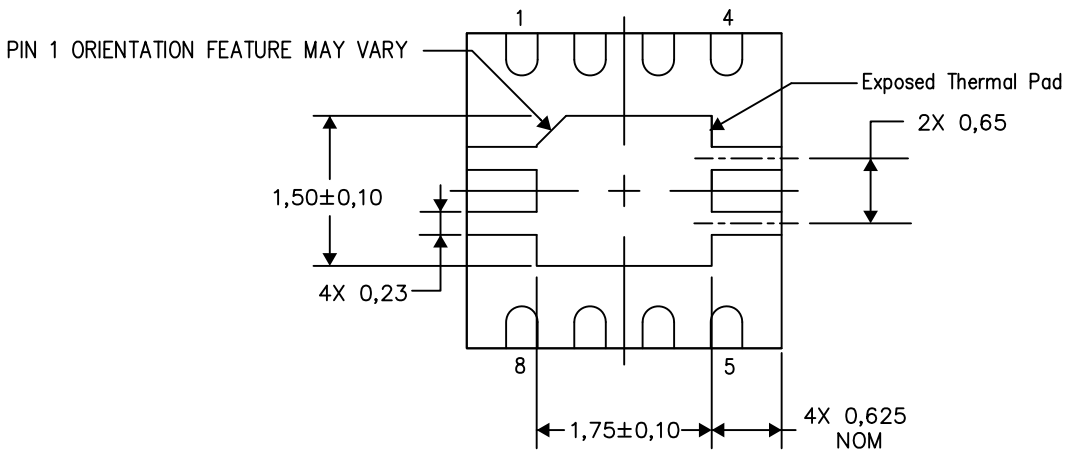
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



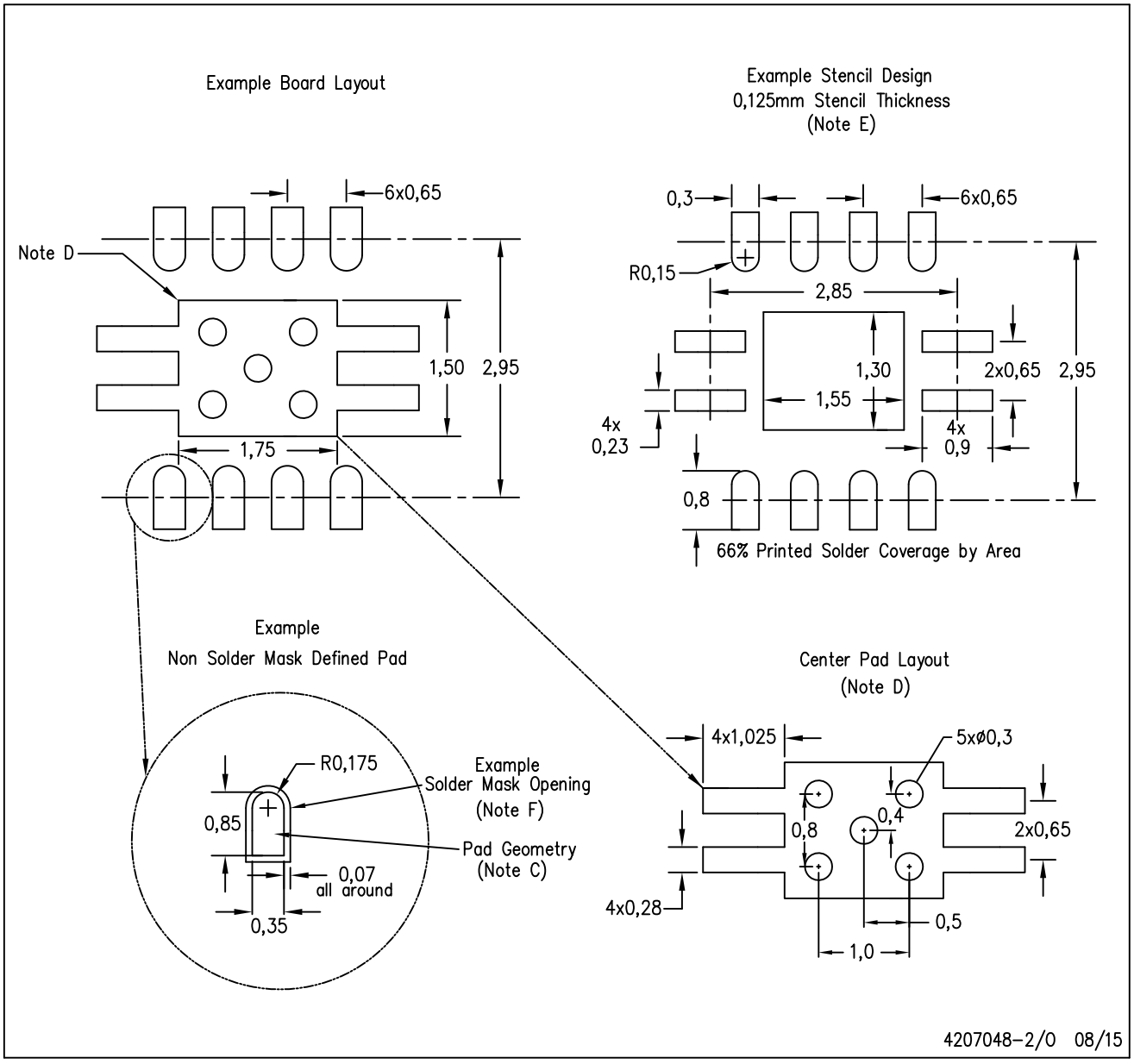
Bottom View

Exposed Thermal Pad Dimensions

4206340–2/T 08/15

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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