# TPS717-Q1
# Low-Noise, High-Bandwidth PSRR, Low-Dropout, 150-mA Linear Regulator

## 1 Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device HBM ESD Classification Level C4B
- Input Voltage: 2.5 V to 6.5 V
- Available in Multiple Output Versions:
  - Fixed Output with Voltages from 0.9 V to 5 V
  - Adjustable Output Voltage from 0.9 V to 6.2 V
- Ultra-High PSRR:
  - 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent Load and Line Transient Response
- Very Low Dropout: 170 mV typical at 150 mA
- Low Noise: 30 $\mu V_{RMS}$ typical (100 Hz to 100 kHz)
- Small 5-pin SOT, 2-mm × 2-mm WSON-6, and 1.5-mm × 1.5-mm WSON-6 Packages

## 2 Applications

- PLLs
- VCOs
- Camera Sensor Power
- Microcontroller Power
- Wireless LAN, Bluetooth®
- ADAS and Infotainment Systems

## 3 Description

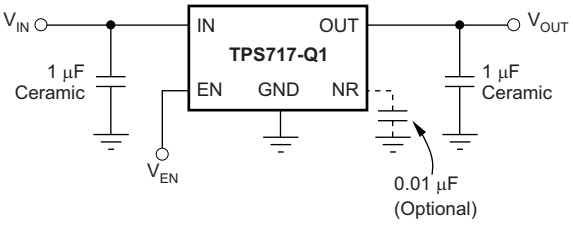
The TPS717-Q1 family of low-dropout (LDO), low-power linear regulators offers very high power-supply rejection (PSRR) and maintains very low 45-µA ground current in an ultra-small, five-pin SOT package. The family uses an advanced BiCMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717-Q1 is stable with a 1-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. The device family is fully specified from $T_J$, $T_A$ = –40°C to 125°C and is offered in a small SOT (SC70-5) package, a 2-mm × 2-mm WSON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm WSON-6 package, which are ideal for small form-factor portable equipment (such as wireless handsets and PDAs). The TPS717-Q1 family of LDOs is qualified for AEC-Q100 grade 1.

**Device Information(1)**

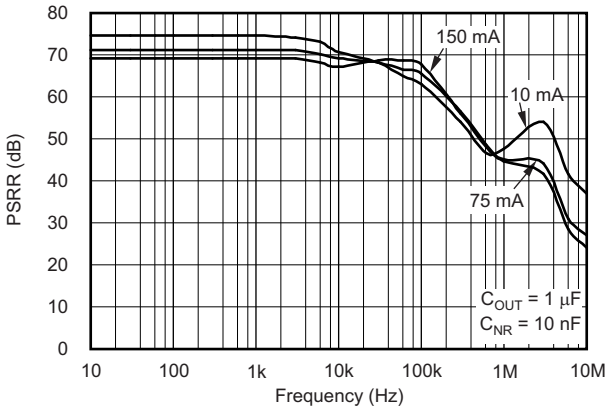
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS717-Q1 | SOT (5) | 2.00 mm × 1.25 mm |
| | WSON (6) | 2.00 mm × 2.00 mm |
| | WSON (6) | 1.50 mm × 1.50 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application Circuit for Fixed-Voltage Versions**




**PSRR vs Frequency**




Power-Supply Rejection Ratio ($V_{IN}$ – $V_{OUT}$ = 1 V)

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (December 2014) to Revision C** **Page**

- Moved AEC-Q100 qualification bullet to first in Features list ..... 1
- Added TI Design ..... 1
- Changed TPS717xx-Q1 to TPS717-Q1 throughout document ..... 1
- Added footnote and $C_{IN}$, $R_2$, and $C_{NR}$ parameters to *Recommended Operating Conditions* table ..... 6
- Changed $V_{FB}$ parameter in *Electrical Characteristics* table ..... 7
- Changed $\Delta V_{OUT(\Delta IOUT)}$ parameter typical specification in *Electrical Characteristics* table ..... 7
- Changed units of $V_n$ parameter in *Electrical Characteristics* table ..... 7
- Deleted UVLO parameter minimum specification from *Electrical Characteristics* table ..... 7
- Changed $T_A$ to $T_J$ in x-axis of Figure 7, Figure 10, and Figure 11 ..... 9
- Changed 40 mV/div to 40 mA/div in y-axis of Figure 28 ..... 12
- Added last two sentences to *Undervoltage Lockout (UVLO)* section ..... 15
- Changed last bulleted condition in *Normal Operation* section ..... 15
- Changed $T_J$ specification in *Normal mode* row of Table 1 ..... 16
- Added last sentence to *Input and Output Capacitor Requirements* section ..... 17
- Clarified discussion of $R_2$ in second paragraph of *Design Considerations* section ..... 19
- Changed first and third paragraphs of *Do's and Don'ts* section ..... 20

**Changes from Revision A (August 2013) to Revision B** **Page**

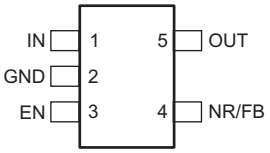
- Changed format to meet latest data sheet standards ..... 1
- Changed Features list on front page: added, deleted, and reordered several bullets ..... 1
- Added *ESD Ratings* table and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections..... 1
- Added several Applications list bullets on front page ..... 1
- Deleted pinout drawings from front page ..... 1
- Changed pin descriptions throughout *Pin Functions* table ..... 4
- Added parametric measurement for $I_{SHDN}$ for DRV package ..... 7
- Changed Figure 1, Figure 2, Figure 3, and Figure 4: removed legend, added call-outs for clarity ..... 8
- Changed title of Figure 15 and Figure 17..... 9
- Changed *Overview* section ..... 13
- Corrected input and output symbols in operational amplifiers in Functional Block Diagrams ..... 13
- Changed *Undervoltage Lockout (UVLO)* section text: reworded for clarity..... 15
- Deleted *Reverse Current Protection* section ..... 17
- Changed Equation 4 ..... 19

**Changes from Original (September 2012) to Revision A** **Page**

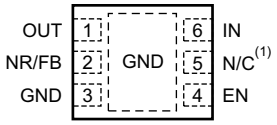
- Changed front page to two-column format. ..... 1
- Added part number TPS71745-Q1. ..... 1
- Changed C3B to C4B in Features list ..... 1
- Removed Ordering Information table ..... 4
- Added Junction Temperature to *Absolute Maximum Ratings* table ..... 5
- Changed C3B to C4B in Absolute Maximum Ratings table. ..... 5
- Changed Application Information section to one-column format. ..... 18

# 5 Pin Configuration and Functions

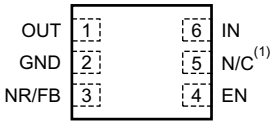
**DCK Package**
**5-Pin SOT**
**Top View**




**DRV Package**
**2-mm × 2-mm, 6-Pin WSON**
**Top View**




**DSE Package**
**1.5-mm × 1.5-mm, 6-Pin WSON**
**Top View**




(1) N/C = No connection

**Pin Functions**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | DCK (SOT) | DRV (WSON) | DSE (WSON) | | |
| EN | 3 | 4 | 4 | I | Driving the enable pin (EN) above $V_{EN(high)}$ turns on the regulator. Driving this pin below $V_{EN(low)}$ puts the regulator into standby mode, thereby disabling the output and reducing operating current. |
| FB | 4 | 2 | 3 | I | Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation. |
| GND | 2 | 3 | 2 | — | Ground |
| IN | 1 | 6 | 6 | I | Input to the device. A 0.1-µF to 1-µF capacitor is recommended for better performance. |
| N/C | — | 5 | 5 | — | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| NR | 4 | 2 | 3 | — | Fixed voltage versions only. An external capacitor connected to this pin bypasses noise generated by the internal band gap, thus lowering output noise. |
| OUT | 5 | 1 | 1 | O | This pin is the regulated output voltage. A minimum capacitance of 1 µF is required for stability from this pin to ground. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted), all voltages are with respect to GND(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 7 | V |
| | $V_{FB}$ | –0.3 | 3.6 | |
| | $V_{NR}$ | –0.3 | 3.6 | |
| | $V_{EN}$ | –0.3 | $V_{IN}$ + 0.3 V(2) | |
| | $V_{OUT}$ | –0.3 | 7 | |
| Current | $I_{OUT}$ | Internally limited | | A |
| Continuous total power dissipation | $P_{DISS}$ | See *Thermal Information* table | | |
| Ambient temperature | $T_A$ | –40 | 125 | °C |
| Operating junction temperature | $T_J$ | –55 | 150 | °C |
| Storage temperature | $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{EN}$ absolute maximum rating is $V_{IN}$ + 0.3 V or 7 V, whichever is greater.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| TPS717-Q1 in DCK and DSE packages | | | | |
| $V_{(ESD)}$ Electrostatic discharge | Charged device model (CDM), per AEC Q100-011 | All pins | ±750 | V |
| | | Corner pins, DCK (1, 3, 4, and 5) | ±750 | |
| | | Corner pins, DSE (1, 3, 4, and 6) | ±750 | |
| TPS717-Q1 in DRV package | | | | |
| $V_{(ESD)}$ Electrostatic discharge | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | V |
| | | Corner pins (1, 3, 4, and 6) | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 6.5 | V |
| $V_{OUT}$ | Output voltage | 0.9 | | 5 | V |
| $I_{OUT}$ | Output current | 0 | | 150 | mA |
| $V_{EN}$ | Enable voltage | 0 | | $V_{IN}$ | V |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $R_2$ | Lower feedback resistor | 160 | 320 | 332 | kΩ |
| $C_{NR}$ | Noise reduction capacitor | | 10 | | nF |
| $C_{OUT}$ | Output capacitor | 1 (1) | | 100 | µF |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

(1) Adjustable voltage version only. When using feedback resistors that are smaller than recommended, the minimum output capacitance must be greater than 5 µF.

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS717-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | DCK (SOT) | DRV (WSON) | DSE (WSON) | |
| | | 5 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 279.2 | 71.1 | 190.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.5 | 96.5 | 94.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 74.1 | 40.5 | 149.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | 2.7 | 6.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 73.1 | 40.9 | 152.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 10.7 | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range(1) | | | | 2.5 | | 6.5 | V |
| $V_{FB}$ | Feedback pin voltage (TPS71701) | | $I_{OUT}$ = 5 mA | | –2% | 0.793 | 2% | V |
| $V_{OUT}$ | Output voltage range | TPS717-Q1 | | | 0.9 | | 5 | V |
| | | TPS71701-Q1 | | | 0.9 | | 6.5 – $V_{DO}$ | |
| $V_{OUT}$ | Output accuracy (nominal) | | $T_A$ = 25°C | | | ±2.5 | | mV |
| | Output accuracy ($V_{OUT}$ < 1 V) | Over $V_{IN}$, $I_{OUT}$, temperature(2) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, 0 mA ≤ $I_{OUT}$ ≤ 150 mA | | –30 | | 30 | |
| | Output accuracy ($V_{OUT}$ ≥ 1 V) | Over $V_{IN}$, $I_{OUT}$, temperature(2) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, 0 mA ≤ $I_{OUT}$ ≤ 150 mA | | –3% | | 3% | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation(1) | | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $I_{OUT}$ = 5 mA | | | 125 | | µV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | | 0 mA ≤ $I_{OUT}$ ≤ 150 mA | | | 70 | | µV/mA |
| $V_{DO}$ | Dropout voltage(3) ($V_{IN}$ = $V_{OUT(nom)}$ – 0.1 V) | | $I_{OUT}$ = 150 mA | | | 170 | 300 | mV |
| $I_{LIM}$ (fixed) | Output current limit (fixed output) | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | | 200 | 325 | 575 | mA |
| $I_{LIM}$ (adjustable) | Output current limit (TPS71701-Q1) | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | | 200 | 325 | 575 | mA |
| $I_{GND}$ | Ground pin current | | $I_{OUT}$ = 0.1 mA | | | 45 | 80 | µA |
| | | | $I_{OUT}$ = 150 mA | | | 100 | | |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | | $V_{EN}$ ≤ 0.4 V, 2.5 V ≤ $V_{IN}$ < 4.5 V, $T_A$ = –40°C to 125°C | | | 0.20 | 1.5 | µA |
| | | | $V_{EN}$ ≤ 0.4 V, 4.5 V ≤ $V_{IN}$ ≤ 6.5 V, $T_A$ = –40°C to 125°C | | | 0.90 | | |
| | | | $V_{EN}$ ≤ 0.4 V, 2.5 V ≤ $V_{IN}$ < 4.5 V, $T_A$ = –40°C to 125°C, DRV package | | | | 2 | |
| $I_{FB}$ | Feedback pin current (TPS71701-Q1) | | | | | 0.02 | 1 | µA |
| PSRR | Power-supply rejection ratio | | $V_{IN}$ = 3.8 V, $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 150 mA | f = 100 Hz | | 70 | | dB |
| | | | | f = 1 kHz | | 70 | | |
| | | | | f = 10 kHz | | 67 | | |
| | | | | f = 100 kHz | | 67 | | |
| | | | | f = 1 MHz | | 45 | | |
| $V_n$ | Output noise voltage | | BW = 100 Hz to 100 kHz, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 10 mA | $C_{NR}$ = none | | 95 × $V_{OUT}$ | | $\mu V_{RMS}/V$ |
| | | | | $C_{NR}$ = 0.001 µF | | 25 × $V_{OUT}$ | | |
| | | | | $C_{NR}$ = 0.01 µF | | 12.5 × $V_{OUT}$ | | |
| | | | | $C_{NR}$ = 0.1 µF | | 11.5 × $V_{OUT}$ | | |
| $t_{STR}$ | Startup time | | $V_{OUT}$ = 90% $V_{OUT(nom)}$, $R_L$ = 19 Ω, $C_{OUT}$ = 1 µF | 0.9 V ≤ $V_{OUT}$ ≤ 1.6 V, $C_{NR}$ = 0.001 µF | | 0.700 | | ms |
| | | | | 1.6 V < $V_{OUT}$ < $V_{OUT(max)}$, $C_{NR}$ = 0.01 µF | | 0.160 | | |
| $V_{EN(high)}$ | Enable high (enabled) | | $V_{IN}$ ≤ 5.5 V | | 1.2 | | 6.5(4) | V |
| | | | 5.5 V < $V_{IN}$ ≤ 6.5 V | | 1.25 | | 6.5 | |
| $V_{EN(low)}$ | Enable low (shutdown) | | | | 0 | | 0.4 | V |
| $I_{EN(high)}$ | Enable pin current, enabled | | EN = 6.5 V | | | 0.02 | 1 | µA |
| $T_{sd}$ | Thermal shutdown temperature | | Shutdown, temperature increasing | | | 160 | | °C |
| | | | Reset, temperature decreasing | | | 140 | | |
| UVLO | Undervoltage lockout | | $V_{IN}$ rising | | | 2.45 | 2.49 | V |
| | Hysteresis | | $V_{IN}$ falling | | | 150 | | mV |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 2.5 V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) $V_{DO}$ is not measured for devices with $V_{OUT(nom)}$ < 2.6 V because minimum $V_{IN}$ = 2.5 V.
(4) Maximum $V_{EN(high)}$ = $V_{IN}$ + 0.3 or 6.5 V, whichever is smaller.

## 6.6 Typical Characteristics

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

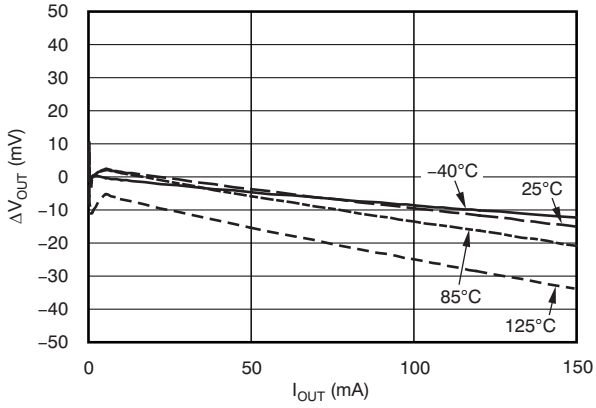



**Figure 1. Load Regulation**

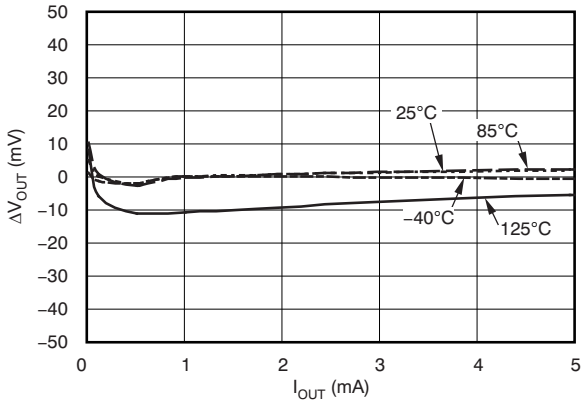



**Figure 2. Load Regulation Under Light Loads**

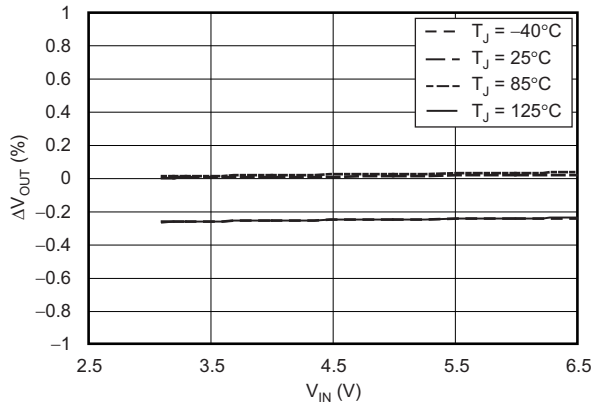



**Figure 3. Line Regulation ($I_{OUT}$ = 5 mA)**

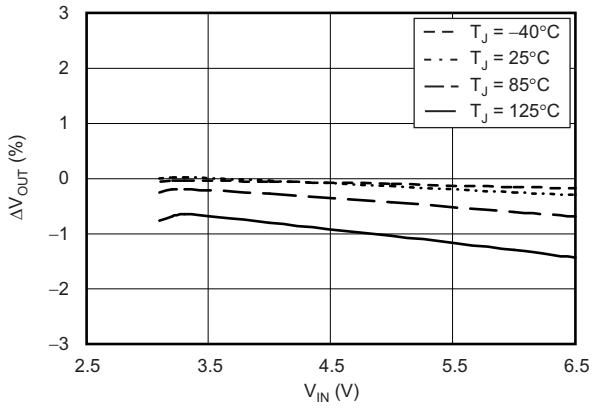



**Figure 4. Line Regulation ($I_{OUT}$ = 150 mA)**

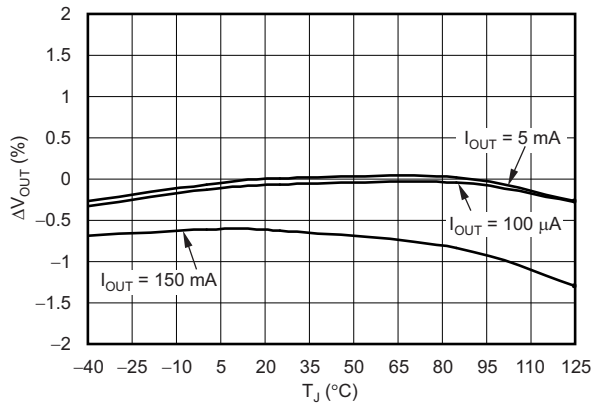



**Figure 5. Output Voltage vs Temperature**

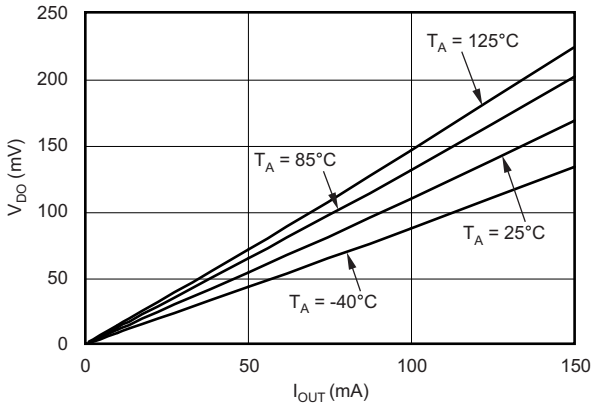



**Figure 6. Dropout Voltage vs Output Current**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

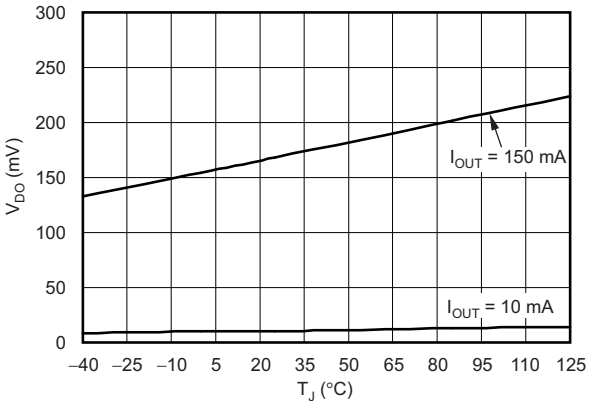



**Figure 7. Dropout Voltage vs Temperature**

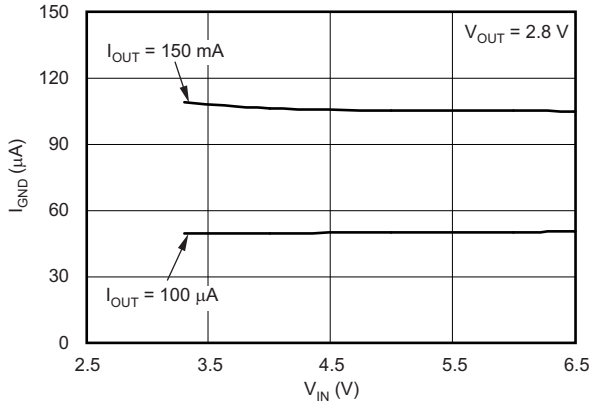



**Figure 8. Ground Pin Current vs Input Voltage**

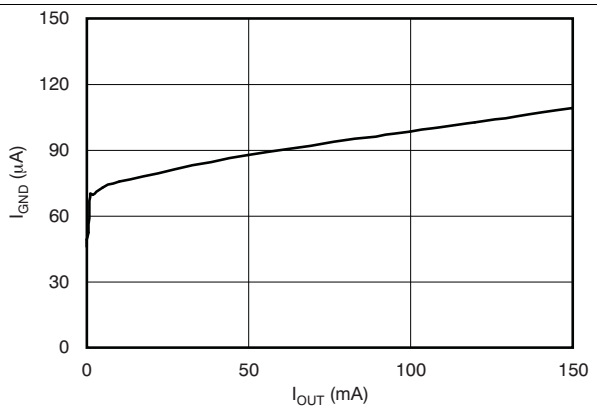



**Figure 9. Ground Pin Current vs Output Current**

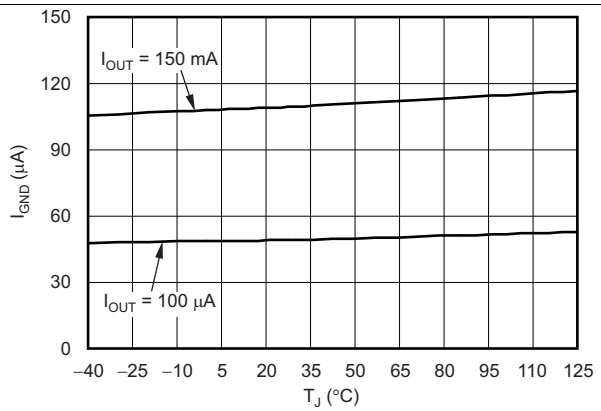



**Figure 10. Ground Pin Current vs Temperature (Enabled)**

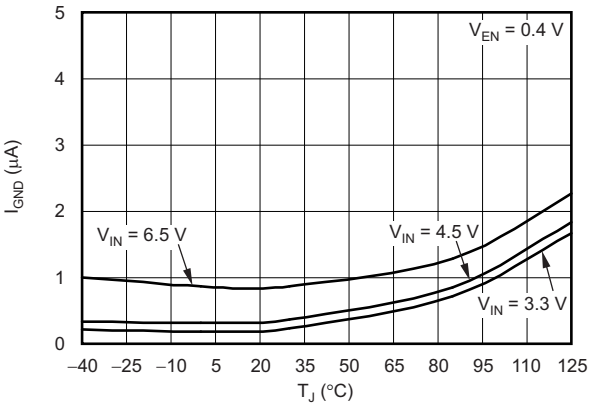



**Figure 11. Ground Pin Current vs Temperature (Disabled)**

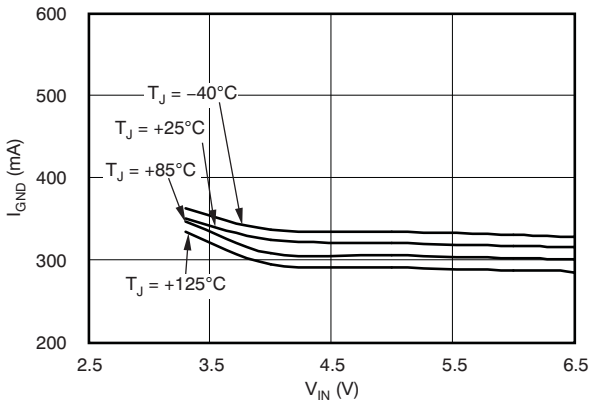



**Figure 12. Current Limit vs Input Voltage**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

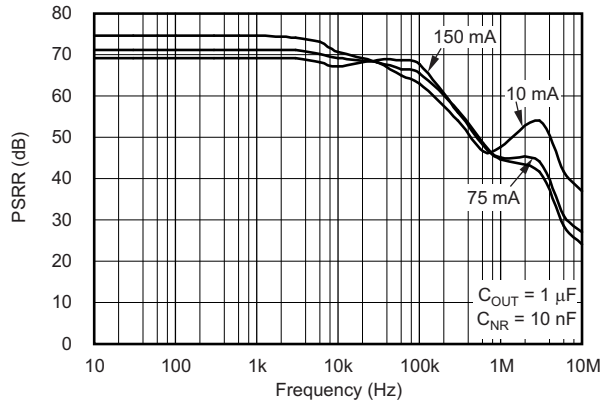



**Figure 13. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

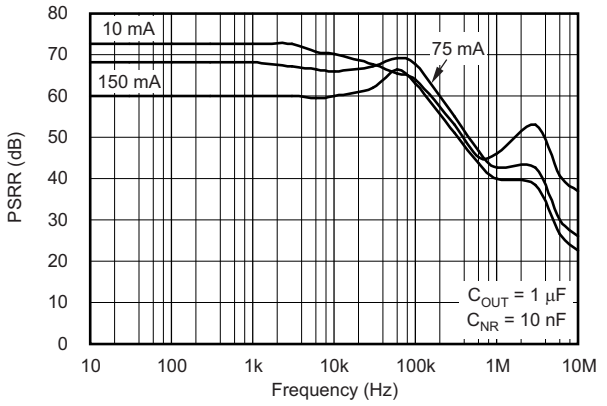



**Figure 14. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 0.5 V)**

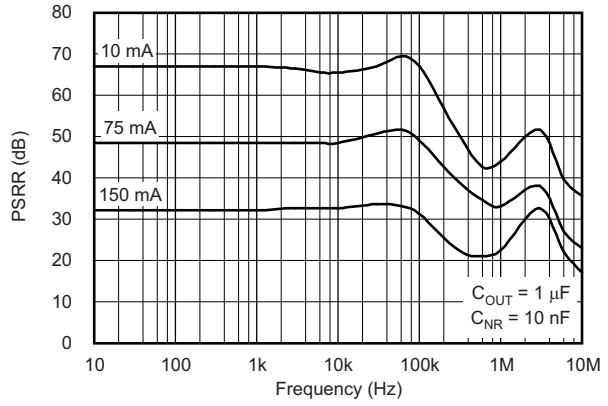



**Figure 15. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions ($V_{IN}$ – $V_{OUT}$ = 0.25 V)**

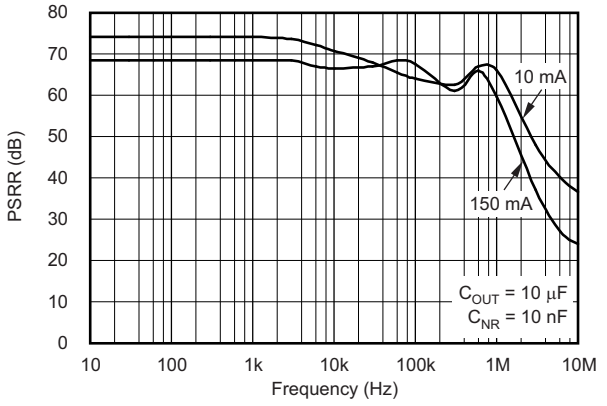



**Figure 16. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

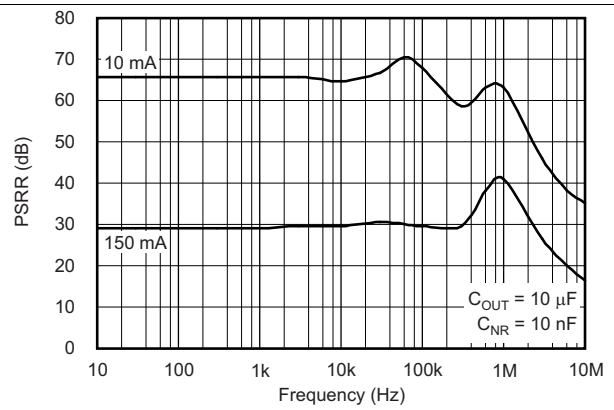



**Figure 17. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions ($V_{IN}$ – $V_{OUT}$ = 0.25 V)**

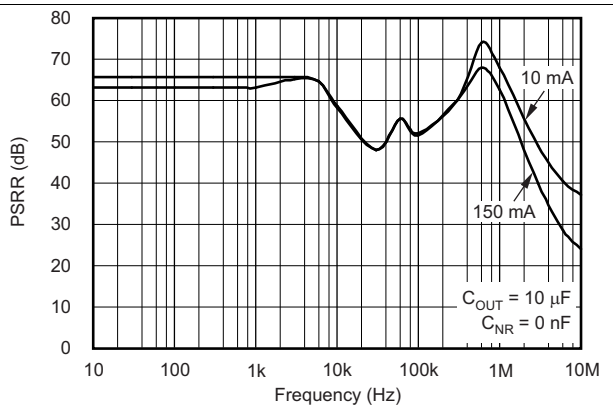



**Figure 18. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

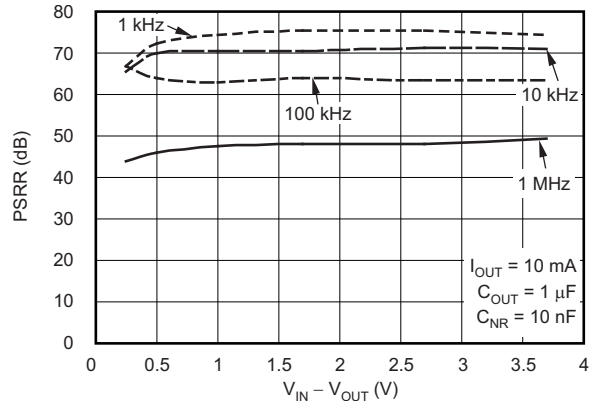



**Figure 19. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

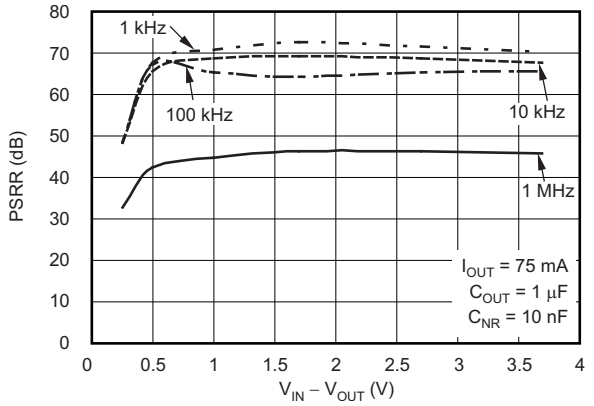



**Figure 20. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

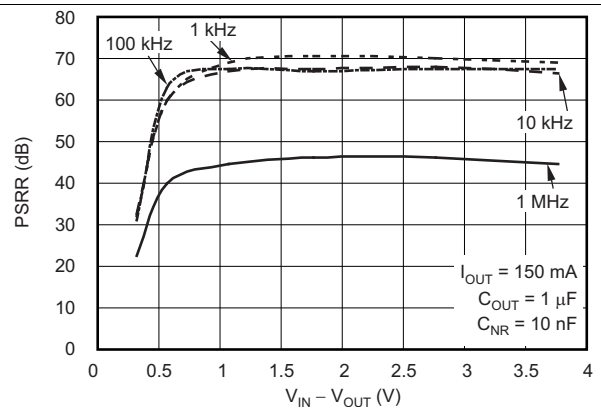



**Figure 21. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

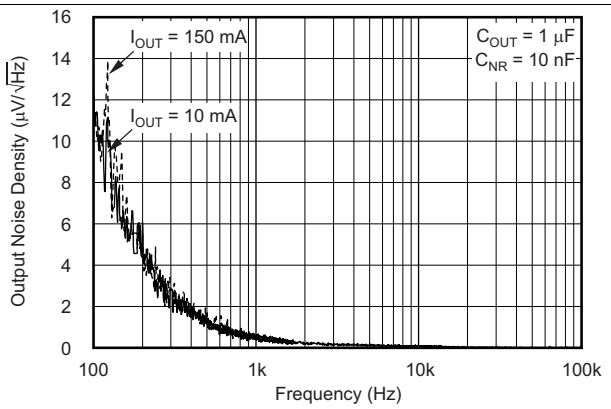



**Figure 22. Output Spectral Noise Density vs Output Current**

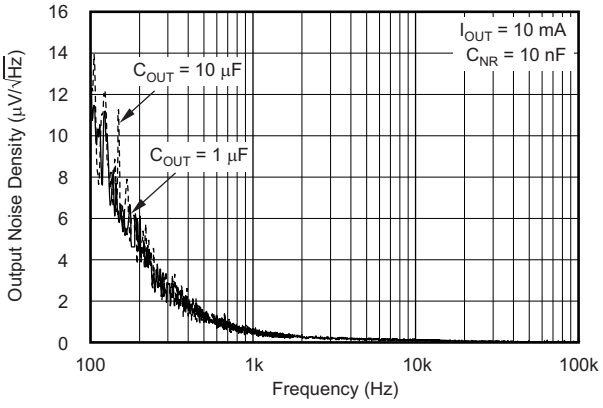



**Figure 23. Output Spectral Noise Density vs Output Capacitance**

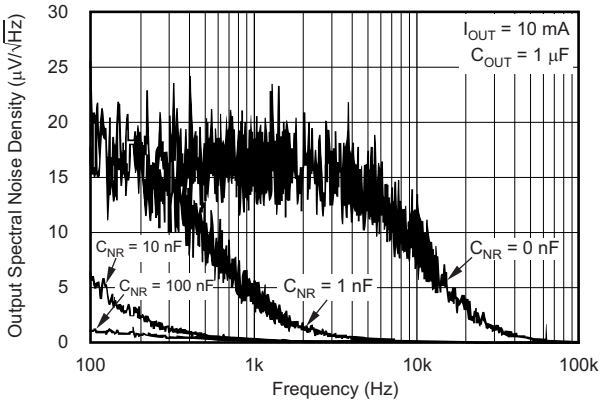



**Figure 24. Output Spectral Noise Density vs Noise Reduction**

## Typical Characteristics (continued)

Over operating temperature range ($T_J$, $T_A$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

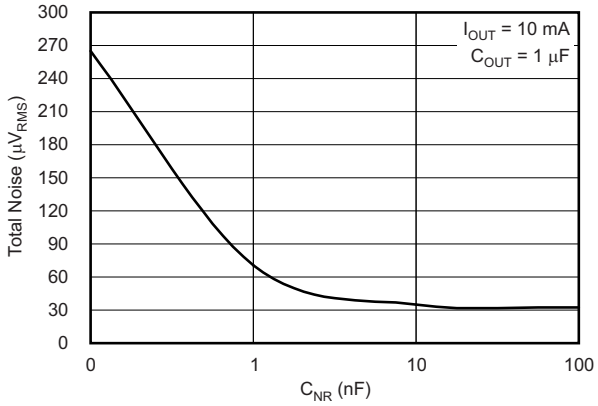



**Figure 25. Total Output Noise vs Noise Reduction**

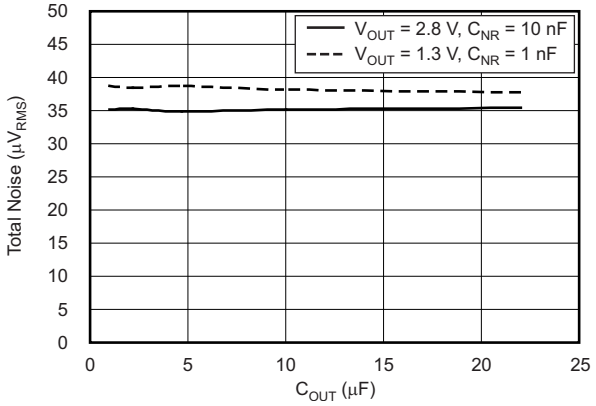



**Figure 26. Total Output Noise vs Output Capacitance**

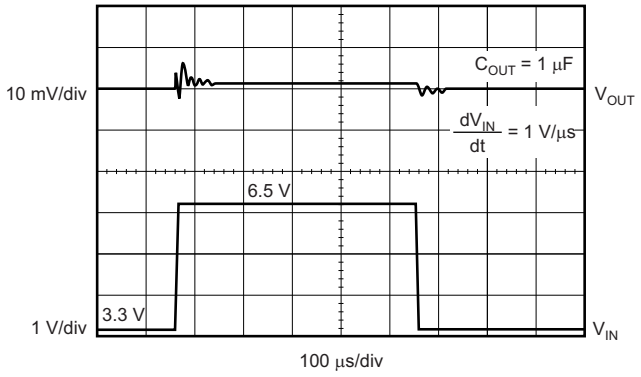



**Figure 27. Line Transient Response**

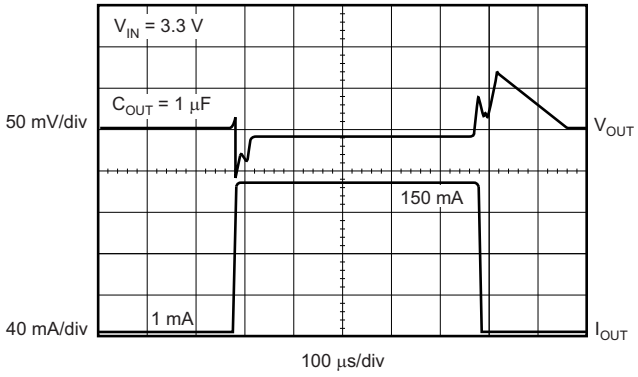



**Figure 28. Load Transient Response**

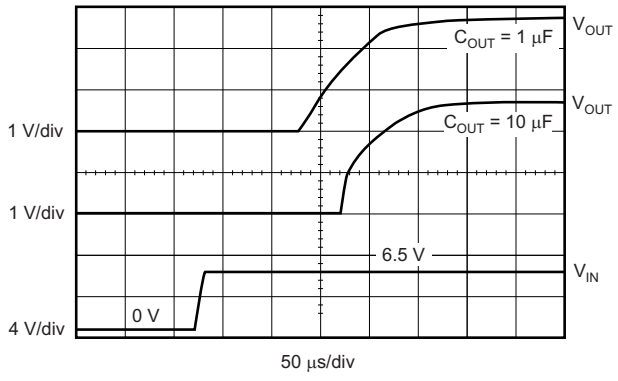



**Figure 29. Turn-On Response**

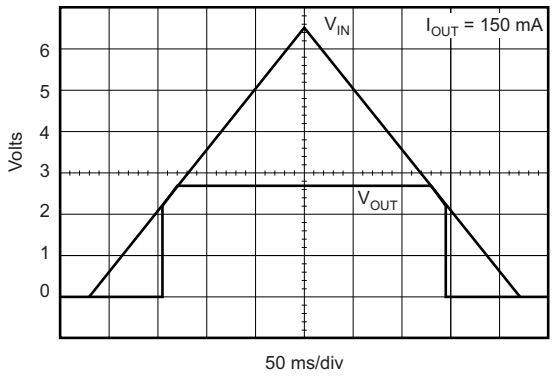



**Figure 30. Power-Up and Power-Down**

# 7 Detailed Description

## 7.1 Overview

The TPS717-Q1 family of low-dropout (LDO) regulators combines the high performance required by many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection with very low headroom ($V_{IN} – V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS717-Q1 family of devices an excellent choice for battery-powered applications. All versions have thermal and overcurrent protection. These devices are all also AEC-100 qualified for the grade 1 temperature range.

## 7.2 Functional Block Diagrams

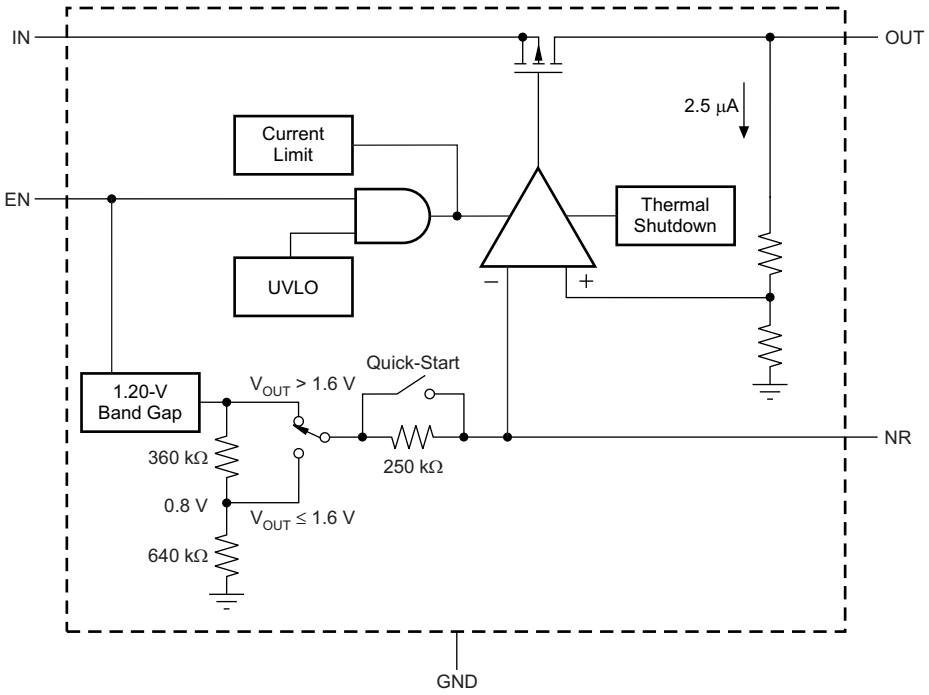



**Figure 31. Fixed Voltage Versions**

## Functional Block Diagrams (continued)

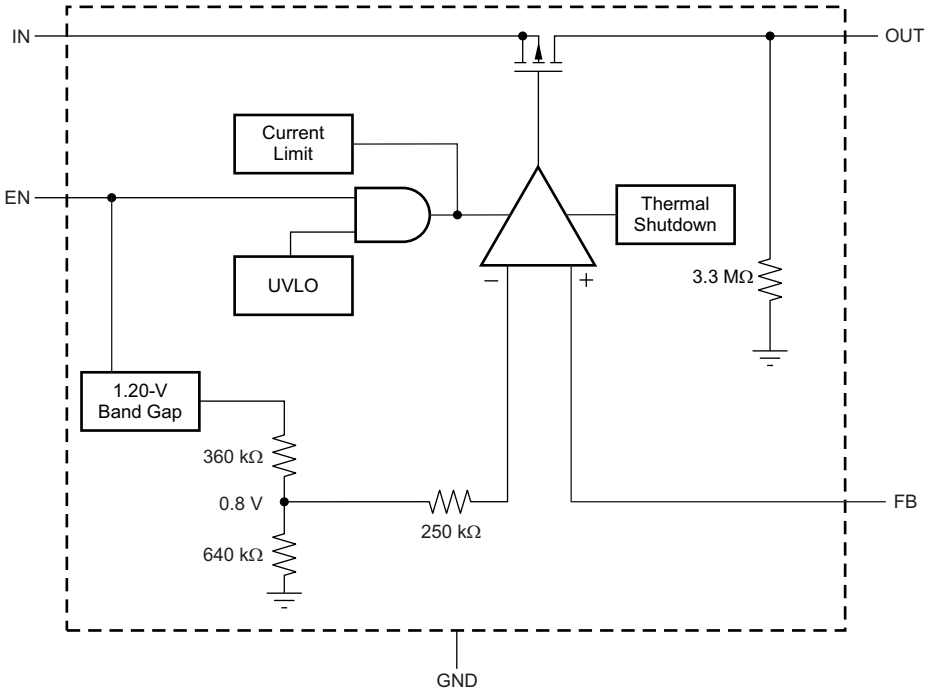



**Figure 32. Adjustable Voltage Version**

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TPS717-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS717-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

### 7.3.2 Shutdown

The enable pin (EN) is active high and compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

### 7.3.3 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS717-Q1 use a quick-start circuit to fast-charge the noise reduction capacitor, $C_{NR}$, if present (see Figure 31). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low-leakage $C_{NR}$ capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, apply $V_{IN}$ first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower; see Figure 29 in the *Typical Characteristics* section. The quick-start switch is closed for approximately 135 µs. To ensure that $C_{NR}$ is fully charged during the quick-start time, use a 0.01-µF or smaller capacitor.

## Feature Description (continued)

For output voltages below 1.6 V, a voltage divider on the band-gap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor ($C_{NR}$) results in slower start-up times for output voltages below 1.6 V.

Equation 1 approximates the start-up time as a function of $C_{NR}$ for output voltages below 1.6 V:

$$t_{START} = 160\mu s + \left(540 \frac{\mu s}{nF} \times C_{NR} nF\right)\mu s \quad (1)$$

### 7.3.4 Undervoltage Lockout (UVLO)

The TPS717-Q1 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a limited glitch immunity so undershoot transients are typically ignored on the input if these transients are less than 5 µs in duration. Note that a slow $V_{IN}$ ramp can cause the output voltage to rise when $V_{IN}$ is between 1.1 V to 1.4 V when at hot temperatures. When the input is lower than 1.4 V, the UVLO circuit may not have enough headroom to keep the output fully off.

### 7.3.5 Minimum Load

The TPS717-Q1 is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717-Q1 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

### 7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS717-Q1 into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is within the specified junction temperature range.

## Device Functional Modes (continued)

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

### 7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal mode | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} >$ UVLO | $V_{EN} > V_{EN(high)}$ | $I_{OUT} < I_{CL}$ | $T_J < 125°C$ |
| Dropout mode | UVLO $< V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(high)}$ | — | $T_J < 165°C$ |
| Disabled mode (any true condition disables the device) | $V_{IN} <$ UVLO $- V_{hys}$ | $V_{EN} < V_{EN(low)}$ | — | $T_J > 165°C$ |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS717-Q1 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ($V_{IN}$ – $V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR when a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for automotive applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to 125°C.

### 8.1.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases duration of the transient. The TPS717-Q1 has an ultra-wide loop bandwidth that allows it to respond quickly to load transient events. As with any regulator, the loop bandwidth is finite and the initial transient voltage peak is controlled by the sizing of the output capacitor. Typically, larger output capacitors reduce the peak and also reduce the bandwidth of the LDO, thus slowing the response time.

### 8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF or larger low equivalent series resistance (ESR) capacitor from IN to GND near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS717-Q1 is designed to be stable with ceramic output capacitors of values 1 µF or larger. The X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. The maximum ESR of the output capacitor must be less than 1 Ω. The minimum output capacitance is increased to 5 µF or larger if using an $R_2$ value outside of the range of 160 kΩ to 320 kΩ.

### 8.1.3 Dropout Voltage

The TPS717-Q1 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DSon}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is illustrated in Figure 15 through Figure 17 in the *Typical Characteristics* section.

## Application Information (continued)

### 8.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current times the voltage drop across the output pass element ($V_{IN}$ to $V_{OUT}$), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

### 8.1.5 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise reduction capacitor ($C_{NR}$) is used with the TPS717-Q1, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5 µA of divider current has the same noise performance as a fixed voltage version.

Equation 3 approximates the total noise referred to the feedback point (FB pin) when $C_{NR}$ = 0.01 µF:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \quad (3)$$

## 8.2 Typical Application

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701-Q1). **Note that the NR pin is not available on the adjustable version**.

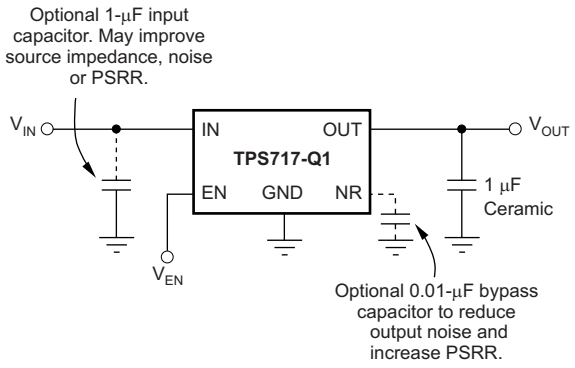



**Figure 33. Typical Application Circuit (Fixed Voltage Versions)**

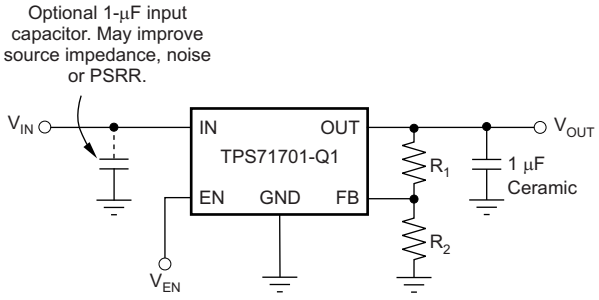



**Figure 34. Typical Application Circuit (Adjustable Voltage Version)**

### 8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 35.

**Table 2. Design Requirements**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.3 V, ±10% |
| Output voltage | 2.8 V, ±5% |
| Output current | 100 mA typical, 150 mA peak |
| Output voltage transient deviation | 5% |
| Maximum ambient temperature | 85°C |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Design Considerations*

For the adjustable version (TPS71701-Q1), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of $R_1$ and $R_2$. The values of $R_1$ and $R_2$ can be calculated for any voltage using the formula given in Equation 4:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

The value of $R_2$ directly affects the operation of the device and must be chosen in the range of approximately 160 kΩ to 332 kΩ. Sample resistor values for common output voltages are shown in Table 3.

**Table 3. Sample 1% Resistor Values For Common Output Voltages**

| $V_{OUT}$ | $R_1$ | $R_2$ |
|---|---|---|
| 1 | 80.6 kΩ | 324 kΩ |
| 1.2 | 162 kΩ | 324 kΩ |
| 1.5 | 294 kΩ | 332 kΩ |
| 1.8 | 402 kΩ | 324 kΩ |
| 2.5 | 665 kΩ | 316 kΩ |
| 3.3 | 1.02 MΩ | 324 kΩ |
| 5 | 1.74 MΩ | 332 kΩ |

#### *8.2.2.2 Powering a PLL Integrated on an SOC*

Figure 35 shows the TPS71701-Q1 powering a phase-locked loop (PLL) that is integrated into a system-on-a-chip (SOC).

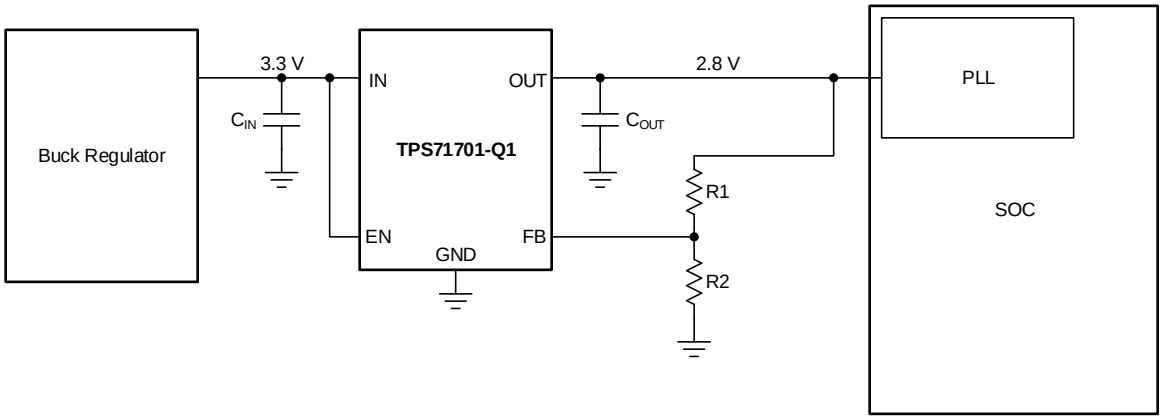



**Figure 35. Typical Application Circuit: PLL on an SOC**

#### 8.2.2.3 Design Considerations

Use the input and output capacitors to ensure the voltage transient requirements. A 1-µF input and 1-µF output capacitor are selected to maximize the capacitance and minimize capacitor size.

R2 is chosen to be 158 kΩ for optimal noise and PSRR, and by Equation 2, R1 is selected to be 402 kΩ. Both R1 and R2 must be 1% tolerance resistors to meet the dc accuracy specification over line, load, and temperature.

### 8.2.3 Application Curve

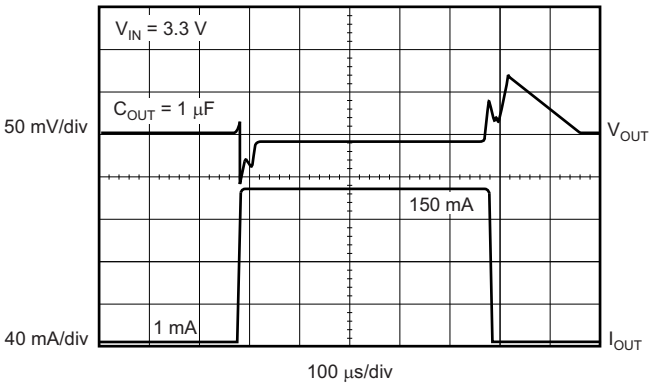



**Figure 36. Load Transient Response**

## 8.3 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible to both the input and output pins of the LDO.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not place any components in the feedback loop except for the input, output, and feed-forward capacitor and the feedback resistors.

Do not exceed the device absolute maximum ratings.

Do not float the enable (EN) pin.

# 9 Power Supply Recommendations

The TPS717-Q1 is designed to operate from an input voltage between 2.5 V and 6.5 V. The input supply must provide adequate headroom for the device to operate in a normal mode of operation.

Connect a low output impedance power supply directly to the IN pin of the TPS717-Q1. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor. To increase the overall PSRR of the power solution, use a pi-filter before the input of the LDO or after the FB network of the LDO.

# 10 Layout

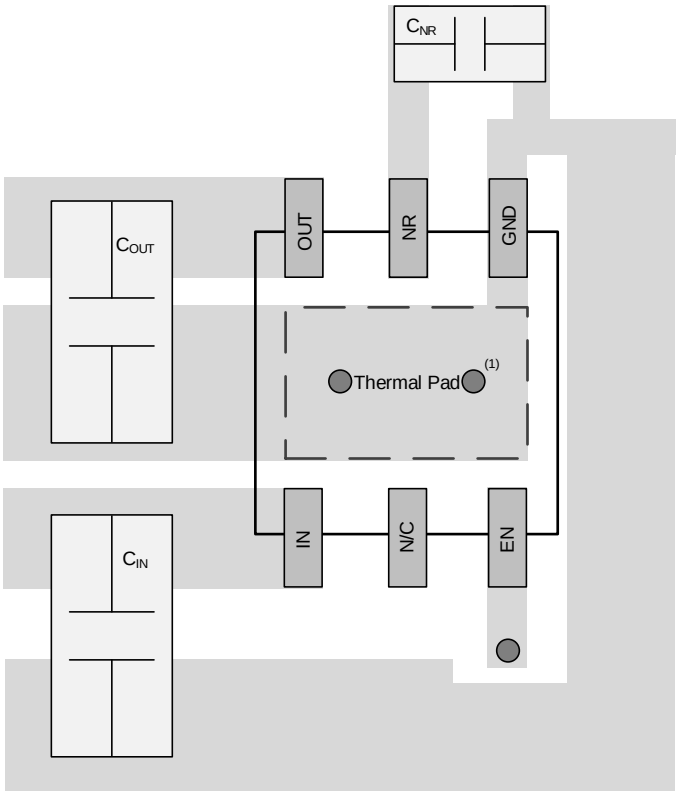
## 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to the GND pin as possible, connected by wide, component-side, copper surface area. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and functions similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

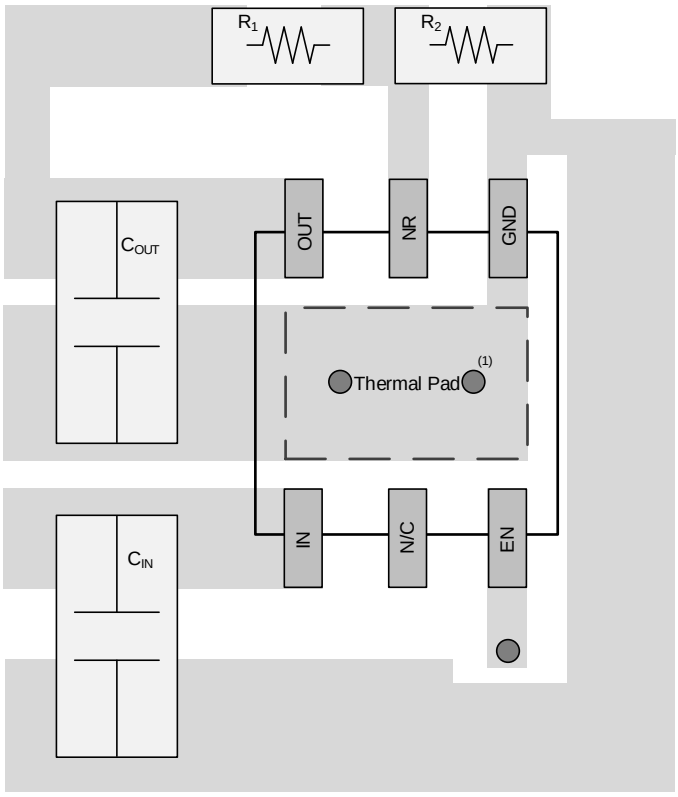
## 10.2 Layout Examples




(1) Circles within thermal pad area indicate vias to other layers on the board.

**Figure 37. Fixed Voltage Layout**

## Layout Examples (continued)




(1) Circles within thermal pad area indicate vias to other layers on the board.

**Figure 38. Adjustable Voltage Layout**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 Evaluation Module*

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS717. The TPS717xxEVM-134 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

### 11.1.2 Device Nomenclature

**Table 4. Device Nomenclature(1)**

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS717**xx(x)QYYYz-Q1** | **xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). An **01** denotes an adjustable voltage version.<br>**YYY** is the package designator.<br>**z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).<br>**Q** and **-Q1** denote an automotive device that is qualified at grade 1. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

PMP10651 Test Results, TIDUAE4

TPS717xxEVM-134 Evaluation Module User Guide, SLVU148

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71701QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 13B | Samples |
| TPS71709QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SHW | Samples |
| TPS71709QDSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BD | Samples |
| TPS71712QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SHX | Samples |
| TPS71715QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SHY | Samples |
| TPS71718QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SHZ | Samples |
| TPS71725QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SIA | Samples |
| TPS71728QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SIB | Samples |
| TPS71730QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SIC | Samples |
| TPS71733QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SID | Samples |
| TPS71745QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SHF | Samples |
| TPS71745QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SIE | Samples |
| TPS71750QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SIF | Samples |
| TPS71750QDSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | AV | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF TPS717-Q1 :**

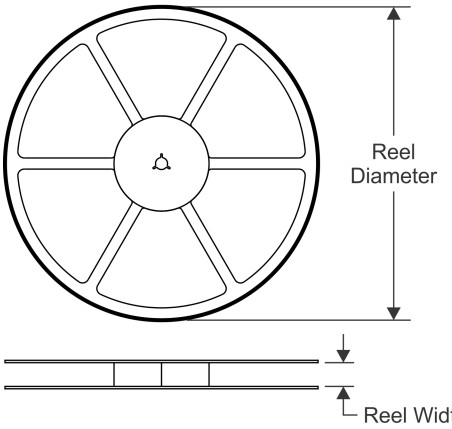
- Catalog: TPS717

NOTE: Qualified Version Definitions:

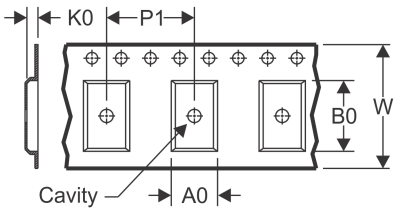
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

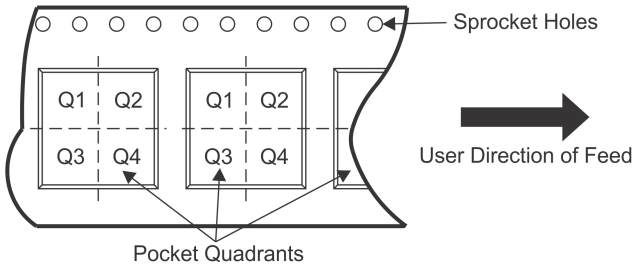



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

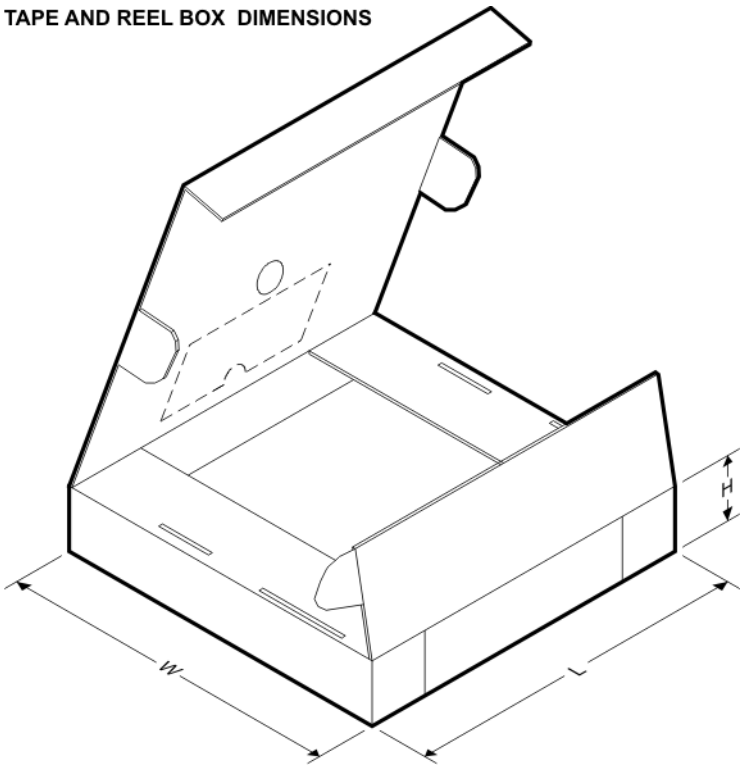
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71701QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71709QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71709QDSERQ1 | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71712QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71715QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71718QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71725QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71728QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71730QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71733QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71745QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71745QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71750QDRVRQ1 | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

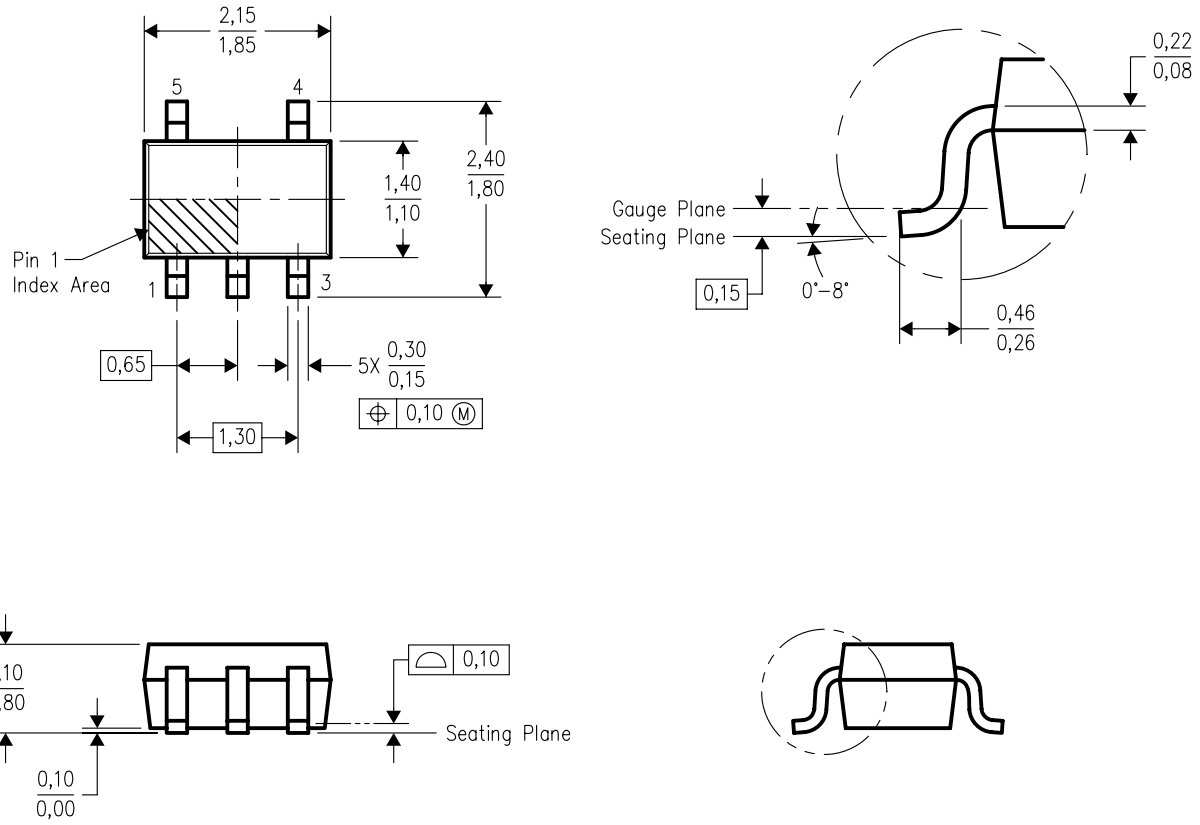
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71701QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71709QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71709QDSERQ1 | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71712QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71715QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71718QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71725QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71728QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71730QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71733QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71745QDCKRQ1 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71745QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71750QDRVRQ1 | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |

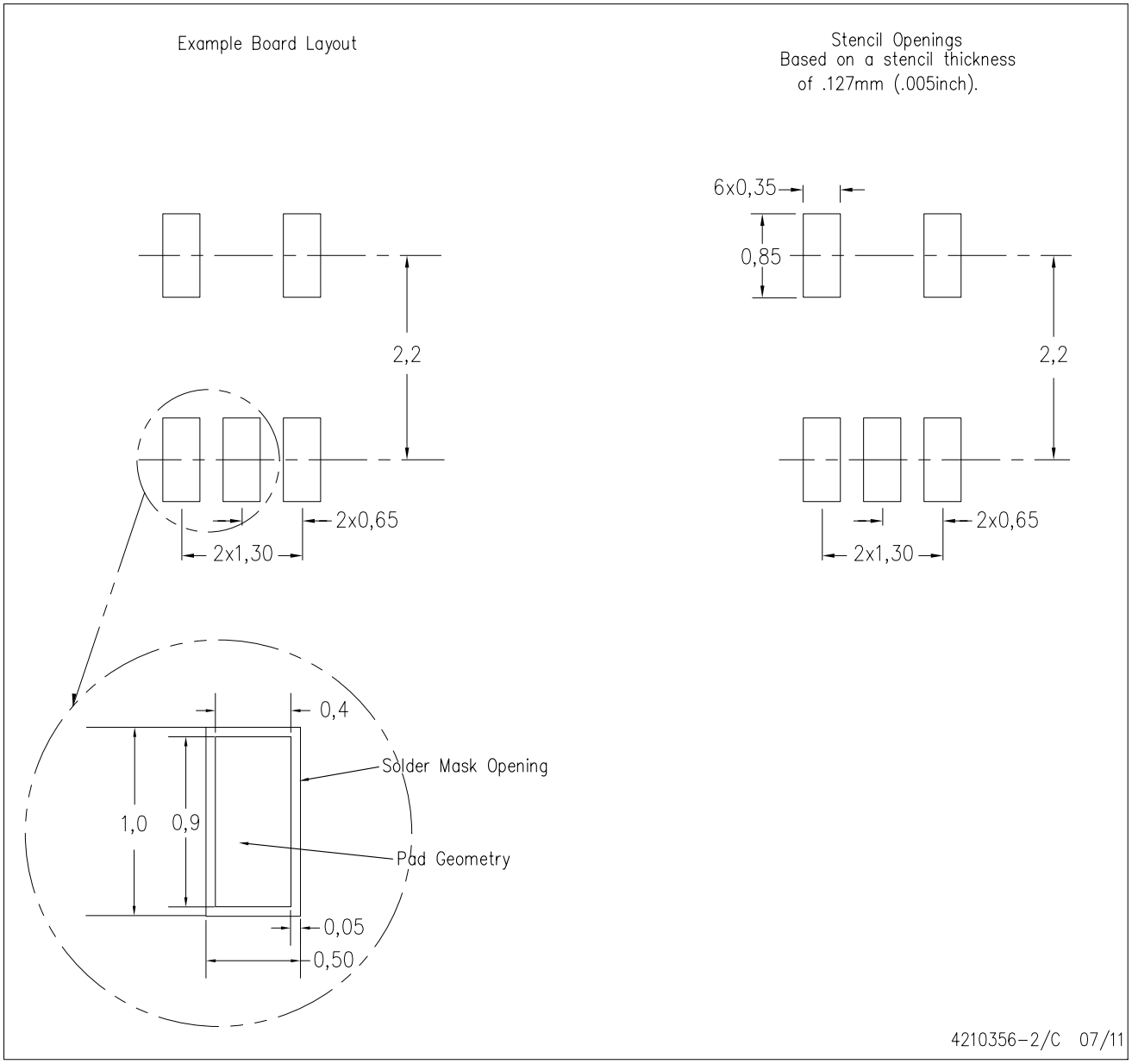
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

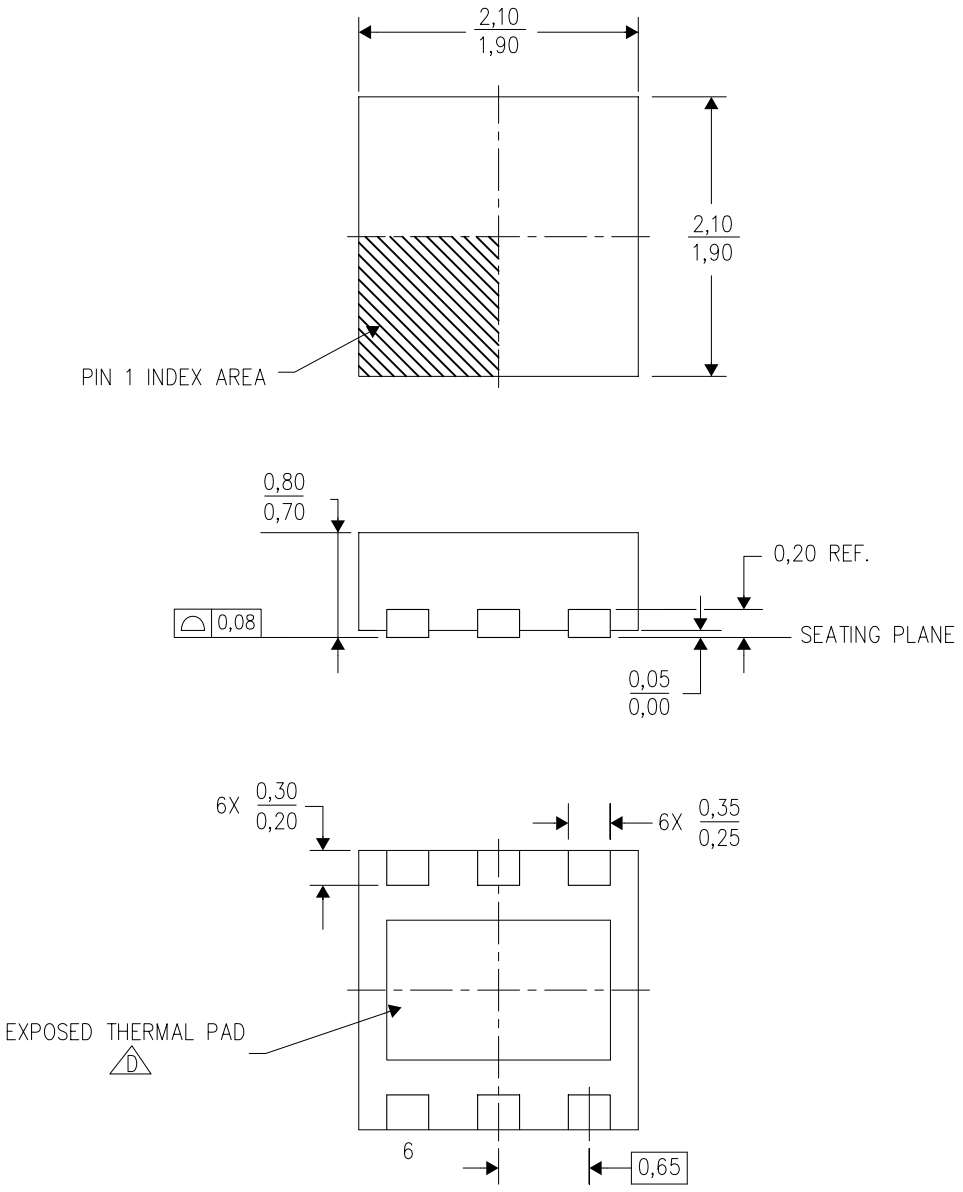
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

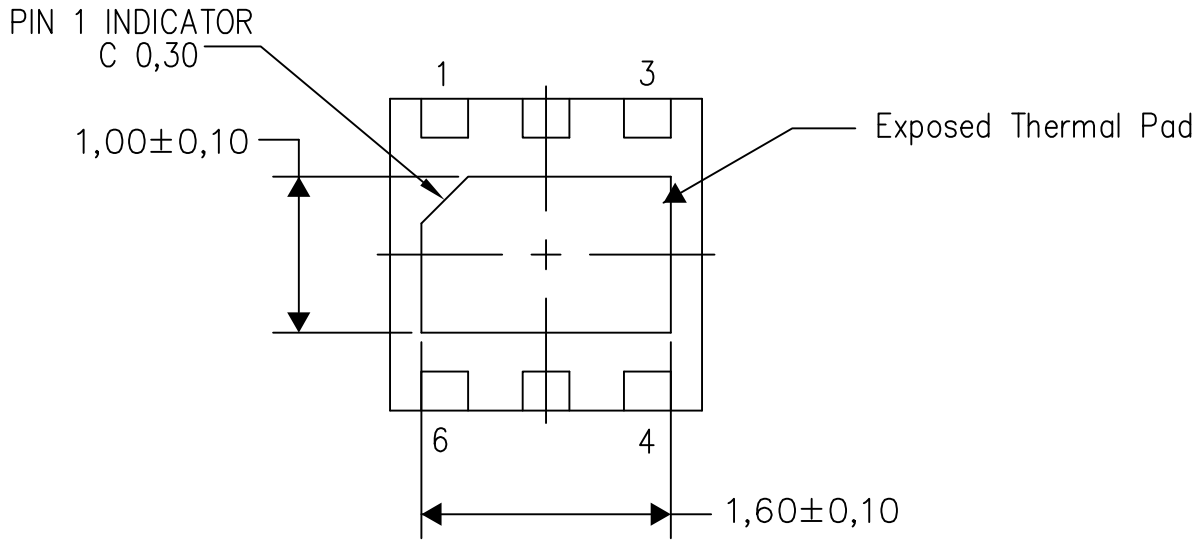
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



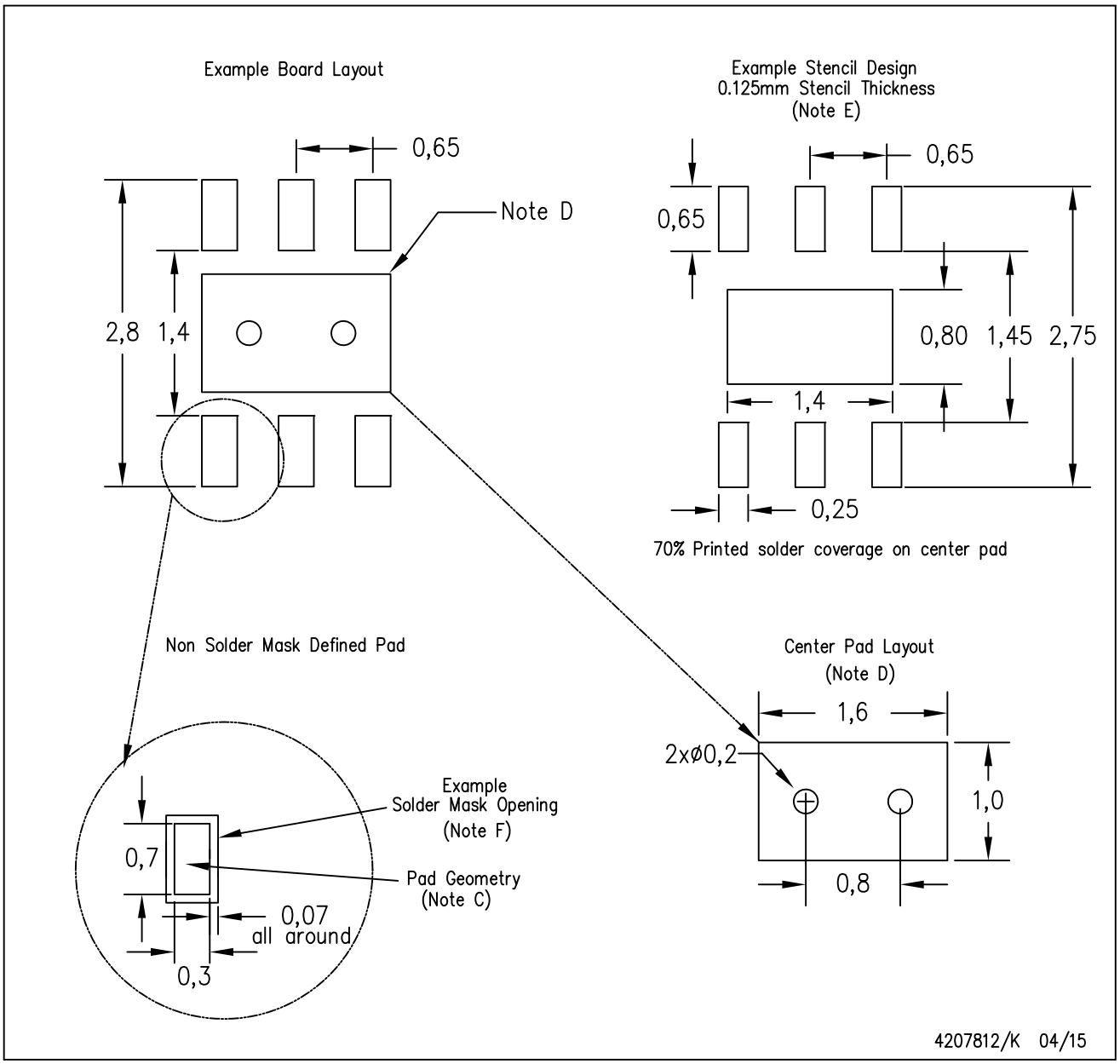

Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

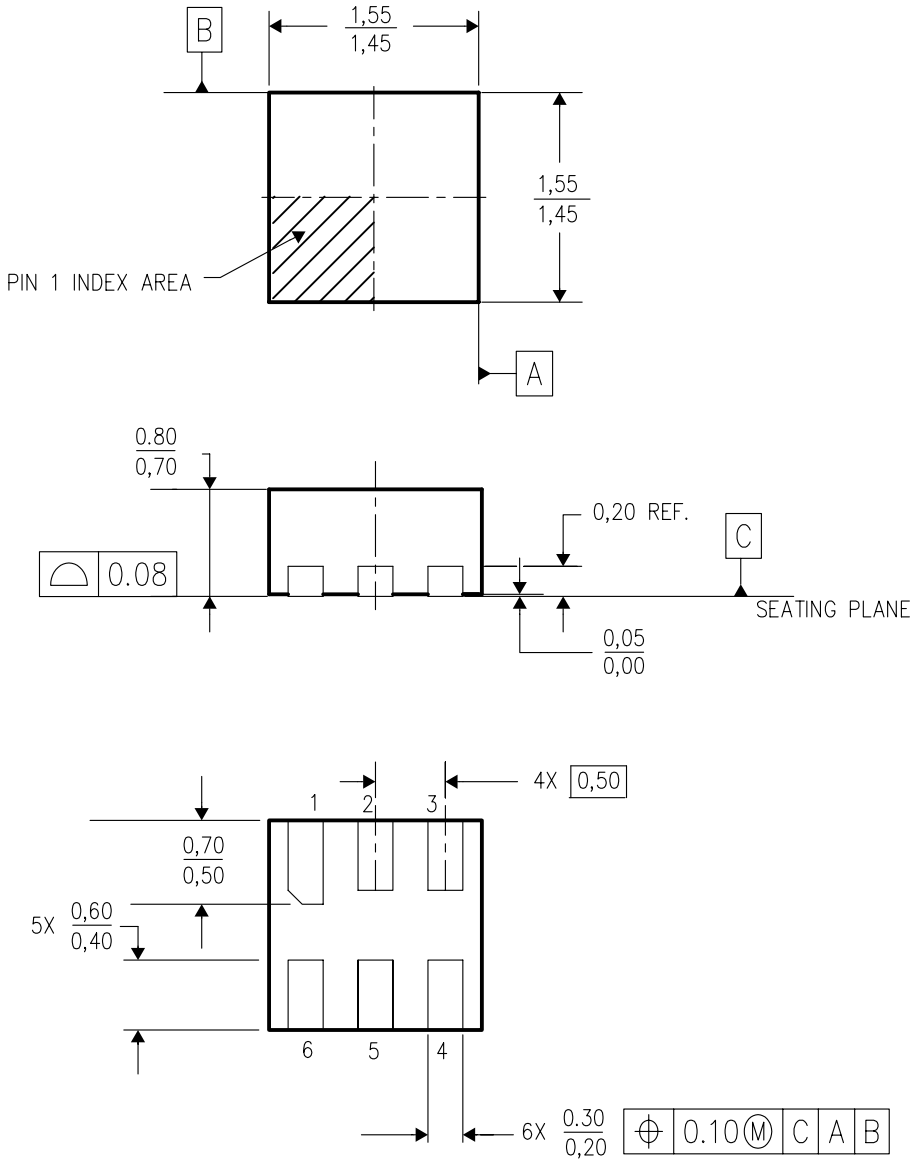
NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE




4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

## IMPORTANT NOTICE

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TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

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