TPS65631W Dual-Output AMOLED Display Power Supply

1 Features

- 2.9-V to 4.5-V Input Voltage Range
- Fixed 4.6-V Positive Output Voltage
- 0.5% V_{POS} Accuracy from 25ºC to 85ºC
- Separate V_{POS} Output Sense Pin
- Negative Output Voltage Digitally Programmable from –1.4 V to –4.4 V (–4 V Default)
- Output Currents up to 200 mA Supported
- Excellent Line Transient Regulation
- Outputs High Impedance During Shut Down
- Short-Circuit Protection
- Thermal Shutdown
- Available in 2.5-mm × 2.5-mm, 10-Pin QFN Package

2 Applications

AMOLED Displays

3 Description

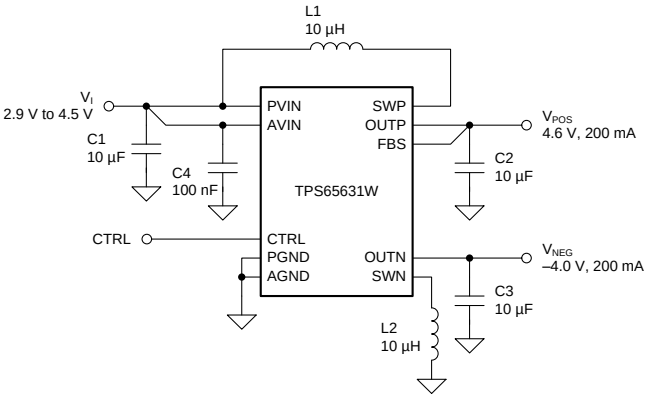
The TPS65631W is designed to drive AMOLED (Active Matrix Organic Light Emitting Diode) displays requiring positive and negative supply rails. The device integrates a boost converter for V_{POS} and an inverting buck boost converter for V_{NEG} and is suitable for battery-operated products. The digital control pin (CTRL) allows programming the negative output voltage in digital steps. The TPS65631W uses a novel technology enabling excellent line transient performance.

Device Information(1)

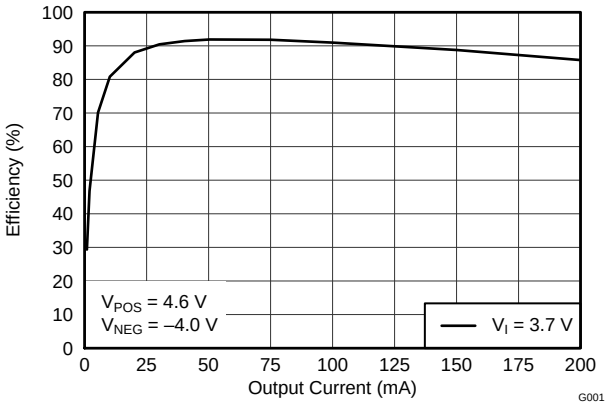
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65631W	QFN (10)	2.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

4 Simplified Schematic



Efficiency vs Output Current



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2015) to Revision C — **Page**

- Deleted sentence in the Overview description. ... 8

Changes from Revision A (September 2014) to Revision B — **Page**

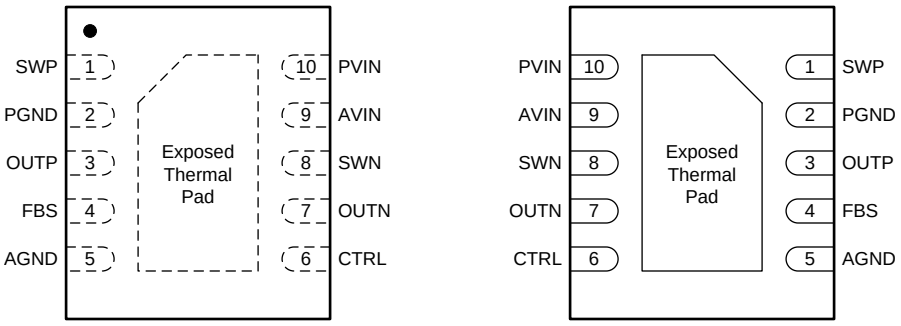
- Added "Outputs High Impedance During Shut Down" to Features. ... 1
- Changed front-page schematic ... 1
- Changed symbol for shut-down time ... 6
- Added t_{OFF} to Timing Requirements ... 6
- Changed Figure 6 ... 9
- Deleted "Output Discharge During Shut Down" subsection ... 10
- Changed "300 mA" to "200 mA" ... 12
- Changed Figure 8 ... 12
- Changed recommended capacitance value for C1 and C3, and reformatted table entries ... 13
- Changed "2 ×10 µF" to "10 µF" ... 16

Changes from Original (July 2013) to Revision A — **Page**

- Added Device Information and Handling Rating tables, Feature Description section, Device Functional Modes, Programming section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 1

6 Pin Configuration and Functions

SON (DSK) PACKAGE
10-PINS



Pin Functions

NAME	NO.	I/O	DESCRIPTION
AGND	5	—	Analog ground.
AVIN	9	—	Input supply voltage for internal analog circuits (both converters).
CTRL	6	I	Control pin. Combined device enable and inverting buck-boost converter output voltage programming pin.
FBS	4	I	Feedback sense pin of the boost converter output voltage.
PGND	2	—	Power ground of the boost converter.
PVIN	12	—	Input supply voltage pin for the inverting buck-boost converter.
SWN	8	O	Switch pin of the inverting buck-boost converter.
SWP	1	O	Switch pin of the boost converter.
OUTN	7	O	Rectifier pin of the inverting buck-boost converter.
OUTP	3	O	Rectifier pin of the boost converter.
Exposed Thermal Pad	13	—	Connect this pad to AGND and PGND.

7 Specifications

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	SWP, OUTP, FBS, PVIN, AVIN	–0.3	6	V
	OUTN	–0.3	–6	V
	SWN	–6	6	V
	CTRL	–0.3	5.5	V
Operating junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to AGND pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{STG}	Storage temperature range		–65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	V
		Machine model (MM) ESD stress voltage	–200	200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process..

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_I	Input supply voltage range		2.9	3.7	4.5	V
V_O	Output voltage range	V_{POS}		4.6		V
		V_{NEG}	–4.4	–4	–1.4	
I_O	Output current range	I_{POS}	0		200	mA
		I_{NEG}	0		200	
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	85	125	

7.4 Thermal Information

THERMAL METRIC (1)		DSK	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	57.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.1	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	21.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	4.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_I = 3.7 V, $V_{(CTRL)}$ = 3.7 V, V_{POS} = 4.6 V, V_{NEG} = –4.0 V, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_I	Shutdown current into AVIN and PVIN	CTRL pin connected to ground.		0.1		µA
V_{UVLO}	Undervoltage lockout threshold	V_I rising.			2.4	V
		V_I falling.			2.1	
BOOST CONVERTER						
V_O	Output voltage			4.6		V
	Output voltage tolerance	25°C ≤ T_J ≤ 85°C, no load	–0.5%		0.5%	
		–40°C ≤ T_J < 85°C, no load	–0.8%		0.8%	
$r_{DS(on)}$	Switch (low-side) on-resistance	$I_{(SWP)}$ = 200 mA		200		mΩ
	Rectifier (high-side) on-resistance	$I_{(SWP)}$ = 200 mA		350		
	Switching frequency	I_O = 200 mA		1.7		MHz
	Switch current limit	Inductor valley current	0.8	1		A
	Short-circuit threshold voltage in operation	V_O falling		4.1		V
	Short-circuit detection time during operation			3		ms
	Output sense threshold voltage using OUTP	$V_{(OUTP)}$ - $V_{(FBS)}$ increasing		300		mV
	Output sense threshold voltage using FBS	$V_{(OUTP)}$ - $V_{(FBS)}$ decreasing		200		mV
	Input resistance of FBS	Between FBS pin and ground		4		MΩ
	Discharge resistance	CTRL pin connected to ground, I_O = 1 mA		30		Ω
	Line regulation	I_O = 200 mA		0.002		%/V
	Load regulation			0.01		%/A
INVERTING BUCK-BOOST CONVERTER						
V_O	Output voltage default			–4.0		V
	Output voltage range		–4.4		–1.4	
	Output voltage tolerance		–0.05		0.05	
$r_{DS(on)}$	Switch (high-side) on-resistance	$I_{(SWN)}$ = 200 mA		200		mΩ
	Rectifier (low-side) on-resistance	$I_{(SWN)}$ = 200 mA		300		
	Switching frequency	I_O = 10 mA		1.7		MHz
	Switch current limit	V_I = 2.9 V	1.5	2.2		A
	Short-circuit threshold voltage during operation	Voltage drop from nominal V_O		500		mV
	Short-circuit threshold voltage during start-up		180	200	230	
t_{SCP}	Short-circuit detection time during start-up			10		ms
	Short-circuit detection time during operation			3		ms
	Discharge resistance	CTRL pin connected to ground, I_O = 1 mA		150		Ω
	Line regulation	I_O = 200 mA		0.006		%/V
	Load regulation			0.31		%/A

Electrical Characteristics (continued)

V_I = 3.7 V, $V_{(CTRL)}$ = 3.7 V, V_{POS} = 4.6 V, V_{NEG} = –4.0 V, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTRL						
	High-level threshold voltage				1.2	V
	Low-level threshold voltage		0.4			V
	Pull-down resistance		150	400	860	kΩ
OTHER						
t_{INIT}	Initialization time			300	400	µs
t_{SDN}	Shut-down time		30		80	µs
t_{STORE}	Data storage time		30		80	µs
T_{SD}	Thermal shutdown temperature			145		°C

7.6 Timing Requirements

		MIN	TYP	MAX	UNIT
CTRL Interface					
t_{HIGH}	High-level pulse duration	2	10	25	µs
t_{LOW}	Low-level pulse duration	2	10	25	µs
t_{OFF}	Shut-down pulse duration (CTRL = low)	200			µs

7.7 Typical Characteristics

At T_A = 25°C, unless otherwise noted.

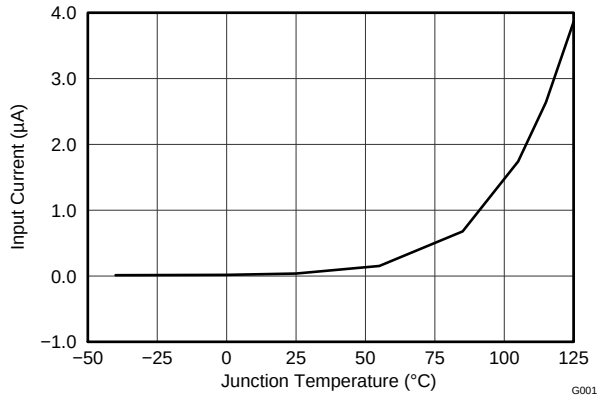


Figure 1. Shutdown Current into AVIN and PVIN

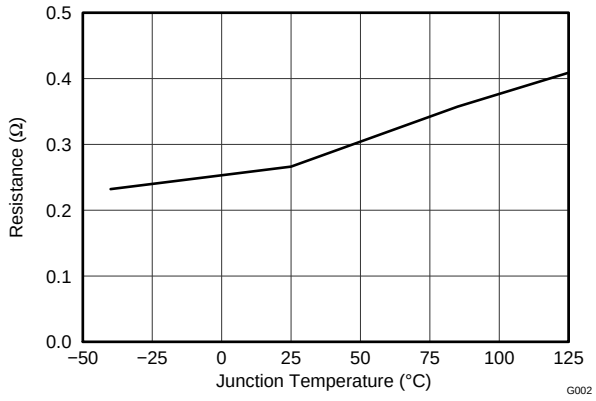


Figure 2. Boost Converter Switch $r_{DS(on)}$

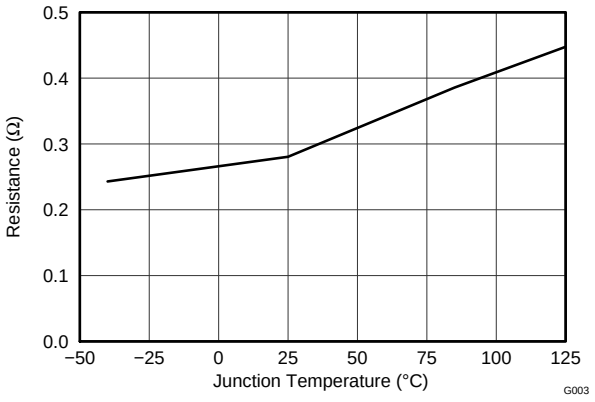


Figure 3. Boost Converter Rectifier $r_{DS(on)}$

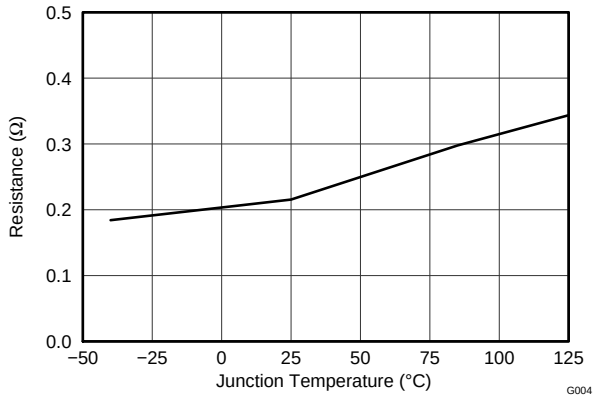


Figure 4. Inverting Buck-Boost Converter Switch $r_{DS(on)}$

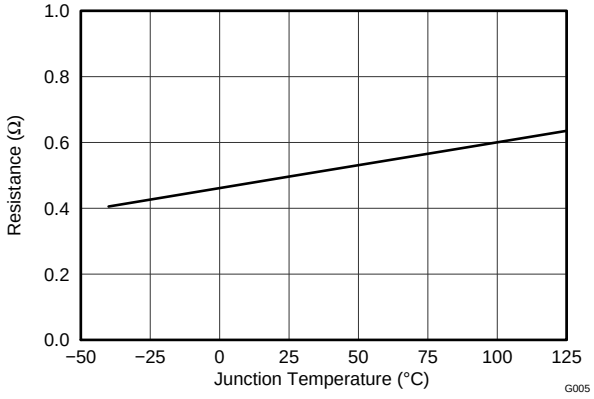


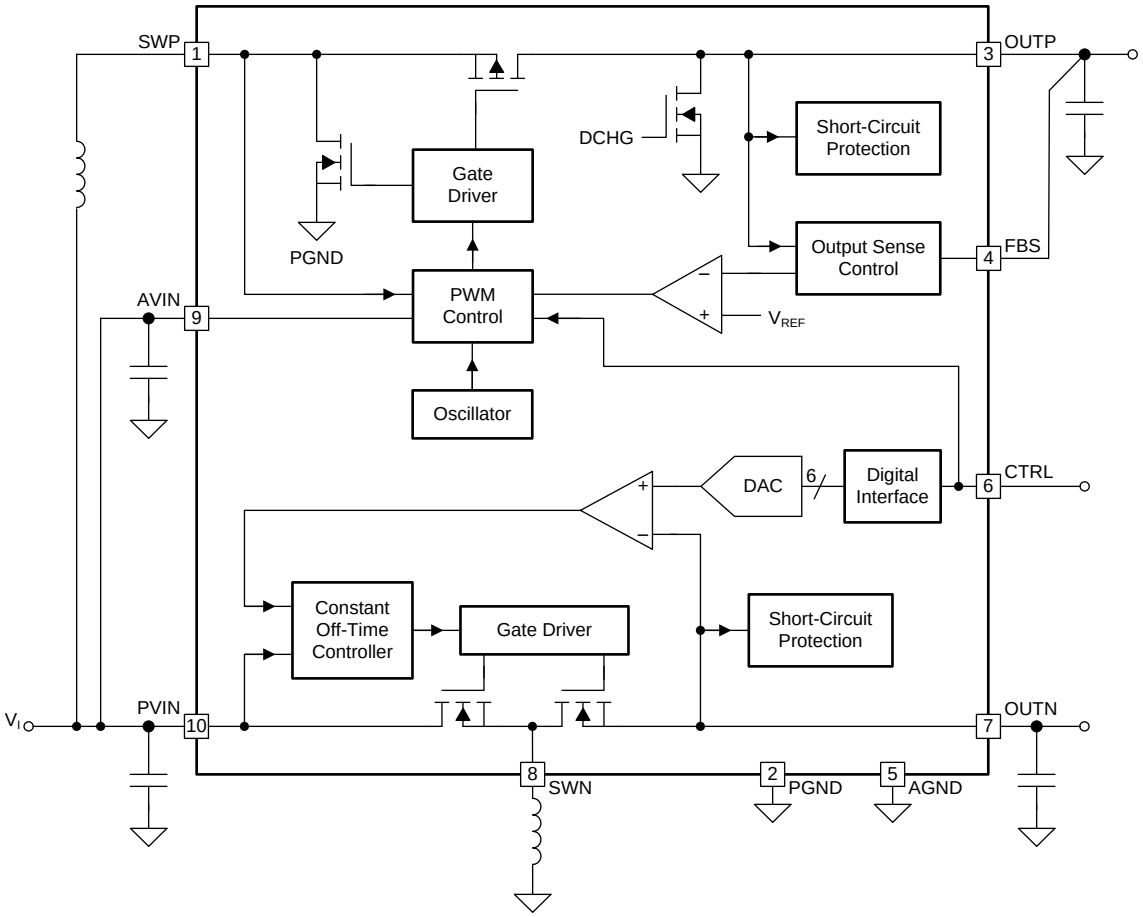
Figure 5. Inverting Buck-Boost Converter Rectifier $r_{DS(on)}$

8 Detailed Description

8.1 Overview

The TPS65631W consists of a boost converter and an inverting buck boost converter. The V_{POS} output is fixed at 4.6 V and V_{NEG} output is programmable via a digital interface in the range of –1.4 V ~ –4.4 V, the default is –4 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter

The boost converter uses a fixed-frequency current-mode topology, and its output voltage (V_{POS}) is fixed at 4.6 V

For the highest output voltage accuracy, connect the output sense pin (FBS) directly to the positive pin of the output capacitor. If not used, the FBS pin can be left floating or connected to ground. If the FBS pin is not used, the boost converter senses its output voltage using the OUTP pin.

8.3.2 Inverting Buck-Boost Converter

The inverting buck-boost converter uses a constant-off-time peak-current mode topology. The converter's default output voltage (V_{NEG}) is –4 V, but it can be programmed to any voltage in the range –1.4 V to –4.4 V (see *Programming V_{NEG}*).

Feature Description (continued)

8.3.3 Soft-Start and Start-Up Sequence

The TPS65631W features a soft-start function to limit inrush current. When the device is enabled by a high-level signal applied to the CTRL pin, the boost converter starts switching with a reduced switch current limit. Ten milliseconds after the CTRL pin goes high, the inverting buck-boost converter starts with a default value of –4 V. A typical start-up sequence is shown in Figure 6.

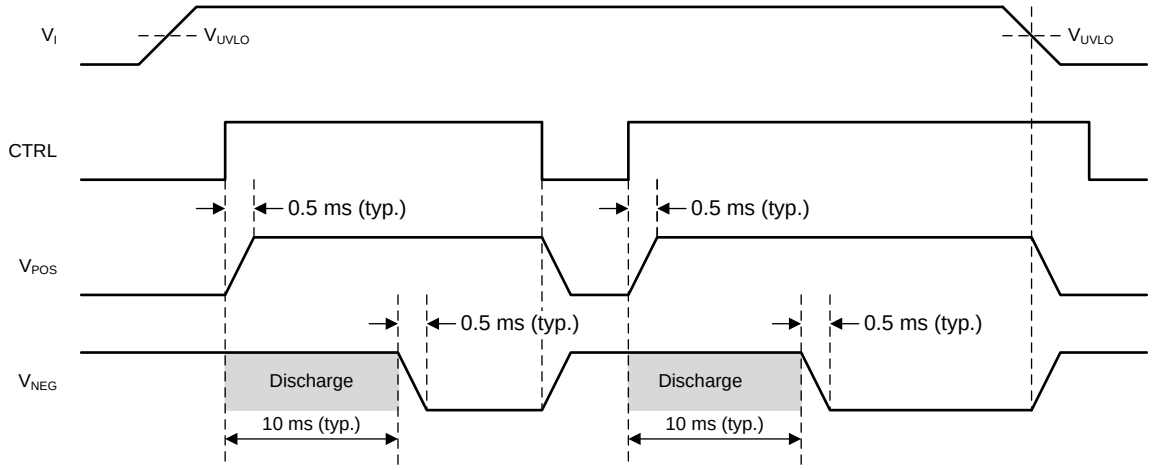


Figure 6. Start-Up Sequence

8.3.4 Enable (CTRL)

The CTRL pin serves two functions. One is to enable and disable the device, and the other is to program the output voltage (V_{NEG}) of the inverting buck-boost converter (see *Programming V_{NEG}*). If the digital interface is not required, the CTRL pin can be used as a standard enable pin for the device, which will come up with its default value on V_{NEG} of –4 V. When CTRL is pulled high, the device is enabled. The device is shut down with CTRL low.

8.3.5 Undervoltage Lockout

The TPS65631W features an undervoltage lockout function that disables the device when the input supply voltage is too low for normal operation.

8.3.6 Short Circuit Protection

The TPS65631W is protected against short-circuits of V_{POS} and V_{NEG} to ground and to each other.

8.3.6.1 Short-Circuits During Normal Operation

During normal operation an error condition is detected if V_{POS} falls below 4.1 V for more than 3 ms or V_{NEG} is pulled above the programmed nominal output by 500 mV for longer than 3 ms. In either case the device enters shutdown mode: the converters are disabled and their outputs are disconnected from the input. To resume normal operation either cycle the input supply voltage or toggle the CTRL pin low and then high again.

8.3.6.2 Short-Circuits During Start-Up

During start up an error condition is detected if:

- V_{POS} is not in regulation 10 ms after a high-level is applied to the CTRL pin.
- V_{NEG} is higher than threshold level 10 ms after a high-level is applied to the CTRL pin.
- V_{NEG} is not in regulation 20 ms after a high-level is applied to the CTRL pin.

To resume normal operation either cycle the input supply voltage or toggle the CTRL pin low and then high again.

Feature Description (continued)

8.3.7 Thermal Shutdown

The TPS65631W enters thermal shutdown mode if its junction temperature exceeds 145°C (typical). During thermal shutdown mode none of the device functions are available. To resume normal operation, either cycle the input supply voltage or toggle the CTRL pin low and then high again.

8.4 Device Functional Modes

8.4.1 Operation with V_I < 2.9 V

The recommended minimum input supply voltage for full performance is 2.9 V. The device continues to operate with input supply voltages below 2.9 V; however, full performance is not guaranteed. The device does not operate with input supply voltages below the UVLO threshold.

8.4.2 Operation with $V_I \approx V_{POS}$ (Diode Mode)

The TPS65631W features a "diode" mode that enables it to regulate its output voltage even when the input supply voltage is close to V_{POS} (that is, too high for normal boost operation). When operating in diode mode the converter's high-side switch stops switching and its body diode is used as the rectifier. Boost converter efficiency is reduced when operating in diode mode. At low output currents (≈2 mA and below), the boost converter automatically transitions from pulse-width modulation to pulse-skip mode. This ensures that V_{POS} stays in regulation but increases the output voltage ripple on V_{POS}.

8.4.3 Operation with CTRL

When a low-level signal is applied to the CTRL pin the device is disabled and switching is inhibited. When the input supply voltage is above the UVLO threshold and a high-level signal is applied to the CTRL pin the device is enabled and its start-up sequence begins.

8.5 Programming

8.5.1 Programming V_{NEG}

The output voltage of the inverting buck-boost converter (V_{NEG}) can be programmed using the CTRL pin. If output voltage programming is not required, the CTRL pin can be used as a standard enable pin (see *Enable (CTRL)*).

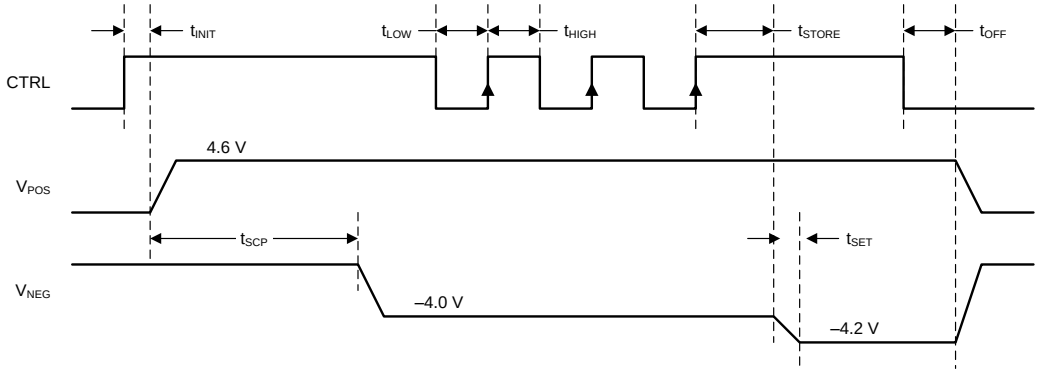


Figure 7. Programming V_{NEG} Using the CTRL Pin

When the CTRL pin is pulled high, the inverting buck-boost converter starts up with its default voltage of –4V. The device now counts the rising edges applied to the CTRL pin and sets the output voltage (V_{NEG}) according to Table 1. For the timing diagram shown in Figure 7, V_{NEG} is programmed to –4.2 V, since three rising edges are detected.

The CTRL interface is designed to work with pulses whose duration is between 2 µs and 25 µs. Pulses shorter than 2 µs or longer than 25 µs are not ensured to be recognized.

Table 1. Programming Table for V_{NEG}

Number of Rising Edges	V_{NEG}	Number of Rising Edges	V_{NEG}
0 / no pulses	–4 V	16	–2.9 V
1	–4.4 V	17	–2.8 V
2	–4.3 V	18	–2.7 V
3	–4.2 V	19	–2.6 V
4	–4.1 V	20	–2.5 V
5	–4.0 V	21	–2.4 V
6	–3.9 V	22	–2.3 V
7	–3.8 V	23	–2.2 V
8	–3.7 V	24	–2.1 V
9	–3.6 V	25	–2.0 V
10	–3.5 V	26	–1.9 V
11	–3.4 V	27	–1.8 V
12	–3.3 V	28	–1.7 V
13	–3.2 V	29	–1.6 V
14	–3.1 V	30	–1.5 V
15	–3.0 V	31	–1.4 V

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 8 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates a positive output voltage V_{POS} of 4.6 V and a negative output voltage of –4 V. Both outputs are capable of supplying up to 200 mA of output current.

9.2 Typical Application

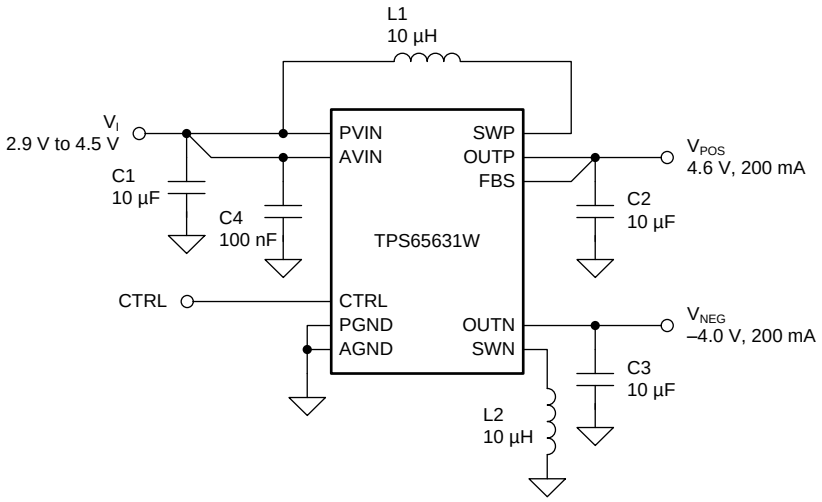


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE
Input voltage range	2.9 V to 4.5 V
Output voltage	V_{POS} = 4.6V, V_{NEG} = –4 V

9.2.2 Detailed Design Procedure

In order to maximize performance, the TPS65631W has been optimized for use with a relatively narrow range of component values, and customers are strongly recommended to use the application circuit shown in Figure 8 with the components listed in Table 3 and Table 4.

9.2.2.1 Inductor Selection

The boost converter and inverting buck-boost converter have been optimized for use with 10 µH inductors, and it is recommended that this value be used in all applications. Customers using other values of inductor are strongly recommended to characterize circuit performance on a case-by-case basis.

Table 3. Inductor Selection(1)

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
L1, L2	10 µH	Toko	DFE252012C-100M
		ABCO	LPP252012-100M
		Taiyo Yuden	MDKK2020T-100M

(1) See *Third-Party Products Disclaimer*

9.2.2.2 Capacitor Selection

The recommended capacitor values are shown in Table 4. Applications using less than the recommended capacitance (e.g. to save PCB area) may experience increased voltage ripple. In general, the lower the output power, the lower the necessary capacitance.

Table 4. Capacitor Selection(1)

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
C1, C2, C3	10 µF	Murata	GRM21BR71A106KE51
C4	100 nF	Murata	GRM21BR71E104KA01

(1) See *Third-Party Products Disclaimer*

9.2.2.3 Stability

Applications using component values that differ significantly from those recommended in Table 3 and Table 4 should be checked for stability over the full range of operating conditions.

9.2.3 Application Curves

The performance shown in the following graphs was obtained using the circuit shown in Figure 8 and the external components shown in Table 3 and Table 4. The output voltage settings for these measurements were V_{POS} = 4.6 V and V_{NEG} = –4 V.

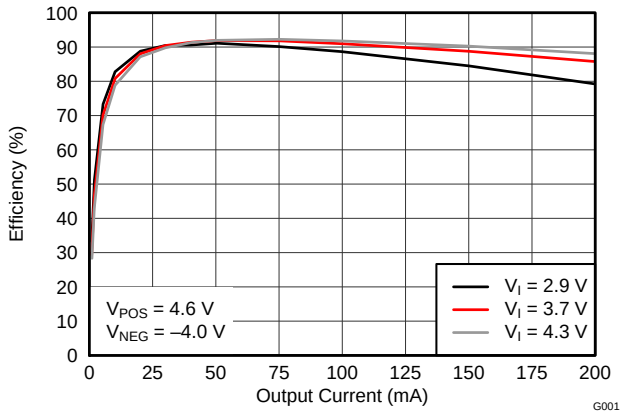


Figure 9. Efficiency vs. Output Current

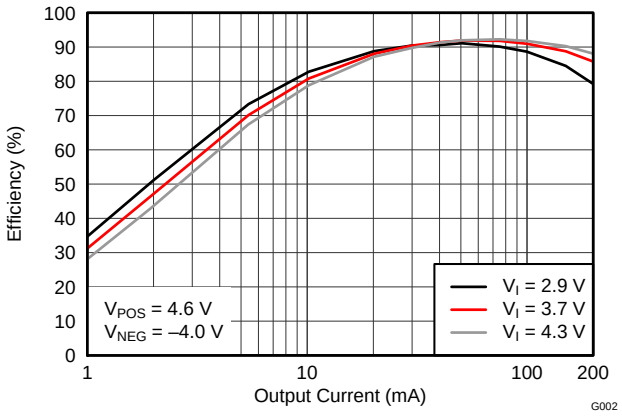


Figure 10. Efficiency vs. Output Current (Log Scale)

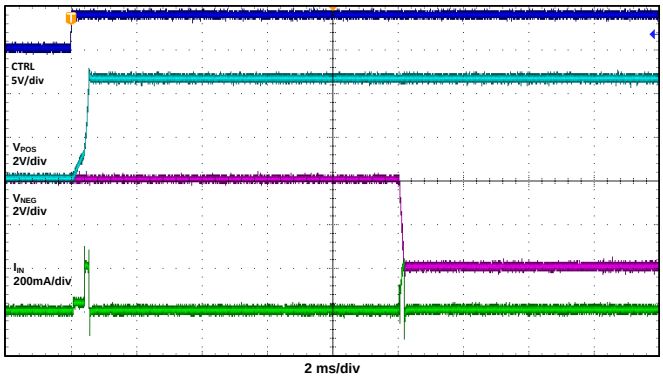


Figure 11. Start-Up Waveforms

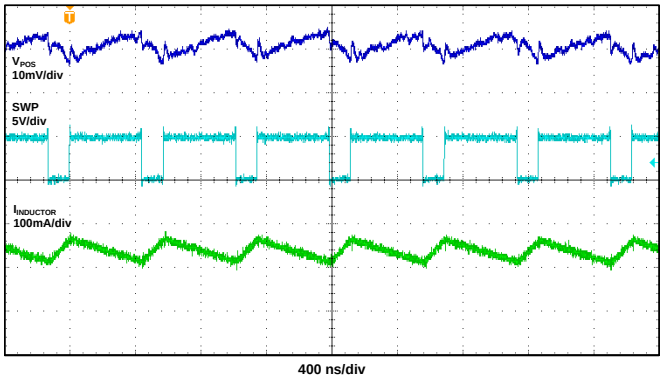


Figure 12. V_{POS} Switch Voltage, Inductor Current and Output Voltage Ripple (I_O = 100 mA)

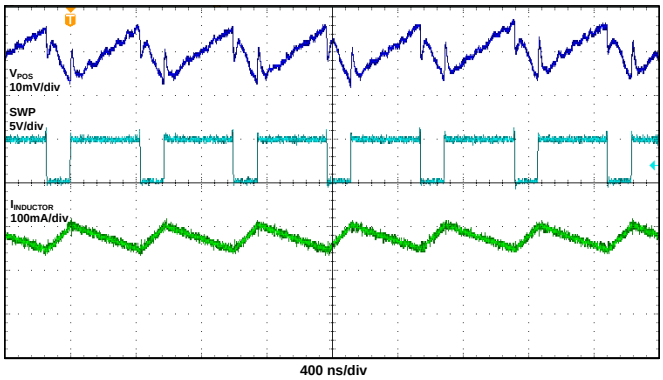


Figure 13. V_{POS} Switch Voltage, Inductor Current and Output Voltage Ripple (I_O = 200 mA)

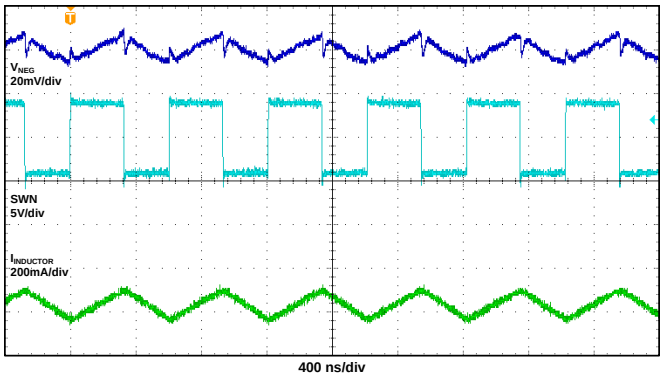


Figure 14. V_{NEG} Switch Voltage, Inductor Current and Output Voltage Ripple (I_O = 100 mA)

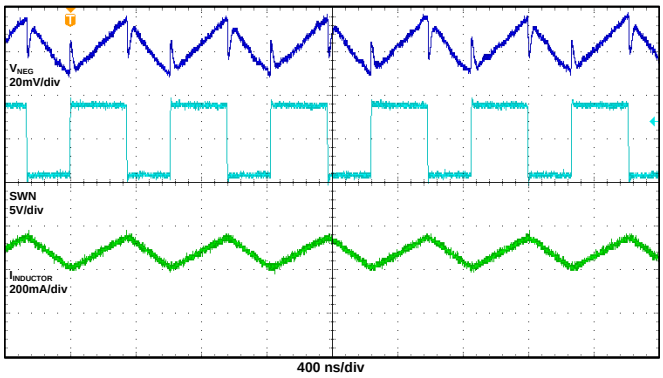


Figure 15. V_{NEG} Switch Voltage, Inductor Current and Output Voltage Ripple (I_O = 200 mA)

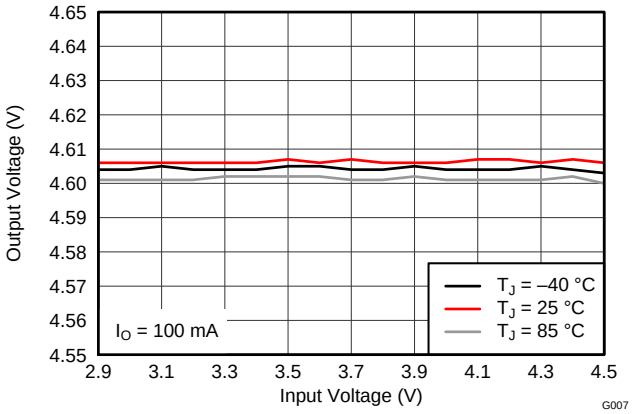


Figure 16. Boost Converter Line Regulation

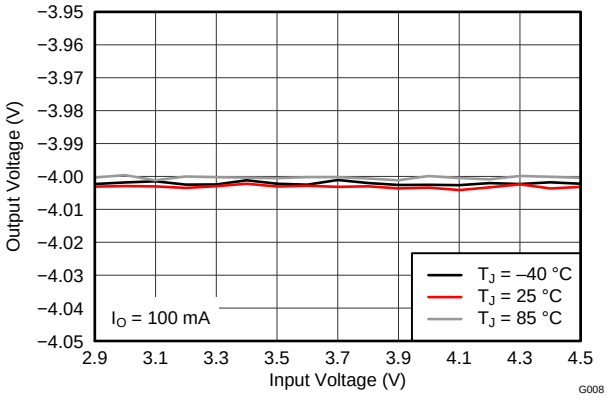


Figure 17. Inverting Buck-Boost Converter Line Regulation

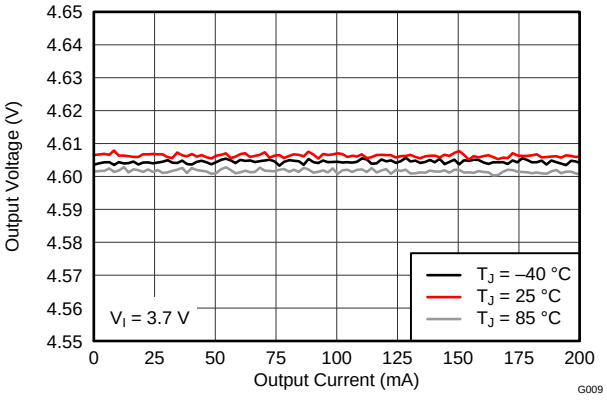


Figure 18. Boost Converter Load Regulation

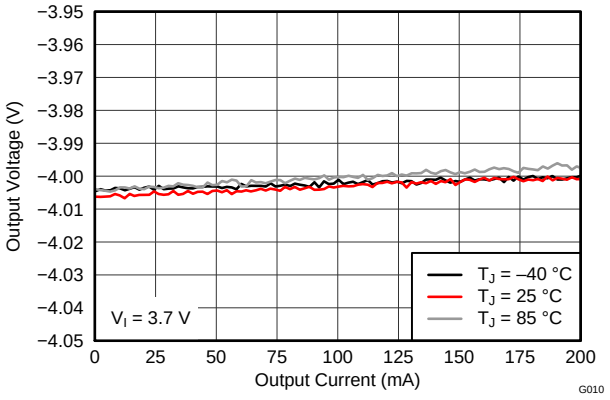


Figure 19. Inverting Buck-Boost Converter Load Regulation

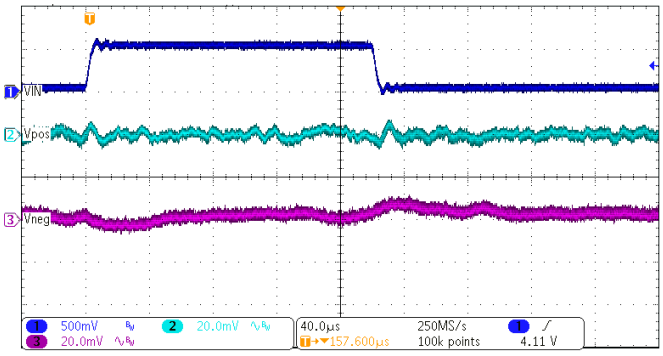


Figure 20. Line Transient Response

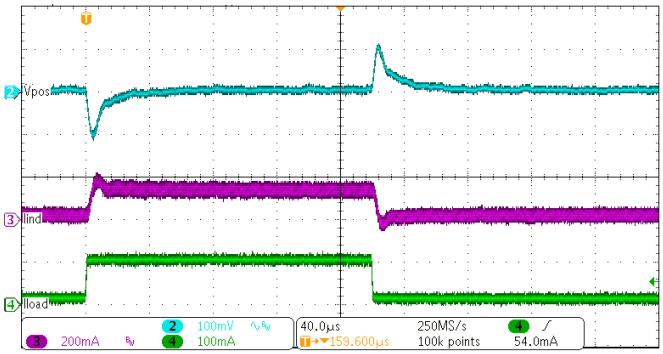


Figure 21. Boost Converter Load Transient Response

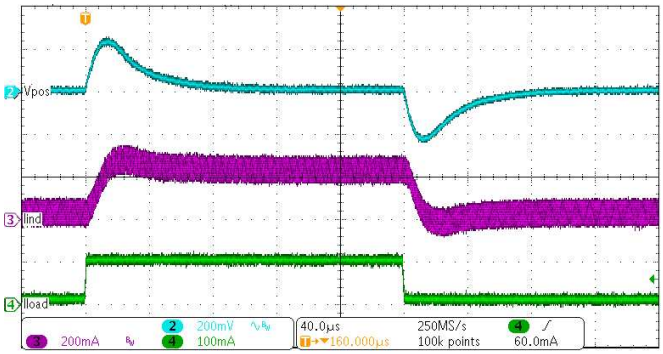


Figure 22. Inverting Buck-Boost Converter Load Transient Response

10 Power Supply Recommendations

The TPS65631W is designed to operate from an input voltage supply range between 2.9 V and 4.5 V. If the input supply is located more than a few centimeters from the TPS65631W additional bulk capacitance may be required. The 10 µF shown in the schematics in this data sheet is a typical choice for this function.

11 Layout

11.1 Layout Guidelines

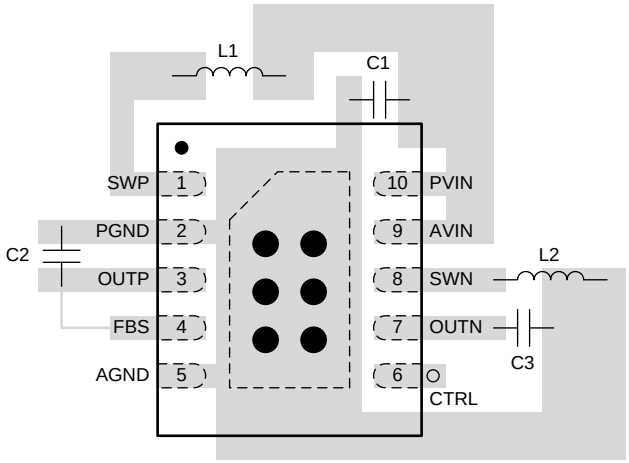
No PCB layout is perfect and compromises are always necessary. However, following the basic principles listed below (in order of importance) should go a long way to achieving good performance:

- Route switching currents on the top layer using short, wide traces. Do not route these signals through vias, which have relatively high parasitic inductance and resistance.
- Use a copper pour on layer 2 as a ground plane and thermal spreader, and connect the thermal pad to it using a number of thermal vias.
- Place C1 as close as possible to pin 10.
- Place C2 as close as possible to pins 2 and 3.
- Place C3 as close as possible to pin 7.
- Place L1 as close as possible to pin 1.
- Place L2 as close as possible to pin 10.
- Use the thermal pad to join AGND and PGND.
- Connect the FBS pin directly to the positive pin of C2, that is, keep this connection separate from the connection between OUTP and C2.

Figure 23 illustrates how a PCB layout following the above principles may be realized in practice.

11.2 Layout Example

Figure 23 shows the above principles implemented for the circuit of Figure 8.



○ Via to signal layer on internal or bottom layer.

● Thermal via to copper pour on internal or bottom layer.

Figure 23. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65631WDSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SJN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

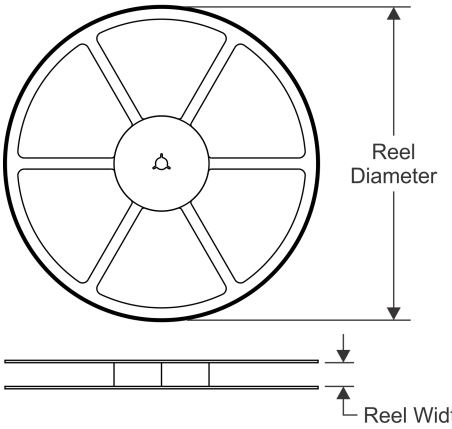
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

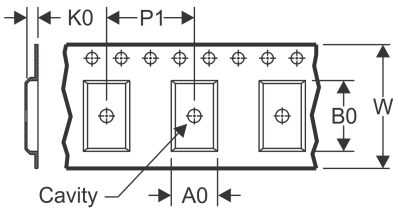
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

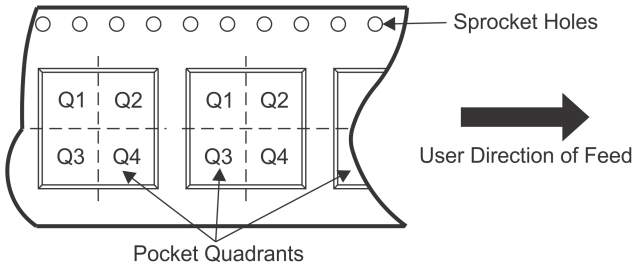


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

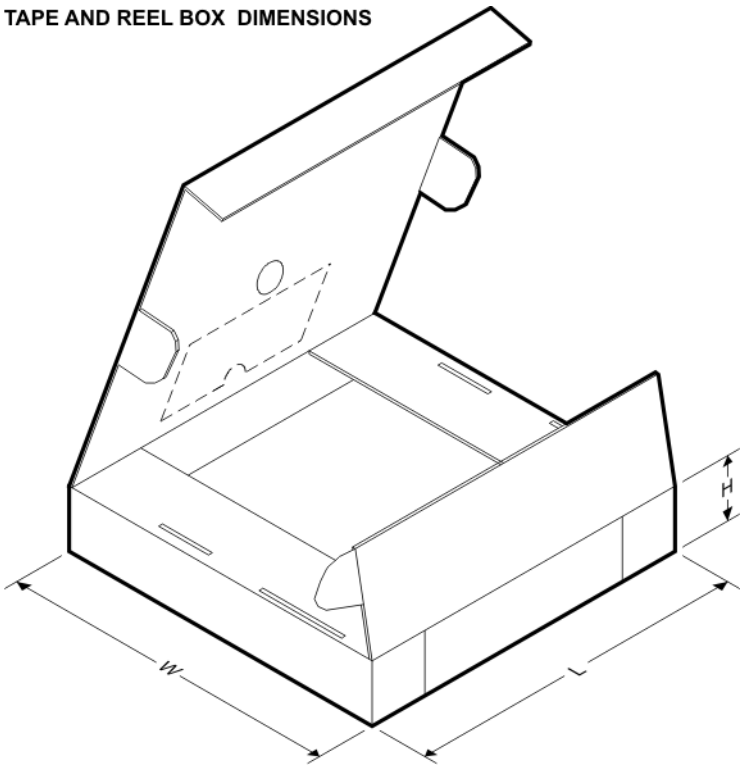
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65631WDSKR	SON	DSK	10	3000	330.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

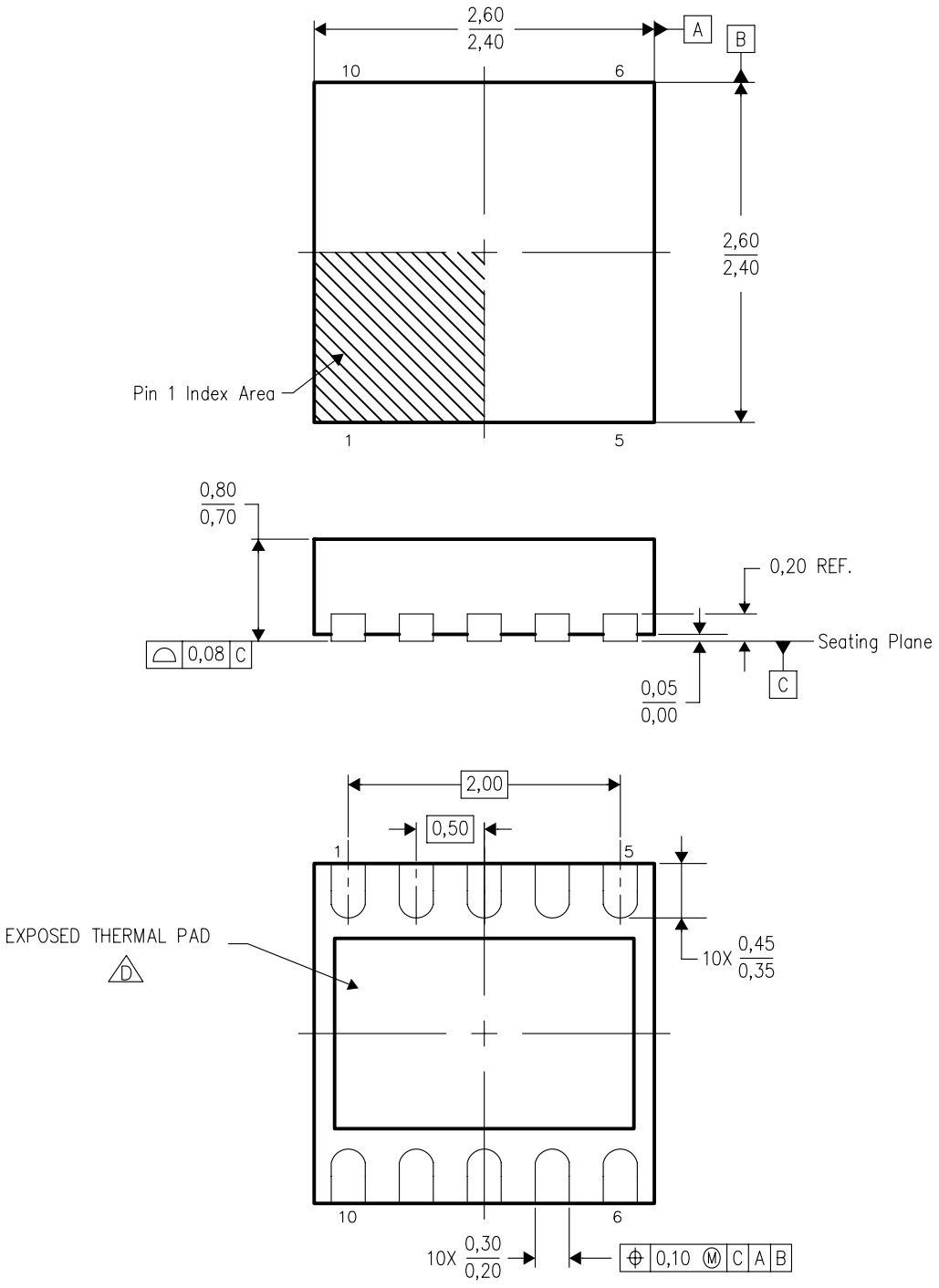
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65631WDSKR	SON	DSK	10	3000	367.0	367.0	35.0

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

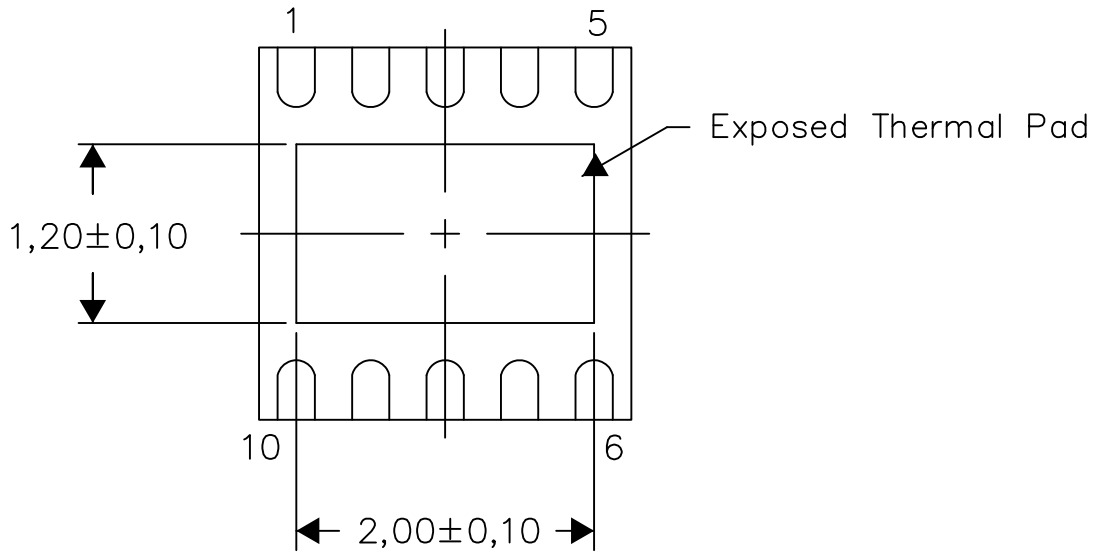
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



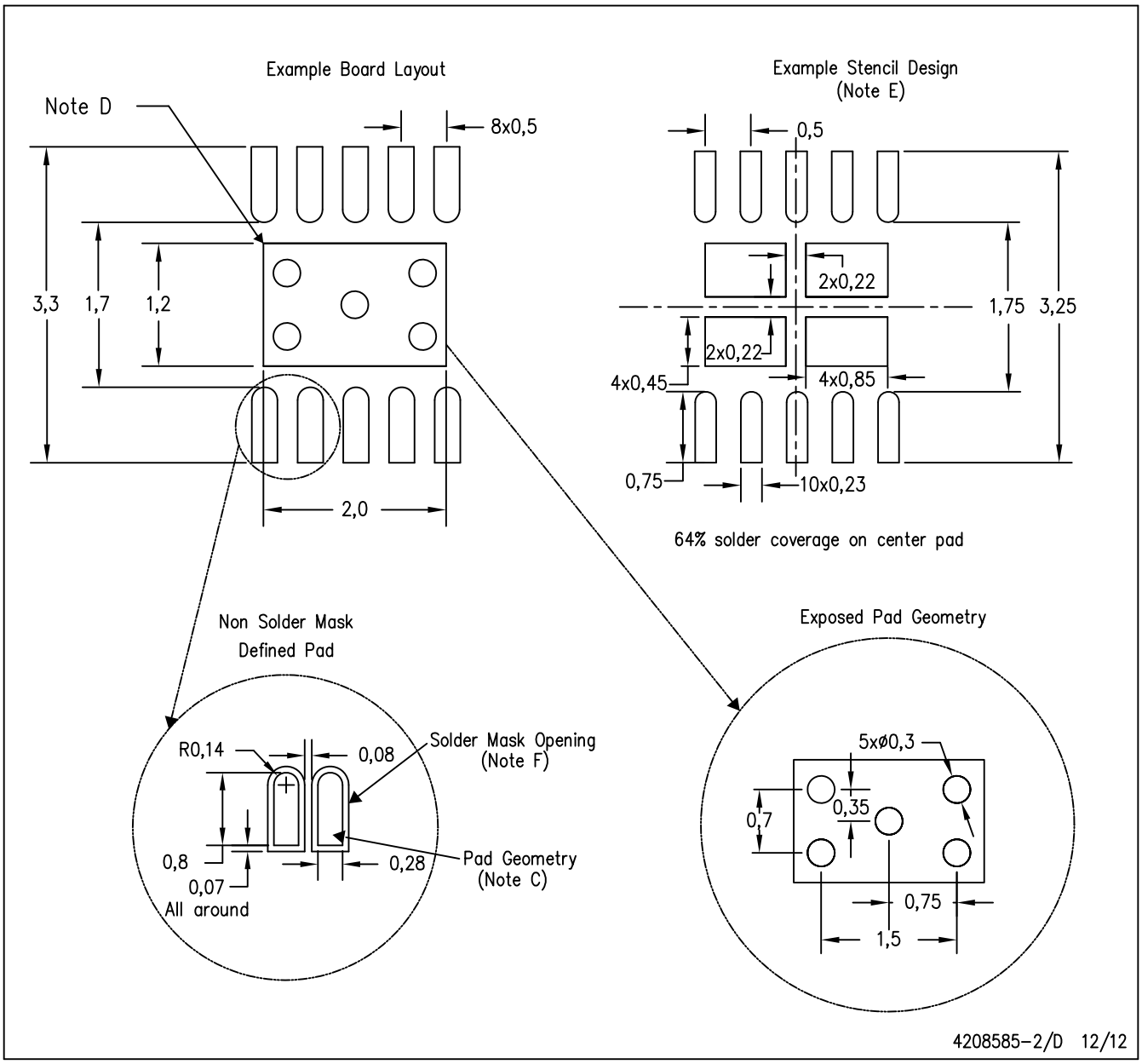
Bottom View

Exposed Thermal Pad Dimensions

4208579–2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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