TPS65400-Q1 4.5- to 18-V Input Flexible Power Management Unit With PMBus/I^{2}C Interface

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Efficiency up to 95% for Each Switching Regulator
- Switching Regulator Specifications:
  - Input Voltage Range: 4.5 to 18 V
  - Vout Range: 0.6 V-90%Vin
  - SW1, SW2 Iout: 4-A Max
  - SW3, SW4 Iout: 2-A Max
- Pre-Bias Startup Algorithm Minimizes Voltage Dip During Startup
- Internal Undervoltage Lockout (UVLO), Overcurrent Protection (OCP), Overvoltage Protection (OVP), and Overtemperature Protection (OTP)
- Thermally-Enhanced 7-mm × 7-mm 48-Pin, 0.5-mm Pitch VQFN Package
- Pin Accessible Features:
  - Adjustable VOUT With External Feedback Resistors
  - Sequencing Control Through Precision Enable Pins for Each Switcher
  - Resistor Adjustable PWM Switching Frequency from 275 kHz to 2.2 MHz
  - Clock Sync Input and Clock Output
  - Soft-Start Delay Through External Capacitor
  - Current Sharing Between SW1 and SW2 and Between SW3 and SW4 Allows Support of Higher Current Needs if Required
- PMBus Runtime Control and Status
  - Runtime Voltage Positioning Through Adjustment of V_{REF}
  - Enable and Disable of Each Switcher
  - Fault and Status Monitoring
- User-Configurable PMBus / I^{2}C Options, Saved in EEPROM
  - Power Supply Turn-On and Turn-Off Sequencing
  - Sequencing can be Based on Fixed Time Delays or PGOOD Dependence
  - Initial Voltage Positioning Through VREF Configuration
  - PWM Frequency Adjustment for Each Switcher
  - Individual PWM Phase Alignment for Each Switcher to Minimize Ripple and Capacitor Size
  - Adjustable Current Limit on Each Regulator Enables Size and Cost Optimization of Inductors
  - Soft-Start Time

2 Applications

- Qualified for Automotive Applications
- Small Cellular Base Stations (BTS) (for Example: Picocells and Microcells); Macro BTS (Using Multiple PMUs)
- Power over Ethernet (PoE) Powered Communications Infrastructure Equipment
- Powering DSP and MCUs
- Industrial and Factory Automation
- Systems Requiring Small Form Factor, High-Efficiency, High-Ambient Operating Temperature, and Flexible Power Management

3 Description

The TPS65400-Q1 is an integrated PMU optimized for applications requiring small form factor and high power conversion efficiency, enabling small space-constrained equipment with high ambient operating temperature without cooling. It provides high-power efficiency at a system level by enabling a single stage conversion from an intermediate distribution bus with an optimized combination of regulators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65400-Q1	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

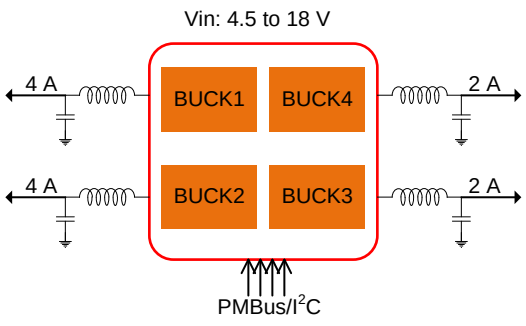


Table of Contents

4 Revision History

DATE	REVISION	NOTES
July 2015	*	Initial release.

5 Description (continued)

TPS65400-Q1 implements a PMBus-I^{2}C-compatible digital interface. It helps Core Chip optimize system performance by runtime changing regulated voltage, power sequence, phase interleaving, operating frequency, read back operating status, and so forth.

The TPS65400-Q1 consists of four high-current buck switching regulators (SW1, SW2, SW3, and SW4) with integrated FETs. The switching power supplies are intended for powering high-current digital circuits such as the processor, FPGA, ASIC, memory, and digital I/Os. SW1 and SW2 support 4 A each, and SW3 and SW4 support 2 A each. Each regulator's switching frequency is independently adjustable up to 2.2 MHz.

Current limit programmability on each switcher enables optimization of inductor ratings for a particular application configuration not requiring the maximum current capability.

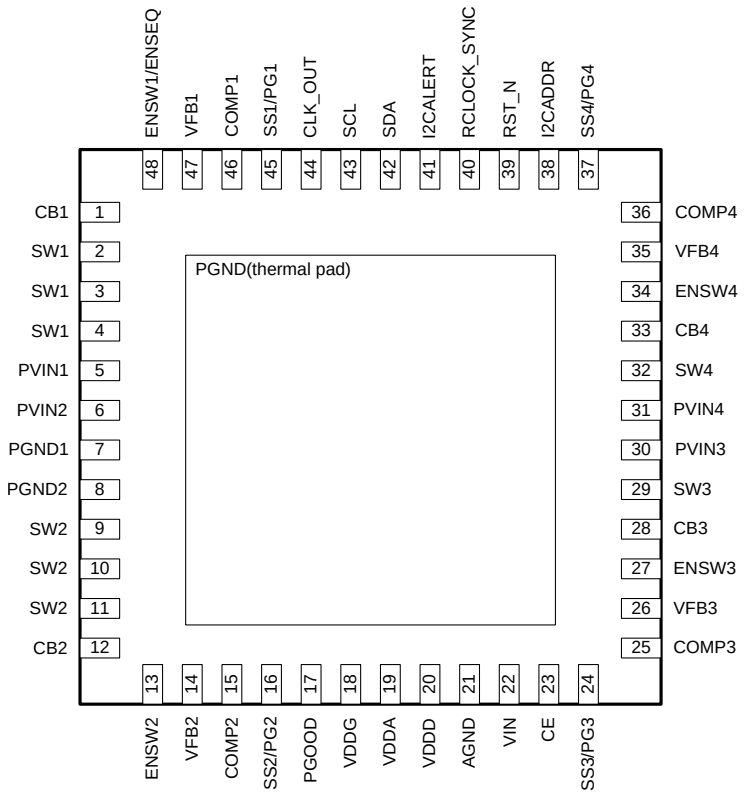
The TPS65400-Q1 can be powered from a single-input voltage rail between 4.5 and 18 V, making it suitable for applications running off a 5- or 12-V intermediate power distribution bus.

Sequencing requirements can be met using the individual enable terminals or by programming the sequence through the I^{2}C bus into the onboard EEPROM. Output voltages can be set through external resistor networks and VREF can be programmed from 0.6 to 1.87 V in 10-mV steps. All control and status info can be accessed through a PMBus-compatible I^{2}C bus.

The TPS65400-Q1 provides a high level of flexibility for monitoring and control through the I^{2}C bus while providing the option of programmability through the use of external components and voltage levels for systems not using I^{2}C.

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



A. Thermal pad must be soldered to PCB as SW3 and SW4 power ground

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
CB1	1	Bootstrap pin for high-side MOSFET gate drive for SW1
SW1	2	Switch pin for SW1
	3	
	4	
PVIN1	5	Power input for buck switching regulator SW1
PVIN2	6	Power input for SW2
PGND1	7	Power ground for buck converters
PGND2	8	Power ground for buck converters
SW2	9	Switch pin for SW2
	10	
	11	
CB2	12	Bootstrap pin for SW2 high-side MOSFET gate drive
ENSW2	13	Enable input pin for SW2. Active high. 2-µA internal pullup current is inside.
VFB2	14	Feedback input pin for SW2
COMP2	15	Compensation pin for external compensation network for SW2. Pulling this line high to VDDD configures the SW1 controller to control both SW1 and SW2.
SS2/PG2	16	Soft-start for SW2 (default). A capacitor is used to set the startup time. This pin can also be reconfigured through I^2C to display the PGOOD2 signal instead.
PGOOD	17	Default PGOOD signal is for all switchers. It can be changed according to *(D2h) PIN_CONFIG_00*. If all switchers are disabled, PGOOD is low.
VDDG	18	Supply for gate drives. Bypass locally to PGND.
VDDA	19	Output of internal regulator for analog controls.
VDDD	20	3.3-V output of internal regulator digital controls
AGND	21	Ground connection for analog controls
VIN	22	Analog V_{IN}. Power input pin for VDDD, VDDA, and VGATE subregulator power
CE	23	Chip enables. Internal pull-up current will default to high if the pin is left floating. Connect to an open-drain output to pull low to disable. Driving with a push-pull output is not recommended. When low, internal regulators are shutdown to minimize power, and functionsa are disabled. Configuration is reloaded from EEPROM as part of the power-up sequence when CE goes high.
SS3/PG3	24	Soft-start for SW3 (default). A capacitor is used to set the startup time. This pin can also be reconfigured through I^2C to display the PGOOD3 signal instead.
COMP3	25	Compensation pin for external compensation network for SW3
VFB3	26	Feedback input pin for SW3
ENSW3	27	Enable input pin for SW3. Active high. 2-µA internal pullup current is inside.
CB3	28	Bootstrap pin for SW3 high-side MOSFET gate drive
SW3	29	Switch pin for SW3. Max rated output current is 2 A.
PVIN3	30	Power input for buck switching regulator SW3
PVIN4	31	Power input for SW4
SW4	32	Switch pin for SW4. Max rated output current is 2 A.
CB4	33	Bootstrap pin for SW4 high-side MOSFET gate drive
ENSW4	34	Enable input pin for SW4. Active high. 2-µA internal pullup current is inside.
VFB4	35	Feedback input pin for SW4
COMP4	36	Compensation pin for external compensation network for SW4. Pulling this line high to VDDD configures the SW3 controller to control both SW3 and SW4.
SS4/PG4	37	Soft-start for SW4 (default). A capacitor is used to set the startup time. This pin can also be reconfigured through I^2C to display the PGOOD4 signal instead
I2CADDR	38	Select I^2C address with resistor to AGND
RST_N	39	Reset of digital logic. When low, all switchers are disabled. Configuration is reloaded from EEPROM when RESET_N is deasserted.
RCLOCK_SYNC	40	Resistor for setting master clock frequency from 275 kHz to 2.2 MHz or for clock sync

Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
I2CALERT	41	Open-drain output that is pulled low for 200 µs when a timeout condition is detected by the I^2C watchdog on either SDA or SCL.
SDA	42	Data input/output pin for I^2C bus
SCL	43	Clock input pin for I^2C bus
CLK_OUT	44	Clock output signal. Open-collector output, requires pull up.
SS1/PG1	45	Soft-start for SW1 (default). A capacitor is used to set the startup time. This pin can also be reconfigured through I^2C to display the PGOOD1 signal instead.
COMP1	46	Compensation pin for external compensation network for SW1
VFB1	47	Feedback input pin for SW1
ENSW1/ENSEQ	48	Enable input pin for SW1. Active high. 2-µA internal pullup current is inside.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	PVIN1, PVIN2, PVIN3, PVIN4, VIN	–0.3	20	V
	CB1, CB2, CB3, CB4 referenced to SWx	–0.3	7.5	
	ENSW1, ENSW2, ENSW3, ENSW4, SCL, SDA, CLK_OUT, VFB1, VFB2, VFB3, VFB4, RST_N, SCL, SDA, I2CALERT, CLK_OUT, I2CADDR, RCLOCK_SYNC	–0.3	VDDD or 3.6	
	SW1, SW2, SW3, SW4	–1	20	
	VDDA, VDDG	–0.3	7.5	
	PGOOD, SS1/PG1, SS2/PG2, SS3/PG3, SS4/PG4, COMP1, COMP2, COMP3, COMP4, CE	–0.3	VDDA or 7.5	
	VDDD	–0.3	3.6	
$T_{J(max)}$	Junction temperature		150	°C
	Maximum lead temperature (soldering, 10 s)		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN1, VIN2, VIN3, VIN4	Input voltage range	4.5	18	V
I_{OUT1}, I_{OUT2}	Load current	0	4	A
I_{OUT3}, I_{OUT4}	Load current	0	2	A
V_{FB1}, V_{FB2}, V_{FB3}, V_{FB4}	Voltage feedback	0.6	1.87	V
T_J	Junction temperature range	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS65400-Q1 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 12 V, F_{SW} = 500 kHz, T_J = –40°C to 125°C, typical values are at T_J = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHER 1 AND SWITCHER 2						
I_{limit1}, I_{limit2}	SW1, SW2 high-side current limit adjustment range		2		6	A
$I_{limit\text{-}accuracy}$	Accuracy to nominal current limit value	I_{limit} = 4 A, 5 A, 6 A	–25%		25%	
Rdson HS	SW1, SW2 HS Rds(on)			66		mΩ
Rdson LS	SW1, SW2 LS Rds(on)			42		mΩ
SWITCHER 3 AND SWITCHER 4						
I_{limit3}, I_{limit4}	SW3 and SW4 current limit		0.5		3	A
$I_{limit\ accuracy}$	Accuracy to nominal current limit value	I_{limit} = 1 A, 2 A, 3 A	–25%		25%	
Rdson HS	SW3 and SW4 HS Rds(on)			120		mΩ
Rdson LS	SW3/4 LS Rds(on)			90		mΩ
FEEDBACK AND ERROR AMPLIFIERS FOR SW1 – SW4						
VFB	Accuracy	V_{REF} = 1 V	–1%		1%	
V_{REFn}	Error amplifier reference voltage	Default value		800		mV
V_{REF_STEP}	I^2C programmable V_{REF} step size			10		mV
Gm	Error amplifier transconductance		95	133	165	µS
I_{sink}	Sink			12		µA
I_{source}	Source			12		µA
PWM SWITCHING CHARACTERISTICS						
Phase_err12 (1)	Phase error between SW1 and SW2	F_{sw} = 1.1 MHz		5º		
Phase_err34 (1)	Phase error between SW3 and SW4	F_{sw} = 1.1 MHz		5º		
F_{sw}	Resistor-configurable PWM switching configuration		275		2200	kHz
$F_{sw\text{-}accuracy}$	PWM switching frequency accuracy	R_{OSC} = 165 kΩ (F_{sw} = 1.1 MHz)	–10%		10%	
V_{rclock_sync}	Voltage reference for RCLOCK_SYNC			0.8		V
t_{ON_min}	Lower duty cycle limit			80	150	ns
t_{OFF_min}	Minimum off-time limit (constrains the maximum achievable duty cycle)			150		ns
CLOCK SYNC						
V_H_{SYNC}	High signal threshold		2.6			V
V_L_{SYNC}	Low signal threshold				1	V
I_{CLKOUT}	Max current sink/source for CLK_OUT			2		mA
t_{min_SYNC}	Minimum detectable time for sync pulse				150	ns
F_{SYNC}	Frequency synchronization range		275		2200	kHz
T_{SYNC_DELAY}	Delay between input pulse to RCLOCK_SYNC and rising edge of CLK_OUT and PWM output			20		ns
TIMING CHARACTERISTICS						
$t_{restart}$	Delay for restart during repeated OCP condition			20		ms
INTERNAL REGULATORS AND UVLO						
V_{DDA}	Internal subregulator output	V_{in} > 6.6 V		6.1		V
		4.5 V < V_{in} 6.6 V		V_{in} – 0.1		
V_{DDD}	Output of internal subregulator			3.2		V
V_{DDG}	Output of Internal regulator for gate drivers	V_{in} > 6.6 V		6.1		V
		4.5 V < V_{in} 6.6 V		V_{in} – 0.1		

(1) Specified by design.

Electrical Characteristics (continued)

V_{IN} = 12 V, F_{SW} = 500 kHz, T_J = –40°C to 125°C, typical values are at T_J = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VIN}	Quiescent non-switching, no load current	CE high, V_{FB} >> V_{REF}, (no switching)		8		mA
I_{SD}	Quiescent shutdown current	CE low		12	27	µA
V_{IN_UVLO}	Input voltage UVLO	Rising		4.25	4.48	V
V_{IN_UVLO}	Input voltage UVLO	Falling	3.4	3.75		V
PGOOD, ENSWx, RST_N, SSx, $\overline{PG}$						
R_L_{PGOOD}	Resistance of PGOOD outputs when low			500		Ω
V_OL_{PGOOD}	Logic output low voltage	I_OL = 100 µA			0.1	V
I_{SS}	Soft-start current		4.1	5.6	7.3	µA
V_{EN_H}	Enable logic high threshold (for ENSW1, ENSW2, ENSW3, ENSW4)	V_{EN} rising	1.12	1.20	1.28	V
V_{EN_L}	Enable logic low threshold (for ENSW1, ENSW2, ENSW3, ENSW4)	V_{EN} falling	0.97	1.07		V
V_{EN_HYS}	Enable hysteresis (for ENSW1, ENSW2, ENSW3, ENSW4)			130		mV
I_{EN}	ENSWx pin pullup current	V_{EN} = 0		2		µA
I_{CE}	CE pin pullup current	V_{CE} = 0		2		µA
V_{IH_CE}	Logic input high for CE		1.3			V
V_{IL_CE}	Logic input low CE				0.4	V
V_{IH_RSTN}	Logic input high RST_N		1.3			V
V_{IL_RSTN}	Logic input low RST_N				0.4	V
I^2C MODULE (SDA, SCL, I2CALERT, I2CADDR)						
V_IL_{I2C}	Logic input low SCL, SDA				0.8	V
V_IH_{I2C}	Logic input high for SCL, SDA		2.1			V
R_L_{I2C}	ON resistance of I^2C pins (SDA,SCL,I2CALERT) to GND	I2CALERT = 1		85		Ω
V_OL_{I2C}	Logic output low voltage for SCL,SDA,I2CALERT pins	I_OL = 350 µA			0.1	V
I_{LEAK}	Input leakage current	SDA, SCL = 3.3 V			1	µA
$I_{I2CADDR}$	Source current of I2CADDR pin	VDDD = 3.3 V, VIN > 4.5 V		20		uA
$t_{TIMEOUT}$	Timeout detection on SDA or SCL low			30		ms
$t_{TIMEOUT\_PULSE}$	Duration of timeout pulse on I2CALERT			200		µs
FAULTS						
T_{TSD} (2)	Thermal shutdown threshold			160		ºC
$T_{TSD\_restart}$ (2)	Thermal shutdown hysteresis			20		ºC
V_{FB_OVP}	OVP threshold rising (fault latched, PGOOD asserted)	0.6V < V_{REF} < 1.87 V		111		% of V_{REF}
	OVP threshold falling (fault cleared, PGOOD deasserted)	0.6 V < V_{REF} < 1.87 V		104		% of V_{REF}
$t_{OVPSDOWN}$	Time after OVP before protection activation and PGOOD fall			55	95	µs
$V_{FB\ UVP}$	Undervoltage threshold (PGOOD deasserted)	0.6 V < V_{REF} < 1.87 V		92		% of V_{REF}
	Undervoltage Threshold (PGOOD asserted)	0.6 V < V_{REF} < 1.87 V		83		% of V_{REF}
$t_{UVPSDOWN}$	Time after UVP before PGOOD fall			55	95	µs

(2) Specified by lab validation.

7.6 System Characteristics

The following specification table entries are specified by the design (component values provided in the typical application circuit are used). These parameters are not specified by production testing. Minimum and Max values apply over the full operating ambient temperature range (–40°C ≤ T_J ≤ 125°C), over the V_{IN} range = 5 to 12 V, and I_{OUT} range unless otherwise specified. L = 3.3 µH, DCR = 10.4 mΩ, V_{OUT} = 1.2 V, 1% FB resistor.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LINEREG}$	Line regulation			0.1		%/V
$V_{LOADREG}$	Load regulation			0.1		%/A
t_r	VOUT step duration (t_r)	For 50-mV step		30		µs
t_s	VOUT step settling time (t_s)	For 50-mV step		30		µs
V_{OVUV}	VOUT step overshoot/undershoot	For 50-mV step		6		mV
	Efficiency (SW1 and SW2)	Vin = 5 V, Vo = 1.2 V, Iout = 4 A, f_{sw} = 500 kHz		77%		
		Vin = 12 V, Vo = 1.2 V Iout = 4 A, f_{sw} = 500 kHz		76%		
	Efficiency (SW3 and SW4)	Vin = 5 V, Vo = 1.2 V, Iout = 2 A, f_{sw}= 500 kHz		77%		
		Vin = 12 V, Vo = 1.2 V Iout = 2 A, f_{sw} = 500 kHz		74%		
$IOUT_{match}$	Average ((1)) current sharing accuracy (SW1 and SW2, SW3 and SW4)	I_{load} = I_{OUTmax}		20%		
IPK_{match}	Peak current ((2)) sharing accuracy (SW1 and SW2, SW3 and SW4)	I_{load} = I_{OUTmax}			20%	
t_{acc}	Timing accuracy for delays and restarts		–10%		10%	
t_{reset_delay}	Time after RSTn or CE is released for power sequence to begin	Default value		1		ms
$t_{reset\_delay\_max0}$	Minimum delay after reset is released for power sequence to begin	t_{reset_delay} set to 0 ms			1.1	ms

(1) Average current sharing accuracy is highly dependent on the matching of the inductor and capacitor.
(2) Peak current sharing accuracy refers to the max inductor current in each phase.

7.7 Operational Parameters

Values recommended that ensure proper system behavior

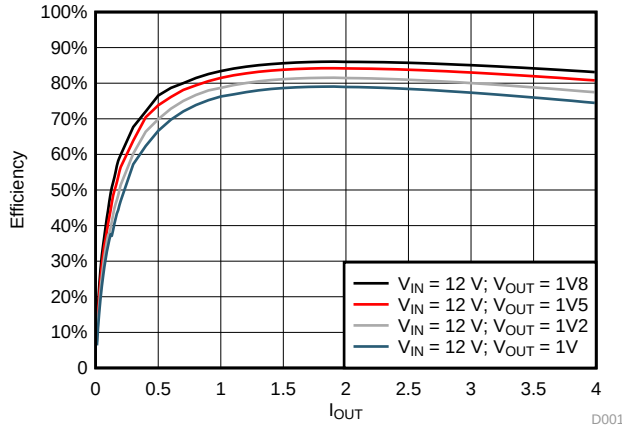
PARAMETER		MIN	TYP	MAX	UNIT
C_A	Stabilization capacitor to be connected to VDDA		4.7		µF
C_D	Stabilization capacitor to be connected to VDDD		3.3		µF
C_G	Stabilization capacitor to be connected to VDDG		10		µF
Vin1, Vin2, Vin3, Vin4	SW1 to SW4 input voltage	4.5		18	V
Vout1, Vout2, Vout3, Vout4	SW1 to SW4 output voltage	0.6		90% of Vin	V

7.8 Package Dissipation Ratings(1)

PACKAGE	$R_{\theta JA}$ (°C/W)	T_A = 25°C	T_A = 55°C	T_A = 85°C
RGZ	29.8	4.5 W	3.14 W	1.77 W

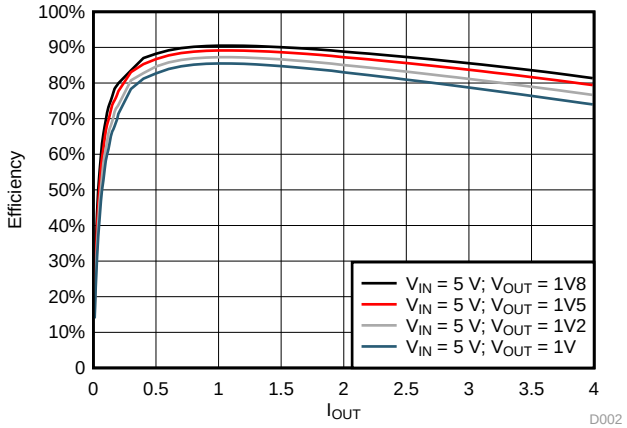
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.9 Typical Characteristics: System Efficiency



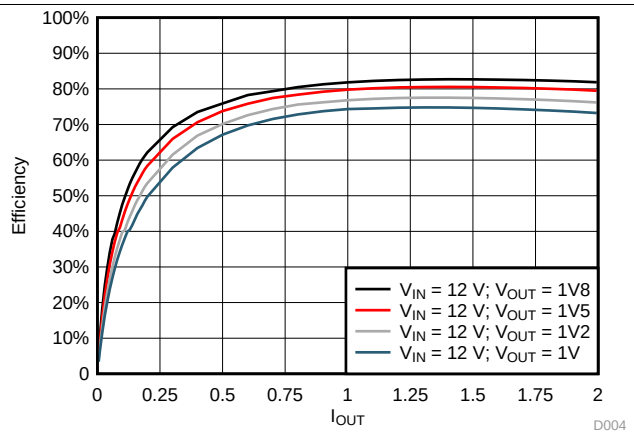
With 500 kHz and XAL6060-472 4.7-µH, 13.2-mΩ inductor

Figure 1. Buck1 and Buck2 Power Efficiency, V_{IN} = 12 V



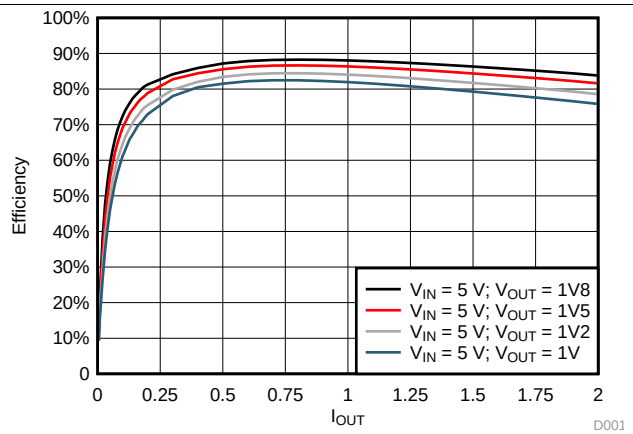
With 500 kHz and XAL6060-472 4.7-µH, 13.2-mΩ inductor

Figure 2. Buck1 and Buck2 Power Efficiency, V_{IN} = 5 V



With 500 kHz F_{SW} and 4.7-µH, 34-mΩ inductor

Figure 3. Buck3 and Buck4 Power Efficiency, V_{IN} = 12 V



With 500 kHz F_{SW} and 4.7-µH, 34-mΩ inductor

Figure 4. Buck3 and Buck4 Power Efficiency, V_{IN} = 5 V

8 Detailed Description

8.1 Overview

The TPS65400-Q1 is an integrated PMU optimized for applications that require small form factor and high-power conversion efficiency enabling small space-constrained equipment with high-ambient operating temperature without cooling. It provides high-power efficiency at a system level by enabling a single-stage conversion from an intermediate distribution bus with an optimized combination of regulators.

The TPS65400-Q1 consists of four high-current buck-switching regulators (SW1, SW2, SW3, and SW4) with integrated FETs. The switching power supplies are intended for powering high-current digital circuits such as the processor, FPGA, ASIC, memory, and digital I/Os. SW1 and SW2 support 4 A each, and SW3 and SW4 support 2 A each. Each regulator's switching frequency is independently adjustable up to 2.2 MHz.

Current limit programmability on each switcher enables optimization of inductor ratings for a particular application configuration not requiring the maximum current capability.

The TPS65400-Q1 can be powered from a single-input voltage rail between 4.5 and 18 V, making it suitable for applications running off a 5- or 12-V intermediate power distribution bus.

Sequencing requirements can be met using the individual enable pins or by programming the sequence through the I^2C bus into the onboard EEPROM. Output voltages can be set through external resistor networks and VREF can be programmed from 0.6 to 1.87 V in 10-mV steps. All control and status info can be accessed through a PMBus-compatible I^2C bus.

The TPS65400-Q1 provides a high level of flexibility for monitoring and control through the I^2C bus while providing the option of programmability through the use of external components and voltage levels for systems not using I^2C.

8.2 Functional Block Diagrams

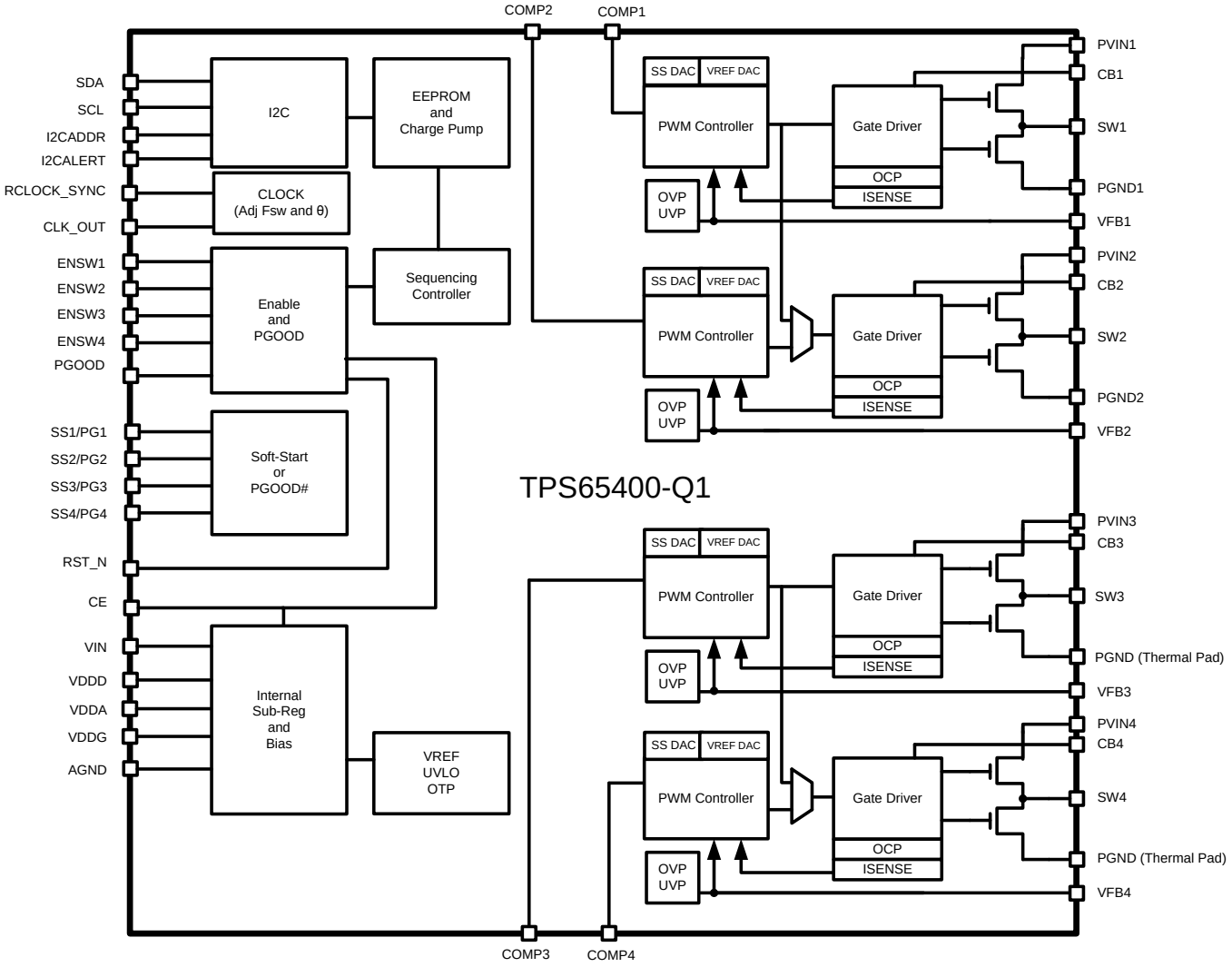
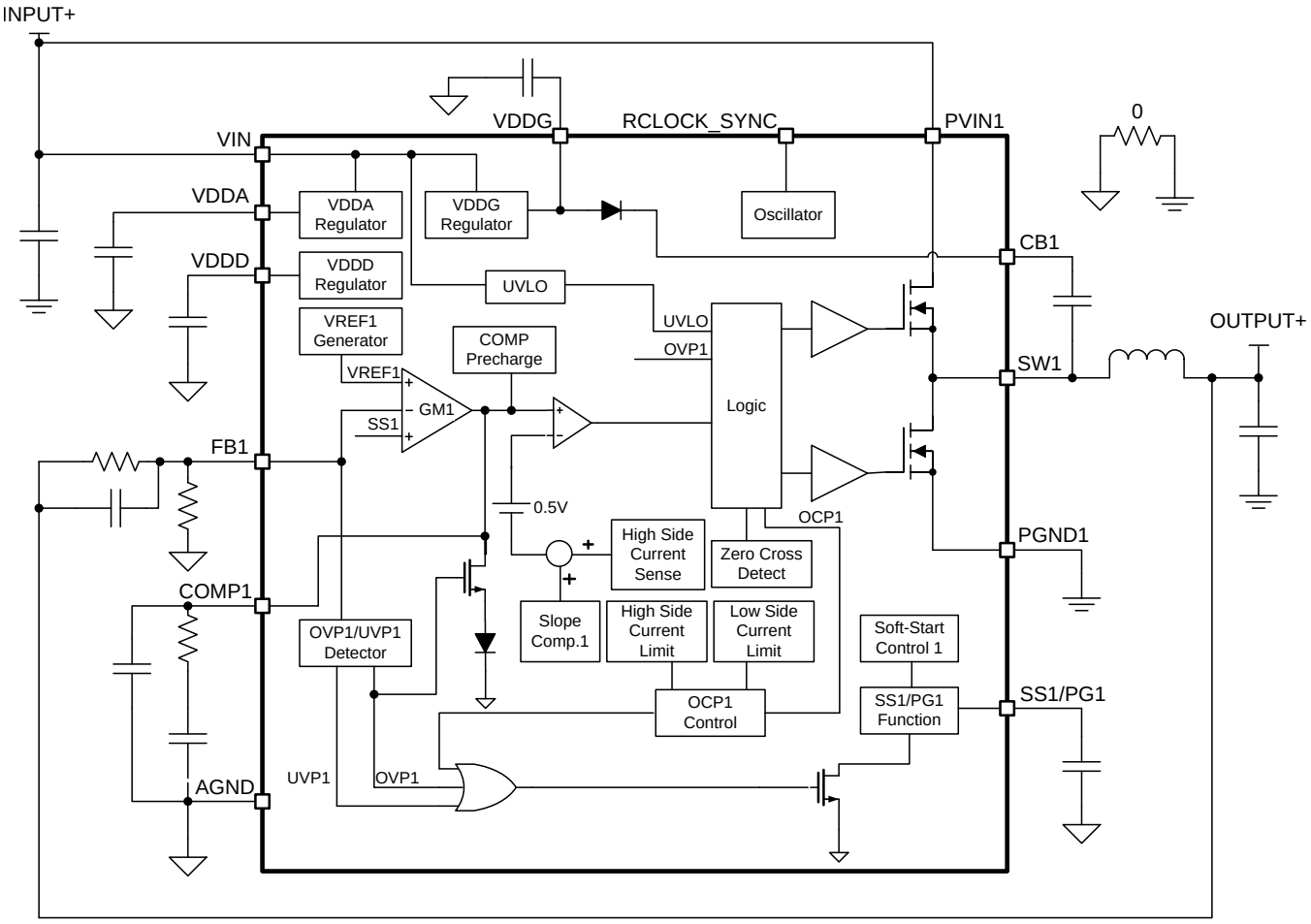


Figure 5. TPS65400-Q1 Functional Block Diagram

Functional Block Diagrams (continued)



A. All other switchers follow the same pattern

Figure 6. Simplified Control Block Diagram for Switcher1

8.3 Feature Description

8.3.1 Startup Timing and Power Sequencing

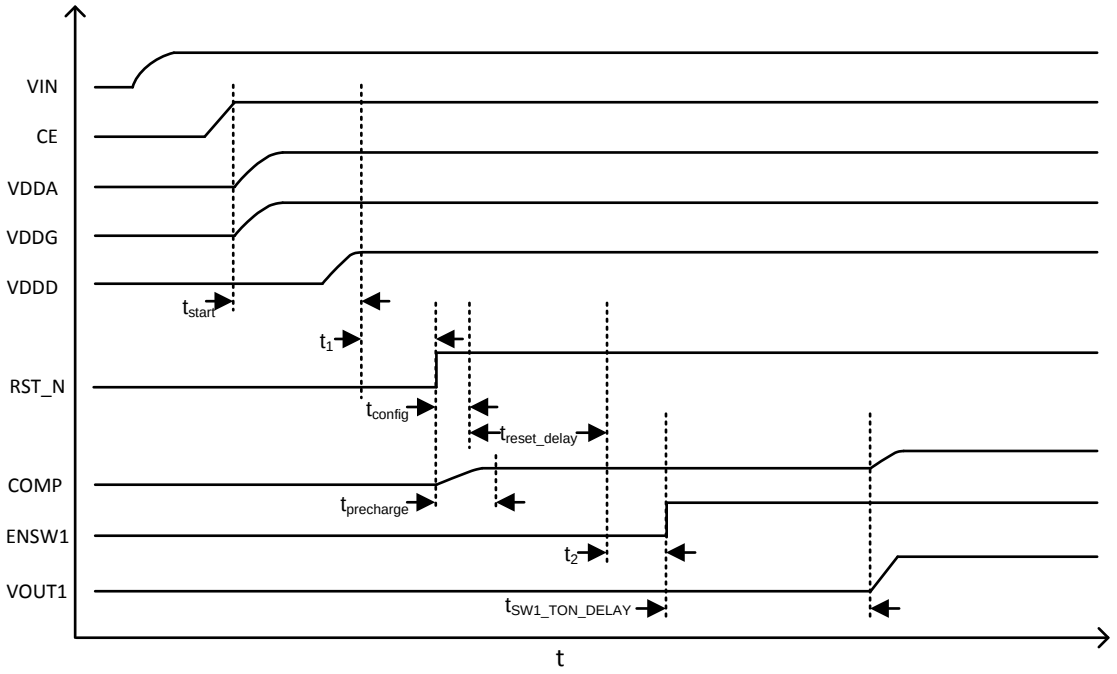
8.3.1.1 Startup Timing

Figure 7 shows the startup timing of the TPS65400-Q1. Upon power-up or the rising edge of CE, the internal power rails VDDA, VDDG, and VDDD startup during the time labeled t_{start}. Following t_{start}, a delay of t_1 follows (which is defined by the user through the timing of RST_N). During time t_{start} and t_1, the COMP terminal is internally discharged through a 1-kΩ resistor. At the rising edge of RST_N, the TPS65400-Q1 begins two actions:

1. The TPS65400-Q1 begins its precharge of the COMP terminal (indicated by $t_{precharge}$). The length of $t_{precharge}$ needed to precharge the COMP terminal depends on the time constant of the R and C components. The internal precharge voltage source remains on even during normal operation, preventing the COMP terminal from falling below 0.6 V except during faults (OVP, OCP, and so forth).
2. The TPS65400-Q1 begins its configuration sequence (indicated by t_{config}), and loads parameters from the EEPROM. Parameters to be set include Vout, switching frequency, soft-start timing, and current limit.

Feature Description (continued)

After t_{config} is complete, t_{reset_delay} begins. The length of t_{reset_delay} is user-configurable through PMBus register DCh. After t_{reset_delay} is complete, the TPS65400-Q1 begins its startup sequence. The startup sequence is EEPROM-configurable, so any of the four switchers could be the first to startup with a configurable delay. In this particular example, SW1 is configured to startup first after a delay of $t_{SW1\_TON\_DELAY}$, which is configurable through PMBus register *(DDh) TON_TOFF_DELAY*.



A. PGOOD1 and ENSW2 are tied together externally, and t_{ON_DELAY1} and t_{ON_DELAY2} are configured through PMBus.

Figure 7. Timing Showing Startup from CE

To summarize, the length of time from rising edge of CE to soft-start of the first switcher in the sequence is:

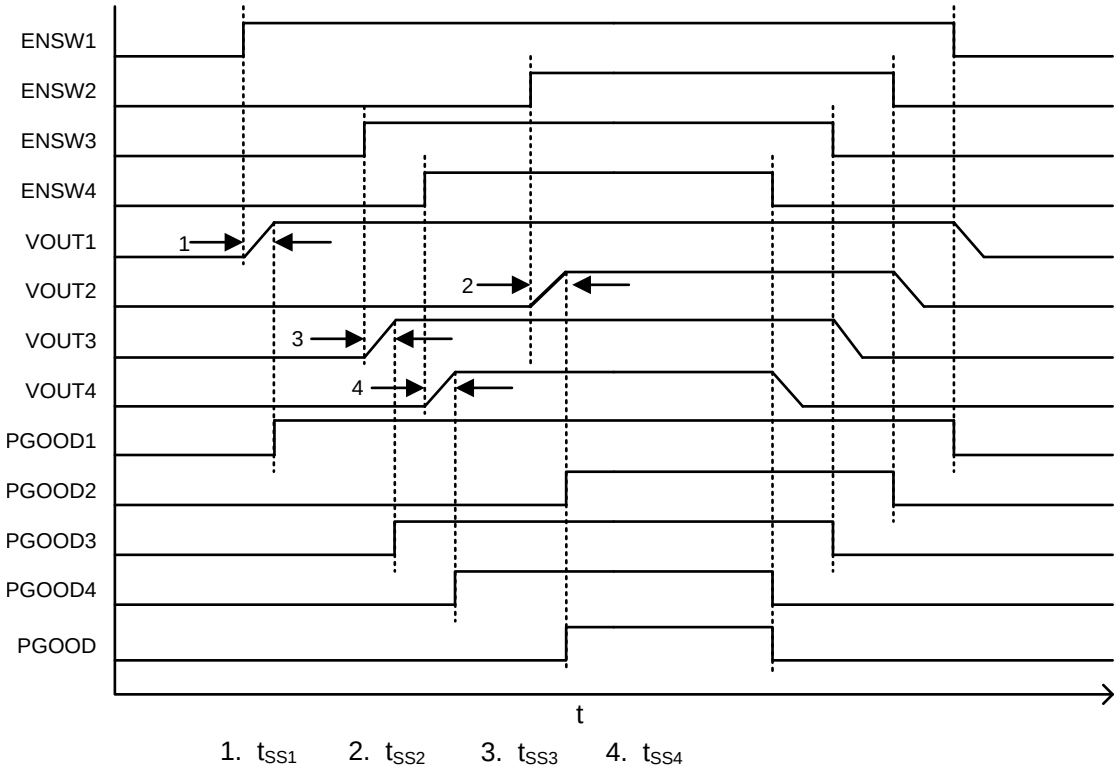
$$t_{CE\_to\_SS} = t_{start} + t_1 + t_{config} + t_{reset\_delay} + t_2 + t_{SW1\_ON\_DELAY} \quad (1)$$

The delays, t_{reset_delay} and $t_{SW1\_ON\_DELAY}$, are both configurable through PMBus. The delay, t_{config}, is typically 1.1 ms. The delays, t_1 and t_2, are determined by the user-defined timing of RST_N and ENSW1. They can both be set to 0 by pulling RST_N high before the end of t_{start} and ENSW1 high before the end of t_{reset_delay}. One simple way to do this would be to tie both signals to VDDD.

8.3.1.2 External Sequencing

To use external sequencing, either connect all the enable pins (ENSW1, ENSW2, ENSW3, and ENSW4) to an external sequencing controller, or connect them to PGOOD outputs as shown in Figure 8. By default, t_{ON_DELAY} and t_{OFF_DELAY} are both set to 5 ms. This allows the user complete flexibility of sequencing order and timing with the ENSWx pins without modifying any of the default settings in the TPS65400-Q1.

Feature Description (continued)



A. Default behavior (external sequencing)

Figure 8. Example of Sequencing Where Timing is Controlled by an External Sequencer With ENSWx Pins

8.3.1.3 Internal Sequencing

The default settings for SEQUENCE_ORDER (see *(D5h) SEQUENCE_ORDER*) effectively disable sequencing by setting all switchers to start at the same time. Therefore, to use internal sequencing, the default values for SEQUENCE_ORDER must be changed to the desired sequence. In addition, the user can configure the start or stop sequence to have a dependence on the PGOOD output of the previous switcher, or to wait for a set delay. If configured to have a dependence on PGOOD, the soft-start for the next switcher begins after PGOOD of the previous goes high and the wait time determined by t_{ON_DELAY} is complete. If configured to wait for a set delay, the wait time determined by t_{ON_DELAY} begins immediately upon the enabling of the previous switcher.

In addition, each supply can be disabled such that it is bypassed in the power-up sequence. For example, if the sequence is SW1-SW2-SW3-SW4, and SW2 is disabled, then SW3 will be powered up after SW1. The initial configuration of the TPS65400-Q1 (for first-time power-up) needs to be done using one of the methods described in *Initial Configuration*.

8.3.2 UVLO and Precision Enables

The TPS65400-Q1 implements a UVLO function that prevents startup when the voltage at VIN (terminal 22) is below 4 V. In most applications, VIN and all of the power rails (PVIN1, PVIN2, PVIN3, and PVIN4) are tied to the same source and this single UVLO function is sufficient. However, in some applications, the power rails may be tied to different input voltages, and there is the possibility that the TPS65400-Q1 may attempt to startup a switcher even when its associated PVINx rail has not reached a high-enough voltage. In these cases, the precision enable threshold on each ENSWx can be used to precisely set the startup threshold for each individual switcher with a simple resistor divider to PVINx.

Feature Description (continued)

In cases where a single UVLO threshold is needed for all four switchers, but at a different level than 4 V, the TPS65400-Q1 can be configured for single-terminal enable (PMBus register D2h, bits 0:1 = 10) where the ENSW1/ENSEQ terminal is used as a sequence enable terminal. Then, a resistor divider to the appropriate PVINx rail can be used to set a precise UVLO threshold that applies to all four switchers.

8.3.3 Soft-Start and Prebiased Startup

The TPS65400-Q1 implements a soft-start function that minimizes discharge of the output when starting up in a prebiased condition. Soft-start time, t_{SS}, is set by $t_{ON\_TRANSITION\_RATE}$ (digital soft-start) or by a capacitor connected to the corresponding SSx pin (analog soft-start). In this setup, the SSx pin sources a 5-µA current charging the capacitor, and the voltage at the SSx pin limits the reference voltage at the input of the error amplifier.

At the beginning of the soft-start, the soft-start input to the error amplifier is set to 0. The SSx input is raised gradually and reaches its target value during the time t_{ss}. If $V_{FB} > V_{SS}$, then no switching occurs. After the Soft-Start signal crosses VFB, the switching begins. The first switching pulse is on the low-side FET, which charges the high-side bootstrap capacitor. The unit runs in discontinuous conduction mode (DCM) with the zero-cross detector enabled on the low side (diode emulation). The high-side FET is pulsed according to the error amplifier output on the COMP pin. If the IC is configured for continuous conduction mode (CCM) operation (default), the low-side FET pulses gradually transition to normal CCM operation; at each successive switching cycle, the low-side gate pulse is gradually ramped until full synchronous switching occurs. At this point, the switcher enters normal CCM operation.

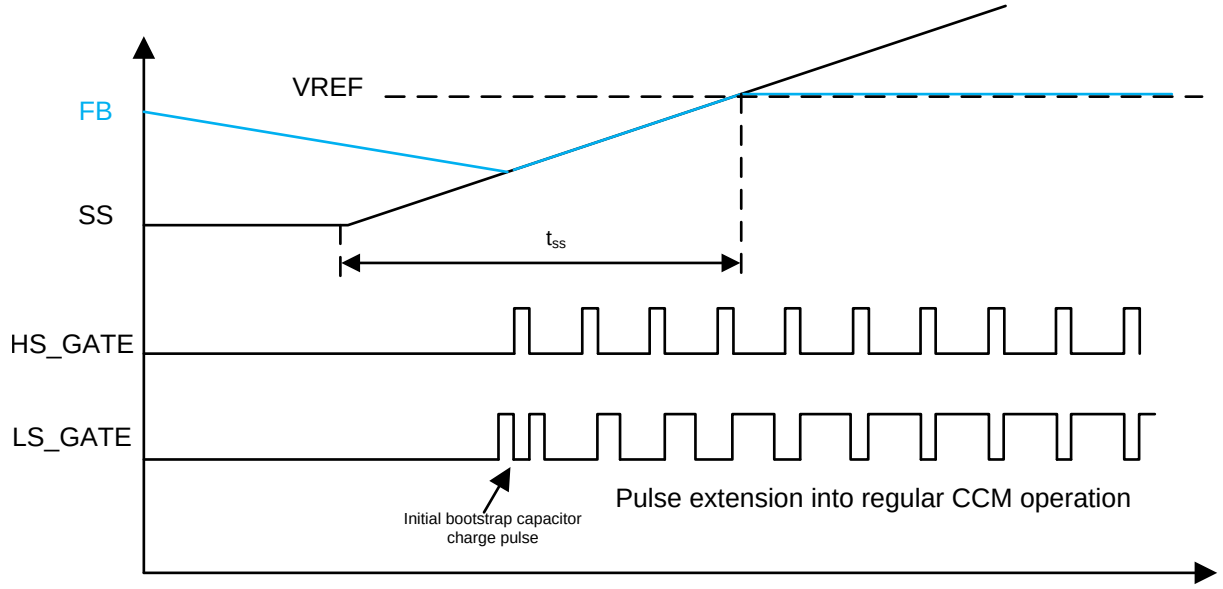


Figure 9. Soft-Start Under Prebiased Condition and CCM Mode Programmed

Feature Description (continued)

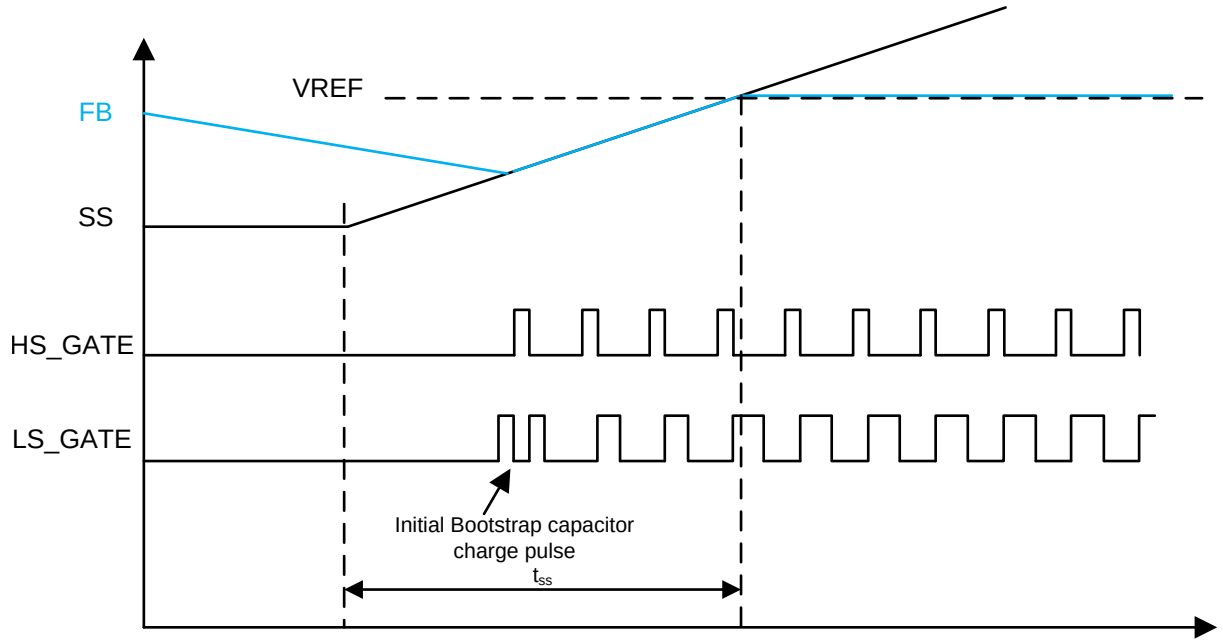


Figure 10. Soft-Start Under Prebiased Condition and DCM Mode Programmed

8.3.3.1 Analog Soft-Start (Default) and Digital Soft-Start

The TPS65400-Q1 has the ability to use an analog-based soft-start ramp based on external capacitors (one input for each switcher) or to use internal signals based on digital logics and DACs to perform the soft-start function.

When using external soft-start configuration (default configuration), the SSx pins are connected to the soft-start input of the error amplifier.

When using the internal digital soft-start signal, the soft-start input to the error amplifier increases step-by-step at a rate set according to the value set in TON_RAMP_RATE (see *(DEh) TON_TRANSITION_RATE*).

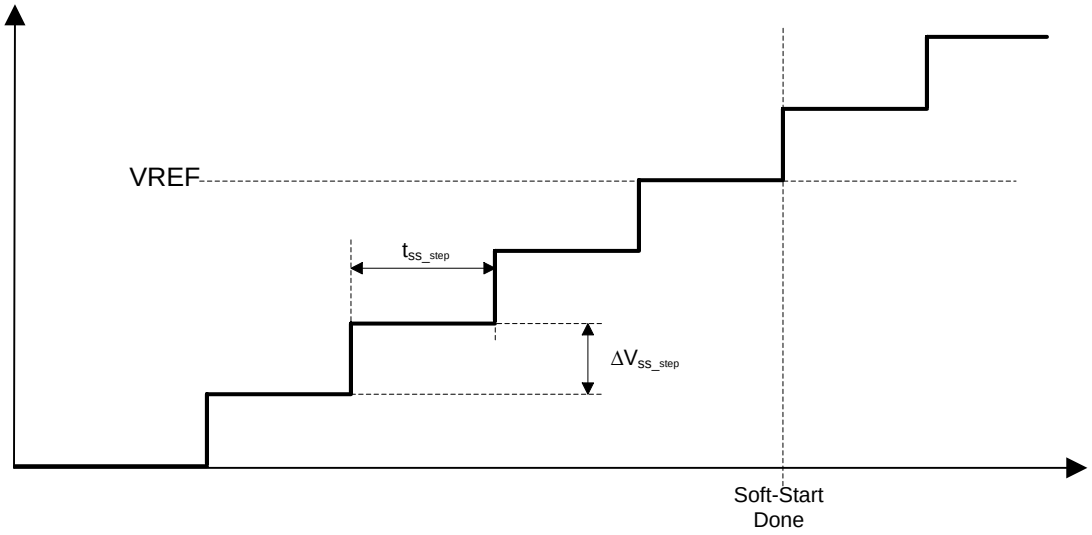


Figure 11. Internal Soft-Start Input to Error Amplifier When Digital Soft-Start is Selected

ΔVSS_step is 10 mV. Tss_step depends on the soft-start time option selected. See *(DEh) TON_TRANSITION_RATE* for more details.

Feature Description (continued)

8.3.3.2 Soft-Start Capacitor Selection

When using external soft-start capacitor to set the soft-start time, use Equation 2.

$$t_{ss} = \frac{Css}{Iss} \times Vref \quad (2)$$

Css is the value of the capacitor connected between the SSx pin and AGND. VREF is the value of the reference voltage (default is 0.8 V). I_{SS} is the current sourced by the SS1/PG1 pin during soft-start.

8.3.4 PWM Switching Frequency Selection

The master clock frequency, F_{OSC}, can be set by external resistor on the RCLOCK_SYNC terminal, or by synchronizing with an external clock. To set using an external resistor, use this formula.

$$F_{SW}\ (kHz) = 138664\ R_{OSC}\ (k\Omega)^{-0.948} \quad (3)$$

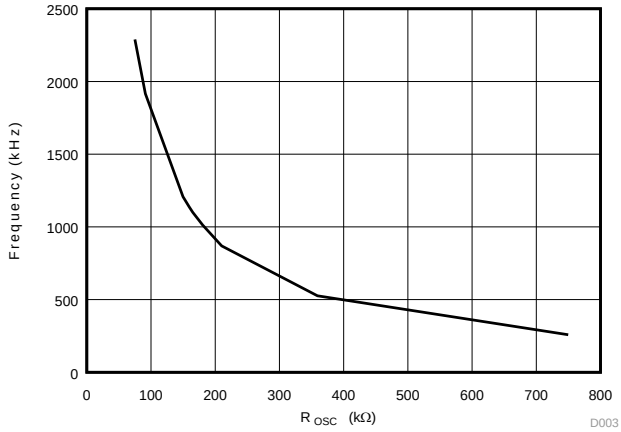
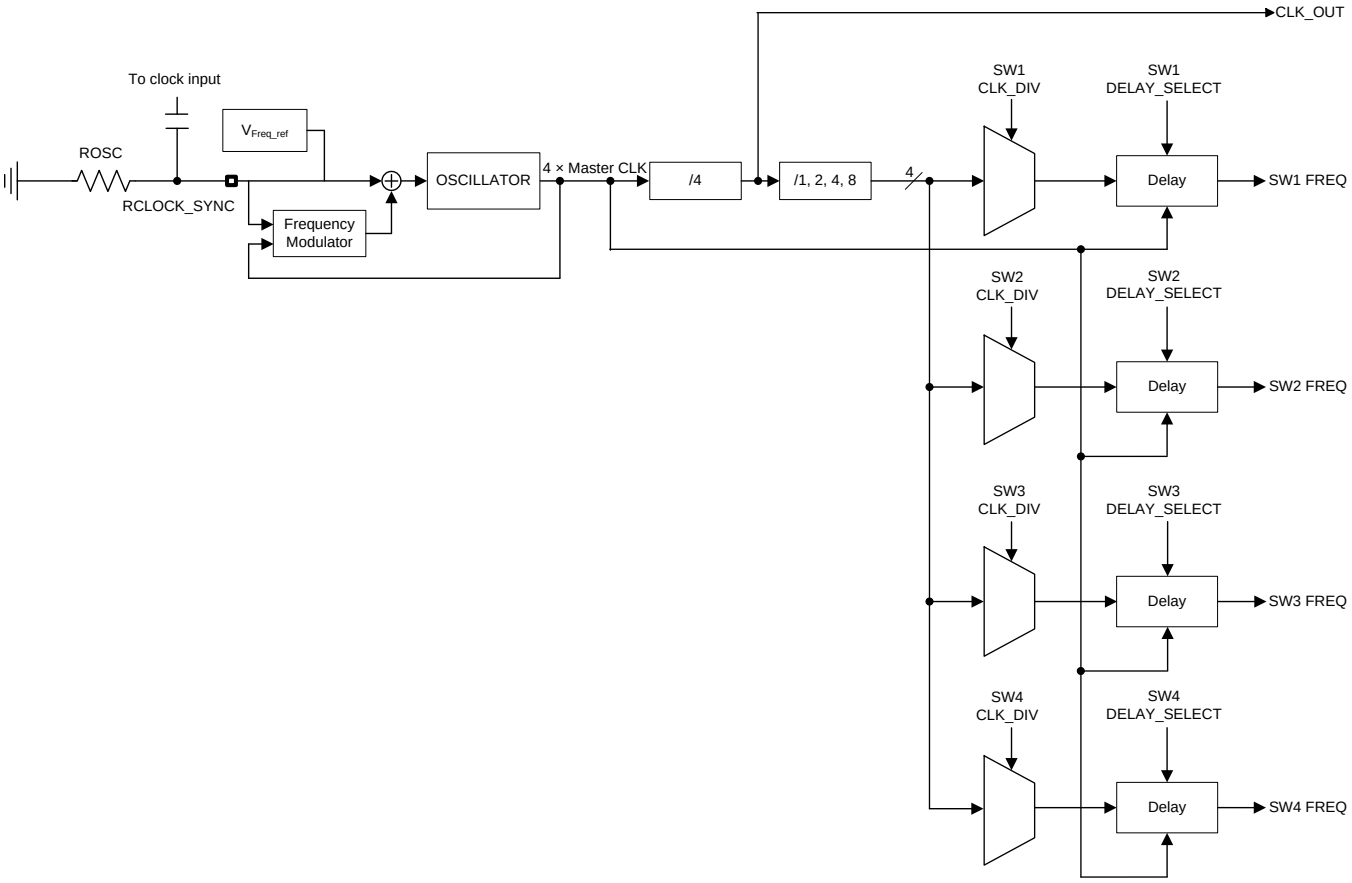


Figure 12. Frequency vs R_{osc}

To sync to an external source, an AC-coupled signal should be applied to the terminal. A fixed resistor should still be connected to set a minimum frequency. The frequency of the input signal to synchronize with should always be higher than the minimum frequency. If the internal PLL cannot synchronize, the switchers will fall back to the minimum frequency set by the resistor. The CLK_OUT terminal outputs the master clock F_{OSC}.

The PWM frequency of each switcher is determined by this master clock frequency and an I^2C-programmable choice of 4 divider ratios (1, 2, 4, or 8) by setting CLK_DIV (see *(D7h) FREQUENCY_PHASE*).

Feature Description (continued)



A. The frequency modulator is used for external clock synchronization.

Figure 13. Diagram of PWM Clock Generation

The intent of the individual divider ratios is to allow users to set the frequency of each switcher independently. For example, with a master clock F_{OSC} of 1.1 MHz, SW1 and SW2 have a divider ratio of 4 for a 275-kHz PWM, and SW3 and SW4 have a divider ratio of 1 for a PWM frequency of 1.1 MHz. Select the divider ratio so that the PWM frequency stays within the range of 275 kHz to 2.2 MHz for whichever master clock frequency is set.

In addition to selecting the frequency, each switcher can have its PWM frequency delayed. This enables the designer to minimize ripple current by properly selecting the delays so that the switching frequencies are out of phase. The default switching frequency is at CLK_DIV = F_{OSC} / 1 with PHASE_DELAY for SW1 at 0˚, SW2 at 180˚, SW3 at 90˚, and SW4 at 270˚. More information on frequency selection and delay is given in (D7h) FREQUENCY_PHASE.

8.3.5 Clock Synchronization

The RCLOCK_SYNC terminal can be used to synchronize the master clock switching frequency, F_{OSC}, with an external clock source or another TPS65400-Q1. The external clock signal (which can come from another TPS65400-Q1 CLK_OUT terminal) should be AC coupled to the RCLOCK_SYNC terminal as shown in Figure 14. Choose the ROSC value so that the fixed frequency is nominally 30% lower than the external synchronizing clock frequency. An internal protection diode clamps the low level of the synchronizing signal to approximately –0.5 V. The internal clock synchronizes to the rising edge of the external clock.

Feature Description (continued)

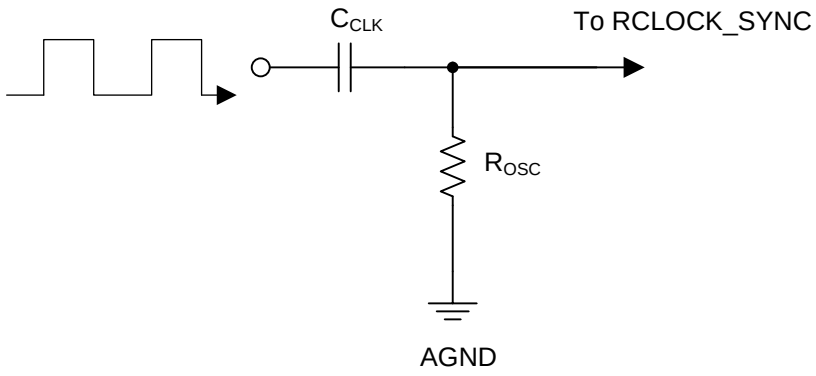


Figure 14. AC-Coupled Clock Synchronization

TI recommends to choose an AC-coupling capacitance in the range of 50 to 100 pF. Exceeding the recommended capacitance may inject excessive energy through the internal clamping diode structure present on the RCLOCK_SYNC terminal. The typical trip level of the synchronization terminal is 1.5 V. To ensure proper synchronization and to avoid damaging the IC, the peak-to-peak value (amplitude) should be between 2.5 V and V_{DDA}. The minimum duration of this pulse must be greater than 200 ns, and its maximum duration must be 200 ns less than the period of the switching cycle.

The external clock synchronization process begins after the TPS65400-Q1 is enabled and an external clock signal is detected. The frequency modulator adjusts the oscillator frequency to match the frequency of the pulses into the RCLOCK_SYNC terminal. It generally takes 50 cycles before the PWM frequency locks. If the external clock signal is removed after frequency synchronization, the master clock F_{OSC} drifts to the frequency selected by ROSC.

8.3.6 Phase Interleaving

The TPS65400-Q1 offers the ability to output rails of higher currents by connecting SW1 and SW2 in parallel, or by connecting SW3 and SW4 in parallel. To configure this option, the COMP2 or COMP4 terminal must be tied to VDDA through a 4-kΩ resistor.

Upon the initialization sequence after a reset, the TPS65400-Q1 attempts to discharge the COMP terminal through a 2-kΩ internal resistor. When it detects that the COMP terminal is pulled high, it configures itself to operate in current sharing mode. If SW2 is set to current sharing mode, its PWM output is controlled by the error amplifier and COMP1 terminal of SW1 and set to the same frequency as SW1. Likewise, if SW4 is set to current sharing mode, its PWM output is controlled by the error amplifier and COMP3 terminal of SW3 and set to the same frequency as SW3. This means that the frequency settings for SW2 and SW4 in the EEPROM are ignored in that mode of operation.

When current sharing mode is detected on a particular pair, the output slave's I^2C access is invalid and the output slave's default settings follow that of its master (see *(00h) PAGE*). The only exception is that the slave switcher PWM is a fixed 180° phase-shift from its master.

Table 1. Programmable Options When Current Sharing Enabled

Pair	Output	Current Sharing Relationship	Switching Frequency	Switching Phase
SW1-SW2	SW1	Master	Programmable	Programmable
	SW2	Slave	Follows master	Master + 180°
SW3-SW4	SW3	Master	Programmable	Programmable
	SW4	Slave	Follows master	Master + 180°

8.3.7 Fault Handling

OVP, OCP, and undervoltage protection (UVP) are handled for each switcher independently. OVP or OCP faults that occur on one switcher do not affect the other outputs. There are two exceptions:

- If current-sharing mode (ISHARE) is detected for a switcher that faults, both switchers in parallel have the same response to OVP or OCP.
- When using internal sequencing, in the case of faults occurring during the initial power-up sequence, all switchers are disabled for 500 ms, after which, the startup sequence is restarted.

During the soft-start time for a switcher, all fault signals (OVP, OCP, and UVP) are disabled and reset to the unfaulted condition. The first moment when faults can be triggered is after the end of the soft-start sequence.

OVP thresholds are set as a percentage of VREF. A deglitching time of 50 µs is used for the overvoltage. When an overvoltage occurs at the OVP upper threshold limit, the high-side FET and the low-side FET are disabled for that switcher until the OVP falling threshold is reached. When the OVP falling threshold is reached, the low-side FET turns on for 200 ns to ensure that the bootstrap capacitor is recharged before resuming normal operation of the converter.

Output voltage falling below the UVP thresholds causes the corresponding PGOOD output to fall, but the switcher continues to operate as it tries to increase the output voltage. However, if the PGOOD terminal is tied to the enable ENSWx signal of another switcher on the PCB (for external sequencing), the output for that ENSWx-PGOOD-tied switcher is disabled until output voltage is nominal and PGOOD is good.

OTP shuts down all switchers. When the temperature drops below the hysteresis level, a soft reset is triggered and the chip restarts from the startup sequence.

Fault Monitoring describes fault reporting and clearing of fault status registers.

The OVP and UVP sensing is deglitched to prevent unwanted tripping. The faults need to be sustained for more than 55 µs typically (60 µs max) to be registered and trigger protection circuits and PGOOD output to fall. Fault detection is disabled on a given switcher when its VREF is being ramped (as result of an I^2C command to change VREF). An additional 100-µs fault blanking time results after VREF has been adjusted to its target level.

8.3.8 OCP for SW1 to SW4

The OCP is I^2C-programmable and set by the IOUT_MAX command. By default, the peak current IOUT_MAX for SW1 and SW2 is 6 A, and for SW3 and SW4 it is 3 A. When the current reaches this threshold, the unit immediately turns off the high-side FET and keeps the low-side FET off for the remainder of the switching cycle. The following cycle are skipped (high-side FET off, low-side FET off) regardless of the inductor current. If the current in the inductor is still higher than the IOUT_MAX after the skipped cycle, the following cycles are also skipped until the current reach below the IOUT_MAX.

If the IOUT_MAX is reached more than 256 active cycles continuously, the switcher shut downs for 20 ms and restarts. If the switcher is running in interleaved operation, both the switcher that tripped the IOUT_MAX threshold and its interleaved counterpart shut down for 20 ms. After that period of time, the unit restarts and goes through soft-start operation. For very-low duty cycle operation and faulty operation with very-fast current increase during the high-side FET on-time (due to inductor saturation and so forth), OCP is also enforced on the low side to ensure no runaway condition exists.

Table 2. Current Limit Options

SWITCHER	IOUT_MAX
SW1, SW2	2 A
	3 A
	4 A
	5 A
	6 A (default)
SW3, SW4	0.5 A
	1 A
	2 A
	3 A (default)

While the converter is shut down following an OCP event spanning more than 256 cycles, the COMP terminal is pulled low for 1.1 ms prior to precharge and re-enabling of the converter. At the same time, the SSx pin is discharged to AGND for 1.1 ms. If the soft-start is digital (SSx pins used as PGOODx outputs), the soft-start value is reset.

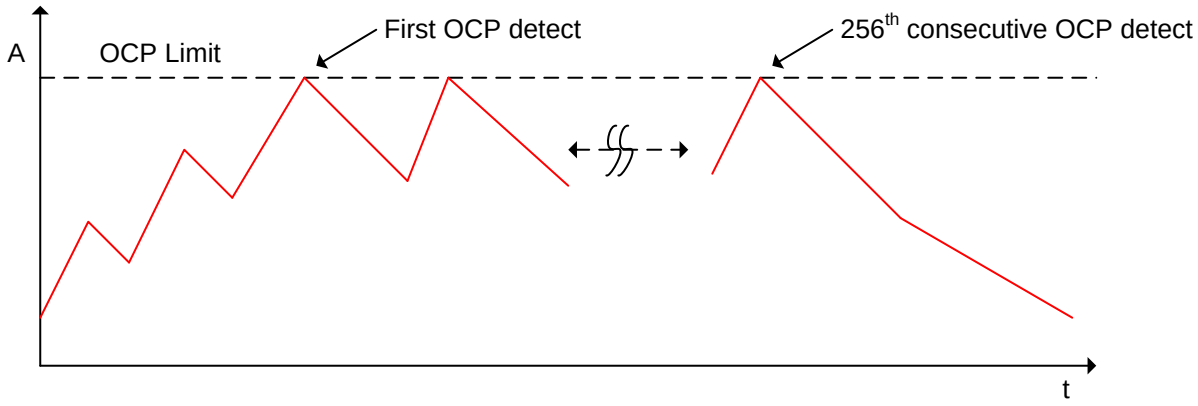


Figure 15. Inductor Current During Overcurrent Event

At high switching frequency (>1 MHz) and particularly when there is a fault in the converter such as saturation of the inductor, the current sensor might not sense the overcurrent event. To ensure that current protection is provided in all operating scenarios, low-side current sensing is also present to provide overcurrent detection and protection when the low-side FET is on. If over-current is detected when the low-side FET is on, the low-side FET stays on (and the high-side FET off) until the current drops below the threshold. A new cycle will then begin (high side on, low side off) when the next switching cycle occurs as driven by the internal clock derived from the oscillator (internal or external synchronization). A dedicated counter records the low-side OCP events and initiates a shutdown of the converter after 256 OCP event counts. Six consecutive cycles without a low-side OCP event resets the counter.

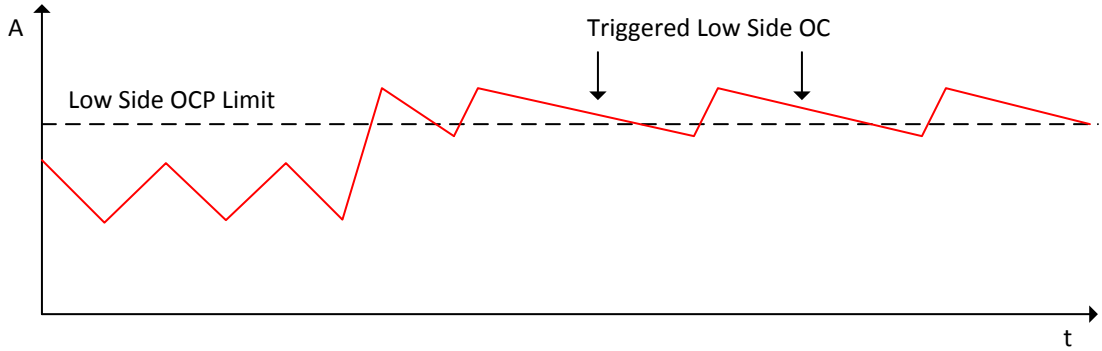


Figure 16. Inductor Current During Overcurrent Event With Low-Side Detection

8.3.9 Overcurrent Protection for SW1 to SW4 in Current Sharing Operation

When the converter is running in interleaved operation, an OCP event will not trigger the COMP terminal to be pulled low to 0.6 V. Instead, the error amplifier is switched off (tri-stated). This ensures that the COMP terminal voltage remains constant so that the other phase continues to operate during the OCP event. An OCP event on one switcher lasting more than 256 cycles triggers the shutdown of both switchers running in interleaved mode.

8.3.10 Recovery on Power Loss

All contents of the registers are saved and stored in the data store (non-volatile memory) with the exceptions listed in Table 4 (Supported PMBus Commands) when STORE_DEFAULT_ALL is issued. Contents of the registers are copied from the data store when power is restored. This allows the system processor to turn on the power supplies as needed with the same default settings before power was lost.

8.3.11 Feedback Compensation

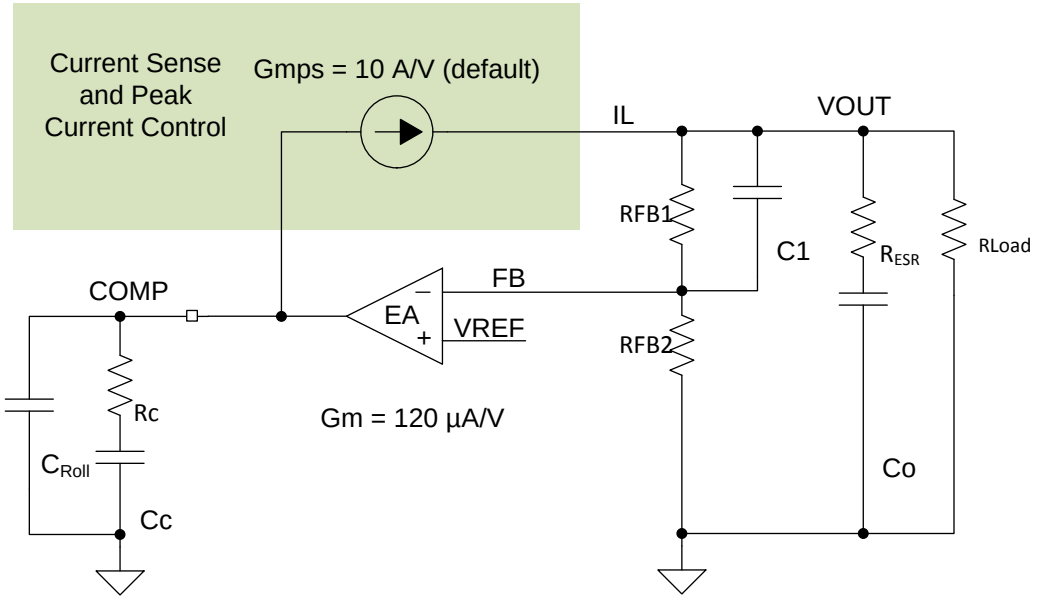


Figure 17. Simplified Equivalent Feedback Compensation Network

A typical compensation circuit could be type II (R_C and C_C) to have a phase margin between 60° and 90°, or type III (R_C, C_C, and C_{ff}) to improve the converter transient response. C_{Roll} adds a high-frequency pole to attenuate high-frequency noise when needed. C_{Roll} should be set to at least twice the crossover frequency to avoid interacting with the feedback compensation. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

Table 3 shows the recommended values for the compensation network components as an initial start. These result in the compensating zero of the Type II to match the dominant pole of the converter.

Table 3. Compensation Calculation Table

	TYPE II	TYPE III
Select cross over frequency to be less than 1/5 of switching frequency (typical is 1/10)	$F_C = \frac{F_{SW}}{10}$	$F_C = \frac{F_{SW}}{10}$
Set R_C	$R_C = \frac{2\pi \times F_C \times V_{OUT} \times C_O}{Gm \times Gm_{PS} \times VREF}$	$R_C = \frac{2\pi \times F_C \times C_O}{Gm \times Gm_{PS}}$
Set C_C	$C_C = \frac{R_{LOAD} \times C_O}{R_C}$	$C_C = \frac{R_{LOAD} \times C_O}{R_C}$
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node.	$C_{Roll} = \frac{R_{esr} \times C_o}{R_C}$	$C_{Roll} = \frac{R_{esr} \times C_o}{R_C}$
C_{ff} compensating capacitor for type III compensation network. Choose fz_{ff} same as F_C.	N/A	$C_{ff} = \frac{1}{2\pi \times fz_{ff} \times R_{FB1}}$

8.3.12 Adjusting Output Voltage

The output voltage of each buck is set with a resistor divider from BUCK output to FB pin and ground. TI recommends to use a 1% tolerance resistor or better one to get higher output voltage accuracy.

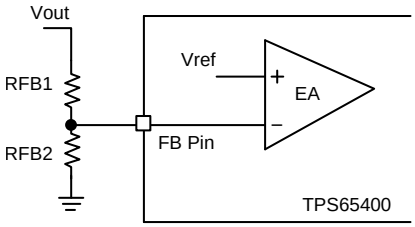


Figure 18.

With RFB1 and RFB2, output voltage is determined by:

$$Vout = Vref \times \left(1 + \frac{RFB1}{RFB2}\right) \quad (4)$$

Default Vref in TPS65400-Q1 is 0.8 V. It can be programed from 0.6 to 1.87 V by digital interface PMBus. See *(D8h) VREF_COMMAND* for more detailed information.

8.3.13 Digital Interface – PMBus

TPS65400-Q1 implements a PMBus-compatible I^2C digital interface. The PMBus specification referenced by this section is *PMBus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface*, Revision 1.2, dated 6 September 2010. The specification is published by the Power Management Bus Implementers Forum and is available from http://pmbus.org/Specifications. See details in *PMBus* and *Register Maps*.

8.3.14 Initial Configuration

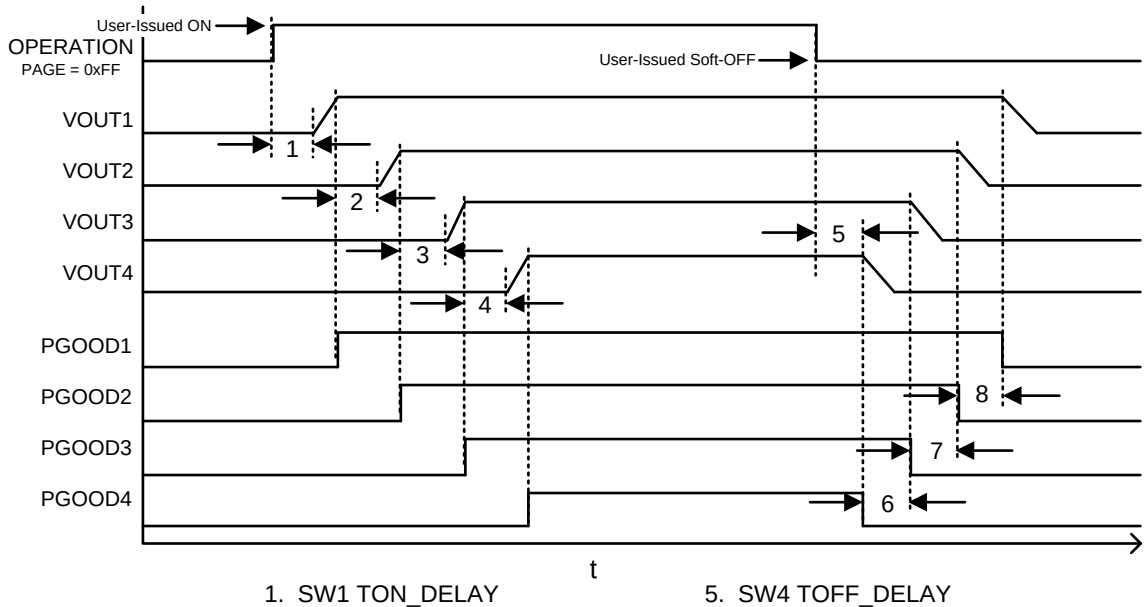
The recommended method of configuring the TPS65400-Q1 the first time is through an external programmer through a separate I^2C programming header (as shown in Figure 19). The programming header needs to connect to the SCL, SDA, CE, VDDD, and DGND lines, and can be done using a USB-to-I^2C tool. This enables the user to tailor the settings of the TPS65400-Q1 for each PCB specifically after PCB assembly, before the first power-up of the board.

An alternative method is to use the firmware in an on-board microcontroller to do the initial configuration. To do this, the user has two options:

- Power the microcontroller and the TPS65400-Q1 (VDDD, CE, and DGND connections needed) from an external source not controlled by the TPS65400-Q1.
- Design the PCB so that the default settings of the TPS65400-Q1 allow the microcontroller to be powered when power is applied to the TPS65400-Q1 the first time. The designer also needs to ensure that the default power-up sequence, ramp-rates, and other default parameters do not damage any components when power is applied the first time. After configuration, the microcontroller should pull CE low, and then all future power-ups result in the newly configured power-up scheme to occur.

Using either method for the microcontroller requires the firmware to check if the TPS65400-Q1 has been previously configured, or if a modification needs to be made to an already programmed configuration. Users may use USER_DATA_BYTE_00 and/or USER_DATA_BYTE_01 to store a version number to identify which version of the configuration is stored in the TPS65400-Q1.

A hybrid option may also be done where the initial configuration is done using an external programmer, and the subsequent revisions are done through the microcontroller firmware. This eliminates the risk from damage caused by the default configuration during the first power-up, but still allows the microcontroller firmware to modify settings such as the VREF settings for subsequent power-ups.



1. SW1 TON_DELAY
2. SW2 TON_DELAY
3. SW3 TON_DELAY
4. SW4 TON_DELAY
5. SW4 TOFF_DELAY
6. SW3 TOFF_DELAY
7. SW2 TOFF_DELAY
8. SW1 TOFF_DELAY

A. Configuration:
   1. Enable pins ENSWx set to inactive in PIN_CONFIG_00
   2. Start sequence order SW1-SW2-SW3-SW4 in SEQUENCE_ORDER
   3. Stop sequence order SW4-SW3-SW2-SW1 in SEQUENCE_ORDER

Figure 19. Example of Internal On Sequencing and Off Sequencing With the Default START_PGOOD Dependence

OPERATION (SWx) refers to OPERATION register in the corresponding PMBus PAGE. See *(01h) OPERATION* for more information on the OPERATION register.

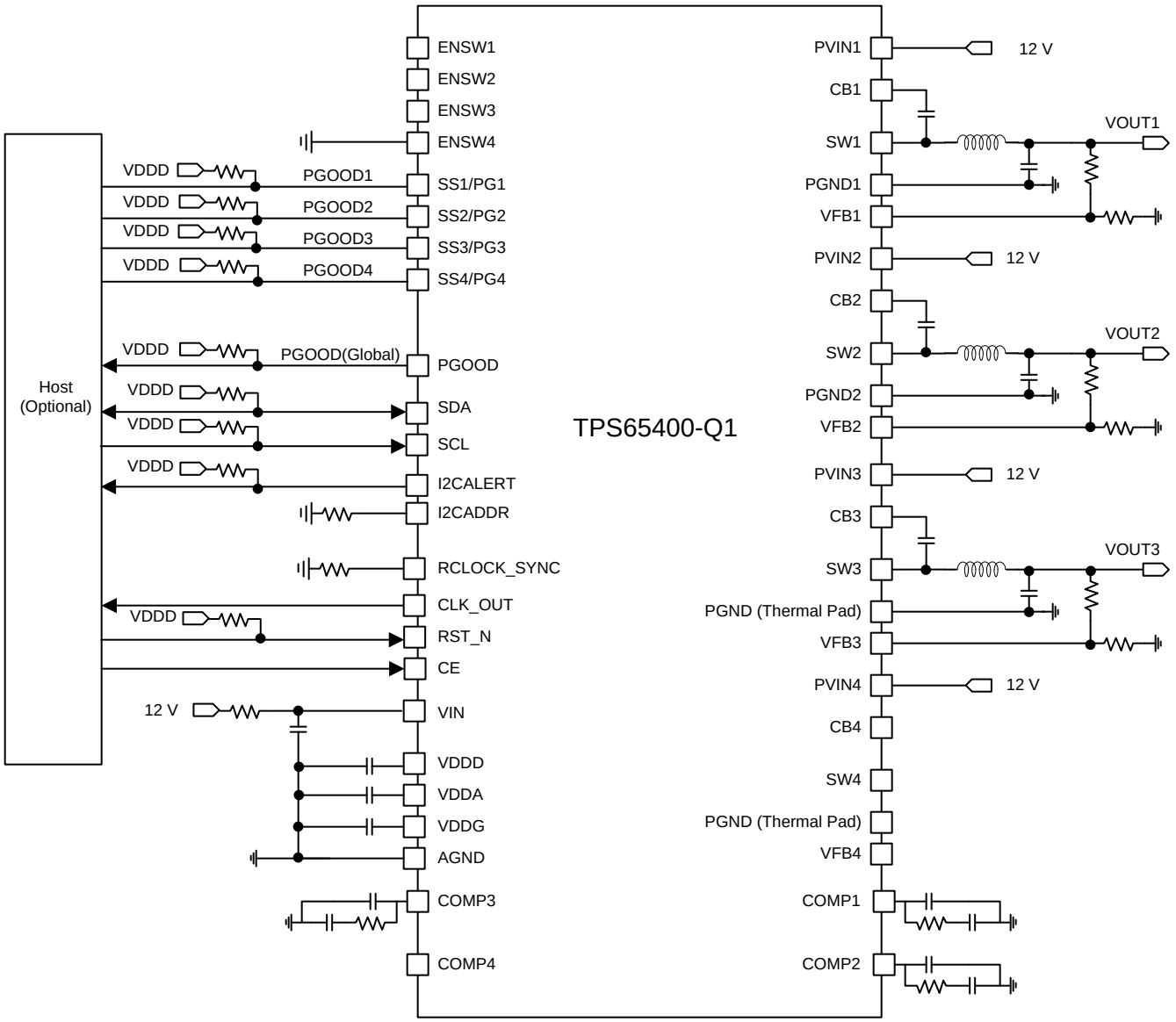


Figure 20. Internal Sequencing Schematic With Host

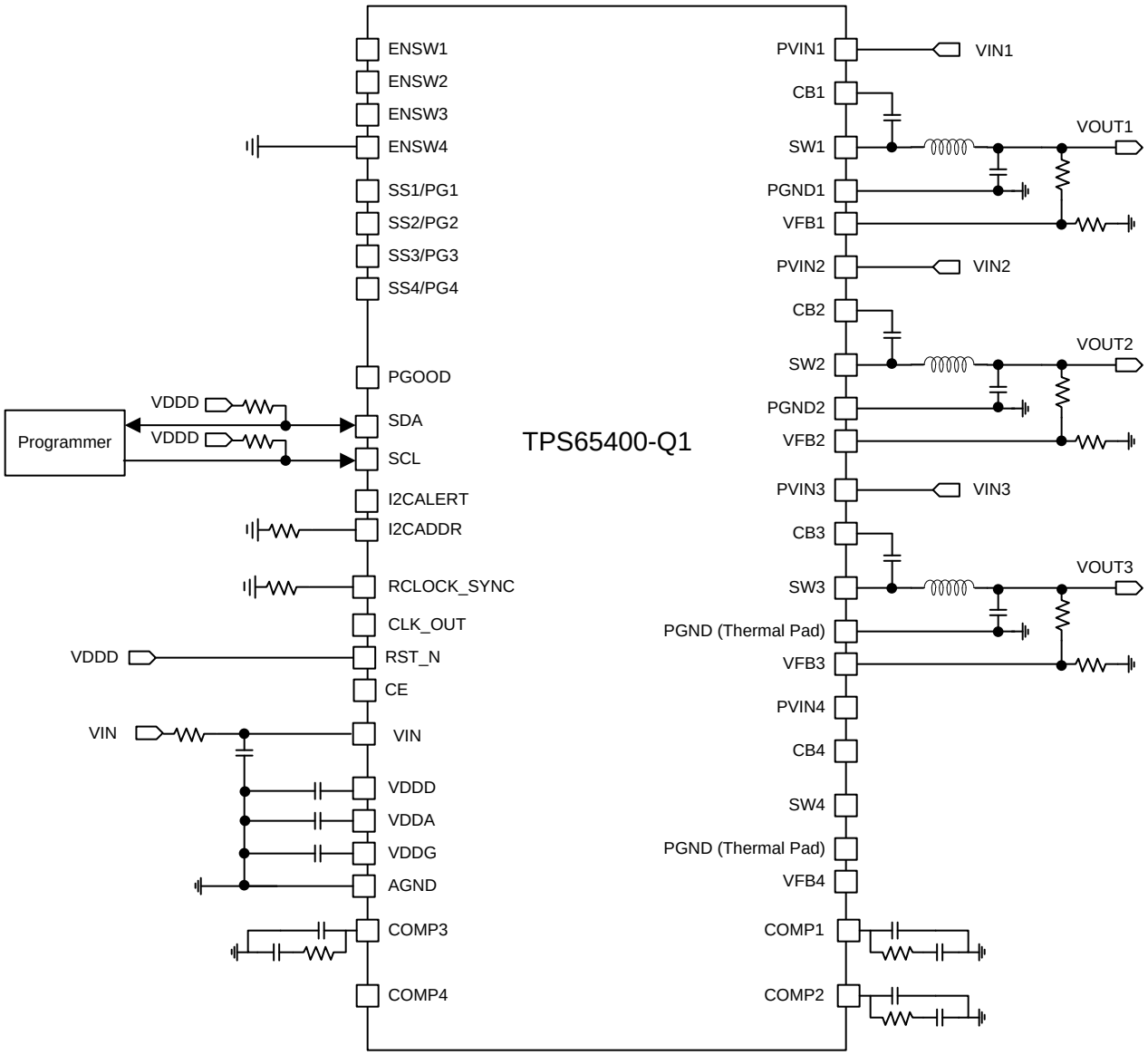


Figure 21. Internal Sequencing Schematic Without Host

8.4 Device Functional Modes

8.4.1 CCM Operation Mode

When the VIN/PVINx are above UVLO threshold and ENSWx are above the threshold, all four switchers operate in continuous current mode(CCM) with IOUT_MODE(see *(D6h) IOUT_MODE*) setting default. In CCM, the converters work in peak current mode for easy loop compensation and cycle-by-cycle high side MOSFET current limit.

8.4.2 CCM/DCM Operation Mode

When DCM mode is enabled by setting IOUT_MODE (see *(D6h) IOUT_MODE*), the switchers transition to DCM operation at light loads. During DCM mode, the low-side FET is turned off to prevent negative inductor current. This increases light-load efficiency, but output ripple and transient response during DCM or during transitions between DCM and CCM mode can be degraded.

Device Functional Modes (continued)

At light load, the COMP terminal is driven by the error amplifier to the minimum clamp voltage. When the COMP voltage reaches below 0.6 V and the error amplifier is sinking more than 5 µA, both the high-side and low-side FET will be tri-stated to prevent the output voltage from rising above the set value. The FET function is re-enabled when the GM amplifier sinks less than 3 µA. This results in a burst mode operation at light load. The low-side FET has a 200-ns one-shot ON-time to ensure that the bootstrap capacitor is charged before the normal function of the converter is resumed.

8.4.3 Current Sharing Mode

When SW1/SW2 pair output and/or SW3/SW4 pair output are shared, the responding pairs current sharing mode is enabled and the ENABLE_PIN_CONFIG is set to single ENABLE. For the detail configuration, see *Current Sharing Typical Application* .

8.5 Register Maps

Table 4 lists the PMBus commands. Commands 00h through CFh are defined in the *PMBus Specification* and are considered to be core commands that are standardized for all manufacturers and products. Commands D0h through FEh are manufacturer-specific and may be unique for each manufacturer and product. Commands that are not supported by the device are not listed.

Table 4. Supported PMBus Commands

Code	Name	SMBUS Transaction Type: Writing Data	SMBUS Transaction Type: Reading Data	Data Bytes	PAGE Support	Saved to Data Flash	Description
00h	PAGE	Write byte	Read byte	1	—	No	Selects output rail (see *(00h) PAGE*)
01h	OPERATION	Write byte	Read byte	1	00-03, FF	No	Starts or stops output (see *(01h) OPERATION*)
03h	CLEAR_FAULTS	Send byte	—	0	00-03, FF	—	Clears all faults (see *(03h) CLEAR_FAULTS*)
10h	WRITE_PROTECT	Write byte	Read byte	1	—	No	Used to lock bus writes (see *(10h) WRITE_PROTECT*)
11h	STORE_DEFAULT_ALL	Send byte	—	0	—	—	Stores operating memory to default store (see *(11h) STORE_DEFAULT_ALL*)
19h	CAPABILITY	—	Read byte	1	—	—	Describes PMBUS capabilities (see *(19h) CAPABILITY*)
78h	STATUS_BYTE	—	Read byte	1	00-03, FF	—	Fault register (see *(78h) STATUS_BYTE*)
79h	STATUS_WORD	—	Read word	2	00-03, FF	—	Fault register (see *(79h) STATUS_WORD*)
7Ah	STATUS_VOUT	—	Read byte	1	00-03, FF	—	Output fault register (see *(7Ah) STATUS_VOUT*)
80h	STATUS_MFR_SPECIFIC	—	Read byte	1	—	—	Status register (PGOOD#_N) (see *(80h) STATUS_MFR_SPECIFIC*)
98h	PMBUS_REVISION	—	Read byte	1	—	—	PMBUS revision support (see *(98h) PMBUS_REVISION*)
ADh	IC_DEVICE_ID	—	Read block	7	—	—	IC part number in ASCII (see *(ADh) IC_DEVICE_ID*)
AEh	IC_DEVICE_REV	—	Read block	2	—	—	IC part revision code (see *(AEh) IC_DEVICE_REV*)
D0h	USER_DATA_BYTE_00	Write byte	Read byte	1	—	Yes	User-defined data (see *(D0h) USER_DATA_BYTE_00*)
D1h	USER_DATA_BYTE_01	Write byte	Read byte	1	—	Yes	User-defined data (see *(D1h) USER_DATA_BYTE_01*)
D2h	PIN_CONFIG_00	Write byte	Read byte	1	—	Yes	Configures pin behavior (see *(D2h) PIN_CONFIG_00*)

Register Maps (continued)

Table 4. Supported PMBus Commands (continued)

Code	Name	SMBUS Transaction Type: Writing Data	SMBUS Transaction Type: Reading Data	Data Bytes	PAGE Support	Saved to Data Flash	Description
D3h	PIN_CONFIG_01	Write byte	Read byte	1	00-03	Yes	Configures rail-specific pin behavior (see *(D3h) PIN_CONFIG_01*)
D4h	SEQUENCE_CONFIG	Write byte	Read byte	1	—	Yes	Configures sequence behavior (see *(D4h) SEQUENCE_CONFIG*)
D5h	SEQUENCE_ORDER	Write byte	Read byte	1	00-03	Yes	Configures sequence order (see *(D5h) SEQUENCE_ORDER*)
D6h	IOUT_MODE	Write byte	Read byte	1	00-03	Yes	Sets CCM / DCM, current sharing status (see *(D6h) IOUT_MODE*)
D7h	FREQUENCY_PHASE	Write byte	Read byte	1	00-03	Yes	Sets switcher frequency and phase (see *(D7h) FREQUENCY_PHASE*)
D8h	VREF_COMMAND	Write byte	Read byte	1	00-03	Yes	Sets reference voltage (V_{REF}) (see *(D8h) VREF_COMMAND*)
D9h	IOUT_MAX	Write byte	Read byte	1	00-03	Yes	Sets current limit (see *(D9h) IOUT_MAX*)
DAh	USER_RAM_00	Write byte	Read byte	1	—	No	RESET notification (see *(DAh) USER_RAM_00*)
DBh	SOFT_RESET	Send byte	—	0	—	—	Soft resets device (see *(DBh) SOFT_RESET*)
DCh	RESET_DELAY	Write byte	Read byte	1	—	Yes	Sets delay after reset (see *(DCh) RESET_DELAY*)
DDh	TON_TOFF_DELAY	Write byte	Read byte	1	00-03	Yes	Sets delay before output begins to turn ON/OFF (see *(DDh) TON_TOFF_DELAY*)
DEh	TON_TRANSITION_RATE	Write byte	Read byte	1	00-03	Yes	Sets soft-start time (see *(DEh) TON_TRANSITION_RATE*)
DFh	VREF_TRANSITION_RATE	Write byte	Read byte	1	00-03	Yes	Sets ramping parameters for real-time Vref settings in output (see *(DFh) VREF_TRANSITION_RATE*)
E0h-EFh	—	—	—	—	—	—	Reserved
F0h	SLOPE_COMPENSATION	Write byte	Read byte	1	00-03	Yes	Adjusts control loop compensation (see *(F0h) SLOPE_COMPENSATION*)
F1h	ISENSE_GAIN	Write byte	Read byte	1	00-03	Yes	Adjusts control loop current sense (see *(F1h) ISENSE_GAIN*)

Register Maps (continued)

Table 4. Supported PMBus Commands (continued)

Code	Name	SMBUS Transaction Type: Writing Data	SMBUS Transaction Type: Reading Data	Data Bytes	PAGE Support	Saved to Data Flash	Description
FCh	DEVICE_CODE	—	Read word	2	—	—	IC part revision code (see *(FCh) DEVICE_CODE*)

Table 5. Command Bit-Mapping

Code	Name	Default Value	Byte	Bits							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
00h	PAGE	0xFF	0	PAGE							
01h	OPERATION	0x80	0	OPERATION				x	x	x	x
03h	CLEAR_FAULTS			—							
10h	WRITE_PROTECT	0x40	0	WRITE_PROTECT							
11h	STORE_DEFAULT_ALL			—							
19h	CAPABILITY	0xA0	0	PEC	BUS		SMB_ALERT	x	x	x	x
78h	STATUS_BYTE	0b0XXXX0XX	0	x	OFF	VOUT_OV	IOUT_OC	TEMPERATURE	x	CML	NONE OF THE ABOVE
79h	STATUS_WORD	0b0XXXX0XX	0	x	OFF	VOUT_OV	IOUT_OC	TEMPERATURE	x	CML	NONE OF THE ABOVE
		0bX00XX000	1	VOUT	x	x	MFR	POWER_GOOD_N	x	x	x
7Ah	STATUS_VOUT	0bX00X0000	0	VOUT_OV	x	x	VOUT_UV	x	x	x	x
80h	STATUS_MFR_SPECIFIC	0b0000XXXX	1	x	x	x	x	POWER_GOOD4_N	POWER_GOOD3_N	POWER_GOOD2_N	POWER_GOOD1_N
98h	PMBUS_REVISION	0x22	0	Part I Revision				Part II Revision			
ADh	IC_DEVICE_ID	0x07	0	Length							
		0x4C	1	‘L’							
		0x4D	2	‘M’							
		0x32	3	‘2’							
		0x36	4	‘6’							
		0x34	5	‘4’							
		0x33	6	‘3’							
		0x30	7	‘0’							
AEh	IC_DEVICE_REV	0x02	0	Length							
		0xFX	1	DEVICE_CODE_ID				DEVICE_CODE_REV			
		0x00	2	DEVICE_CODE_ID							
D0h	USER_DATA_BYTE_00	0x00	0	USER_DATA_BYTE_00							

Table 5. Command Bit-Mapping (continued)

Code	Name	Default Value	Byte	Bits							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
D1h	USER_DATA_BYTE_01	0x00	0	USER_DATA_BYTE_01							
D2h	PIN_CONFIG_00	0x3C	0	x	PGOOD_PIN_CONFIG					ENABLE_PIN_CONFIG	
D3h	PIN_CONFIG_01	0x00	0	x	x	x	x	x	x	x	SSPG_PIN_CONFIG
D4h	SEQUENCE_CONFIG	0x00	0	x	x	x	x	x	x	x	START_PGOOD
D5h	SEQUENCE_ORDER	0x00	0	x	x	x	x	STOP_ORDER		START_ORDER	
D6h	IOUT_MODE	0b000000X1	0	x	x	x	x	x	x	IOUT_SHARE	CCM
D7h	FREQUENCY_PHASE	PAGE: 0x00 / 0x01 / 0x02 / 0x03 — Val: 0x00 / 0x08 / 0x04 / 0x0C	0	x	PHASE_DELAY					CLK_DIV	
D8h	VREF_COMMAND	0x14	0	x	VREF_COMMAND						
D9h	IOUT_MAX	PAGE: 0x00 / 0x01 / 0x02 / 0x03 — Val: 0x04 / 0x04 / 0x03 / 0x03	0	x	x	x	x	x	IOUT_MAX		
DAh	USER_RAM_00	0x00	0	x	x	x	x	x	x	x	USER_RAM_00
DBh	SOFT_RESET		—								
DCh	RESET_DELAY	0x00	0	x	x	x	x	x	RESET_DELAY		
DDh	TON_TOFF_DELAY	0x01	0	x	x	TON_DELAY			TOFF_DELAY		
DEh	TON_TRANSITION_RATE	0x02	0	x	x	x	x	x	x	TON_RAMP_RATE	

Table 5. Command Bit-Mapping (continued)

Code	Name	Default Value	Byte	Bits							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
DFh	VREF_TRANSITION_RATE	0x98	0	VREF_RAMP_ENABLE	x	VREF_RAMP_TIMESTEP			VREF_RAMP_BITSTEP		
F0h	SLOPE_COMPENSATION	0x01	0	x	x	x	x	x	x	SLOPE_COMPENSATION	
F1h	ISENSE_GAIN	0x01	0	x	x	x	x	x	x	ISENSE_GAIN	
FCh	DEVICE_CODE	0xFX	0	DEVICE_CODE_ID				DEVICE_CODE_REV			
		0x00	1	DEVICE_CODE_ID							

8.5.1 PMBus

8.5.1.1 Overview

The TPS65400-Q1 implements a lightweight PMBus-compliant layer supporting packet error checking, high-speed bus, and group commands.

8.5.1.2 PMBus Protocol

The PMBus specification follows SMBus version 2.0. Figure 22 through Figure 29 show all supported command transactions.

8.5.1.2.1 PMBus Protocol

Figure 22. Send Byte Protocol With PEC

1	7	1	1	8	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	PEC	Ack	Stop

Figure 23. Write Byte Protocol With PEC

1	7	1	1	8	1	8	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Data byte	Ack	PEC	Ack	Stop

Figure 24. Read Byte Protocol With PEC

1	7	1	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Restart

7	1	1	8	1	8	1	1
Slave address	Rd	Ack	Data byte	Ack	PEC	Nack	Stop

Figure 25. Read Word Protocol With PEC

1	7	1	1	8	1	1	7	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Restart	Slave address	Rd	Ack

8	1	8	1	8	1	1
Data word (low)	Ack	Data word (high)	Ack	PEC	Nack	Stop

8.5.1.2.2 Transactions (No PEC)

Figure 26. Send Byte Protocol

1	7	1	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Stop

Figure 27. Write Byte Protocol

1	7	1	1	8	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Data byte	Ack	Stop

Figure 28. Read Byte Protocol

1	7	1	1	8	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Restart

7	1	1	8	1	1
Slave address	Rd	Ack	Data byte	Nack	Stop

Figure 29. Read Word Protocol

1	7	1	1	8	1	8	7	1	1
Start	Slave address	Wr	Ack	Command code	Ack	Restart	Slave address	Rd	Ack

8	1	8	1	1
Data word (low)	Ack	Data word (high)	Nack	Stop

8.5.1.2.3 Addressing

The 7-bit I^2C address is set through the I2CADDR terminal with a resistor RADDR connected to AGND. Table 6 shows the connection between the voltage at the I2CADDR terminal and the set I^2C address at V_{DDD} = 3 V. The I^2C address is determined only upon startup during t_{RESET_DELAY} after rising edge of CE or RST_N. This makes it immune to noise that may occur during normal operation. TI recommends resistors with 5% or lower tolerance. If I^2C is not necessary in the application, TI recommends to tie the I2CADDR terminal directly to VDDD.

Table 6. I^2C Address Selection

R_{ADDR}	7-bit Address
180 kΩ	1101 111
120 kΩ	1101 110
82 kΩ	1101 101
56 kΩ	1101 100
39 kΩ	1101 011
22 kΩ	1101 010
10 kΩ	1101 001
2 kΩ	Test mode (factory-use only)

8.5.1.2.4 Startup

After CE is asserted and V_{DDD} has reached 3.3 V, there is approximately a 320 µs delay before the PMBus interface is active. During this time the TPS65400-Q1 is restoring its configuration from the EEPROM.

8.5.1.2.5 Bus Speed

100- and 400-kHz bus speeds are supported.

8.5.1.2.6 I2CALERT Terminal

When a timeout condition occurs, the I2CALERT terminal is pulsed low for 200 µs. A timeout condition is defined as per SMBUS 2.0, $t_{TIMEOUT}$. In addition to SCL, a timeout condition also occurs when the SDA line is asserted low. If the timeout condition persists, I2CALERT continues to pulse every $t_{TIMEOUT}$. The TPS65400-Q1 never intentionally pulls the SCL low beyond $t_{LOW:SEXT}$ (1), as that violates timing specifications. Therefore, the I2CALERT terminal acts as a watchdog for other devices sharing the same bus that violate the cumulative clock low extend time. On a system level, it can be seen as a non-maskable interrupt (NMI) signal for the I^2C bus.

(1) $t_{LOW:SEXT}$: Cumulative clock low extend time (slave device). See more details on SMBus specification http://smbus.org/specs/.

Table 7. Timeout Specifications

PARAMETER		MIN	MAX	UNIT
$t_{TIMEOUT:SCL}$	Detect clock low timeout	25	35	ms
$t_{TIMEOUT:SDA}$	Detect data low timeout	25	35	ms

8.5.1.2.7 CONTROL Terminal

The TPS65400-Q1 enable terminals ENSWx are equivalent to the CONTROL terminals in the fault handling. The enable terminals behave as follows:

- Unit does not power up until commanded by the enable terminal and OPERATION command. By default, the OPERATION command is ON, so the powering up of the unit depends on the enable terminal state.
- To start, the unit requires that the on/off portion of the OPERATION command is instructing the unit to run. Depending on PIN_CONFIG_00, the unit may also require the enable terminal to be asserted for the unit to start and energize the output.
- Polarity of the enable terminal is active high. If unconnected, the terminal goes high.
- When commanding the unit to turn on or off through the enable terminals, the programmed turn on delays, turn off delays are always observed.

There are differences in enable terminal functionality depending on terminal configuration PIN_CONFIG_00. For more information, refer to OPERATION and PIN_CONFIG_00.

8.5.1.2.8 Packet Error Checking

The TPS65400-Q1 supports an optional PEC code to be validated at the end of every write and to be appended to the end of every read. TI highly recommends it, but it is not required.

8.5.1.2.9 Group Commands

Fully-compliant group commands are supported.

8.5.1.2.10 Unsupported Features

All undocumented, optional features are not supported. Extended commands are not supported.

8.5.2 PMBus Register Descriptions

The PMBus specification referenced by this section is *PMBus Power System Management Protocol Specification Part II – Command Language, Revision 1.2*, dated 6 September 2010. The specification is published by the Power Management Bus Implementers Forum and is available from http://pmbus.org/specifications.

8.5.2.1 Overview

The following parameters can be programmed and read. These are individually available for each power supply output (SW1-SW4):

- Voltage reference
- Start sequencing
- Stop sequencing
- Switching frequency
- Switching phase
- Soft-start time
- Current limit
- Current sharing operation with SW1-SW2 and/or SW3-SW4 pairs
- Power Good
- Fault status

Each power supply has its own set of PMBus commands. Paging is supported to allow device selection for a PMBus session ((00h) PAGE). Table 4 lists supported PMBus commands and paging values.

8.5.2.2 Memory Model

Supported PMBus Commands describes the memory model for PMBus devices. Values used by the PMBus device are loaded into volatile operating memory from the following places:

- Values hard-coded into an IC design
- Values programmed from hardware terminals
- A non-volatile memory called the default store
- Communications from the PMBus

On-board data flash memory is used to implement the hard-coded values and the default store values. Values in the default store may be changed using the STORE_DEFAULT_ALL command described in *(11h) STORE_DEFAULT_ALL*. The user store is not supported. Table 4 describes the ordering of memory loading and precedence. In general, the hard-coded parameters are loaded into operating memory first. Second, any terminal-programmable settings take effect. Third, values from the default store are loaded. Later, commands issued from the PMBus take effect. In all cases, an operation on a parameter overwrites any prior value that was already in the operating memory.

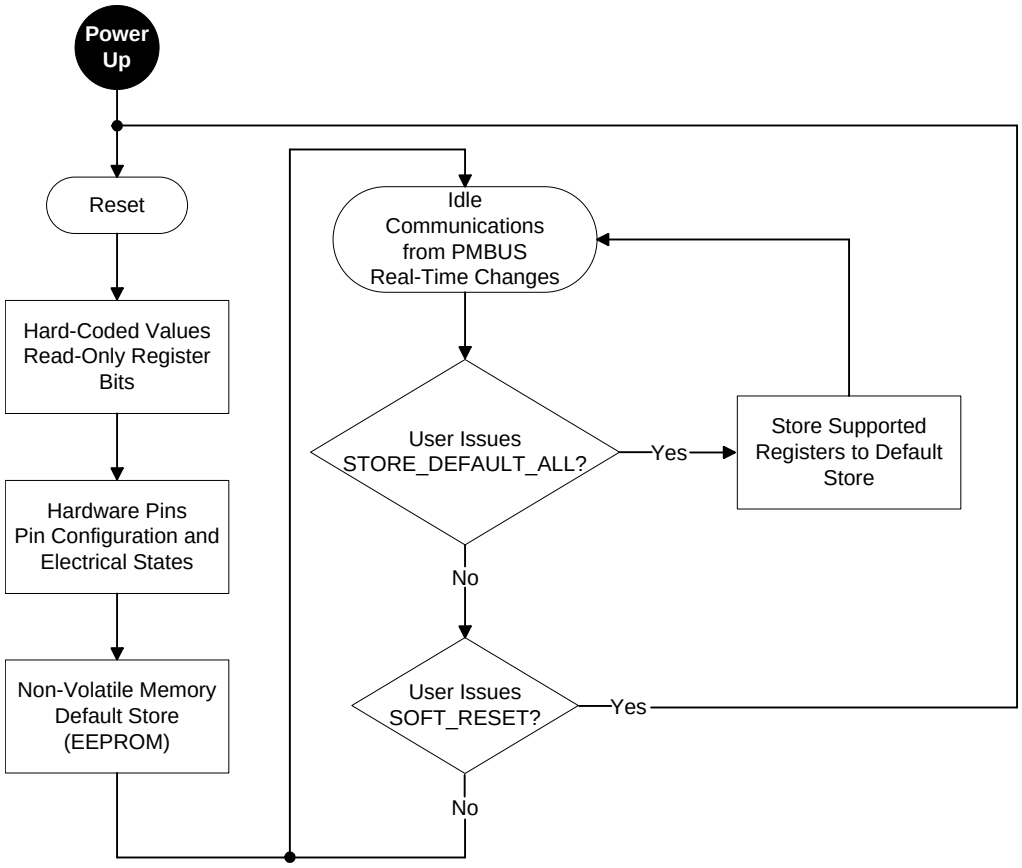


Figure 30. Memory Model

8.5.2.3 Data Formats

Data is sent as a byte, an 8-bit binary value, a word, a 16-bit binary value, or a block of bytes whose length is specified by a length byte.

8.5.2.4 Fault Monitoring

Registers *(78h) STATUS_BYTE*, *(79h) STATUS_WORD*, *(7Ah) STATUS_VOUT* of the PMBus specification describe fault monitoring for PMBus devices. The TPS65400-Q1 only supports reporting faults. Fault conditions are set in the corresponding status register and the host or power system manager can poll it. Any bits set in the status register remain set even if the fault condition is removed or corrected. The fault bits in the status register remain set until one of the following occur:

- The device receives a CLEAR_FAULTS command.
- A RESET signal is asserted by either issuing a SOFT_RESET or by asserting/deasserting the CE terminal.
- Bias power is removed from the PMBus device.

Fault Handling describes fault thresholds and specific response behaviors.

8.5.3 PMBus Core Commands

These PMBus core commands are defined in the PMBus Specification. This section describes details that are unique to the TPS65400-Q1 implementation.

8.5.3.1 (00h) PAGE

The PAGE command provides the ability to configure, control, and monitor multiple outputs on a single TPS65400-Q1 using a single PMBus physical address. All subsequent commands that depend on PAGE are applied to the rail selected by the PAGE command.

Rails are numbered starting with one, while pages are numbered starting at 0. Table 8 shows the relationship between the PMBus PAGE value and the rail number.

Table 8. PAGE Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	VALUE	OUTPUT RAIL	PAIRING	CURRENT SHARING RELATIONSHIP
7:0	PAGE	R/W	0xFF	0x00	SW1	SW1-SW2	Master
				0x01	SW2		Slave
				0x02	SW3	SW3-SW4	Master
				0x03	SW4		Slave
				0x04 to 0xFE	Invalid	—	—
				0xFF	All	—	—

On the TPS65400-Q1, current share is organized in pairs (PAGE = 0x00, 0x01 and PAGE = 0x02, 0x03). When current sharing mode is detected on a particular pair, the slave PAGE is invalid and the slave's default settings follow that of its master PAGE. The only exception is that the slave switcher PWM will be a fixed 180° phase-shift from its master (see *(D7h) FREQUENCY_PHASE*). Additionally, the ISHARE bit will be asserted (see *(D6h) IOUT_MODE*).

(00h) PAGE of the register map describes the PAGE command in more detail.

NOTE

The PAGE parameter is not stored in the default store in data flash.

8.5.3.2 (01h) OPERATION

The OPERATION command in conjunction with input from the enable pins ENSWx is used to turn on or off (enable or disable) the currently selected switching regulator as determined by the current PAGE. Margins are not supported. Data byte contents are given in Table 9.

Table 9. Operation Data Byte Contents

PAGE SUPPORT	BITS [7:6]	BITS [5:4]	BITS [3:2]	BITS [1:0]	SEQUENCING	OUTPUT ON OR OFF	DELAY
0x00 to 0x03, 0xFF	00	XX	XX	XX	No	Immediate off	None
0x00 to 0x03	01	XX	XX	XX	No	Soft off	t_{OFF_DELAY}
0xFF	01	XX	XX	XX	Yes	Soft off	t_{OFF_DELAY}
0x00 to 0x03	10	00	XX	XX	No	On with soft-start (default)	t_{ON_DELAY}

Table 9. Operation Data Byte Contents (continued)

PAGE SUPPORT	BITS [7:6]	BITS [5:4]	BITS [3:2]	BITS [1:0]	SEQUENCING	OUTPUT ON OR OFF	DELAY
0xFF	10	00	XX	XX	Yes	On with soft-start (default(1))	t_{ON_DELAY}

(1) This is also the default behavior upon reset with active ENABLE selected (see *(D2h) PIN_CONFIG_00*)

Input from the enable pin overrides the off state of the corresponding output. The pin function configuration command PIN_CONFIG_00 can accept or ignore enable pins as well as disable OPERATION sequencing command support (see *(01h) OPERATION*). If the OPERATION state is on, and PIN_CONFIG_00 is set to accept enable pins, action from enable pins would result in a delay specified by TON_TOFF_DELAY. Figure 31 shows how the on/off states are triggered.

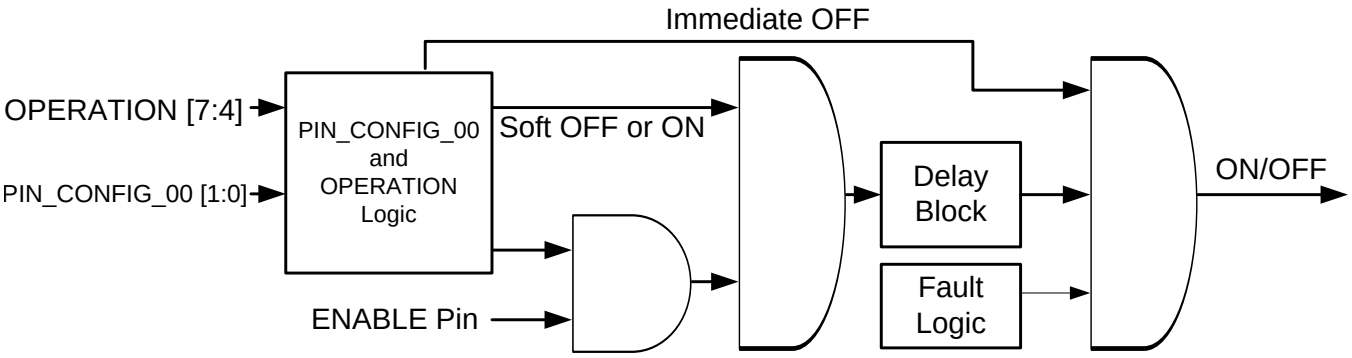


Figure 31. On/Off Configuration (Per Output)

When a fault occurs, the output state will turn OFF and possibly attempt to turn ON repeatedly for persistent faults. Specific fault response behaviors are described in *Fault Handling*.

NOTE

TI recommends that if OPERATION is to be used exclusively, all outputs should be set to the same order and enable pins should be ignored (see *(D5h) SEQUENCE_ORDER*, and *(D2h) PIN_CONFIG_00*).

The OPERATION parameter is not stored in the default store in data flash.

8.5.3.3 (03h) CLEAR_FAULTS

The CLEAR_FAULTS command clears all faults for the selected output. If PAGE 0xFF is selected, all faults for all PAGE outputs are cleared.

NOTE

POWER_GOOD_N and OFF indicate the current state of the outputs and cannot be cleared.

8.5.3.4 (10h) WRITE_PROTECT

The WRITE_PROTECT command disables writes on the PMBus. It has one data byte, described in Table 10.

Table 10. WRITE_PROTECT Command Data Byte Contents

DATA BYTE VALUE	MEANING
1000 0000	Disable all writes except to the WRITE_PROTECT command
0100 0000 (default)	Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands
0010 0000	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VREF_COMMAND commands

Table 10. WRITE_PROTECT Command Data Byte Contents (continued)

DATA BYTE VALUE	MEANING
0000 0000	Enable writes to all commands

If an invalid command is received, a communications fault is set. WRITE_PROTECT does not protect against CLEAR_FAULTS. The user is able to CLEAR_FAULTS anytime regardless of the WRITE_PROTECT state.

This command has no PAGE support.

NOTE

The WRITE_PROTECT parameter is not stored in the default store in data flash.

8.5.3.5 (11h) STORE_DEFAULT_ALL

The STORE_DEFAULT_ALL command saves the PMBus parameters from operating memory into the default store in data flash (EEPROM). The TPS65400-Q1 uses the most recently written set of default store values at startup. The maximum time it takes for the data flash to be written is 70 ms.

This command has no PAGE support.

NOTE

The OPERATION, PAGE, and WRITE_PROTECT parameters are not stored in the default store in data flash.

CAUTION

When STORE_DEFAULT_ALL is issued, operating memory should not be written to during the save.

8.5.3.6 (19h) CAPABILITY

The CAPABILITY command is a read-only command.

This command has no PAGE support.

Table 11. CAPABILITY COMMAND Data Byte Contents

BIT	READ / WRITE	DEFAULT VALUE	MEANING
7	R	1	Packet error checking is supported
6:5	R	01	Maximum supported bus speed is 400 kHz
4	R	0	Device does not have a $\overline{\text{SMBALERT}}$ pin and does not support the SMBus alert response protocol
3:0	R	0000	Reserved

8.5.3.7 (78h) STATUS_BYTE

The STATUS_BYTE command is a read-only command. Write mask is not supported. The bits are listed in Table 12.

Table 12. STATUS_BYTE Data Byte Contents

PAGE SUPPORT	BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
—	7	Not supported	R	0	—
Yes	6	OFF	R	—	Output is off
Yes	5	VOUT_OV	R	—	Output overvoltage fault
Yes	4	IOUT_OC	R	—	Output overcurrent fault

Table 12. STATUS_BYTE Data Byte Contents (continued)

PAGE SUPPORT	BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
No	2	TEMPERATURE	R	—	Overtemperature fault
—	3	Not supported	R	0	—
No	1	CML	R	—	Invalid command code, data, or packet
Yes	0	NONE OF THE ABOVE	R	—	A fault or warning not listed in bits [7:1] has occurred

Overtemperature fault and CML is independent of PAGE. When there is PAGE support, the meaning of the bits applies only for the selected output PAGE. For PAGE = 0xFF, STATUS_BYTE is a logical OR of all PAGE = 0x00 to 0x03 STATUS_BYTE values.

An exception to NONE OF THE ABOVE is that the MFR bit in STATUS_WORD is ignored due to no PAGE support.

PAGE support is for outputs 0x00 to 0x03, 0x0FF.

8.5.3.8 (79h) STATUS_WORD

The STATUS_WORD command is a read-only command. Write mask is not supported. Only the parameters in Table 13 are supported.

Table 13. STATUS_WORD Data Word Contents (Upper Byte)

PAGE SUPPORT	BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
Yes	7	VOUT	R	—	Output voltage fault set if any bit in STATUS_VOUT is asserted (for the same page)
—	6	Not supported	R	0	—
—	5	Not supported	R	0	—
No	4	MFR	R	—	Set if any bit in STATUS_MFR_SPECIFIC is asserted
Yes	3	POWER_GOOD_N	R	—	Output voltage is within PGOOD range, negated
—	2	Not supported	R	0	—
—	1	Not supported	R	0	—
—	0	Not supported	R	0	—

The lower byte of STATUS_WORD is STATUS_BYTE.

The MFR bit is independent of PAGE. When there is PAGE support, the meaning of the bits applies only for the selected output PAGE. For PAGE = 0xFF, STATUS_WORD is a logical OR of all PAGE = 0x00 to 0x03 STATUS_WORD values.

PAGE support is for outputs 0x00 to 0x03, 0x0FF.

8.5.3.9 (7Ah) STATUS_VOUT

The STATUS_VOUT command is a read-only command. Write mask is not supported. Only the parameters in Table 14 are supported.

Table 14. STATUS_VOUT Data Byte Contents

BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
7	VOUT_OV	R	—	VOUT overvoltage fault
6	Not supported	R	0	—
5	Not supported	R	0	—
4	VOUT_UV	R	—	VOUT undervoltage fault
3	Not supported	R	0	—
2	Not supported	R	0	—

Table 14. STATUS_VOUT Data Byte Contents (continued)

BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
1	Not supported	R	0	—
0	Not supported	R	0	—

STATUS_VOUT shows the voltage output status for the PAGE selected output. For PAGE = 0xFF, STATUS_VOUT is a logical OR of all PAGE = 0x00-0x03 STATUS_ VOUT values. VOUT_OV in STATUS_VOUT is identical to VOUT_OV in STATUS_BYTE for the same PAGE.

PAGE support is for outputs 0x00 to 0x03, 0x0FF.

8.5.3.10 (80h) STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command is a read-only command. Write mask is not supported. Only the parameters in Table 15 are supported.

Table 15. STATUS_MFR_SPECIFIC Data Byte Contents

BIT	NAME	READ / WRITE	DEFAULT VALUE	MEANING
7	Not supported	R	0	—
6	Not supported	R	0	—
5	Not supported	R	0	—
4	Not supported	R	0	—
3	POWER_GOOD4_N	R	—	SW4 output voltage is within PGOOD range, negated
2	POWER_GOOD3_N	R	—	SW3 output voltage is within PGOOD range, negated
1	POWER_GOOD2_N	R	—	SW2 output voltage is within PGOOD range, negated
0	POWER_GOOD1_N	R	—	SW1 output voltage is within PGOOD range, negated

STATUS_MFR_SPECIFIC reports the individual output negated PGOODs. These bit values also can be retrieved from POWER_GOOD_N if an individual output is selected through PAGE.

This command has no PAGE support.

8.5.3.11 (98h) PMBUS_REVISION

The PMBUS_REVISION command is a read-only command.

Table 16. PMBUS_REVISION Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	MEANING
7:4	Part I revision	R	0010	Supports version 1.2
3:0	Part II revision	R	0010	Supports version 1.2

This command has no PAGE support.

8.5.3.12 (ADh) IC_DEVICE_ID

The IC_DEVICE_ID command is a read-only block command and returns the ASCII characters of the part number TPS65400-Q1.

Table 17. IC_DEVICE_ID Data Block Contents

BYTE	NAME	READ / WRITE	DEFAULT VALUE	ASCII VALUE
7	IC_DEVICE_ID	R	0x30	0
6			0x33	3
5			0x34	4
4			0x36	6
3			0x32	2
2			0x4D	M
1			0x4C	L
0	Length byte	R	0x07	—

This command has no PAGE support.

8.5.3.13 (AEh) IC_DEVICE_REV

The IC_DEVICE_REV command is a read-only block command and returns the 2-byte device code of the part. The device code is identical to the 2-byte DEVICE_CODE. Refer to DEVICE_CODE for details (see *(FCh) DEVICE_CODE*).

Table 18. IC_DEVICE_REV Data Block Contents

BYTE	NAME	READ / WRITE	DEFAULT VALUE
2:1	DEVICE_CODE	R	See DEVICE_CODE
0	Length byte	R	0x02

This command has no PAGE support.

8.5.4 Manufacturer-Specific Commands

8.5.4.1 (D0h) USER_DATA_BYTE_00

The USER_DATA_BYTE_00 command contains 8 bits for reading and writing user-defined data. Upon issuing STORE_DEFAULT_ALL, contents of this command are saved to the default store in data flash.

Table 19. USER_DATA_BYTE_00 Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE
7:0	USER_DATA_BYTE_00	R/W	0x00

This command has no PAGE support.

8.5.4.2 (D1h) USER_DATA_BYTE_01

The USER_DATA_BYTE_01 command contains 7 bits, USER_DATA_BITS_01, for reading and writing user-defined data. Upon issuing STORE_DEFAULT_ALL, contents of this command are saved to the default store in data flash.

The most significant bit, STORED, is a read-only bit that indicates whether the user has written to the default store through STORE_DEFAULT_ALL. This indicator bit cannot be cleared.

Table 20. USER_DATA_BYTE_01 Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE
7	STORED	R	0
6:0	USER_DATA_BYTE_01	R/W	0000000

This command has no PAGE support.

8.5.4.3 (D2h) PIN_CONFIG_00

The PIN_CONFIG_00 command selects pin function and behavior for enable pins ENSWx and the global PGOOD pin.

ENABLE_PIN_CONFIG selects between active ENABLE, inactive ENABLE, or single ENABLE behavior for ENSWx pins.

- When active ENABLE is selected, each pin in conjunction with OPERATION controls its respective switcher on/off. For details, see *(01h) OPERATION* and *(DDh) TON_TOFF_DELAY*.
- When inactive ENABLE is selected, the state of all ENSWx pins is ignored.
- When single ENABLE is selected, ENSW1 pin acts as a sequence start and sequence stop pin, with all other ENSWx pins ignored. This allows the device to emulate classic sequencing behavior. A start sequence begins when ENSW1 is asserted, and a stop sequence begins when ENSW1 is deasserted. If ENSW1 were to de-assert before a start sequence were complete, a stop-sequence would begin immediately.

PGOOD_PIN_CONFIG sets the function of the global PGOOD pin.

- By default, the global PGOOD pin is configured to output a logical AND of each individual power supply's PGOOD. If all supplies were to turn off, the global PGOOD pin would be de-asserted.
- The global PGOOD pin can be selected to output the status of any individual power supply's $\overline{\text{PGOOD}}$, or any OR/AND combination thereof. If an individual supply's PGOOD#_MASK bit is masked, its PGOOD status would be masked from the global PGOOD pin. If all PGOOD#_MASK pins were masked, the output of the global PGOOD pin would be at logic zero regardless of the PGOOD_LOGIC selected.
- PGOOD#_MASK only applies to the output pin logic and does not affect STATUS_WORD or sequencing.

Table 21. PIN_CONFIG_00 Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	MEANING	PINS AFFECTED
7	—	R	0	—	—	—
6	PGOOD_PIN_CONFIG : PGOOD_LOGIC	R/W	0	0	AND of all unmasked PGOODs	Global PGOOD pin
				1	OR of all unmasked PGOODs	
5	PGOOD_PIN_CONFIG : PGOOD4_MASK	R/W	1	0	PGOOD4 is masked	
				1	PGOOD4 is unmasked	
4	PGOOD_PIN_CONFIG : PGOOD3_MASK	R/W	1	0	PGOOD3 is masked	
				1	PGOOD3 is unmasked	
3	PGOOD_PIN_CONFIG : PGOOD2_MASK	R/W	1	0	PGOOD2 is masked	
				1	PGOOD2 is unmasked	
2	PGOOD_PIN_CONFIG : PGOOD1_MASK	R/W	1	0	PGOOD1 is masked	
				1	PGOOD1 is unmasked	
1:0	ENABLE_PIN_CONFIG	R/W	00	00	Active ENABLE Enable pins ENSWx control each switcher independently	ENSW# pins
				01	Inactive ENABLE All enable pins ENSWx are ignored	
				1X	Single ENABLE ENSW1 starts and stops sequencing. All other enable pins are ignored.	

Table 22 shows example configurations for PGOOD_PIN_CONFIG.

Table 22. PGOOD_PIN_CONFIG Example Configurations

PGOOD_PIN_CONFIG BINARY VALUE	GLOBAL PGOOD PIN
01111 (default)	PGOOD1 and PGOOD2 and PGOOD3 and PGOOD4

Table 22. PGOOD_PIN_CONFIG Example Configurations (continued)

PGOOD_PIN_CONFIG BINARY VALUE	GLOBAL PGOOD PIN
11111	PGOOD1 or PGOOD2 or PGOOD3 or PGOOD4
00101	PGOOD1 and PGOOD3
X0001	PGOOD1
X0010	PGOOD2
X0100	PGOOD3
X1000	PGOOD4

This command has no PAGE support.

CAUTION

Changing PIN_CONFIG_00 during normal operation has no effect. The configuration can only be modified by storing into EEPROM and then reloading the configuration upon reset.

8.5.4.4 (D3h) PIN_CONFIG_01

PIN_CONFIG_01 command selects pin function and behavior for the selected output's SSx/$\overline{PG}$ pin.

SSPG_PIN_CONFIG sets the selected power supply's SSx/$\overline{PG}$ pin to a soft-start time input pin or a power good output pin.

- When selected as soft-start time input pin SSx, the internal soft-start ramp rate TON_TRANSITION_RATE is ignored. A 5-µA current source will be connected internally and an external capacitor can be used to set the soft-start delay.
- When selected as a power good output pin $\overline{PG}$ ($\overline{PGOOD}$), the pin outputs the status of the selected power supply's power good.

Table 23. PIN_CONFIG_01 Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	MEANING	PINS AFFECTED
7:1	—	R	0000000	—	—	—
0	SSPG_PIN_CONFIG	R/W	0	0	SSx pin	SSx/$\overline{PG}$ pin
				1	$\overline{PG}$ pin	

PAGE support is for outputs 0x00 through 0x03.

CAUTION

Changing PIN_CONFIG_01 during normal operation will have no effect. The configuration can only be modified by storing into EEPROM and then reloading the configuration upon reset.

8.5.4.5 (D4h) SEQUENCE_CONFIG

The SEQUENCE_CONFIG command determines sequencing behavior.

START_PGOOD determines whether the next output in sequence looks at the previous output's PGOOD before turning on. For turning on, the previous output's PGOOD must be good. For the first in sequence, there is no PGOOD reference so START_PGOOD for those particular switchers are ignored. START_PGOOD applies to all switchers.

Table 24. SEQUENCE_CONFIG Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	MEANING
7:1	—	R	0000000	—	—
0	START_PGOOD	R/W	0	0	PGOOD is checked
				1	PGOOD is ignored

This command has no PAGE support.

CAUTION

TI does not recommend changing SEQUENCE_CONFIG during start sequencing or stop sequencing.

8.5.4.6 (D5h) SEQUENCE_ORDER

The SEQUENCE_ORDER command determines the order in which each output starts and stops. If two or more supplies are assigned the same sequence number, they start/stop at the same time. If sequencing is not used, all sequence bits should be set to the same value. For PGOOD sequencing options, see *(D4h) SEQUENCE_CONFIG*.

Table 25. SEQUENCE_ORDER Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:4	—	R	0000	—	—	—
3:2	STOP_ORDER	R/W	00	00	1 (first to stop)	Stop sequence order number
				01	2	
				10	3	
				11	4 (last to stop)	
1:0	START_ORDER	R/W	00	00	1 (first to start)	Start sequence order number
				01	2	
				10	3	
				11	4 (last to start)	

CAUTION

TI does not recommend changing SEQUENCE_ORDER during start sequencing or stop sequencing.

PAGE support is for outputs 0x00 to 0x03.

8.5.4.7 (D6h) IOUT_MODE

The IOUT_MODE command configures the selected output to be:

- Operating in CCM
- Operating in Mixed CCM/DCM

There is a read-only bit, IOUT_SHARE, that indicates that the current selected output:

- Shares its current
- Does not share its current

On the TPS65400-Q1, current share is organized in pairs (PAGE = 0x00, 0x01 and PAGE = 0x02, 0x03). When current sharing mode is detected on a particular pair, the slave PAGE is invalid and the slave's default settings follow that of its master PAGE. The only exception is that the slave switcher PWM is a fixed 180° phase-shift from its master (see *(D7h) FREQUENCY_PHASE*).

Table 26. IOUT_MODE Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	MEANING
7:2	—	R	000000	—	—
1	IOUT_SHARE	R	—	0	Current is not shared
				1(1)	Current is shared(1)
0	CCM	R/W	1	0	Mixed CCM/DCM
				1	CCM

(1) This bit is only observable from the master PAGEs (see *(00h) PAGE*).

PAGE support is for outputs 0x00 through 0x03.

CAUTION

Changing IOUT_MODE during normal operation has no effect. The configuration can only be modified by storing into EEPROM and then reloading the configuration upon reset.

8.5.4.8 (D7h) FREQUENCY_PHASE

The FREQUENCY_PHASE command sets the output switching frequency and phase of the selected output. The switching frequency is a quotient from the division of the master clock, F_{OSC}, by the selected divisor CLK_DIV. PHASE_DELAY determines the phase shift as a multiple of the internal PLL period, which is scaled at 4× less than the master clock period 1 / F_{OSC}.

Table 27. FREQUENCY_PHASE Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7	—	R	0	—	—	—
6:2	PHASE_DELAY	R/W	See Table 28	00000	0	Switching delay time (phase)
				00001	1 / (4 × FOSC)	
				..	..	
				11110	30 / (4 × FOSC)	
				11111	31 / (4 × FOSC)	
1:0	CLK_DIV	R/W	00	00	FOSC / 1	Switching frequency
				01	FOSC / 2	
				10	FOSC / 4	
				11	FOSC / 8	

Table 28. PHASE_DELAY Default Data Bit Values

PAGE	PHASE_DELAY BINARY VALUE	PHASE SHIFT (°)
0x00	00000	0
0x01	00010	180
0x02	00001	90
0x03	00011	270

The phase shift in degrees is calculated by Equation 5.

$$\text{Phase shift} = \frac{\text{PHASE\_DELAY}}{2^{\text{CLK\_DIV}}} \text{ (degrees)} \quad (5)$$

When current sharing mode is detected on a particular pair, the slave PAGE is invalid and the slave's default settings follow that of its master PAGE. The only exception is that the slave switcher PWM is a fixed 180° phase-shift from its master. Additionally, the ISHARE bit is asserted (see *(D6h) IOUT_MODE*).

PAGE support is for outputs 0x00 through 0x03.

CAUTION

Changing the FREQUENCY_PHASE during normal operation has no effect. The configuration can only be modified by storing into EEPROM and then reloading the configuration upon reset.

8.5.4.9 (D8h) VREF_COMMAND

The VREF_COMMAND command sets the voltage reference (VREF) for the selected output. Values range from 0.6 to 1.87 V with a bit resolution of 10 mV per LSB.

Table 29. VREF_COMMAND Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7	—	R	0	—	—	—
6:0	VREF_COMMAND	R/W	0010100	0000000	0.60 V	Reference voltage
				0000001	0.61 V	
				…	…	
				0010100	0.8 V	
				…	…	
				1111110	1.86 V	
				1111111	1.87 V	

The voltage reference can be changed while one or more voltage outputs are enabled. To reduce the effect of large transient steps, digital slew rate limiting is implemented. The larger the change in the voltage reference, the greater the delay that is incurred as the voltage steps toward the new reference. For details, see *(DFh) VREF_TRANSITION_RATE*.

Faults are blanked during transition. A 100-s fault blanking time results after a transition completes.

PAGE support is for outputs 0x00 through 0x03.

8.5.4.10 (D9h) IOUT_MAX

The IOUT_MAX command sets the current limit for the selected output.

Table 30. IOUT_MAX Data Byte Contents, PAGE = 0x00, 0x01

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:3	—	R	00000	—	—	—
2:0	IOUT_MAX	R/W	100	000	2 A	Current limit
				001	3 A	
				010	4 A	
				011	5 A	
				1XX	6 A	

Table 31. IOUT_MAX Data Byte Contents, PAGE = 0x02, 0x03

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:2	—	R	000000	—	—	—
1:0	IOUT_MAX	R/W	11	00	0.5 A	Current limit
				01	1 A	
				10	2 A	
				11	3 A	

The limit set by the IOUT_MAX byte sets both the high-side and low-side current limit.

PAGE support is for outputs 0x00 through 0x03.

8.5.4.11 (DAh) USER_RAM_00

The USER_RAM_00 command is a reset notification status. Upon any RESET condition, the device clears this value to 0x00. This value can only be set to 0x01 by the PMBus master.

Table 32. USER_RAM_00 Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE
7:1	—	R	0000000
0	USER_RAM_00	R/W	0

This command has no PAGE support.

8.5.4.12 (DBh) SOFT_RESET

The SOFT_RESET command triggers a software reset of the device. It is equivalent to sending an assert-deasserting pulse to the CE pin. Consequently, all switchers turn off and all faults are cleared.

This command has no PAGE support.

8.5.4.13 (DCh) RESET_DELAY

The RESET_DELAY command sets the delay time before any switcher can begin its soft-start after CE is asserted. Thus, if the turn-on sequence or an individual switcher is enabled before this delay is over, no action occurs until the delay is completed. After this delay period is passed, enabling the turn-on sequence of an individual switcher would have an immediate effect subject to the t_{ON_DELAY} and soft-start time.

Table 33. RESET_DELAY Data Byte Contents(1)

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:3	—	R	00000	—	—	—
2:0	RESET_DELAY	R/W	000	000	1 ms(2)	Reset delay time
				001	50 ms	
				010	100 ms	
				011	250 ms	
				100	500 ms	
				101	1000 ms	
				110	1500 ms	
				111	2000 ms	

(1) All the delay times are subject to the delay between the rising edge of CE and the stabilizing delay time of the VDDD supply, which can be up to 1.1 ms, depending on the bypass capacitor sizing for these rails. The RESET_DELAY in the table is in addition to this power-up delay and has an accuracy of ±62.5 µs.

(2) When setting the RESET_DELAY to 1 ms, TI recommends that the t_{ON_DELAY} for the outputs starting up first be greater than 5 ms. Because, the COMP pin precharge starts at the same time as the RESET_DELAY. If RESET_DELAY is 1 ms, and t_{ON_DELAY} is 0 ms, then the COMP pin precharge may not stabilize before the switcher soft-start begins. The time needed to stabilize the COMP pin precharge depends on the RC compensation values connected to the COMP pin.

This command has no PAGE support.

8.5.4.14 (DDh) TON_TOFF_DELAY

The TON_TOFF_DELAY command sets the delay times after receiving an on or off command for the selected output to begin turning on or off.

TON_DELAY of this command are lexically equivalent to TON_DELAY. If TON_DELAY is set to 0 ms, the device would begin turning on immediately. If TOFF_DELAY is set to 0 ms, the device would begin turning off immediately.

Table 34. TON_TOFF_DELAY Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:6	—	R	00	—	—	—
5:3	TON_DELAY	R/W	010	000	0 ms	Delay time before starting
				001	1 ms	
				010	5 ms	
				011	25 ms	
				100	100 ms	
				101	500 ms	
				110	1000 ms	
				111	2000 ms	
2:0	TOFF_DELAY	R/W	000	000	0 ms	Delay time before stopping
				001	1 ms	
				010	5 ms	
				011	25 ms	
				100	100 ms	
				101	500 ms	
				110	1000 ms	
				111	2000 ms	

These delays are always in effect including when the outputs are internally or externally sequenced, or arbitrarily turned on or off. The only exceptions are:

- The device receives an immediate OFF from the OPERATION command.
- The device turns its output off internally (such as in a fault condition).

PAGE support is for outputs 0x00 through 0x03.

8.5.4.15 (DEh) TON_TRANSITION_RATE

The TON_TRANSITION_RATE command sets the soft-start ramp rate for the selected output. This command is ignored by default because soft-start is set externally through the SSx/$\overline{PG}$ pin. Only when the SSx/$\overline{PG}$ pin is configured as $\overline{PG}$ through PIN_CONFIG_01 will TON_TRANSITION_RATE determine the soft-start rate.

The soft-start ramp rate refers to the rate at which the reference voltage is increased. The time to complete the soft-start can be calculated from the target reference voltage as Equation 6.

$$t_{ss} = \frac{Vref}{\text{Soft start ramp rate}} \quad (6)$$

For example, if VREF is set to 0.6 V and the default soft-start ramp rate of 0.5 V/ms is selected, then the soft-start time would be 1.2 ms. If VREF is set to 1 V and the soft-start ramp rate of 0.25 V/ms is selected, then the soft-start time would be 4 ms.

Table 35. TON_TRANSITION_RATE Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:2	—	R	000000	—	—	—
1:0	TON_RAMP_RATE	R/W	10	00	2 V/ms	Soft-start ramping rate
				01	1 V/ms	
				10	0.5 V/ms	
				11	0.25 V/ms	

PAGE support is for outputs 0x00 through 0x03.

8.5.4.16 (DFh) VREF_TRANSITION_RATE

The VREF_TRANSITION_RATE command determines the stepping rate and stepping size when dynamically switching the reference voltage VREF of the selected output.

Table 36. VREF_TRANSITION_RATE Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7	VREF_RAMP_ENABLE	R/W	1	0	—	Ramping disabled
				1	—	Ramping enabled
6	—	R	0	—	—	—
5:3	VREF_RAMP_TIMESTEP	R/W	011	000	1 µs	Delay time per ramping step
				001	2 µs	
				010	3 µs	
				011	4 µs	
				100	6 µs	
				101	8 µs	
				110	12 µs	
				111	16 µs	
2:0	VREF_RAMP_BITSTEP	R/W	000	See Table 37	See Table 37	Ramp up and ramp down LSB increments / decrements

Table 37. VREF_RAMP_BITSTEP Data Bit Values

VREF_RAMP_BITSTEP BINARY VALUE	RAMP UP (LSB increments)	RAMP DOWN (LSB decrements)
000 (default)	1	1
001	2	1
010	4	2
011	6	3
100	8	4
101	10	5
110	12	6
111	16	8

VREF_RAMP_BITSTEP sets the amount of voltage reference bits to ramp up and ramp down per VREF_RAMP_TIMESTEP time. During ramping, if the target step is less than or equal to the VREF_RAMP_BITSTEP setting, ramping reduces to a fine voltage step of 1 LSB per VREF_RAMP_TIMESTEP time until the target voltage has been reached. For the actual voltage change per LSB, refer to *(D8h) VREF_COMMAND*.

PAGE support is for outputs 0x00 through 0x03.

8.5.4.17 (F0h) SLOPE_COMPENSATION

The SLOPE_COMPENSATION command modifies control loop compensation parameters to compensate for inductor ripple current harmonics from switching.

Table 38. SLOPE_COMPENSATION Data Byte Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:2	—	R	000000	—	—	—

Table 38. SLOPE_COMPENSATION Data Byte Contents (continued)

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
1:0	SLOPE_COMPENSATION	R/W	01	00	45 mV/µs	Slope compensation
				01	70 mV/µs	
				10	100 mV/µs	
				11	145 mV/µs	

The default slope compensation will be adequate for most applications. The equivalent current slope compensation ramp on the inductor can be found by the following formula:

$$\Delta I_L = -G_{mps} \times SL_{comp} \quad (A/S) \tag{7}$$

Where Gmps is the current sense gain of the peak current control to COMP voltage in Amps per Volt and SLcomp is the slope compensation voltage expressed in the table above.

Ideal slope compensation is achieved when:

$$\left|\Delta I_L\right| > \frac{V_{out}}{L} \tag{8}$$

PAGE support is for outputs 0x00 through 0x03.

8.5.4.18 (F1h) ISENSE_GAIN

The ISENSE_GAIN command modifies the current sense G_{mps} of the feedback loop for the selected output. *(F0h) SLOPE_COMPENSATION* describes the equivalent current slope compensation ramp on the inductor.

Table 39. ISENSE_GAIN Data Byte Contents, PAGE = 0x00, 0x01

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:2	—	R	000000	—	—	—
1:0	ISENSE_GAIN	R/W	01	00	20 A/V	Current sense gain
				01	10 A/V	
				10	5 A/V	
				11	2.5 A/V	

Table 40. ISENSE_GAIN Data Byte Contents, PAGE = 0x02, 0x03

BITS	NAME	READ / WRITE	DEFAULT VALUE	BINARY VALUE	VALUE	MEANING
7:2	—	R	000000	—	—	—
1:0	ISENSE_GAIN	R/W	01	00	10 A/V	Current sense gain
				01	5 A/V	
				10	2.5 A/V	
				11	1.25 A/V	

PAGE support is for outputs 0x00 through 0x03.

8.5.4.19 (FCh) DEVICE_CODE

The DEVICE_CODE command returns a 2-byte read-only device code. For the TPS65400-Q1, this is 0x00FX, where 'X' is the revision/version number. This command has no PAGE support.

Table 41. DEVICE_CODE Data Word Contents

BITS	NAME	READ / WRITE	DEFAULT VALUE
15:4	DEVICE_CODE_ID	R	0x00F
3:0	DEVICE_CODE_REV	R	X

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65400-Q1 PMU is designed to support the trend towards smaller space-constrained systems, which require high-efficiency to limit power dissipation in a closed environment. The TPS65400-Q1 is intended to provide a complete highly-efficiency power management solution in a small form factor while providing maximum control through the I^2C bus and ease of use.

The TPS65400-Q1 can support input voltages from 4.5 to 18 V, allowing it to be used in systems powered from a single 5- or 12-V intermediate power bus. High system power conversion efficiency is achieved by providing a single-stage conversion from, for example, the 12-V input voltage to the high-current voltage rails required by the digital circuits.

The two buck regulators SW1 and SW2 can provide an output voltage in the range of 0.6 V to 90%Vin and up to 4-A peak continuous current.

The two buck regulators SW3 and SW4 can provide an output voltage in the range of 0.6 V to 90%Vin and up to 2-A peak continuous current. (1) (2)

(1) ESD using the human body model, which is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
(2) Maximum sustainable DC current depends on ambient temperature and IC power dissipation (see *Thermal Information*)

9.2 Typical Applications

9.2.1 Internal Operation Typical Application

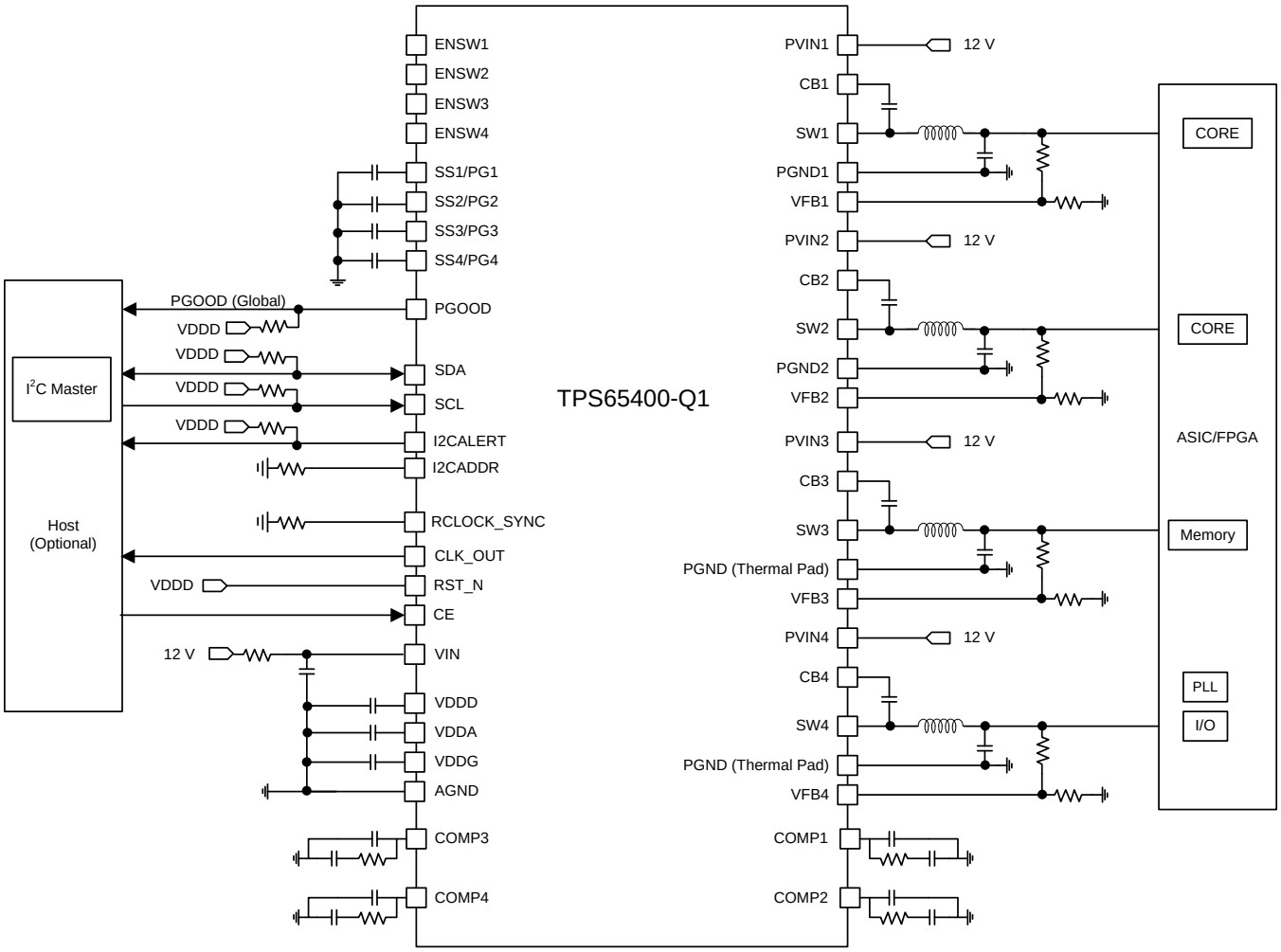


Figure 32. Typical Application Schematic

9.2.1.1 Design Requirements

Table 42 lists PMBus commands to configure this device.

Table 42. PMBus Commands Used for Internal Operation

COMMAND NAME	CODE	NAME	BITS	COMMENT
PAGE	00h	—	7:0	Selects output rail
STORE_DEFAULT_ALL	11h	—	—	Save settings as default
PIN_CONFIG_00	D2h	PGOOD_PIN_CONFIG	6:2	Configure PGOOD pin to mask PGOOD4
		ENABLE_PIN_CONFIG (1)	1:0	Active ENABLE (manufacturer default)
PIN_CONFIG_01	D3h	SSPG_PIN_CONFIG	0	Set to $\overline{PG}$ for internal soft-start
SEQUENCE_CONFIG	D4h	START_PGOOD	0	Disable PGOOD dependence
SEQUENCE_ORDER	D5h	START_ORDER	3:2	Start sequence order
		STOP_ORDER	1:0	Stop sequence order
RESET_DELAY	DCh	RESET_DELAY (1)	2:0	Reset delay time

(1) Only necessary if the defaults have been overwritten since device manufacture

Typical Applications (continued)

Table 42. PMBus Commands Used for Internal Operation (continued)

COMMAND NAME	CODE	NAME	BITS	COMMENT
TON_TOFF_DELAY	DDh	TON_DELAY	5:3	Delay time before starting
		TOFF_DELAY	2:0	Delay time before stopping
TON_TRANSITION_RATE	DEh	TON_RAMP_RATE	1:0	Internal soft-start ramping rate

To achieve the timing requirements shown in Table 42, an example configuration script is shown in Table 43.

Table 43. Example Configuration Script for Internal Operation

COMMAND NAME	CODE	WRITE BYTE	COMMENT
PAGE	00h	0xFF	Selects all
PIN_CONFIG_00	D2h	0x1C	PGOOD pin is a function of PGOOD1 and PGOOD2 and PGOOD3
SEQUENCE_CONFIG	D4h	0x01	Disable PGOOD dependence
RESET_DELAY(1)	DCh	0x02	100-ms reset delay
PAGE	00h	0x00	Selects SW1
PIN_CONFIG_01	D3h	0x01	Configure SS1/PG1 pin to PG1 for internal soft-start
SEQUENCE_ORDER	D5h	0x08	First to Start, third to Stop
TON_TOFF_DELAY	DDh	0x04	0-ms turn-on delay 100-ms turn-off delay
TON_TRANSITION_RATE	DEh	TON_RAMP_RATE	Internal soft-start ramping rate
PAGE	00h	0x02	Selects SW3
PIN_CONFIG_01	D3h	0x01	Configure SS3/PG3 pin to PG3 for internal soft-start
SEQUENCE_ORDER	D5h	0x05	Second to start, second to stop
TON_TOFF_DELAY	DDh	0x23	100-ms turn-on delay 25-ms turn-off delay
TON_TRANSITION_RATE	DEh	TON_RAMP_RATE	Internal soft-start ramping rate
PAGE	00h	0x01	Selects SW2
PIN_CONFIG_01	D3h	0x01	Configure SS2/PG2 pin to PG2 for internal soft-start
SEQUENCE_ORDER	D5h	0x02	Third to start, first to stop
TON_TOFF_DELAY	DDh	0x23	100-ms turn-on delay 25-ms turn-off delay
TON_TRANSITION_RATE	DEh	TON_RAMP_RATE	Internal soft-start ramping rate
STORE_DEFAULT_ALL	11h	—	Save settings as default

(1) Only necessary if the defaults have been overwritten after device manufacture.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Component Selection

9.2.1.2.1.1 Output Inductor Selection

Equation 9 gives the current ripple flowing in the inductor in CCM.

$$\Delta I_L = \frac{V_{out} \times \left(1 - \frac{V_{out}}{V_{in}}\right)}{L \times f_{sw}}$$

where

- ΔI_L is the current ripple in the inductor.
- V_{out} is the output voltage.
- V_{in} is the input voltage of the converter.
- L is the value of the inductor in henry.

- f_{sw} is the switching frequency of the converter. (9)

Typically, the value of L is chosen to have the ripple current be 0.1× to 0.3× the full-load current. Choose the inductor so that the saturation current is higher than the maximum expected current plus half the current ripple at maximum operating temperature.

9.2.1.2.1.2 Output Capacitor Selection

The output capacitor needs to be properly sized to reduce voltage ripple due to the switching action (ripple voltage) and to reduce output voltage swings during transient load currents. Equation 10 gives the output voltage ripple.

$$\Delta V_{out\_ripple} = \frac{(V_{in} - V_{out}) \times V_{out}}{8 f_{sw}^{2} \times C \times L \times V_{in}} \quad (10)$$

Equation 11 gives the voltage variation during output current transients.

$$\Delta V_{out\_transient} = \frac{\Delta I_{out\_transient}^{2} \times L}{C_o \times V_{out}} \quad (11)$$

9.2.1.2.2 Internal Operation With Some Switchers Disabled

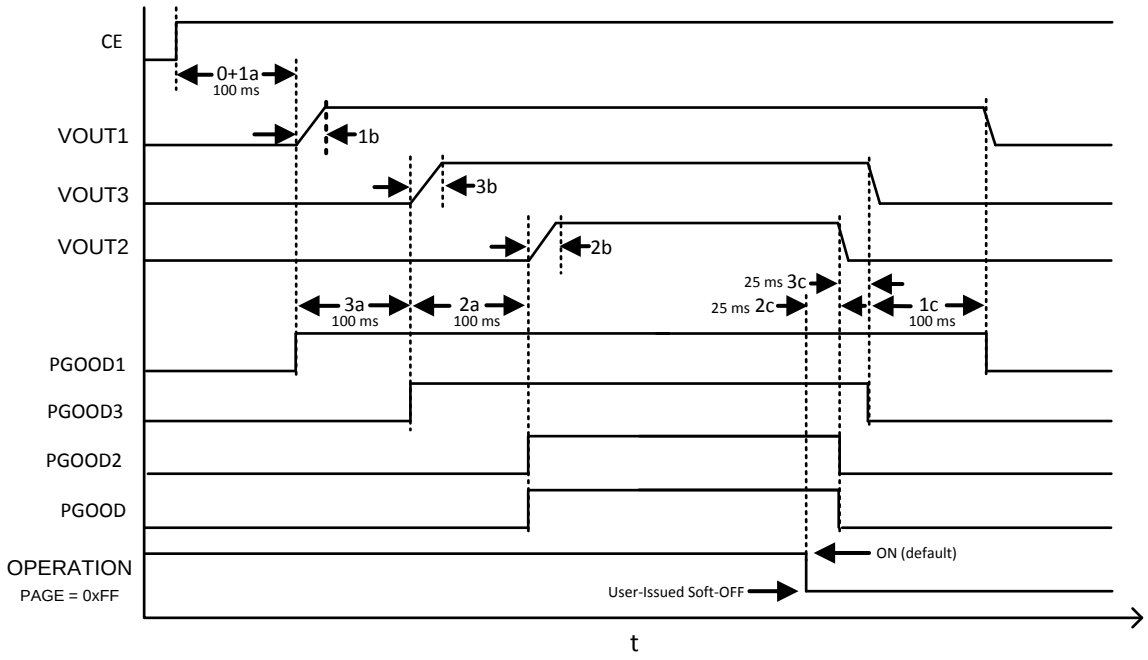
For applications where the internal settings for sequencing and soft-start are sufficient, all used output rails should have their enable terminals ENSWx tied high or floating and all unused output rails should have their enable pins ENSWx tied low for the default active ENABLE setting of ENABLE_PIN_CONFIG. This prevents the device from turning on an unused output by software default from an OPERATION ON request. This requirement extends to unpowered switchers; if a pair of switchers is unused, then both ENSWx pins must be tied low.

9.2.1.2.3 Internal Operation With All Switchers Enabled

For applications where all outputs rails will be used, it is sufficient to leave all enable terminals ENSWx disconnected and to set ENABLE_PIN_CONFIG to inactive.

9.2.1.2.4 Example Configuration

Figure 33 shows an internal sequencing schematic example where only switchers 1 to 3 are used for a set of timing requirements. If the internal configuration and fault handling is sufficient, and provided that the user configures the chip through SDA/SCL before placing it on a target board, then it is not necessary for a supervisory and housekeeping host controller chip like a MCU or DSP to be connected to the TPS65400-Q1. In such a case, digital terminals PGOOD, SSx/$\overline{PG}$, SDA/SCL, I2CALERT, and CLK_OUT can be left unconnected with no pull-ups required, during normal operation. RST_N can be tied directly to VDDD (no pull-up required). I2CADDR can be tied directly to VDDD after programming. Control line CE can be left unconnected if the chip is constantly powered after VIN is provided.



0. RESET_DELAY 1. SW1 2. SW2 3. SW3

a. TON_DELAY b. V_{REF} / TON_RAMP_RATE c. TOFF_DELAY

PGOOD dependence disabled, switcher 4 disabled

Figure 33. Example Timing Diagram for Internal Sequencing

9.2.1.2.5 Unused Switchers

If the default setting active ENABLE of ENABLE_PIN_CONFIG is selected, ENSWx for unused switchers must always be tied low.

9.2.1.3 Application Curves

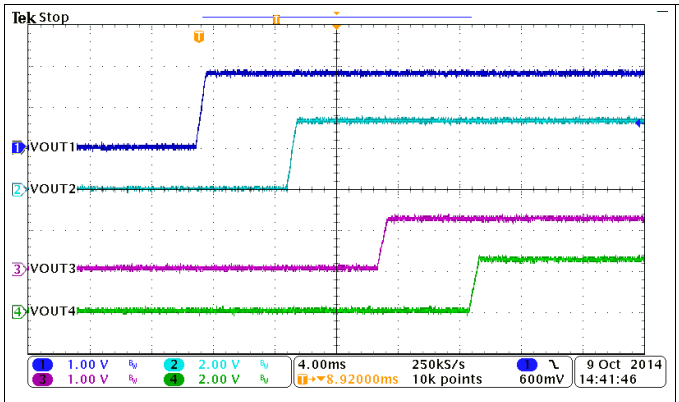


Figure 34. Configurable Power-Up Sequence

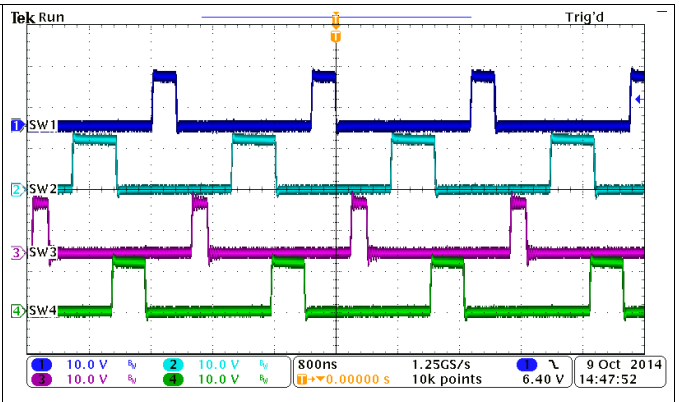


Figure 35. Phase Shift Between Channels

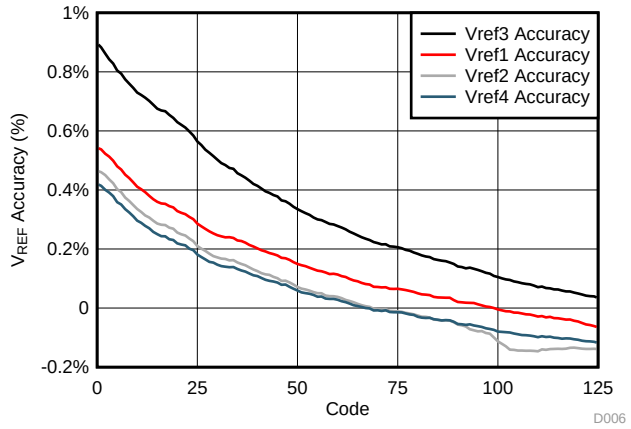


Figure 36. V_{REF} Accuracy vs Code

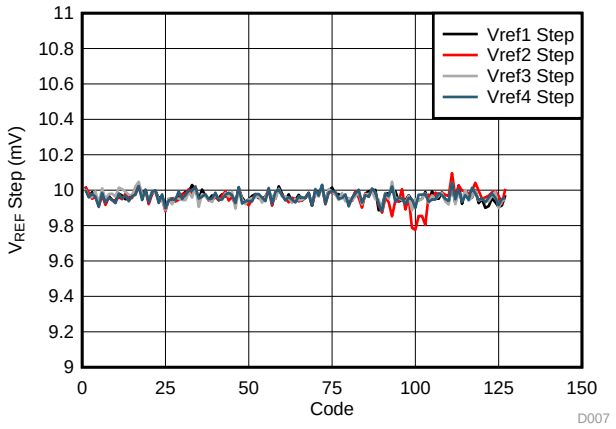


Figure 37. V_{REF} Step Accuracy vs Code

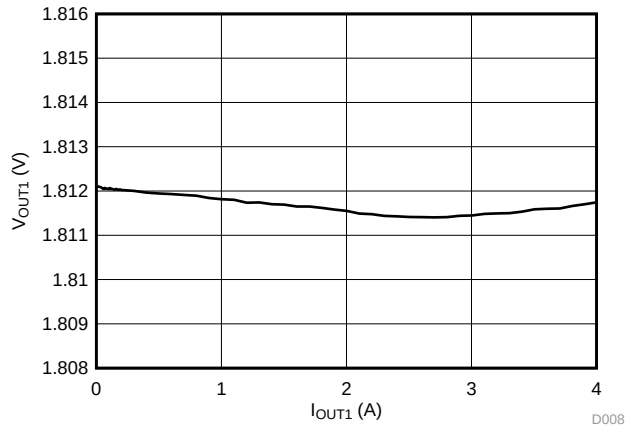


Figure 38. V_{OUT1} Load Regulation

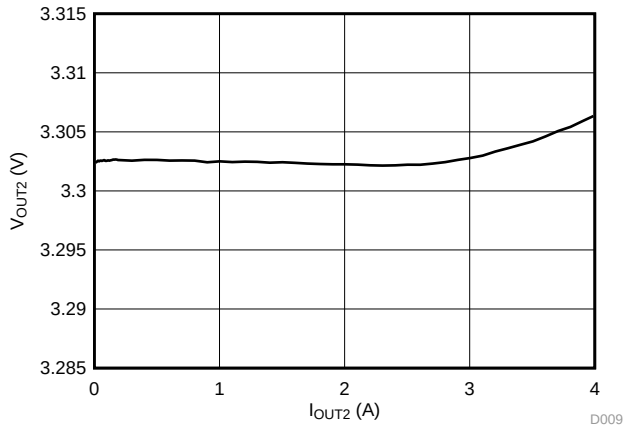


Figure 39. V_{OUT2} Load Regulation

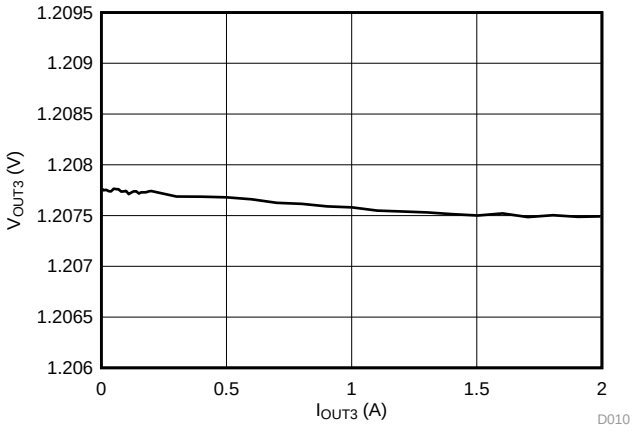


Figure 40. V_{OUT3} Load Regulation

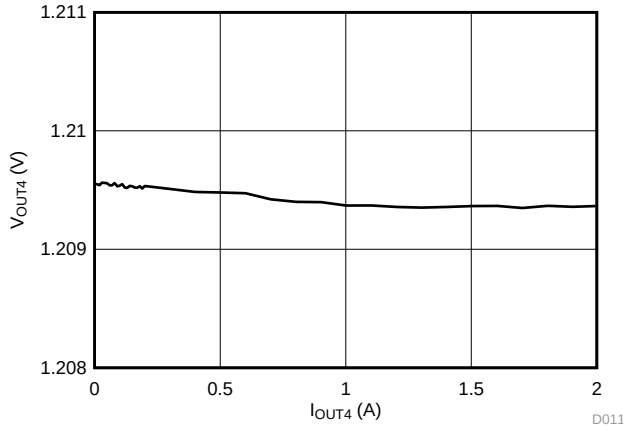


Figure 41. V_{OUT4} Load Regulation

9.2.2 Current Sharing Typical Application

An example configuration is shown where both pairs of outputs are current shared. Soft-start time is configured externally with capacitors (this is the default setting) and ENABLE_PIN_CONFIG is set to single ENABLE.

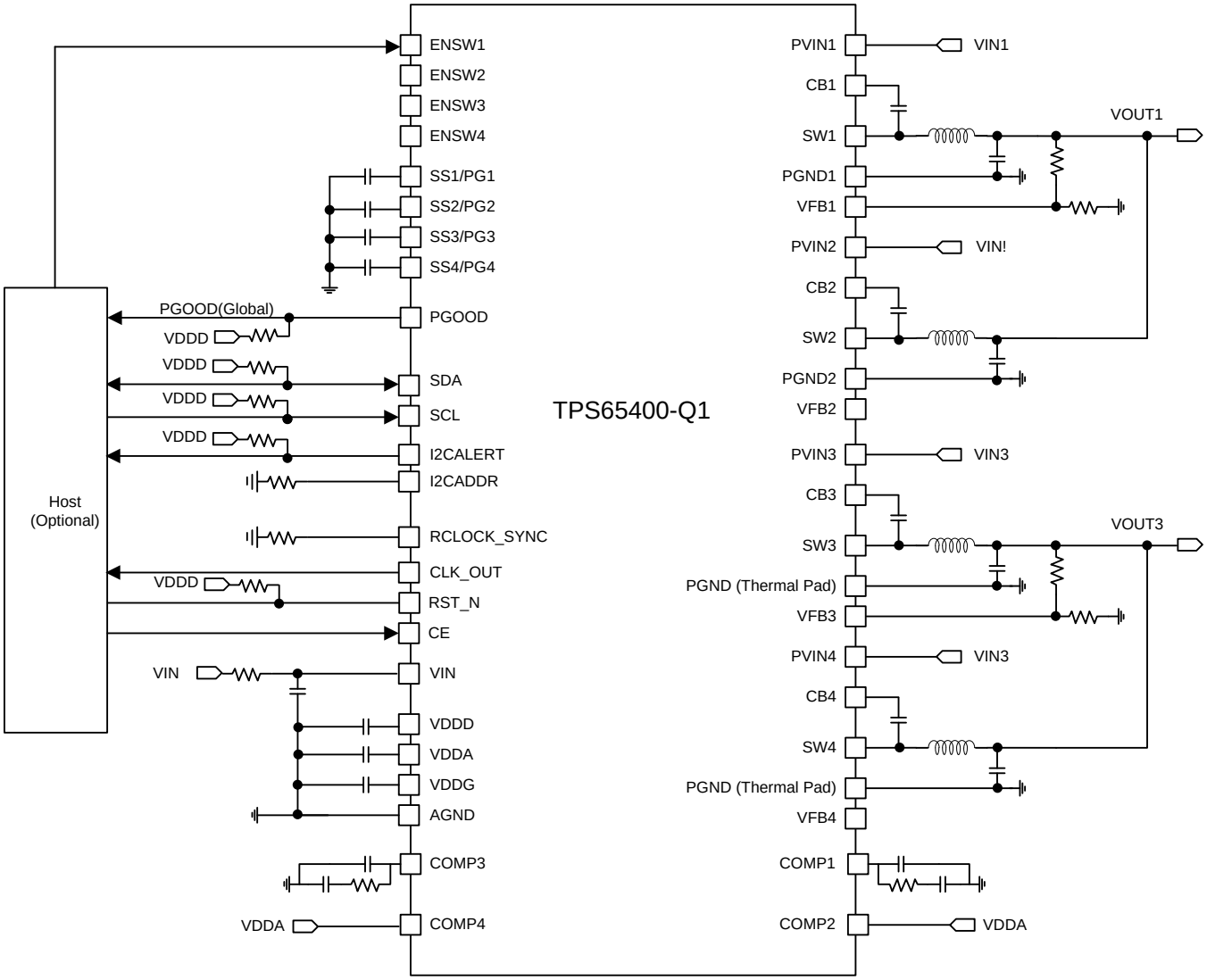


Figure 42. Current Sharing Schematic

9.2.2.1 Design Requirements

Table 44 lists PMBus commands to configure this device.

Table 44. PMBus Commands Used for Current Sharing With Single-Pin Enable(1)

COMMAND NAME	CODE	NAME	BITS	COMMENT
PAGE	00h	—	7:0	Selects output rail
STORE_DEFAULT_ALL	11h	—	—	Save settings as default
PIN_CONFIG_00	D2h	PGOOD_PIN_CONFIG(1)	6:2	PGOOD pin and of all $\overline{\text{PGOOD}}$ (manufacturer default)
		ENABLE_PIN_CONFIG	1:0	Single ENABLE
PIN_CONFIG_01	D3h	SSPG_PIN_CONFIG(1)	0	Set to SSx for external soft-start (manufacturer default)
SEQUENCE_CONFIG	D4h	START_PGOOD(1)	0	Enable PGOOD dependence (manufacturer default)
SEQUENCE_ORDER	D5h	START_ORDER	3:2	Start sequence order
		STOP_ORDER	1:0	Stop sequence order
TON_TOFF_DELAY	DDh	TON_DELAY	5:3	Delay time before starting
		TOFF_DELAY	2:0	Delay time before stopping

(1) Only necessary if the defaults have been overwritten since device manufacture.

To achieve the timing requirements shown in Table 44, see the example configuration script in Table 45.

Table 45. Example Configuration Script for Current Sharing With Single-Pin Enable

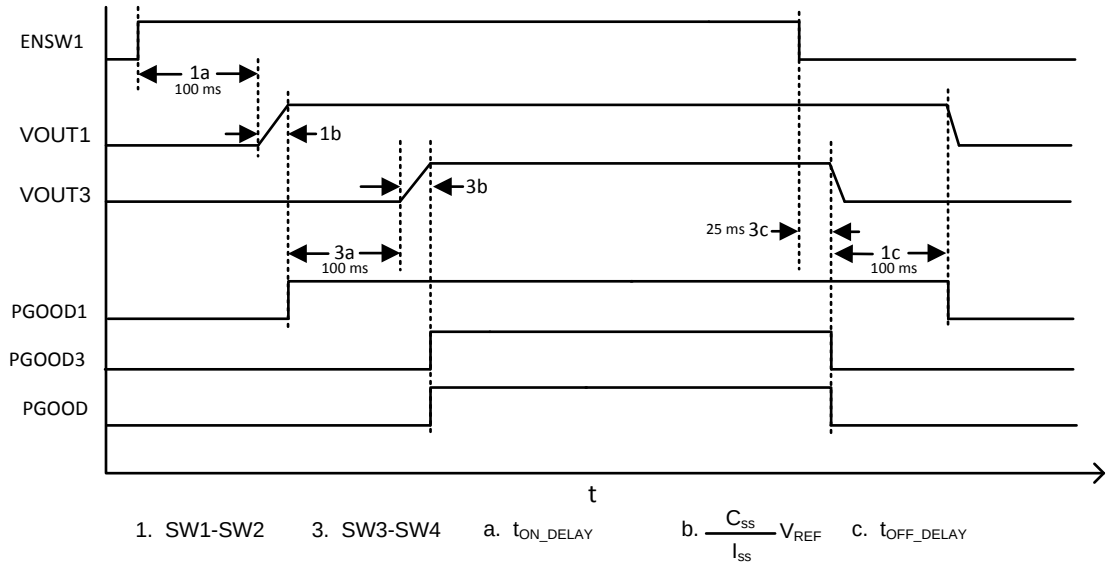
COMMAND NAME	CODE	WRITE BYTE	COMMENT
PAGE	00h		Selects all
PIN_CONFIG_00	D2h		Single ENABLE
SEQUENCE_CONFIG(1)	D4h		Enable PGOOD dependence (manufacturer default)
PAGE	00h		Selects SW1 to SW2 pair
PIN_CONFIG_01(1)	D3h		Configure SS1/PG1 pin to SS1 for external soft-start (manufacturer default)
SEQUENCE_ORDER	D5h	0x04	First to start, second to stop
TON_TOFF_DELAY	DDh	0x24	100-ms turn-on delay 100-ms turn-off delay
PAGE	00h	0x02	Selects SW3 to SW4 pair
PIN_CONFIG_01(1)	D3h	0x00	Configure SS2/PG2 pin to SS2 for external soft-start (manufacturer default)
SEQUENCE_ORDER	D5h	0x01	Second to start, first to stop
TON_TOFF_DELAY	DDh	0x23	100-ms turn-on delay 25-ms turn-off delay
STORE_DEFAULT_ALL	11h	—	Save settings as default

(1) Only necessary if the defaults have been overwritten since device manufacture.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Current Sharing Timing Example

Figure 43 shows an example configuration in which both the SW1-SW2 pair and SW3-SW4 pair are current shared. The enable pin of the slave converter can either follow the master converter or be floating. For the PGOOD pin, the slave PGOOD follows the master PGOOD. Due to internal pull-ups to VDDD on ENSWx lines, the user has an option to control ENSWx if an always on condition is desired.

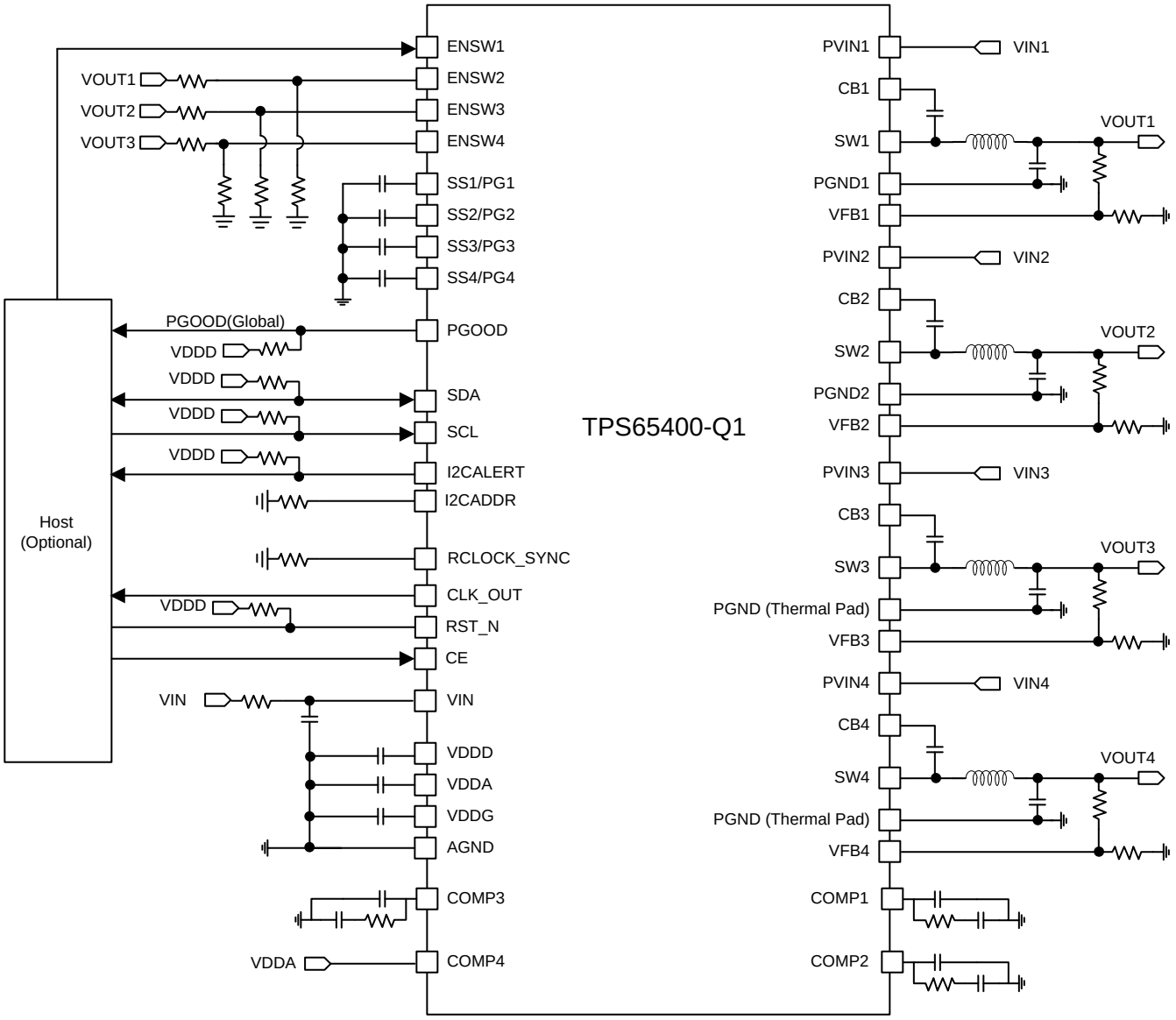


A. External soft-start, single ENABLE

Figure 43. Example Timing Diagram for Current Sharing With Single-Pin Enable

9.2.3 External Sequencing Application

Figure 44 shows an example configuration where the VOUT outputs are linked to enable terminal ENSWx inputs in a daisy-chain configuration for start sequence SW1-SW2-SW3-SW4.



A. Sequencing through $\overline{\text{VOUT}}$

Figure 44. External Sequencing Schematic, $\overline{\text{Vout}}$ > VEN

9.2.3.1 Design Requirements

Table 46 and Table 47 list PMBus commands to configure this device.

Table 46. PMBus Commands Used for External Sequencing through $\overline{\text{VOUT}}$

COMMAND NAME	CODE	NAME	BITS	COMMENT
PAGE	00h	—	7:0	Selects output rail
STORE_DEFAULT_ALL	11h	—	—	Save settings as default
PIN_CONFIG_00	D2h	PGOOD_PIN_CONFIG(1)	6:2	PGOOD pin and of all $\overline{\text{PGOOD}}$ (manufacturer default)
		ENABLE_PIN_CONFIG(1)	1:0	Active ENABLE (manufacturer default)
PIN_CONFIG_01	D3h	SSPG_PIN_CONFIG(1)	0	Set to SSx for external soft-start (manufacturer default)
TON_TOFF_DELAY	DDh	TON_DELAY	5:3	Delay time before starting
		TOFF_DELAY(1)	2:0	Delay time before stopping
RESET_DELAY	DCh	RESET_DELAY(1)	2:0	Reset delay time

(1) Only necessary if the defaults have been overwritten since device manufacture.

To achieve the timing requirements shown in Table 46, see Table 47 for an example configuration script.

Table 47. Example Configuration Script for External Sequencing through $\overline{\text{VOUT}}$

COMMAND NAME	CODE	WRITE BYTE	COMMENT
PAGE	00h	0xFF	Selects all
PIN_CONFIG_00(1)	D2h	0x3C	Active ENABLE (manufacturer default)
RESET_DELAY(1)	DCh	0x02	100-ms reset delay
PAGE	00h	0x00	Selects SW1
PIN_CONFIG_01(1)	D3h	0x00	Configure SS1/PG1 pin to SS1 for external soft-start
TON_TOFF_DELAY	DDh	0x20	100-ms turn-on delay 0-ms turn-off delay
PAGE	00h	0x01	Selects SW2
PIN_CONFIG_01(1)	D3h	0x00	Configure SS2/PG2 pin to SS2 for external soft-start
TON_TOFF_DELAY	DDh	0x20	100-ms turn-on delay 0-ms turn-off delay
PAGE	00h	0x02	Selects SW3
PIN_CONFIG_01(1)	D3h	0x00	Configure SS3/PG3 pin to SS3 for external soft-start
TON_TOFF_DELAY	DDh	0x20	100-ms turn-on delay 0-ms turn-off delay
PAGE	00h	0x03	Selects SW4
PIN_CONFIG_01(1)	D3h	0x00	Configure SS4/PG4 pin to SS4 for external soft-start
TON_TOFF_DELAY	DDh	0x20	100-ms turn-on delay 0-ms turn-off delay
STORE_DEFAULT_ALL	11h	—	Save settings as default

(1) Only necessary if the defaults have been overwritten since device manufacture.

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 External Sequencing Through $\overline{\text{PG}}$ Pins

In an application where the programmable soft-start ramping rate is sufficient and where stop sequencing is not required, it is possible to wire Power Good pins (global PGOOD, $\overline{\text{PG}}$) to enable pins (ENSWx) according to the desired start sequence. This is useful in cases where multiple PMUs are configured and the $\overline{\text{PG}}$ or global PGOOD output of one PMU is required to turn on an output of another PMU.

9.2.3.2.2 External Sequencing Through $\overline{\text{SW}}$

In an application where output voltages exceed the threshold voltage of the enable pins ENSWx, it is possible to wire a properly divided VOUT directly to the enable pins according to the desired start sequence.

9.2.3.2.3 Example Configuration

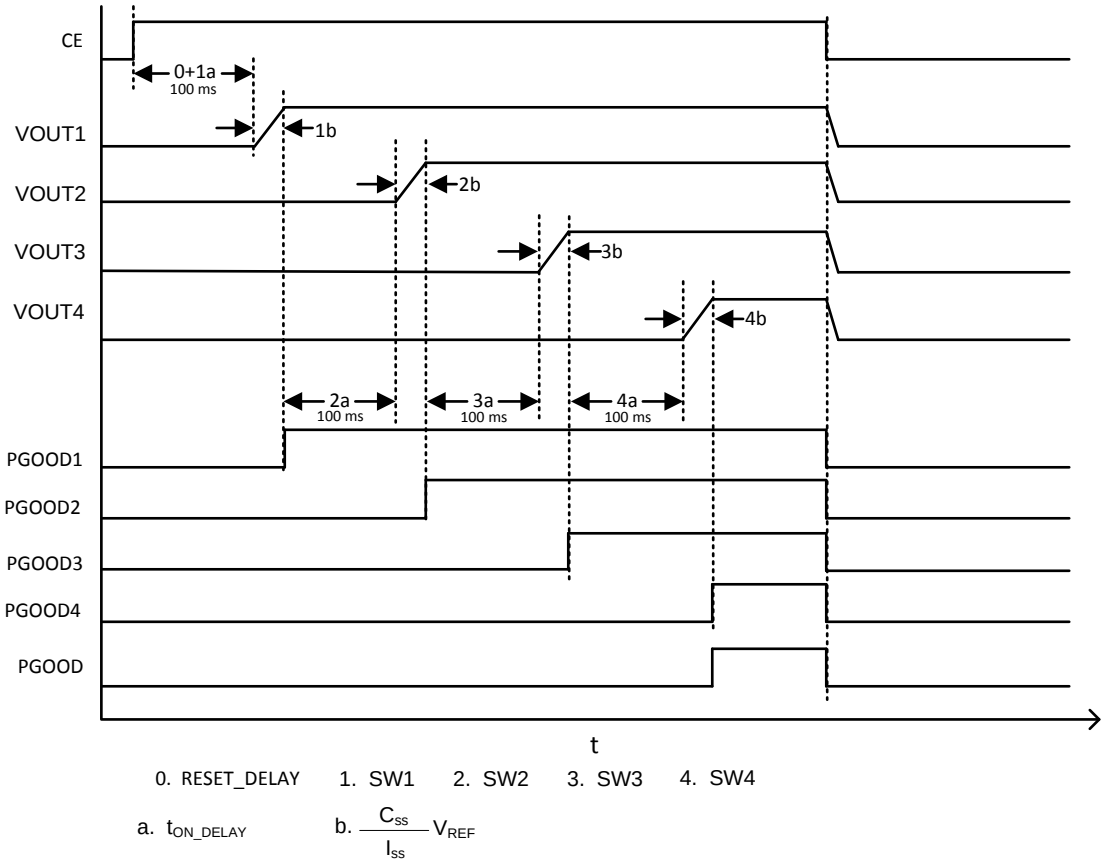


Figure 45. Example Timing Diagram for External Sequencing Through $\overline{VOUT}$

NOTE

Only necessary if the defaults have been overwritten since device manufacture.

10 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 and 18 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65400-Q1 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of high-current multi-channel DC-DC. Follow these guidelines for layout. See *Layout Example* for a PCB layout example.

- Place VOUT and SW on the top layer and an inner power plane for VIN.
- Also on the top layer, fit connections for the remaining pins of TPS65400-Q1 and a large top-side area filled with ground.
- Connect the top layer ground area to the internal ground layer or layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS65400-Q1 device to provide a thermal path from the power pad to ground.
- Tie the AGND pin directly to the power pad under the IC.
- For operation at full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipating area.
- Several signals paths conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies' performance. To help eliminate these problems, bypass the VIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Because the SW connection is the switching node, the output inductor should be located close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIND input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.
- The VFB node is a high-impedance analog node which is easier to pick noise on board. Keep FB node trace as short as possible.

11.2 Layout Example

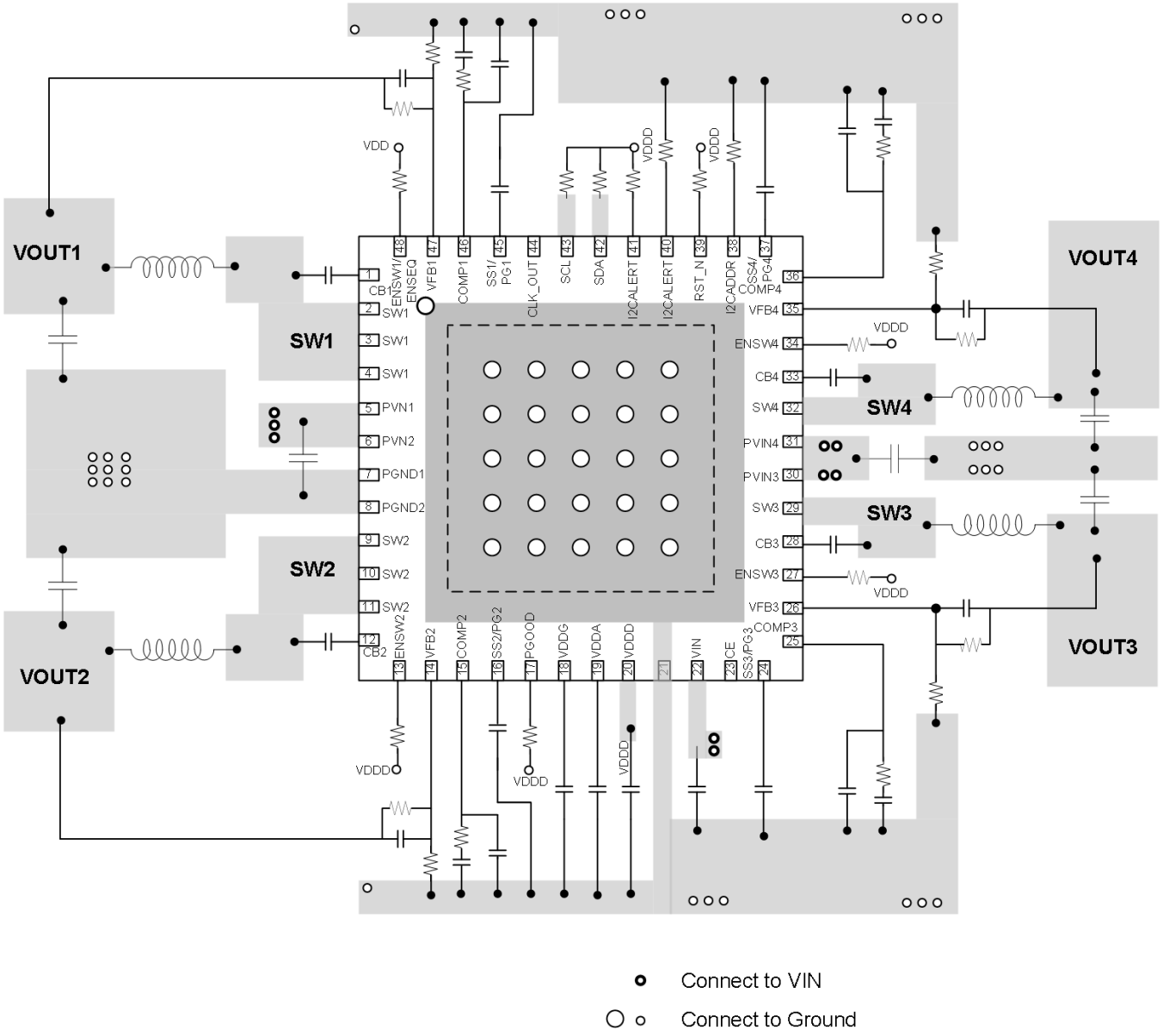


Figure 46. Layout Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *PMBus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface*, Revision 1.2, dated 6 September 2010, published by the Power Management Bus Implementers Forum (http://pmbus.org/Specifications).

12.1.2 Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
TPS65262	4.5- to 18-V, triple buck with dual adjustable LDOs	Triple buck 3-A/1-A/1-A output current, dual LDOs 100-mA/200-mA output current, automatic power sequencing
TPS65263	4.5- to 18-V, triple buck with I^2C interface	Triple buck 3-A/2-A/2-A output current, I^2C-controlled dynamic voltage scaling (DVS)
TPS65651-1/2/3	4.5- to 18-V, triple buck with different PGOOD deglitch time	Triple buck 3-A/2-A/2-A output current, support 1-s, 32-ms, and 256-ms PGOOD deglitch time, adjustable current limit setting by external resistor
TPS65287	4.5- to 18-V, triple buck with power switch and push-button control	Triple buck 3-A/2-A/2-A output current, up to 2.1-A USB power with overcurrent setting by external resistor, push-button control for intelligent system power-on/power-off operation
TPS65288	4.5- to 18-V, triple buck with dual power switches	Triple buck 3-A/2-A/2-A output current, 2 USB power switches current limiting at typical 1.2 A (0.8/1/1.4/1.6/1.8/2/2.2 A available with manufacture trim options)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65400QRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65400Q	Samples
TPS65400QRGZTQ1	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65400Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS65400-Q1 :

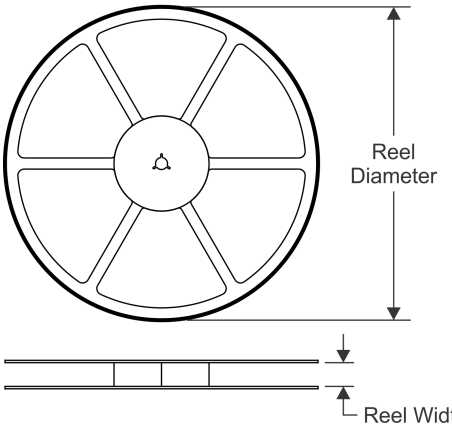
- Catalog: TPS65400

NOTE: Qualified Version Definitions:

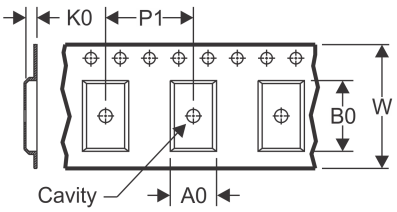
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

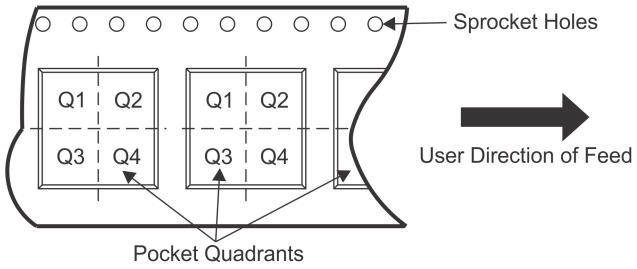


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

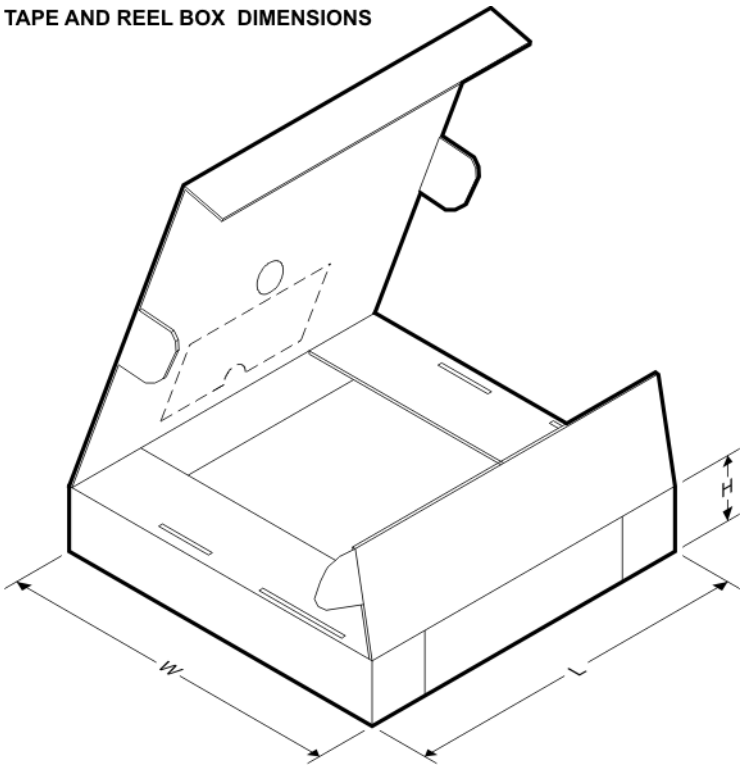
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65400QRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TPS65400QRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

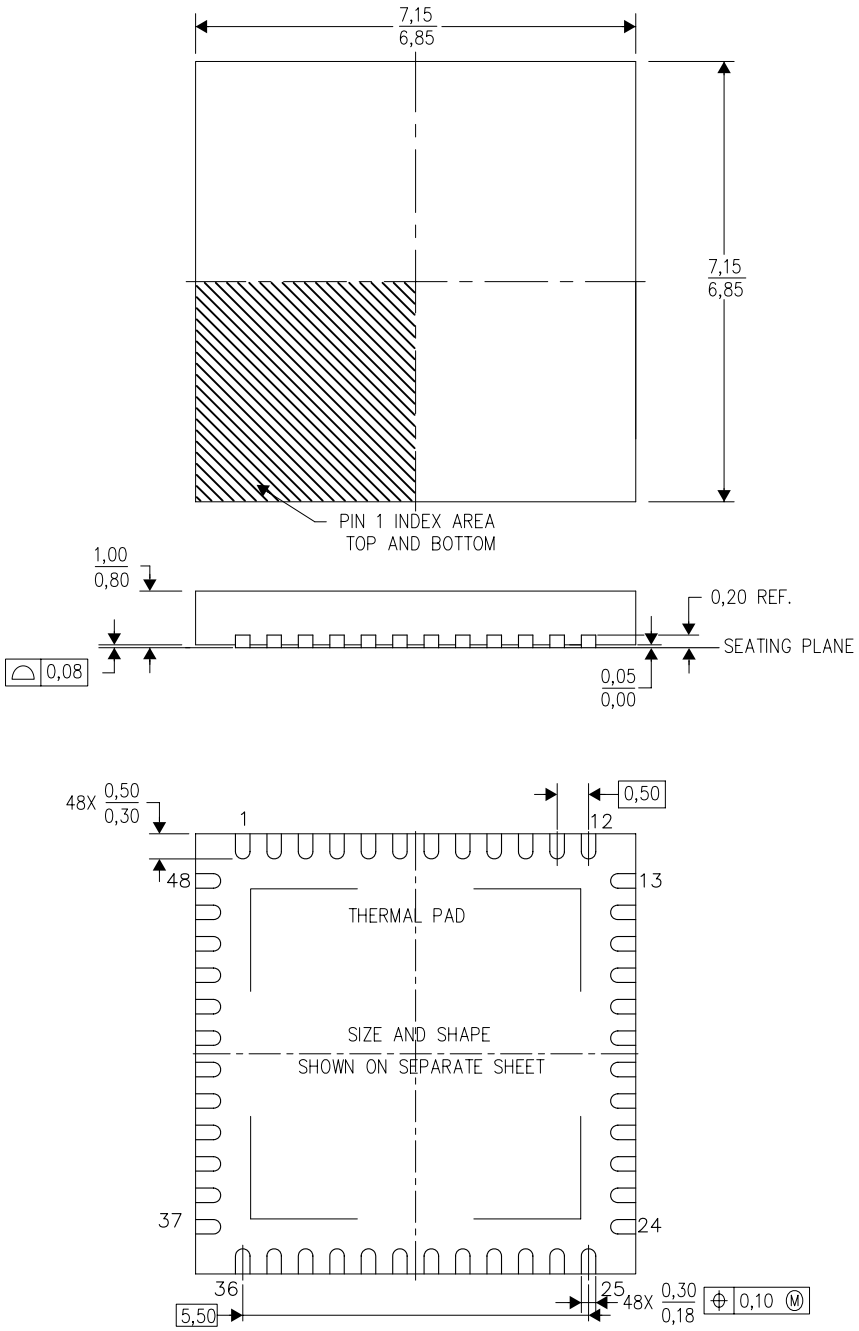
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65400QRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65400QRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

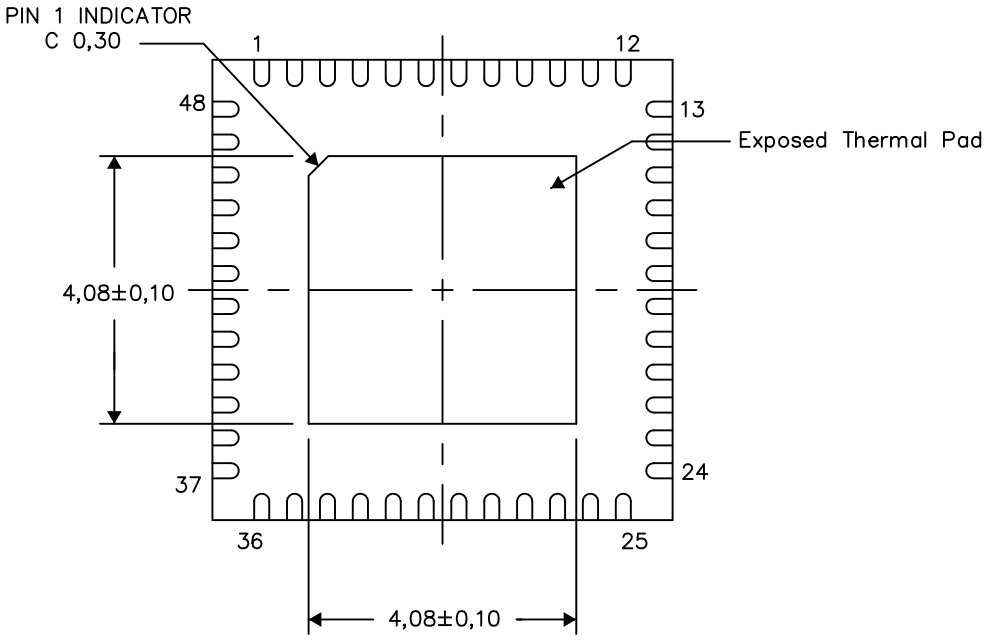
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206354–8/Z 03/15

NOTE: All linear dimensions are in millimeters

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265