TEXAS INSTRUMENTS

TPS65235-1 LNB Voltage Regulator With I²C Interface

1 Features

- Complete Integrate Solution for LNB and I²C Interface
- DiSEqC 2.x, and DiSEqC 1.x Compatible
- Supports 5 V, 12 V and 15 V Power Rail
- Up to 1000 mA Accurate Output Current Limit Adjustable by External Resistor
- Boost Switch Peak Current Limit Proportional to LDO Current Limit
- Boost Converter with 140 mΩ Low $R_{ds(on)}$ Internal Power Switch
- Boost Switching Frequency 1 MHz or 500 kHz Selectable
- Audible Noise Avoided at Force PWM Mode
- Dedicated Enable Pin for Non-I²C Application
- Low Drop Output LDO With Push-pull Output Stage for VLNB Output
- Built-in Accurate 22-kHz Tone Generator and External Tone Input Support
- Supports Both External 44-kHz and 22-kHz Tone Input
- Adjustable Soft-start and 13-V to 18-V Voltage Transition Time
- 650 mV to 750 mV 22-kHz Tone Amplitude Selection
- I²C Registers Accessible with EN Low
- Short Circuit Dynamic Protection
- Diagnostics for Output Voltage Level, DiSEqC Tone Input and Output, Current Level, and Cable Connection
- Thermal Protection Available
- 20-Lead WQFN 3 mm x 3 mm (RUK) Package

2 Applications

- Set Top Box Satellite Receiver
- TV Satellite Receiver
- PC card Satellite Receiver
- Satellite TV

3 Description

Designed for analog and digital satellite receivers, the TPS65235-1 is a monolithic voltage regulator with I²C interface; specifically to provide the 13-V to 18-V power supply and the 22-kHz tone signal to the LNB down converter in the antenna dish or to the multi-switch box. It offers a complete solution with minimum component count, low power dissipation together with simple design and I²C standard interface.

TPS65235-1 features high power efficiency. The boost converter integrates a 140-mΩ power MOSFET running at 1 MHz or 500 kHz selectable switching frequency. Drop out voltage at the linear regulator is 0.8 V to minimize power loss. TPS65235-1 provides multiple ways to generate the 22 kHz signal. Integrated linear regulator with push-pull output stage generates 22-kHz tone signal superimposed at the output even at zero loading. Current limit of linear regulator can be programmed by external resistor with ±10% accuracy. Full range of diagnostic read by I²C is available for system monitoring.

TPS65235-1 has a special design at FCCM mode to avoid the audible noise especially when VIN is higher or closer to the VLNB output.
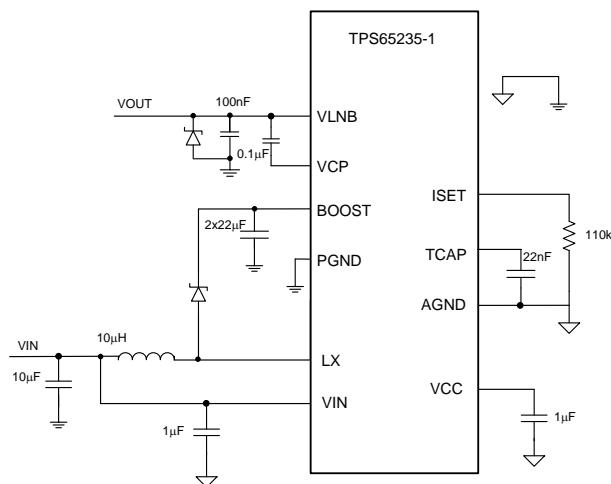
TPS65235-1 supports advanced DiSEqC 2.x standard with 22-kHz tone detection circuit and output interface.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65235-1	WQFN	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

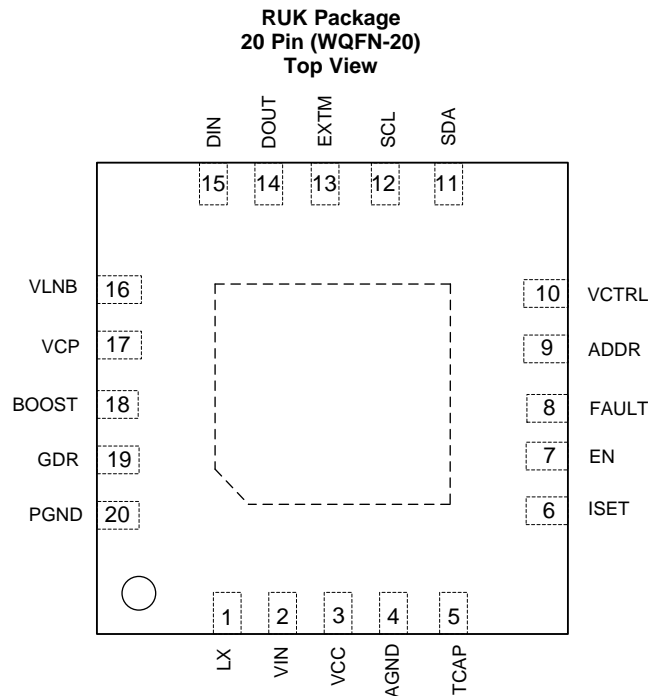Copyright © 2016, Texas Instruments Incorporated

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4 Revision History

DATE	REVISION	NOTES
January 2017	*	Initial release.

5 Pin Configuration and Functions

RUK Package
20 Pin (WQFN-20)
Top View

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
LX	1	I	Switching node of the boost converter
VIN	2	S	Input of internal linear regulator
VCC	3	O	Internal 6.3-V power supply. Connect a 1-µF ceramic capacitor from this pin to ground. When V_{IN} is 5 V, connect VCC to VIN.
AGND	4	S	Analog ground. Connect all ground pins and power pad together.
TCAP	5	O	Connect a capacitor to this pin to set the rise time of the LNB output.
ISET	6	O	Connect a resistor to this pin to set the LNB output current limit.
EN	7	I	Enable pin to enable the VLNB output; pull to ground to disable output, and output will be pulled to ground, when the EN is low, the I²C can be accessed
FAULT	8	O	Open drain output pin, it goes low if any fault flag is set.
ADDR	9	I	Connecting different resistor to this pin to set different I²C address, see Table 4.
VCTRL	10	I	Voltage level at this pin to set the output voltage, see Table 3.
SDA	11	I/O	I²C compatible bi-directional data
SCL	12	I	I²C compatible clock input
EXTM	13	I	External modulation logic input pin which activates the 22-kHz tone output, feeding signal can be 22-kHz tone or logic high or low.
DOUT	14	O	Tone detection output
DIN	15	I	Tone detection input
VLNB	16	O	Output of the power supply connected to satellite receiver or switch.
VCP	17	O	Gate drive supply voltage, output of charge pump, connect a capacitor between this pin to pin VLNB.
BOOST	18	O	Output of the boost regulator and Input voltage of the internal linear regulator.
GDR	19	O	Control the gate of the external MOSFET for DiSEqc 2.x support.
PGND	20	S	Power ground for Boost Converter
Thermal PAD			Must be soldered to PCB for optimal thermal performance. Have thermal Vias on the PCB to enhance power dissipation.

(1) I = input, O = output, I/O = input and output, S = power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	VIN, LX, BOOST, VLNB	1	30	V
	VCP	VLNB	7	
	GDR	VLNB	VCP	
	VCC, EN, ADDR, FAULT, SCL, SDA, VCTRL, EXTM, DOUT, DIN, TCAP	−0.3	7	
	ISET	−0.3	3.6	
	PGND	−0.3	0.3	
Operating junction temperature, T_J		−40	150	°C
Storage temperature, T_{stg}		−55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input operating voltage	4.5		20	V
T_A	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS65235-1 RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range	VIN	4.5	12	20	V
$I_{DD(SDN)}$	Shutdown supply current	EN = 0	90	120	150	µA
$I_{LDO(Q)}$	LDO quiescent current	EN = 1, I_O = 0 A, VLNB = 18.2 V	1.5	5	8.5	mA
UVLO	V_{IN} Undervoltage Lockout	V_{IN} Rising	4.15	4.3	4.45	V
		Hysteresis	280	480	550	mV
OUTPUT VOLTAGE						
V_{OUT}	Regulated output voltage	$V_{(ctrl)}$ = 1, I_O = 500 mA	18	18.2	18.4	V
		$V_{(ctrl)}$ = 0, I_O = 500 mA	13.25	13.4	13.55	V
		SCL = 1, $V_{(ctrl)}$ = 1, I_O = 500 mA (Non I²C)	19.18	19.4	19.62	V
		SCL = 1, $V_{(ctrl)}$ = 0, I_O = 500 mA (Non I²C)	14.44	14.6	14.76	V
$I_{(OCP)}$	Output short circuit current limit	$R_{(SET)}$ = 200 kΩ, Full temperature	580	650	720	mA
		T_J = 25°C	629	650	688	mA
Fsw	Boost switching frequency	1 MHz	977	1060	1134	kHz
$I_{(limitsw)}$[(1)]	Switching current limit	V_{IN} = 12 V, V_{OUT} = 18.2 V, $R_{(SET)}$ = 200 kΩ	2.4	3	3.6	A
$R_{ds(on)\_LS}$	On resistance of low side FET	V_{IN} = 12 V	90	140	210	mΩ
$V_{(drop)}$	Linear regulator voltage drop-out	I_O = 500 mA, TONEAMP = 0	0.44	0.7	1	V
		I_O = 500 mA, TONEAMP = 1	0.55	0.8	1.12	V
$I_{(cable)}$	Cable good detection current threshold	V_{IN} = 12 V, V_{OUT} = 13.4 V or 18.2 V	0.9	5	8.8	mA
$I_{(rev)}$	Reverse bias current	EN = 1, VLNB = 21 V	49	58	65	mA
$I_{(rev\_dis)}$	Disabled reverse bias current	EN = 0, VLNB = 21 V	3.72	4.6	5.63	mA
LOGIC SIGNALS						
$V_{(EN)}$	Enable threshold High		1.6			V
	Enable threshold Low				0.8	V
$I_{(EN)}$	Enable internal pull up current	$V_{(EN)}$ = 1.5 V	5	6	7	µA
		$V_{(EN)}$ = 1 V	2	3	4	µA
$V_{(VCTRL\_H)}$ $V_{(EXTM\_H)}$	VCTRL, EXTM Logic threshold level	High level input voltage	2			V
$V_{(VCTRL\_L)}$ $V_{(EXTM\_L)}$		Low level input voltage			0.8	V
$V_{OL(FAULT)}$	FAULT output low voltage	FAULT open drain, I_{OL} = 1 mA			0.4	V
TONE						
$f_{(tone)}$	Tone frequency	22 kHz tone output	20	22	24	kHz
$A_{(tone)}$	Tone amplitude	I_O = 0 mA to 500 mA, C_O = 100 nF, TONEAMP = 0	667	700	746	mV
		I_O = 0 mA to 500 mA, C_O = 100 nF, TONEAMP = 1	753	800	853	mV
$D_{(tone)}$	Tone duty cycle		45%	50%	55%	
$f_{(EXTM)}$	External tone input frequency range	22 kHz tone output	17.6	22	26.4	kHz
		44 kHz tone output	35.2	44	52.8	kHz
TONE DETECTION						
$f_{(DIN)}$	Tone detector frequency capture range	0.4 V_{PP} sine wave	17.6	22	26.4	kHz
$V_{(DIN)}$	Tone detector input amplitude	Sine wave, 22 kHz	0.3		1.5	V
$V_{(DOUT)}$	DOUT output voltage	Tone present, I_{load} = 2 mA			0.4	V
GDR	Bypass FET gate voltage/LNB	TONE_TRANS = 1, $V_{(LNB)}$ = 18.2 V	23.11	23.5	24.03	V
		TONE_TRANS = 0, $V_{(LNB)}$ = 18.2 V	18.17	18.2	18.23	V
THERMAL SHUT-DOWN (JUNCTION TEMPERATURE)						
$T_{(TRIP)}$	Thermal protection trip Point	Temperature Rising		160		°C
$T_{(HYST)}$	Thermal protection hysteresis			20		°C

(1) Lab test data

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C READ BACK FAULT STATUS						
$V_{(PGOOD)}$	PGOOD trip levels	Feedback voltage UVP low	94%	96%	97.1%	
		Feedback voltage UVP high	93%	94.5%	95.5%	
		Feedback voltage OVP high	104%	106.6%	108%	
		Feedback voltage OVP low	102%	104.6%	106%	
$T_{(warn)}$	Temperature warning Threshold			125		°C
I²C INTERFACE						
V_{IH}	SDA,SCL input high voltage		2			V
V_{IL}	SDA,SCL input low voltage				0.8	V
I_I	Input current	SDA, SCL, V_I = 0.4 to 4.5 V	–10		10	µA
V_{OL}	SDA output low voltage	SDA open drain, I_{OL} = 2 mA			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency		400			kHz

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
OUTPUT VOLTAGE						
t_r, t_f	13 V to 18 V transition rising falling time	$C_{(TCAP)}$ = 22 nF		2		ms
$t_{ON(min)}$	Minimum on time for the Low side FET		75	102	130	ns
TONE						
$t_{r(tone)}$	Tone rise time	I_O = 0 mA to 500 mA, C_O = 100 nF, Control Reg1[0] = 0		11		µs
		I_O = 0 mA to 500 mA, C_O = 100 nF, Control Reg1[0] = 1, and EXTM has 44 kHz input		5.5		µs
$t_{f(tone)}$	Tone fall time	I_O = 0 mA to 500 mA, C_O = 100 nF, Control Reg1[0] = 0		10.8		µs
		I_O = 0 mA to 500 mA, C_O = 100 nF, Control Reg1[0] = 1, and EXTM has 44 kHz input		5.4		µs
PROTECTION						
t_{ON}	Overcurrent protection ON Time	TIMER=0	2.3	3.75	5.52	ms
t_{OFF}	Overcurrent protection OFF Time	TIMER=0	98.5	118	133.5	ms
I²C INTERFACE						
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{HD_STA}	Hold time (repeated) START condition		0.6			µs
t_{SU_STO}	Setup time for STOP condition		0.6			µs
t_{LOW}	LOW period of the SCL clock		1			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Setup time for a repeated START condition		0.6			µs
t_{SU_DAT}	Data setup time		0.1			µs
t_{HD_DAT}	Data hold time		0		0.9	µs
t_{RCL}	Rise time of SCL signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{RCL1}	Rise time of SCL Signal after a Repeated START condition and after an acknowledge BIT	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{FCL}	Fall time of SCL signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{RDA}	Rise time of SDA signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{FDA}	Fall time of SDA signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
C_B	Capacitance of one bus line(SCL and SDA)				400	pF

Product Folder Links: *TPS65235-1*

6.7 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1 MHz, C_{Boost} = 2 x 22 µF/35 V (unless otherwise noted)

L = 4.7 µH
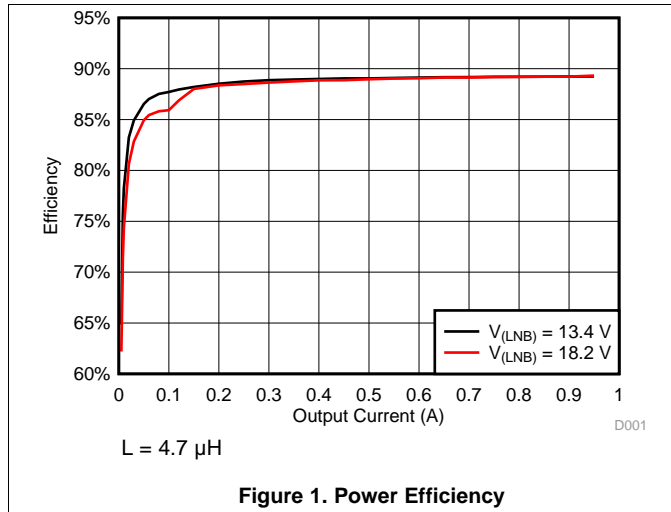
Figure 1. Power Efficiency

$V_{(LNB)}$ = 13.4 V

Figure 2. Load Regulation

$V_{(LNB)}$ = 18.2 V
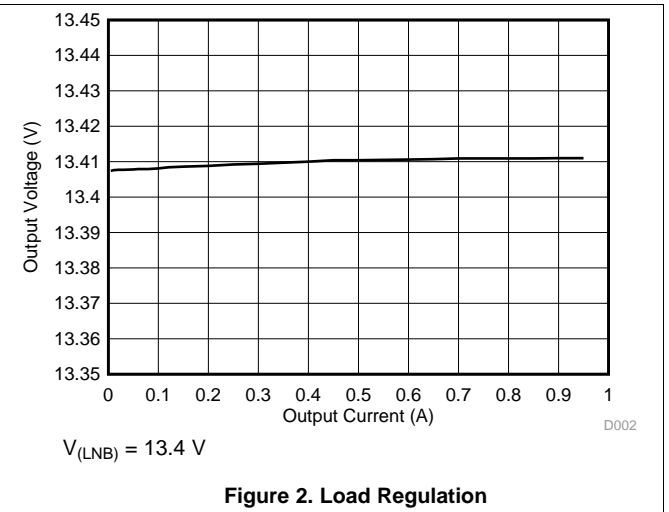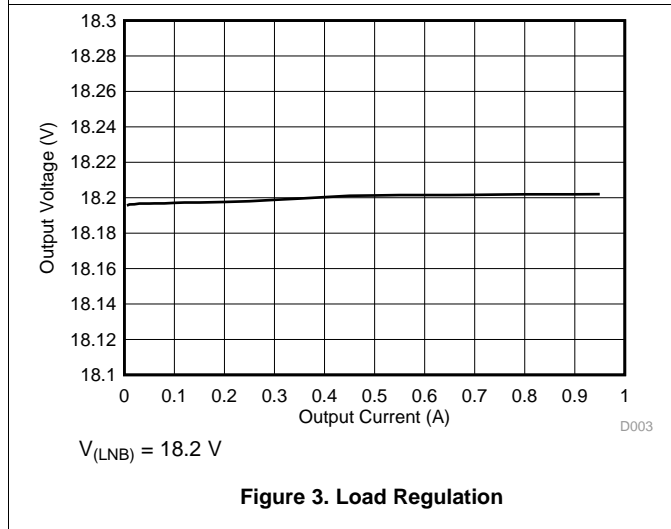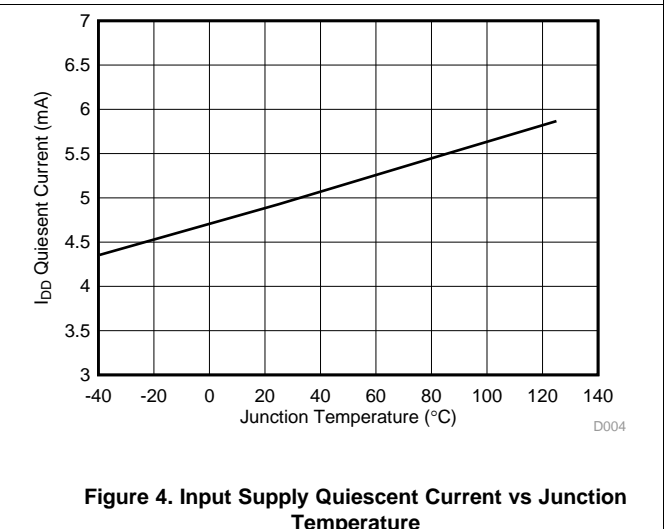
Figure 3. Load Regulation

Figure 4. Input Supply Quiescent Current vs Junction Temperature
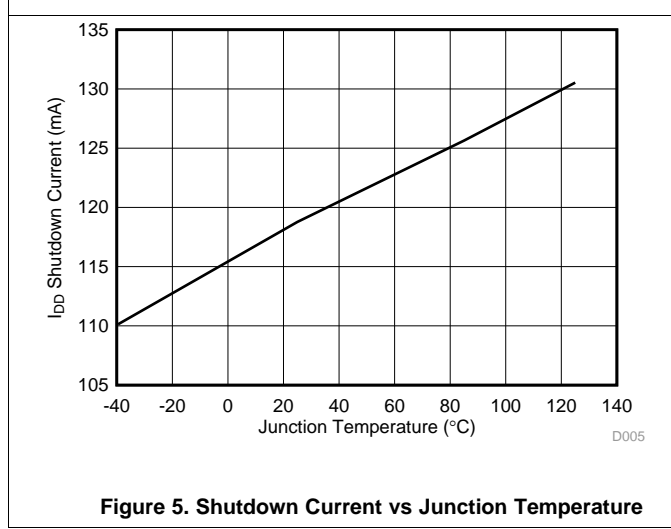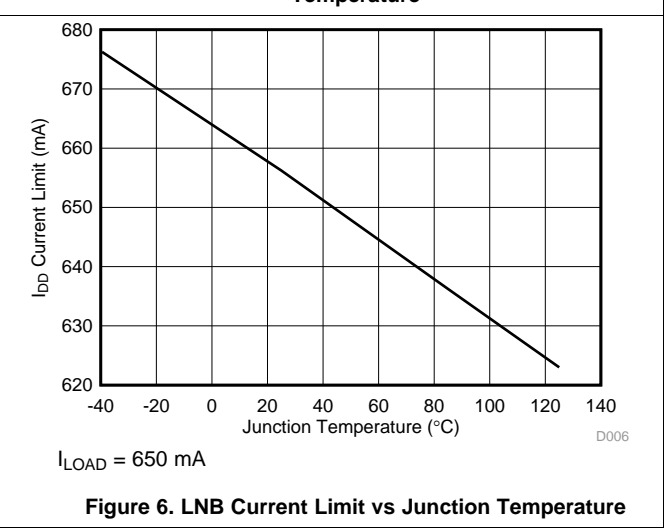

Figure 5. Shutdown Current vs Junction Temperature

I_{LOAD} = 650 mA

Figure 6. LNB Current Limit vs Junction Temperature

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7 Detailed Description

7.1 Overview

TPS65235-1 is the Power management IC that integrates a boost converter, a LDO and a 22 kHz tone generator to serve as a LNB power supply. This solution compiles the DiSEqC 2.x standard with or without I²C interface. Output current limitation can be precisely programmed by an external resistor. There are two ways to generate the 22 kHz tone signal, with or without I²C. Integrated boost features low $R_{ds(on)}$ MOSFET and internal compensation. 1 MHz or 500 kHz selectable switching frequency is designed to save passive components size and be flexible for design.

TPS65235-1 can support the 44-kHz tone output, when the EXTM has 44-kHz tone input, and the bit EXTM TONE of *Control Register 1* is set to "1", the LNB tone output is 44 kHz. By default, the TPS65235-1 has a typical 22-kHz tone output.

7.2 Functional Block Diagram
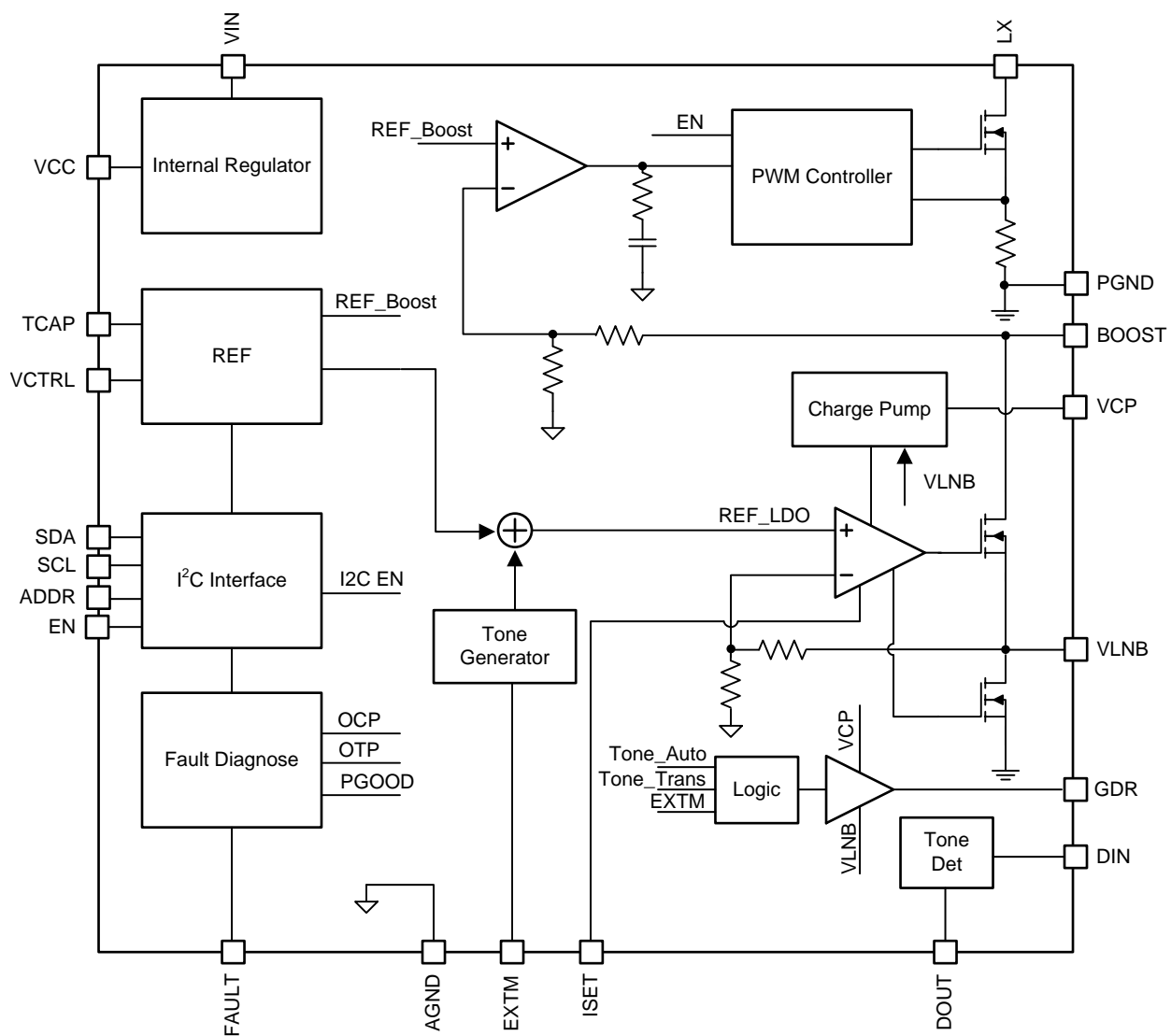
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7.3 Feature Description

7.3.1 Boost Converter

The TPS65235-1 consists of an internal compensated boost converter and linear regulator. The boost converter tracks the LNB output voltage within 800 mV even at loading 1000 mA, which minimizes power loss. When the input voltage VIN is greater than the expected output voltage VLNB, the linear regulator drops the voltage difference between VIN and VLNB, which causes the lower efficiency and the higher power loss on the internal linear regulator if the current loading is high. For this application, care must be taken to ensure that the safe operating temperature range of the TPS65235-1 is not exceeded. Recommend to work at force PWM mode when $V_{IN} > V_{OUT}$ to reduce output ripple.

As default, the boost converter operates at 1 MHz. TPS65235-1 has internal cycle-by-cycle peak current limit in the boost converter and DC current limit in the LNB output to protect the IC against short circuits and over loading. When the LNB output is shorted to ground, the LNB output current is clamped at the LDO current limit. The LDO current limit is set by the external resistor at ISET pin; meanwhile the Boost switch current limit is proportional with LDO current limit. If overcurrent condition lasts for more than 4 ms, the Boost converter enters hiccup mode and will re-try startup in 128 ms. This hiccup mode ON/OFF time can be selectable by I^2C control register 0x01, either 4 ms / 128 ms or 8 ms / 256 ms. At extremely light loads, the boost converter operates in a pulse-skipping mode automatically.

Boost converter is stable with either ceramic capacitor or electrolytic capacitor.

If two or more set top box LNB outputs are connected together, one output voltage could be set higher than others. The output with lower set voltage would be effectively turned off. Once the voltage drops to the set level, the LNB output with lower set output voltage returns to normal conditions.

7.3.2 Linear Regulator and Current Limit

The linear regulator is used to generate the 22-kHz tone signal by changing the LDO reference voltage. The linear regulator features low drop out voltage to minimize power loss while keeps enough head room for the 22-kHz tone with 650-mV amplitude. It also implements a tight current limit for overcurrent protection. The current limit is set by an external resistor connected to ISET pin. Figure 7 shows the relationship between the current limit threshold and the resistor value.
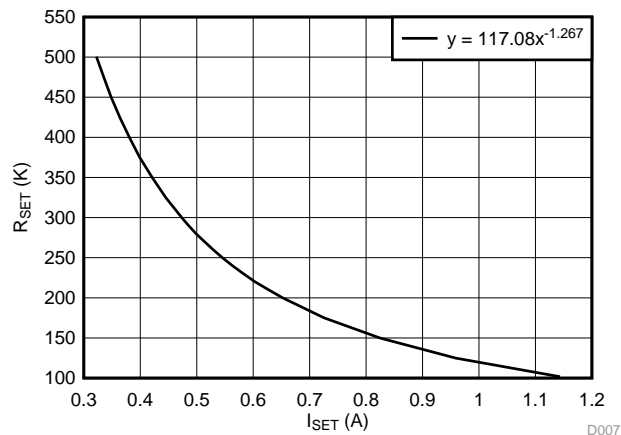

Figure 7. Linear Regulator Current Limit Vs Resistor

$$R_{SET}(k\Omega) = 117.08 \times I_{SET}^{-1.267}(A)$$

(1)

A 200-kΩ resistor sets the current to be 0.65 A, and 110-kΩ resistor sets the current to approximately 1 A.

Submit Documentation Feedback

Product Folder Links: *TPS65235-1*

Feature Description (continued)

7.3.3 Boost Converter Current Limit

The boost converter has the cycle-by-cycle peak current limit on the internal Power MOSFET switch to serve as the secondary protection when LNB output is hard short. With ISW bit default setting "0" on I^{2}C control register 0x01, the switch current limit I$_{SW}$ is proportional as LDO current limit I$_{(OCP)}$ set by ISET pin resistor, and the relationship can be expressed as:

$$I_{SW} = 3 \times I_{(OCP)} + 0.8A \tag{2}$$

For the 5 V V$_{IN}$, if LNB current load is up to 1 A, the ISW bit should be written as "1", the switch current limit I$_{SW}$ for the internal Power MOSFET is:

$$I_{SW} = 5 \times I_{(OCP)} + 0.8A \tag{3}$$

While due to the high power loss at 5 V, V$_{IN}$, it has a chance to trigger the thermal shutdown before the loading is up to 1 A, especially the VLNB output is high.

7.3.4 Charge Pump

The charge pump circuitry generates a voltage to drive the NMOS of the linear regulator. The voltage across the charge pump capacitor between VLNB and VCP is about 5.4 V, so the absolute value of the VCP voltage will be VLNB + 5.4 V.

7.3.5 Slew Rate Control

When LNB output voltage transits from 13.4 V to 18.2 V or 18.2 V to 13.4 V, the cap at pin TCAP controls the transition time. This transition time makes sure the boost converter output to follow LNB output change. Usually boost converter has low bandwidth and can't response fast. The voltage at TCAP acts as the reference voltage of the linear regulator. The boost converter's reference is also based on TCAP with additional fixed voltage to generate a 0.8 V above the LNB output.

The charging and discharging current is 10 µA, thus the transition time can be estimated as:

$$t_{TCAP}(ms) = 0.8 \times \frac{C_{SS}(nF)}{I_{SS}(\mu A)} \tag{4}$$

A 22-nF capacitor generates about 2 ms transition time.

In light load conditions, when LNB output voltage is set from 18.2 V to 13.4 V, the voltage drops very slow, which causes wrong VOUT_GOOD (Bit 0 at status register 0x02) logic for LNB output voltage detection. TPS65235-1 has integrated a pull down circuit to pull down the output during the transition. This ensures the voltage change can follow the voltage at TCAP. When the 22-kHz tone signal is superimposing on the LNB output voltage, the pull down current can also provide square wave instead of a distorted waveforms.

7.3.6 Short Circuit Protection, Hiccup and Overtemperature Protection

The LNB output current limit can be set by an external resistor. When short circuit conditions occur or current limit is triggered, the output current is clamped at the current limit for 4 ms with LDO on. If the condition retains, the converter will shut down for 128 ms and then restart. This hiccup behavior prevents IC from being overheat. The hiccup ON/OFF time can be set by I^{2}C register. Refer to *Control Register 1* for detail.

The low side MOSFET of the boost converter has a peak current limit threshold which serves as the secondary protection. If boost converter's peak current limit is triggered, the peak current will be clamped as high as 3.8 A when setting I$_{SW}$ default and LNB current limit up to 1 A. If loading current continues to increase, output voltage starts to drop and output power drops.

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the junction temperature exceeds 160°C, the output shuts down. When the die temperature drops below its lower threshold typically 140°C, the output is enabled.

Feature Description (continued)

When the chip is in overcurrent protection or thermal shutdown, the I^{2}C interface and logic are still active. The Fault pin is pulled down to signal the processor. The Fault pin signal remains low unless the following action is taken:

1. If I^{2}C interface is not used to control, EN pin must be recycled in order to pull Fault pin back to high.
2. If I^{2}C interface is used, the I^{2}C master need to read the status *Control Register 2*, then the Fault pin will be back to high.

7.3.7 Tone Generation

22 kHz tone signal is implemented at the LNB output voltage as a carrier for DiSEqC command. This tone signal can be generated by feeding an external 22-kHz clock at the EXTM pin, and it can also be generated with its internal tone generator controlled by EXTM pin. If EXTM pin is toggled to high, the internal tone signal will be superimposed at the LNB output, if EXTM pin is low, there will be no tone superimposed at the output stage of the regulator facilitates a push-pull circuit, so even at zero loading; the 22-kHz tone at the output is still clean without distortion.

There are two ways to generate the 22 kHz tone signal at the output.

For option1, if the EXTM has 44-kHz tone input, and the bit EXTM TONE of the *Control Register 1* is set to "1", the LNB tone output is 44 kHz.
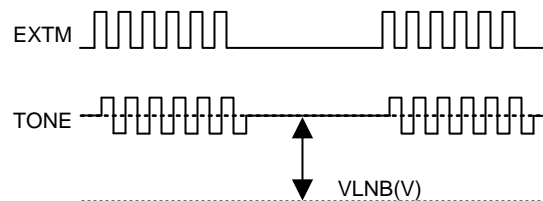
Option 1. Use external tone, gated by EXTM logic pulse
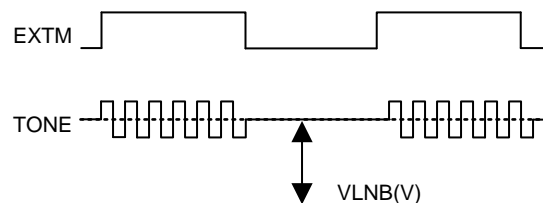
Option 2. Use internal tone, gated by EXTM logic envelop

Figure 8. Two Ways to Generate 22 kHz Tone

7.3.8 Tone Detection

A 22-kHz tone detector is implemented in the TPS65235-1 solution. The detector extracts the AC coupled tone signal from the DIN input and provides it as an open-drain signal on the DOUT pin. With bit DOUTMODE default setting of the *Control Register 2*, if tone is present, the DOUT output is logic low; if tone is not present, the internal output FET is off. If a pull high resistor is connected to the DOUT pin, the output is logic high. The maximum tone out delay with respect to the input is one and half tone cycle.

Bit DOUTMODE of *Control Register 2* is reserved and should not be used.
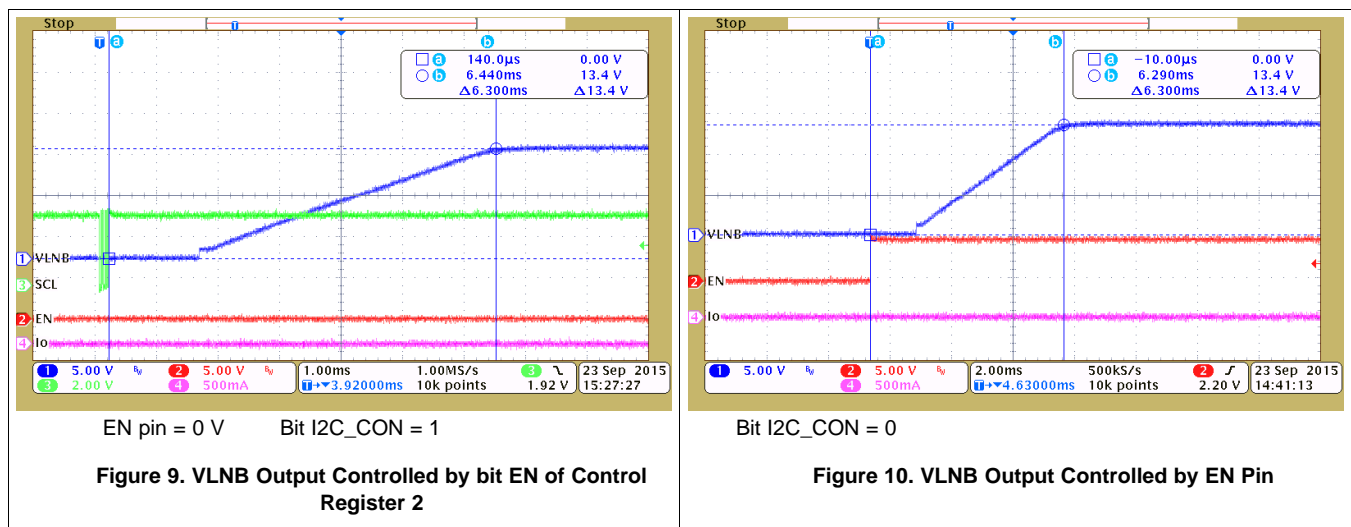
Feature Description (continued)

7.3.9 Audio Noise Rejection

When the TPS65235-1 works at PSM mode, it is possible that the switching frequency locates at the range of audio frequency. Which causes the audible noise, especially VLNB voltage is lower or closer to the VIN, and the current load is light.

When audible noise occurs. setting the TPS65235-1 to work at the Force PWM mode is recommended. At Force PWM mode, a special design is implemented to avoid the audible noise.

7.3.10 Disable and Enable

TPS65235-1 has a dedicated EN pin to disable and enable the LNB output. At non-I^{2}C application, when the EN pin is pulled to high, the LNB output is enabled, when the EN pin is pull to low, the LNB output is disabled. At I^{2}C application, either EN pin is low or high, the I^{2}C registers can be accessed, which allows customer to change the default LNB output when system power up. When the bit I2C_CON of *Control Register 1* is set to "1", the LNB output enable or disable is controlled by bit EN of *Control Register 2*. By default, the bit I2C_CON of the control register is set to "0", which makes the LNB output is controlled by the EN pin. Figure 9 and Figure 10 shows the detail control behavior.

EN pin = 0 V   Bit I2C_CON = 1

Figure 9. VLNB Output Controlled by bit EN of Control Register 2

Bit I2C_CON = 0

Figure 10. VLNB Output Controlled by EN Pin

7.3.11 Component Selection

7.3.11.1 Boost Inductor

TPS65235-1 is recommended to operate with a boost inductor value of 4.7 µH or 10 µH. The boost inductor must be able to support the peak current requirement to maintain the maximum LNB output current without saturation. Below formula can be used to estimate the peak current of the boost inductor.

$$I_{peak} = \frac{I_{OUT}}{1-D} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_S} \tag{5}$$

$$D = 1 - \frac{V_{IN}}{VLNB + 0.8} \tag{6}$$

With the different inductance, the system will have different gain and phase margins, Figure 11 shows a Bode plot of boost loop with 2 x 10 µF / 35 V of boost capacitor and 4.7 µH, 5.6 µH, 6.8 µH, 8.2 µH and 10 µH of boost inductance. As the boost inductance increases, the 0 dB crossover frequency keeps relatively constant while the phase and gain margins reduced. With 4.7 µH, the phase margin is 66.96° and with 10 µH the phase margin is 39.63°.
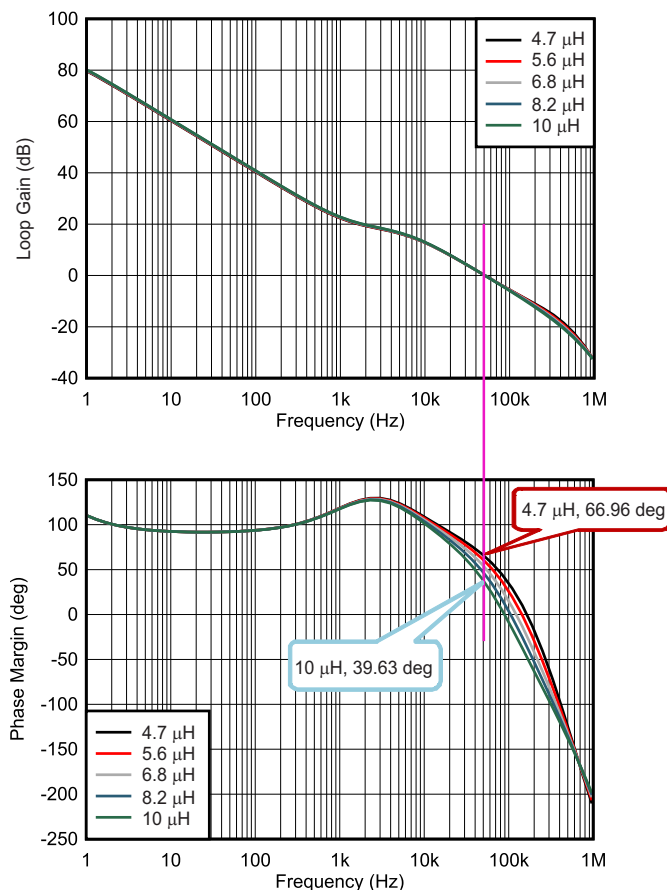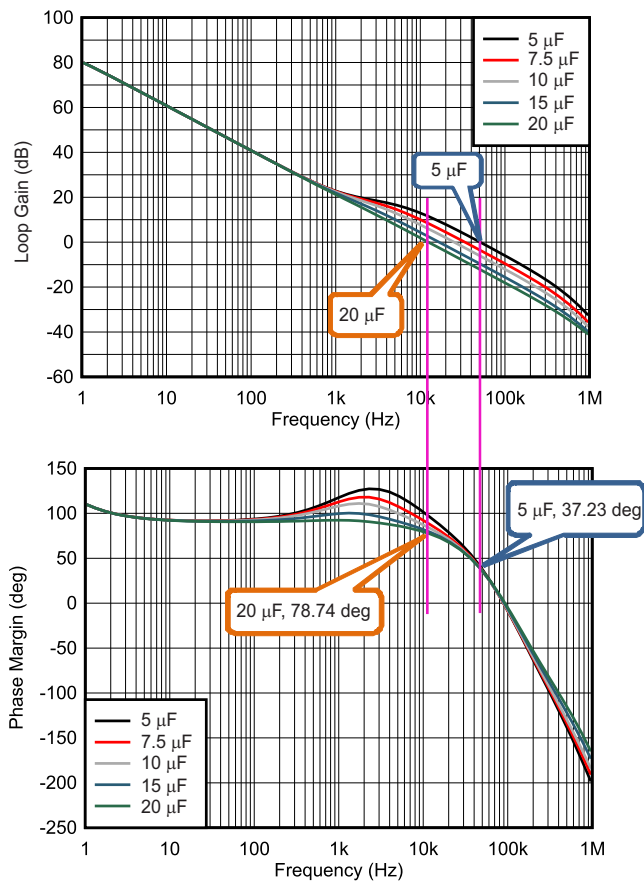
Feature Description (continued)

Figure 11. Gain and Phase Margin of the Boost Loop with Different Inductance
(V_{IN} = 12 V, V_{OUT} = 18.2 V, I_{LOAD} = 1 A, F_{SW} = 1 MHz, 5 µF, Typical Bode Plot)

7.3.11.2 Capacitor Selection

TPS65235-1 has a 1 MHz non-synchronous boost converter integrated and the boost converter features the internal compensation network. TPS65235-1 works well with both ceramic capacitor and electrolytic capacitor.

In TPS65235-1 application, the recommended ceramic capacitors rated are at least X7R/X5R, 35 V rating and 1206 size for the achieving lower LNB output ripple. Table 1 shows the recommended ceramic capacitors list for both 4.7uH and 10uH boost inductors.

If lower cost is demanded, a 100-µF electrolytic (Low ESR) and a 10-µF/35-V ceramic capacitor also work well, this solution provides lower system cost.

Table 1. Boost Inductor and Capacitor Selections

Boost Inductor	Capacitors	Tolerance (%)	Rating (V)	Size
10 µH	2 x 22 µF	±10	35	1206
	2 x 10 µF	±10	35	1206
4.7 µH	2 x 22 µF	±10	35	1206
	2 x 10 µF	±10	35	1206
	22 µF	±10	35	1206

Figure 12 and Figure 13 show a Bode plot of boost loop with 4.7 µH / 10 µH inductance and 4 µF, 5 µF, 7.5 µF, 10 µF, 15 µF and 20 µF of boost capacitance after degrading. As the boost capacitance increases, the phase margin increases.
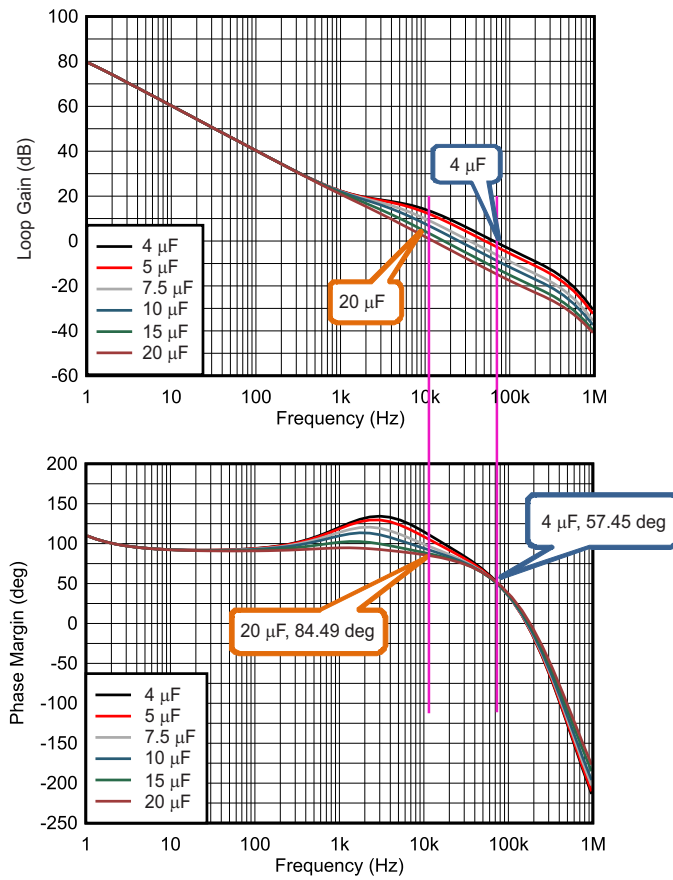
Figure 12. Gain and Phase Margin of the Boost Loop With Different Boost Capacitance
(V_{IN} = 12 V, V_{OUT} = 18.2 V, I_{LOAD} = 1 A, F_{SW} = 1 MHz, 4.7 µH, Typical Bode Plot)

Product Folder Links: *TPS65235-1*

Figure 13. Gain and Phase Margin of the Boost Loop With Different Boost Capacitance
(V$_{IN}$ = 12 V, V$_{OUT}$ = 18.2 V, I$_{LOAD}$ = 1 A, F$_{SW}$ = 1 MHz, 10 µH, Typical Bode Plot)

7.3.11.3 Surge Components

If surge test is needed for the application, D0 and D2 should be added as the external protection components. If no surge test needed. The D0 and D2 can be removed.

Table 2. Surge Components

Designator	Description	Part Number	Manufacturer [1]
D0	Diode, TVS, Uni, 28 V, 1500 W, SMC	SMCJ28A	Fairchild Semiconductor
D2	Diode, Schottky, 40 V, 2 A, SMA	B240A-13-F	Diodes Inc.

(1) See *Third-party Products Disclaimer*
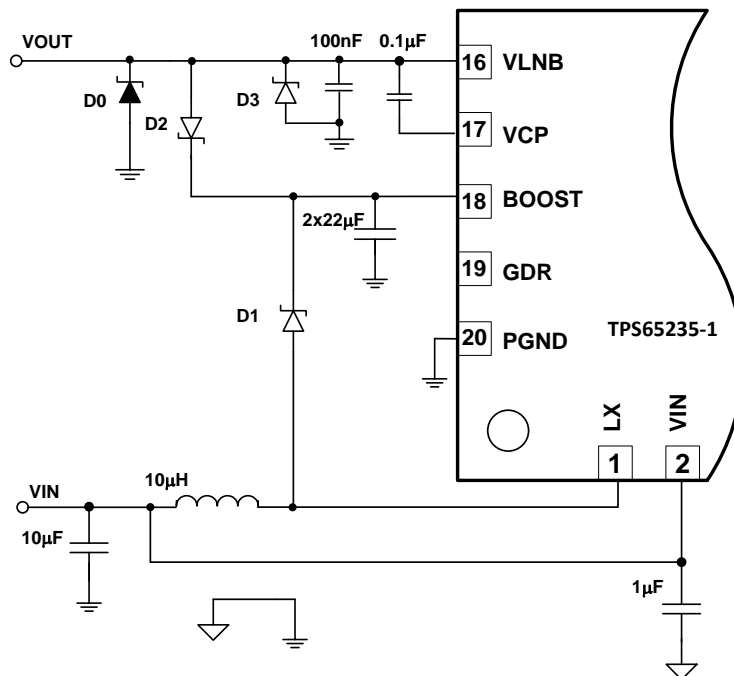
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Figure 14. Surge Components Selection

7.3.11.4 Consideration for Boost Filtering and LNB Noise

Smaller capacitance on boost will lead the cost down for the system, while when the inductor in system is same, the smaller capacitance on the boost and the larger ripple on the LNB output.

7.4 Device Functional Modes

Table 3. Logic table

EN	12C_CON[1][2][3]	SCL	VCTRL	VLNB[4]
H	0	H	H	19.4 V
H	0	H	L	14.6 V
H	0	L	H	18.2 V
H	0	L	L	13.4 V
X	1	X	X	Controlled by VSET[3:0] bits at 0x01 register[5]
L	0	X	X	0 V

(1) I2C_CON is the bit7 of the I^{2}C control register 0x01, which is used to set the VLNB output controlled by the I^{2}C register or not.
(2) When I^{2}C interface is used in design, all the I^{2}C registers are accessible even if the I2C_CON bit is "0".
(3) When I2C_CON is "1", the VLNB output is controlled by the I^{2}C control register even if the EN pin is low.
(4) When I^{2}C interface is used in design, it is recommended to set the I2C_CON with "1", if not, the LNB output will be variable because the SCL is toggled by the I^{2}C register access as the clock signal.
(5) Bit EN of the control register2 is used to disable or enable the LNB output, by default , the bit EN is "1" which enable the LNB output

7.5 Programming

7.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high external. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65235-1 device works as a slave and supports the following data transfer modes, as defined in the I^2CBus Specification: standard mode (100 kbps), and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.5 V (typical).

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The TPS65235-1 device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS65235-1 device has a 7-bit address set by ADDR pin. Table 4 shows how to set the I^2C address.

Table 4. I^2C Address Selection

ADDR PIN	I^2C ADDRESS	Address Format (A6 ≥ A0)
Connect to VCC	0x08H	000 1000
Floating	0x09H	000 1001
Connected to GND	0x10H	001 0000
Resistor divider to make ADDR pin voltage in 3 V ~ V_{CC} - 0.8 V	0x11H	001 0001
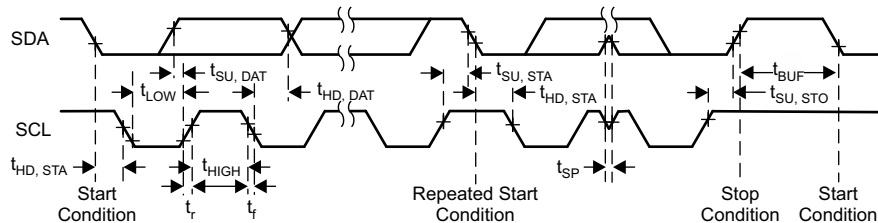
Figure 15. I^2C Interface Timing Diagram

7.5.2 TPS65235-1 I²C Update Sequence

The TPS65235-1 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS65235-1 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. TPS65235-1 performs an update on the falling edge of the LSB byte.

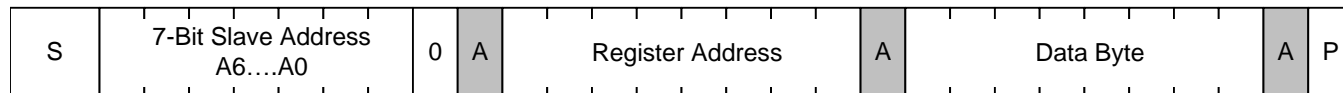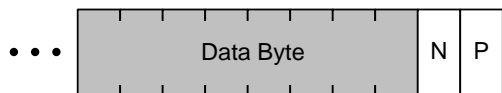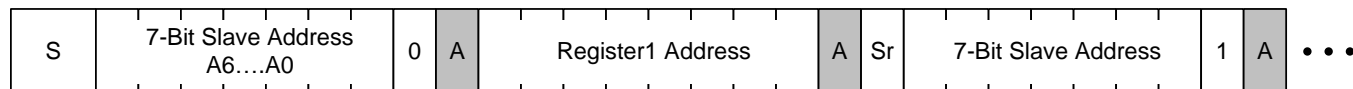When the TPS65235-1 is disabled (EN pin tied to ground) the device cannot be updated via the I²C interface.

S	7-Bit Slave Address A6….A0	0	A	Register Address	A	Data Byte	A	P

Figure 16. I²C Write Data Format

S	7-Bit Slave Address A6….A0	0	A	Register1 Address	A	Sr	7-Bit Slave Address	1	A	• • •

• • •	Data Byte	N	P

A: Acknowledge

N: Not Acknowledge

S: Start

P: Stop   ☐ System Host

Sr: Repeated Start   ▨ Chip

Figure 17. I²C Read Data Format

7.6 Register Maps

7.6.1 Control Register 1 (address = 0x00H) [reset = 00010000]

Figure 18. Control Register 1

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Control Register 1

Bit	Field	Type	Reset	Description
7	I2C_CON	R/W	0	1: I^{2}C control enabled 0: I^{2}C control disabled
6	PWM/PSM	R/W	0	0: PSM at light load 1: Forced PWM
5		R/W		See Table 6 for output voltage selection
4	VSET3	R/W	0	
3	VSET2	R/W	1	
2	VSET1	R/W	0	
1	VSET0	R/W	0	
0	EXTM TONE	R/W	0	1: EXTM 44-kHz tone input support, with 44-kHz tone output at LNB 0: EXTM 44-kHz tone input not support, with only 22-kHz tone output at LNB

Table 6. LNB Output Voltage Selection

VSET3	VSET2	VSET1	VSET0	LNB(V)
0	0	0	0	11
0	0	0	1	11.6
0	0	1	0	12.2
0	0	1	1	12.8
0	1	0	0	13.4
0	1	0	1	14
0	1	1	0	14.6
0	1	1	1	15.2
1	0	0	0	15.8
1	0	0	1	16.4
1	0	1	0	17
1	0	1	1	17.6
1	1	0	0	18.2
1	1	0	1	18.8
1	1	1	0	19.4
1	1	1	1	20

7.6.2 Control Register 2 (address = 0x01H) [reset = 0000101]

Figure 19. Control Register 2

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Control Register 2

Bit	Field	Type	Reset	Description
7	TONEAMP	R/W	0	1: 22 kHz tone amplitude is 750 mV (typ) 0: 22 kHz tone amplitude is 650 mV (typ)
6	TIMER	R/W	0	1: Hiccup ON/OFF time set to 8 ms / 256 ms 0: Hiccup ON/OFF time set to 4 ms / 128 ms
5	I_{SW}	R/W	0	1: Boost switch peak current limit set to 5 x Iocp + 0.8 A 0: Boost switch peak current limit set to 3 x Iocp + 0.8 A
4	FSET	R/W	0	1: 500 kHz switching frequency 0: 1 MHz switching frequency
3	EN	R/W	1	1: LNB output voltage Enabled 0: LNB output disabled
2	DOUTMODE	R/W	0	1: Reserved, cannot set to "1" 0: DOUT is kept to low when DIN has the tone input
1	TONE_AUTO	R/W	0	1: GDR (External bypass FET control) is automatically controlled by 22 kHz tones transmit 0: GDR (External bypass FET control) is controlled by TONE_TRANS
0	TONE_TRANS	R/W	1	1: GDR output with VCP voltage. Bypass FET is ON for tone transmit from TPS65235-1 0: GDR output with VLNB voltage for tone receive. Bypass FET is OFF for tone receiving from satellite

Table 8. 22-kHz Tone Receive Mode Selection

TONE_AUTO	TONE_TRANS	Bypass FET
0	0	OFF
0	1	ON
1	x	Auto Detect

TPS65235-1 has full range of diagnostic flags for operation and debug. Processor can read the status register to check the error conditions. Once the error happens, the flags are changed, once the errors are gone, the flags are set back without I^{2}C access.

If flags TSD and OCP are triggered, FAULT pin will be pulled low, so FAULT pin can be the interrupt signal to processor. Once TSD and OCP are set to "1", the FAULT pin logic is latched to low, processor need to read this status register in order to release the fault conditions.

7.6.3 Status Register (address = 0x02H) [reset = x0100000]

Figure 20. Status Register

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Status Register

Bit	Field	Type	Reset	Description
7	Reserved	R		Reserved
6	TDETGOOD	R	0	1: 22 kHz tone detected on DIN pin is in range 0: 22 kHz tone detected on DIN pin is out of range
5	LDO_ON	R	1	1: Internal LDO is turned on and boost converter is on 0: Internal LDO is turned off but boost converter is on
4	T125	R	0	Die temperature > 125°C Die temperature < 125°C
3	TSD	R	0	1: Thermal shutdown triggered. The Fault pin logic is latched to low, processor need to read this register in order to release the fault conditions 0: No thermal shutdown triggered
2	OCP	R	0	1: Over current protection triggered. The Fault pin logic is latched to low, processor need to read this register in order to release the fault conditions 0: Overcurrent protection conditions released
1	CABLE_GOOD	R	0	1: Cable connection good 0: Cable not connected
0	VOUT_GOOD	R	0	1: LNB output voltage in range 0: LNB output voltage out of range

Product Folder Links: *TPS65235-1*

8   Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1   Application Information

8.2   Typical Application for DiSEqc1.x Support

TPS65235-1 can work at both I^{2}C and non I^{2}C interface mode, Figure 21 shows the application with I^{2}C interface for supporting DiSEqC 1.x application. With non I^{2}C mode, the SCL, SDA and ADDR pins can be floating.
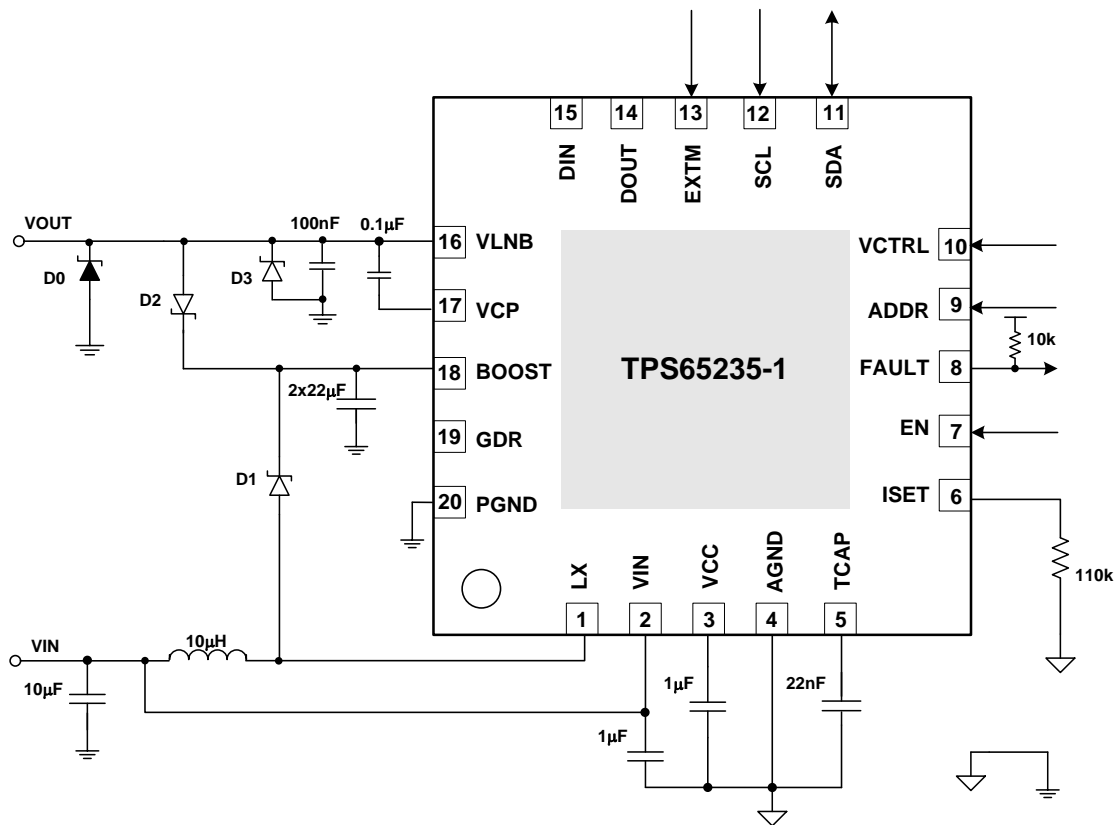
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Figure 21. Application for DiSEqc1.x Support

8.2.1   Design Requirements

For this design example, see the parameters in Table 10.

Table 10. Design Parameters

PARAMETER	VALUE
Input voltage range, V$_{IN}$	4.5 V to 20 V
Output voltage range V$_{LNB}$	11 V to 20 V
Output current range	0 A to 1 A

8.2.2 Detailed Design Procedure

To begin the design process, following need to be done:

- Inductor choose
  - Based on the cost requirement, ripple requirement and *Component Selection* to choose the appropriate inductor.
- Boost capacitor choose
  - Based on the cost requirement, ripple requirement and *Component Selection* to choose the appropriate capacitors.
- Diodes choose.
  - D0 and D2 are for the surge protection requirement, if not requirement for surge, it can be removed. Refer to *Surge Components* for the part selection.
  - D1 is for the boost loop, schottky diode is recommended. The current and voltage capability of the D1 can be determined by the detail application which including input and output power range, and current requirement.
  - D3 is for the V_{LNB} output protection, schottky diode is recommended. The current and voltage capability of the D3 can be determined by the detail application for the output.

Product Folder Links: *TPS65235-1*

8.2.3 Application Curves

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1 MHz, C_{Boost} = 2 x 22 µF/35 V (unless otherwise noted)
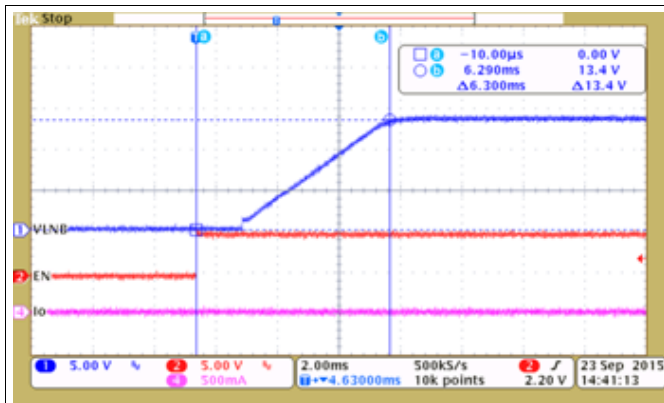
V_{LNB} = 13.4 V

Figure 22. Soft Start, Delay from EN High to LNB Output High
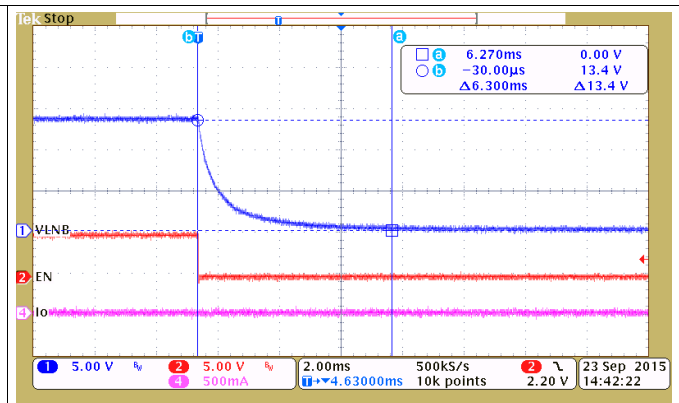
V_{LNB} = 13.4 V

Figure 23. Disabled, Delay From EN Low to LNB Output Low
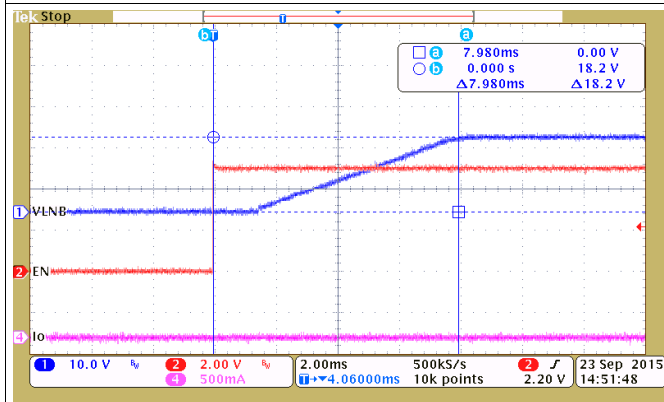
V_{LNB} = 18.2 V

Figure 24. Soft Start,Delay from EN High to LNB Output High
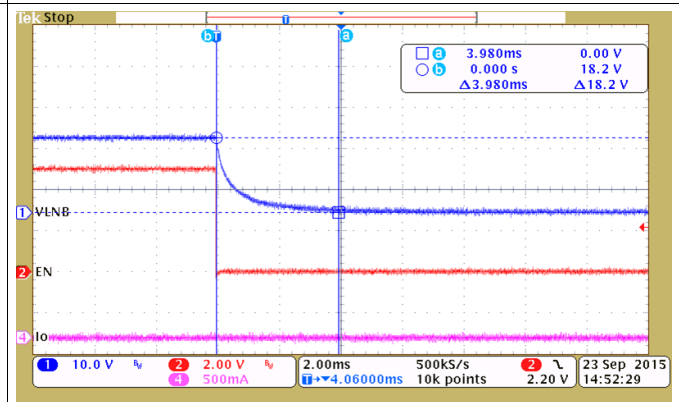
VLNB = 18.2 V

Figure 25. Disabled, Delay From EN Low to LNB Output Low
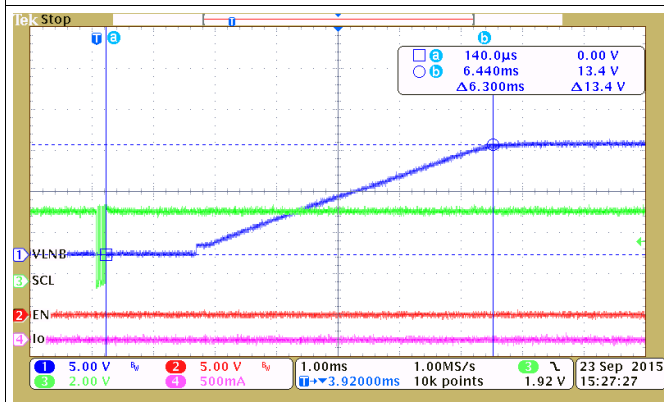
EN = 0 V_{LNB} = 13.4 V

Figure 26. Soft Start, Delay From I²C Enable (I2C_CON=1) to LNB Output High
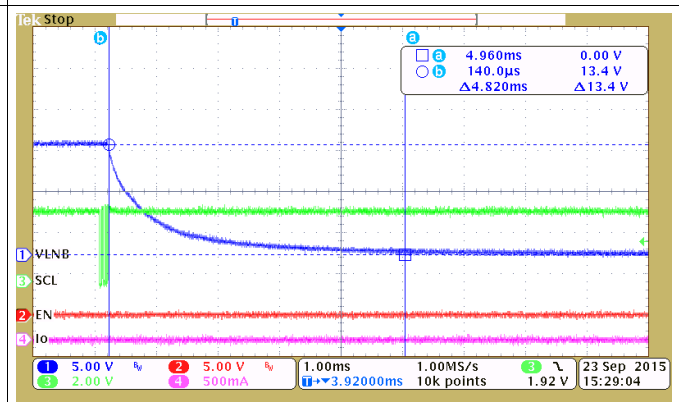
EN = 0 V_{LNB} = 13.4 V

Figure 27. Delay From I²C Disable (I2C_CON=0) to LNB Output Low
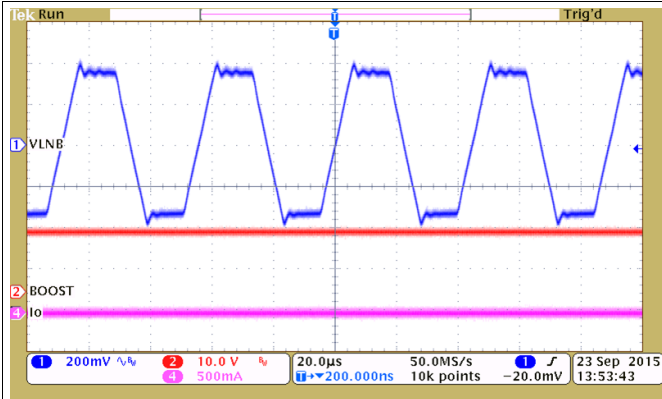
V_{LNB} = 13.4 V

Figure 28. No Load, 22 kHz Tone Output
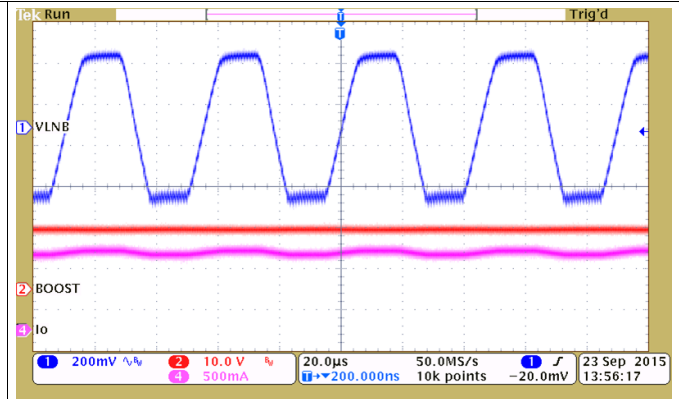
V_{LNB} = 13.4 V

Figure 29. 950 mA Load, 22 kHz Tone Output
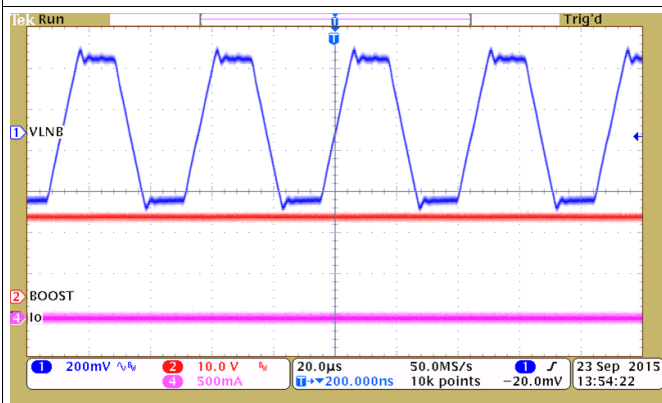
V_{LNB} = 18.2 V

Figure 30. No Load, 22 kHz Tone Output
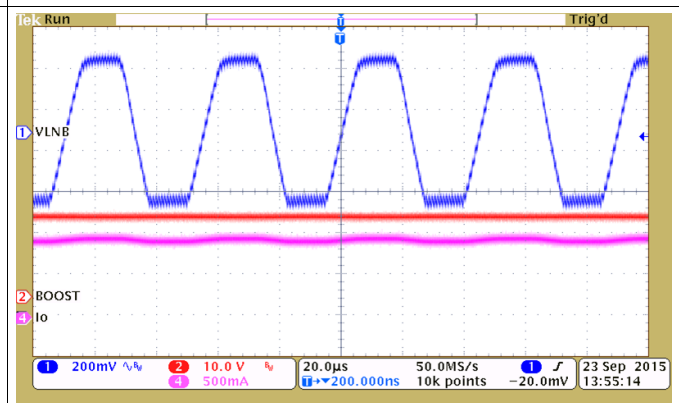
V_{LNB} = 18.2 V

Figure 31. 950 mA Load, 22 kHz Tone Output
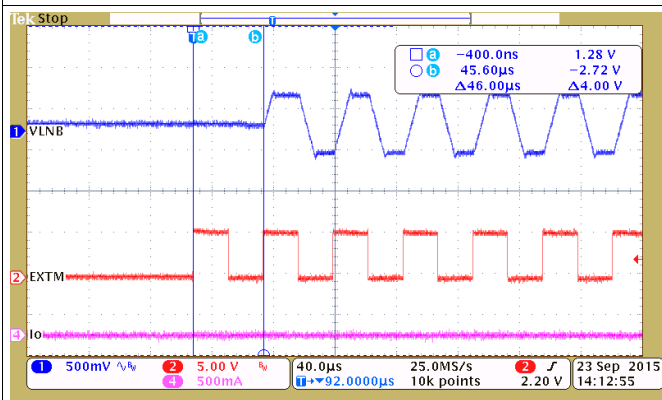
Figure 32. No load, 22 kHz Tone Delay from EXTM 22 kHz Input Turns High To Output Tone On
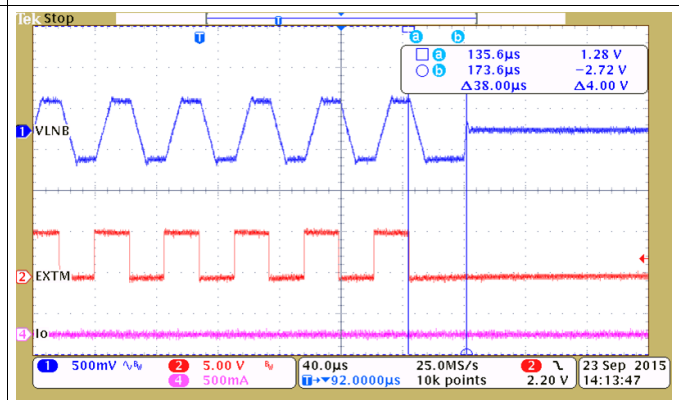
Figure 33. No load, 22 kHz Tone Delay from EXTM 22 kHz Input Turns Low To Output Tone Off

Product Folder Links: *TPS65235-1*
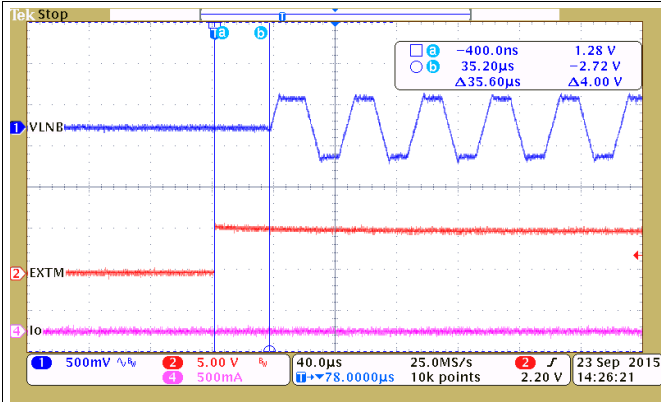
Figure 34. No Load, 22 kHz Tone Delay From EXTM Tone Envelop Input Turns High To Output Tone On
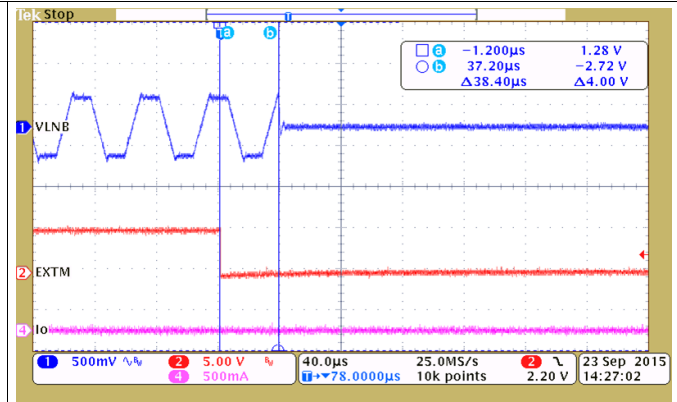
Figure 35. No Load, 22 kHz Tone Delay From EXTM Tone Envelop Input Turns Low To Output Tone Off
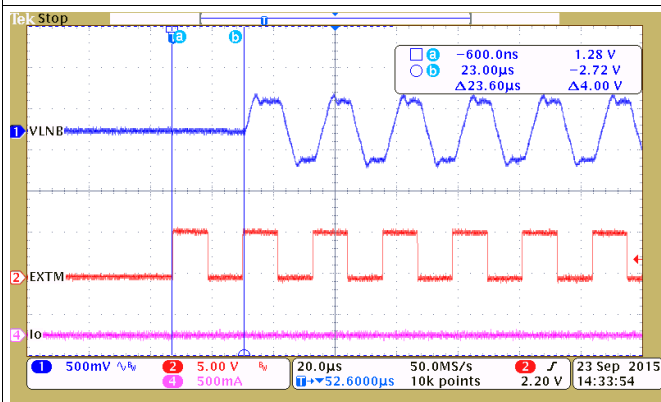
Figure 36. No Load, 44 kHz Tone Delay From EXTM 22 kHz Input Turns High To Output Tone On
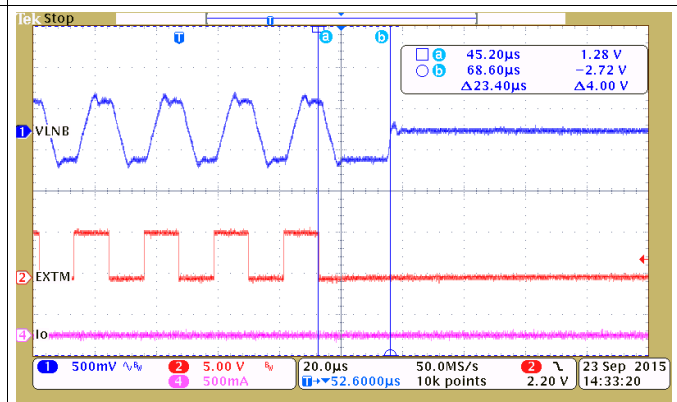
Figure 37. No Load, 44 kHz Tone Delay From EXTM 22 kHz Input Turns Low To Output Tone Off

8.2.4 Typical Application for DiSEqc2.x Support

TPS65235-1 can support both DiSEqC 1.x application and DiSEqC 2.x application, Figure 38 shows the application for supporting DiSEqC 2.x application.
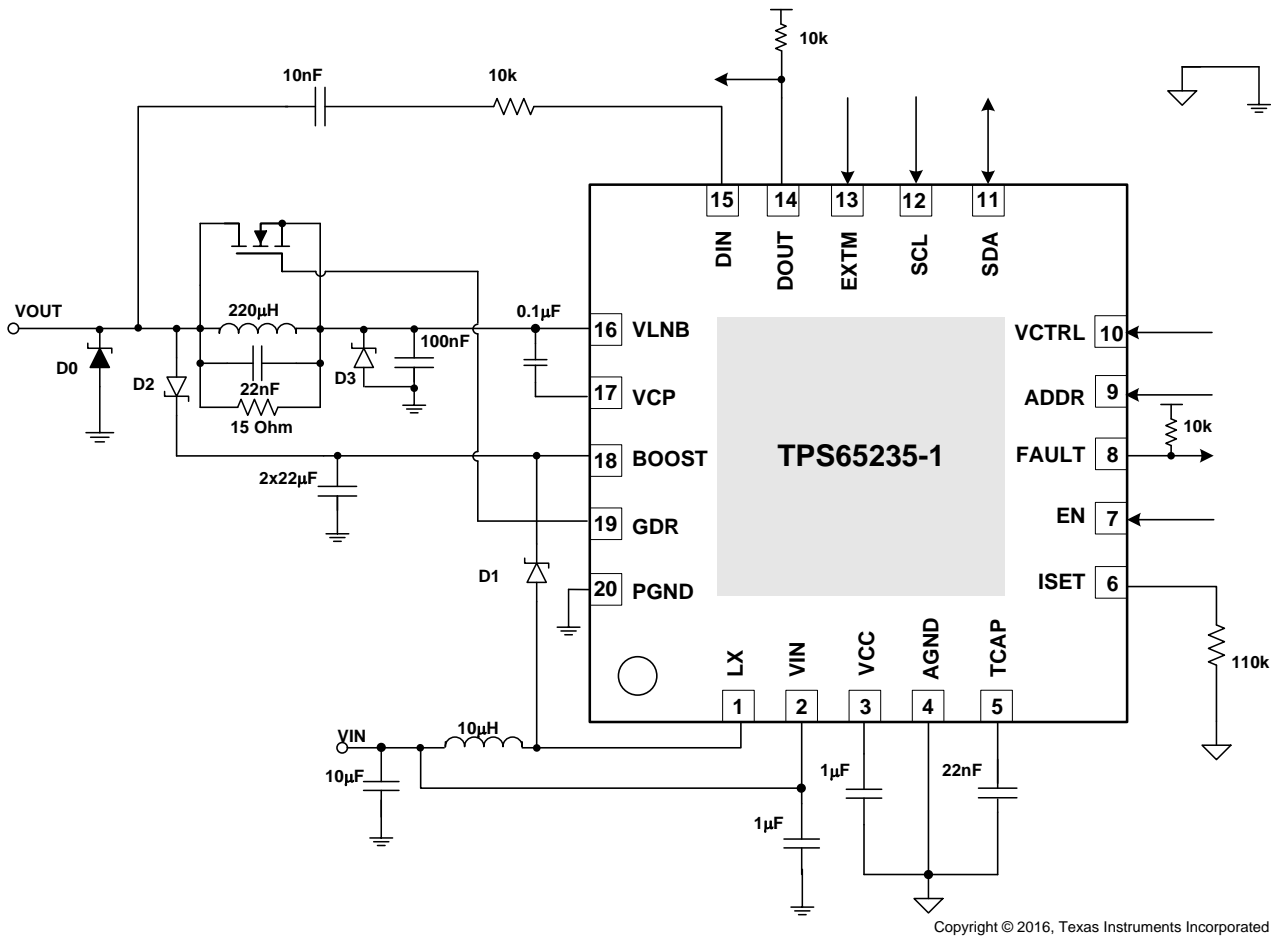
Figure 38. Application for DiSEqc2.x Support

8.2.4.1 Design Requirements

Refer to *Typical Application for DiSEqc1.x Support* for design requirements.

8.2.4.2 Detailed Design Procedure

Refer to *Typical Application for DiSEqc1.x Support* for detailed design procedures.

8.2.4.3 Application Curves

Refer to *Typical Application for DiSEqc1.x Support* for application curves. While Figure 39 is special for DiSEqC 2.x application for tone detection.
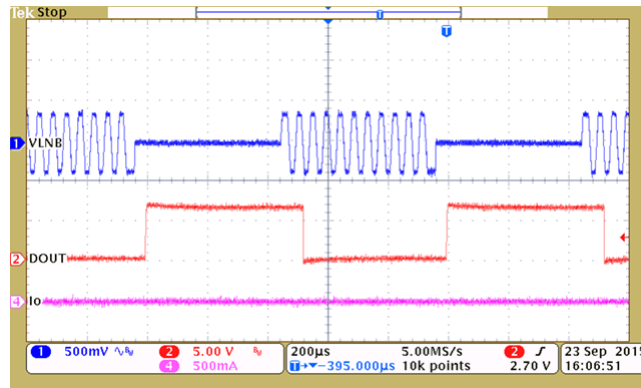
Figure 39. DOUT Tone Detection Output

9 Power Supply Recommendations

The devices are designed to operate from an input supply ranging from 4.5 V to 20 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter, an additional bulk capacitance, typically 100 μF, may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

TPS65235-1 is designed to layout in 2-layer PCB. To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- It is critical to make sure the GND of input capacitor, output capacitor and the boost converter are connected at one point at same layer.
- PGND and AGND are in different region, they are connected to the thermal pad. Other components are connected AGND.
- Put the capacitors for boost as close as possible.
- The loop from V_{IN}, inductor to LX should be as short as possible.
- The loop from V_{IN}, inductor, D1 Schottky diode to Boost should be as short as possible.
- The loop for boost capacitors to PGND should be within the loop from LX, D1 Schottky diode to Boost.

10.2 Layout Example

Figure 40. Layout

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Product Folder Links: *TPS65235-1*
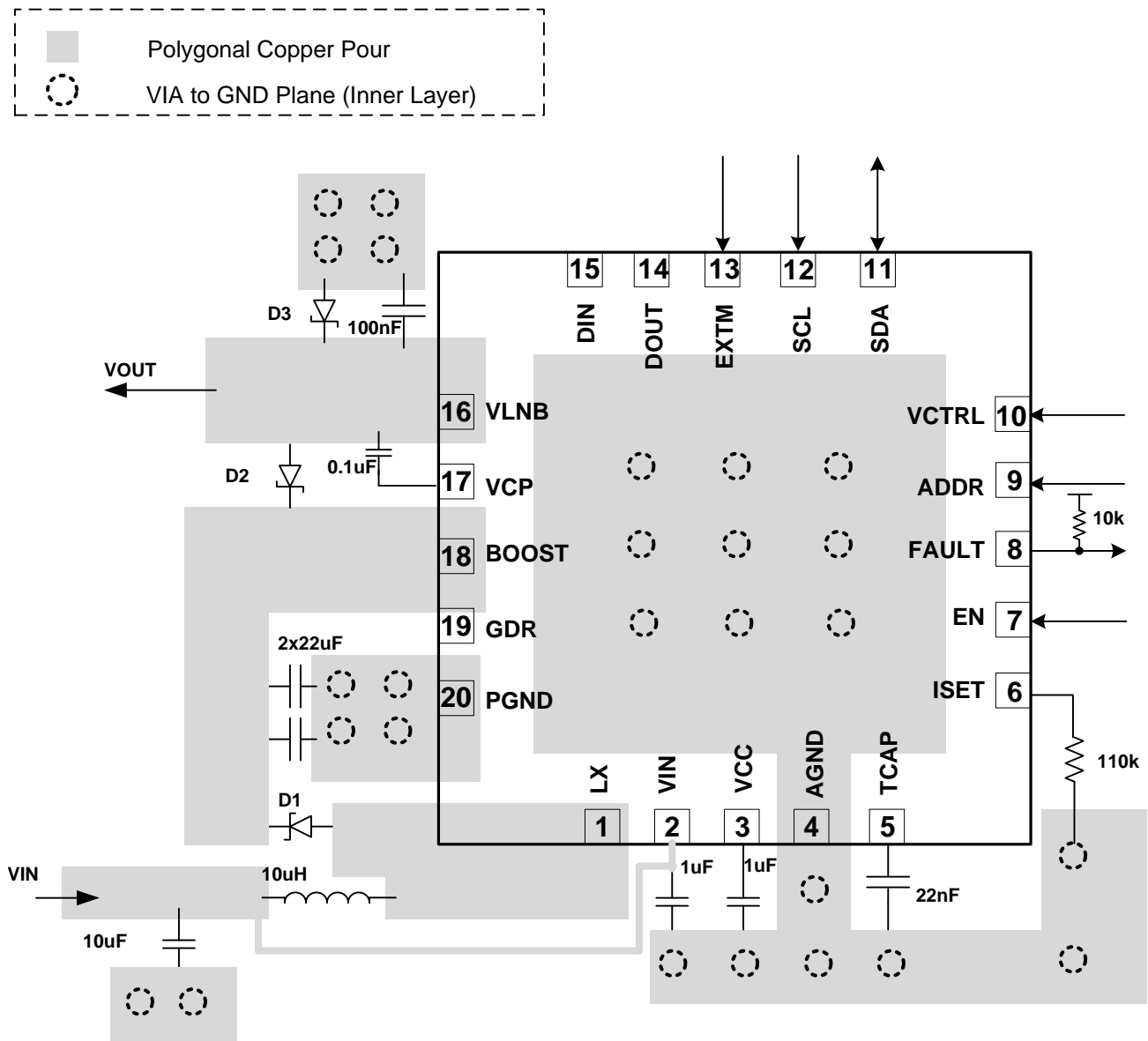
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:
* TPS65235-1 User's Guide, SLVUAZ0
* Evaluation Module for the TPS65235-1 LNB Voltage Regulator With I2C Interface for DiSEqC1.x Application, SLVUAZ1

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.
   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65235-1RUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	652351	Samples
TPS65235-1RUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	652351	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65235-1RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65235-1RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

![Texas Instruments logo] **TEXAS INSTRUMENTS**

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65235-1RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS65235-1RUKT	WQFN	RUK	20	250	210.0	185.0	35.0

RUK (S−PWQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{3,10}{2,90}$

$\frac{3,10}{2,90}$

$\frac{0,80}{0,70}$

0,20 REF.

SEATING PLANE

$\frac{0,05}{0,00}$

△ 0,08

$20X \frac{0,50}{0,30}$

1   5

20   6

THERMAL PAD

SIZE AND SHAPE SHOWN
ON SEPARATE SHEET

16   10

15   11

$20X \frac{0,25}{0,15}$

⊕ 0,10 Ⓜ C A B

0,40

1,60
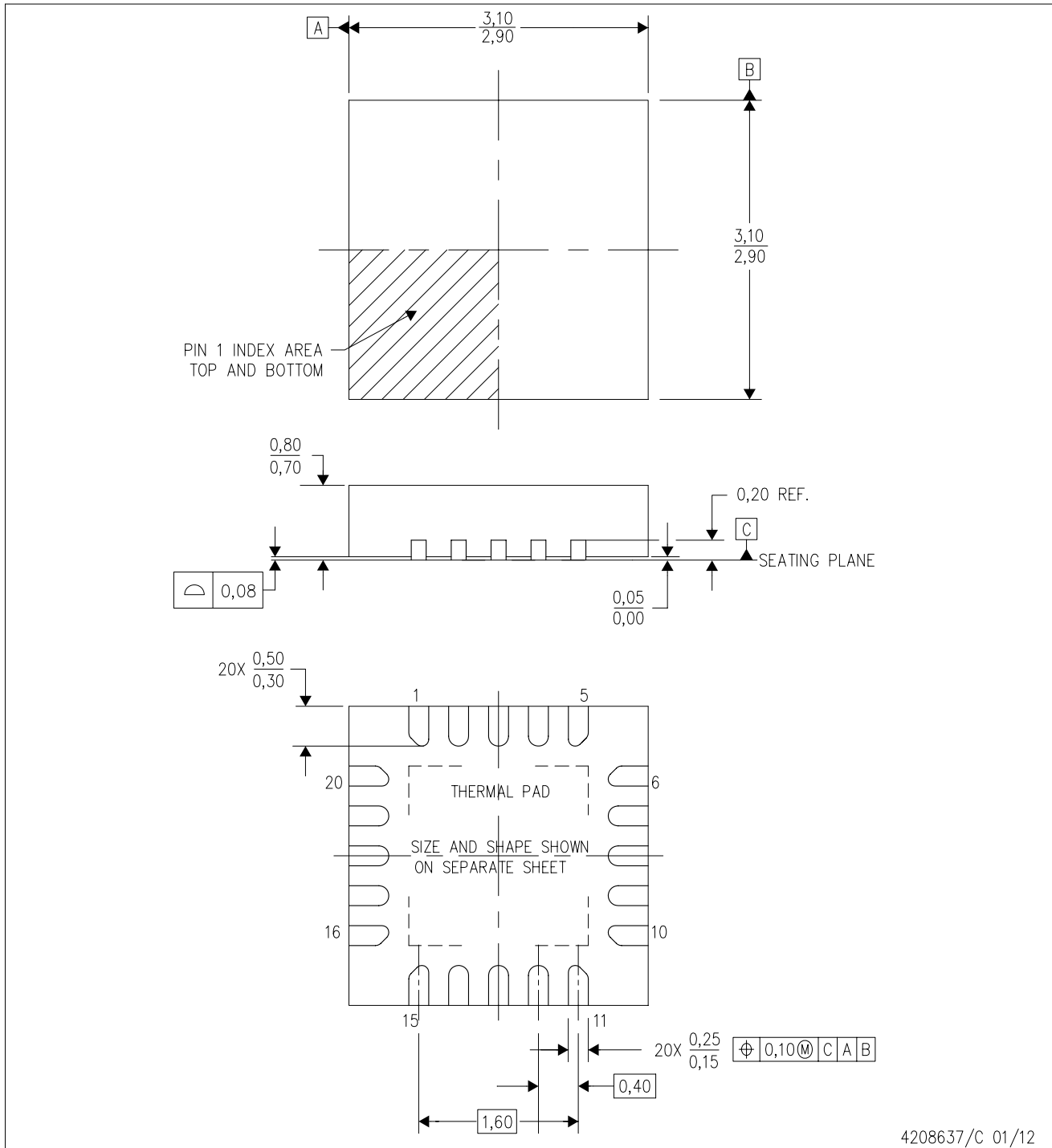
4208637/C 01/12

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

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RUK (S−PWQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C 0,30

1   5

Exposed Thermal Pad

20   6

1,70±0,10

16   10

15   11

1,70±0,10

Bottom View
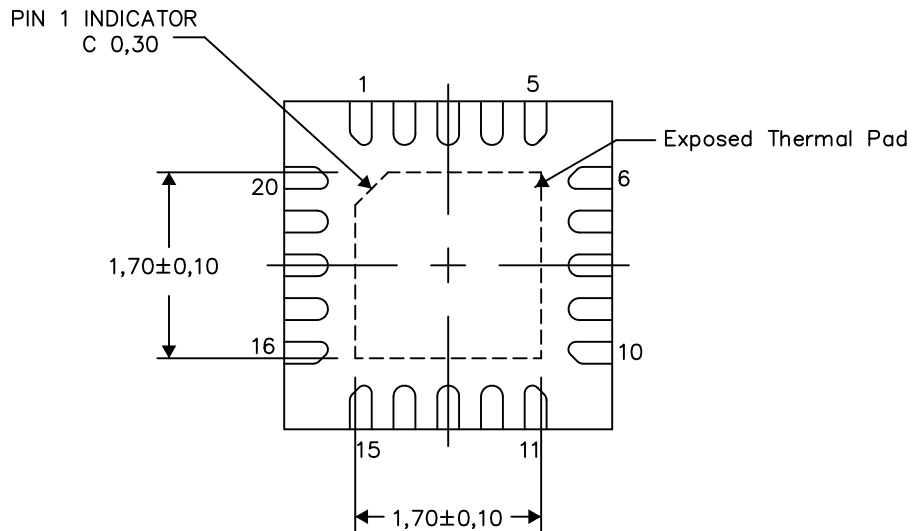
Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

RUK (S−PWQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD
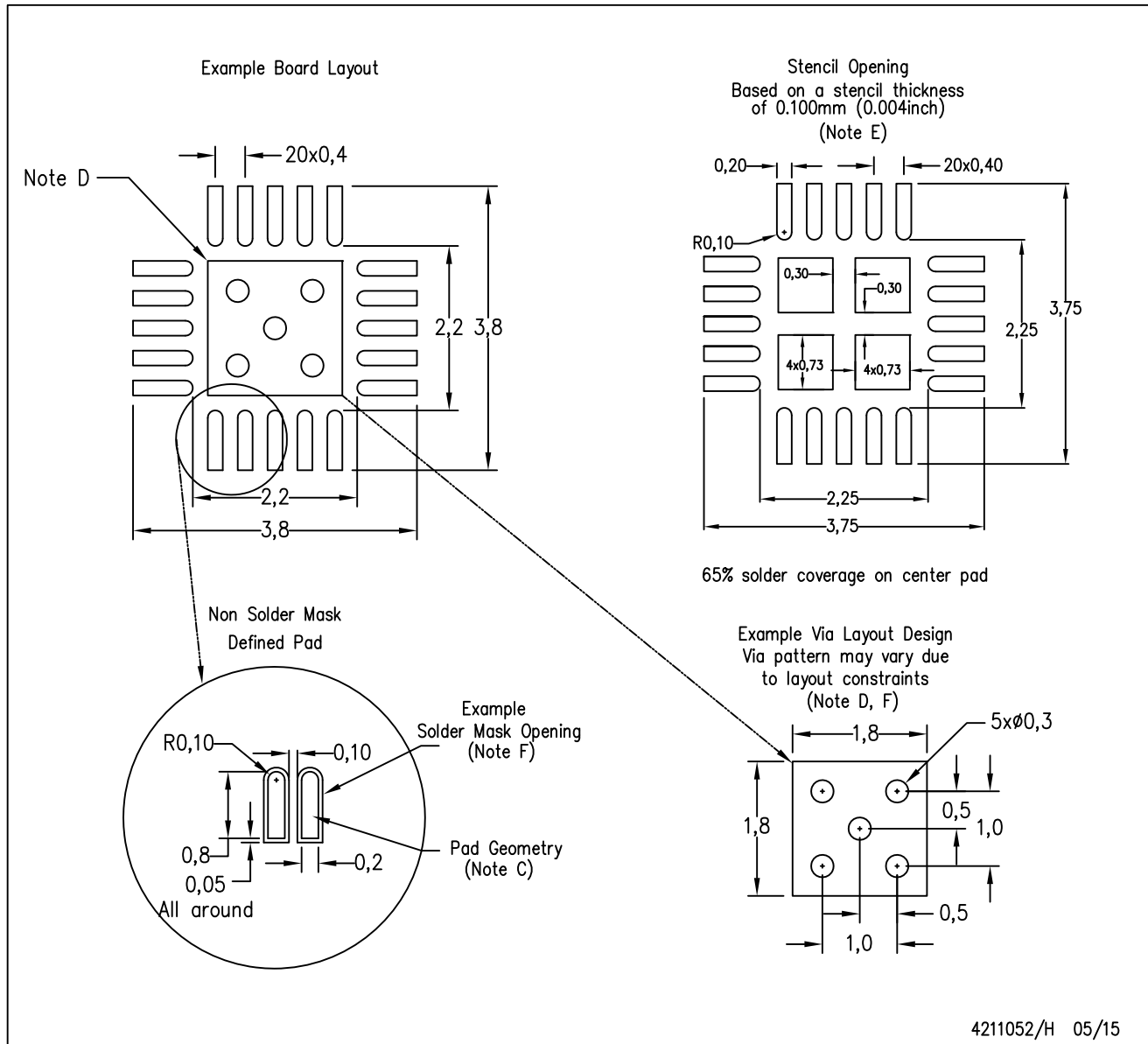
Example Board Layout

Note D

20x0,4

2,2 3,8

2,2

3,8

Non Solder Mask
Defined Pad

R0,10   0,10

0,8

0,05

All around

0,2

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Stencil Opening
Based on a stencil thickness
of 0.100mm (0.004inch)
(Note E)

0,20   20x0,40

R0,10

0,30   0,30

4x0,73   4x0,73

3,75

2,25

2,25

3,75

65% solder coverage on center pad

Example Via Layout Design
Via pattern may vary due
to layout constraints
(Note D, F)

1,8   5xØ0,3

1,8   0,5   1,0

1,0   0,5

4211052/H 05/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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