200mA Dual Output AMOLED Display Power

Check for Samples: TPS65137

FEATURES

- **2.3 V to 5.5 V Input Voltage Range**
- **1% Output Voltage Accuracy V_{POS}**
- **Excellent Line Transient Regulation**
- **Low Noise Operation**
- **200 mA Output Current**
- **Fixed 4.63 V Positive Output Voltage**
- **Digitally Programmable Negative Output Voltage Down to –5.23V**
- **–4.93V Default Value for V_{NEG}**
- **Advanced Power Save Mode**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **TPS65137A High impedance output in shutdown**
- **3×3 mm 10 Pin QFN Package**

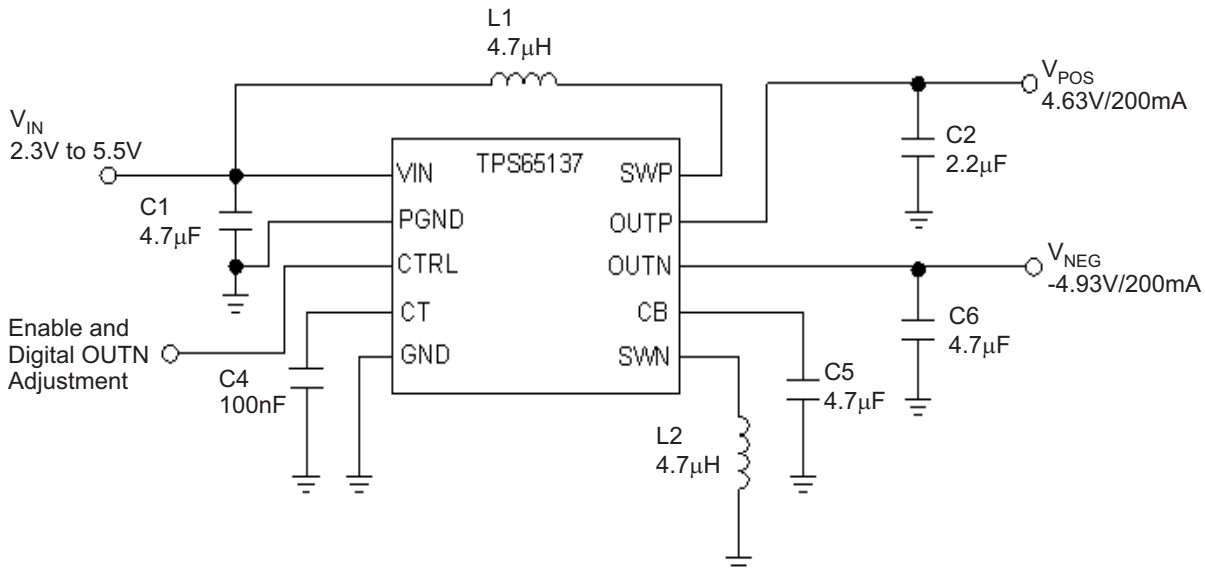
APPLICATIONS

- **Active Matrix OLED Power Supply**

DESCRIPTION

The TPS65137 is designed to provide best in class picture quality for AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring positive and negative voltage supply rails. With its wide input voltage range the device is ideally suited for AMOLED displays, which are used in mobile phones and smart phones. With this device the input voltage can be higher than the positive output voltage and still maintains accurate regulation of V_{POS}. Using the digital control pin (CTRL) allows adjusting the negative output voltage in digital steps. The TPS65137 uses a novel technology enabling excellent line and load regulation with minimum output voltage ripple by using a LDO post regulator for V_{POS}. This is required avoiding disturbance of the AMOLED display due to input voltage transients occurring during transmit periods in mobile phones.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1) (2)

T_A	ORDERING P/N	PACKAGE MARKING
–40°C to 85°C	TPS65137A	PTTI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.
(2) Contact the factory for the availability of the TPS65137 with output voltage discharge function.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range(2)	VIN	–0.3	7.0	V
	CTRL, SWP, OUTP	–0.3	7.0	
	SWP, OUTP	–0.3	7.0	
	OUTN	+0.3	–5.5	
	CB	–0.3	7.0	
	CT	–0.3	3.6	
ESD rating	HBM		2	kV
	MM		200	V
	CDM		500	V
Continuous total power dissipation		See Thermal Information Table		
Operating junction temperature range	T_J	–40	150	°C
Operating ambient temperature range	T_A	–40	85	°C
Storage temperature range	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65137 DSC 10	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	56.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	65.8	
θ_{JB}	Junction-to-board thermal resistance (4)	25.2	
ψ_{JT}	Junction-to-top characterization parameter (5)	1.0	
ψ_{JB}	Junction-to-board characterization parameter (6)	17.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.3		5.5	V
T_A	Operating ambient temperature	–40		+85	°C
T_J	Operating junction temperature	–40		+125	°C

(1) Refer to application section for further information.

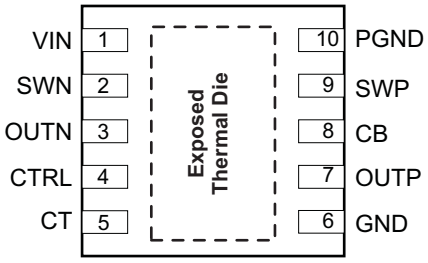
ELECTRICAL CHARACTERISTICS

V_{IN} = 3.5V, EN = VIN, OUTP = 4.63V, OUTN = –4.93V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.3		5.5	V
I_Q	Operating quiescent current into Vin			400		µA
I_{SD}	Shutdown current into Vin			0.1	1.0	µA
UVLO	Under-voltage lockout threshold	V_{IN} falling			2.0	V
		V_{IN} rising			2.3	
f_s	Switching frequency	Iout = 100 mA		1.6		MHz
	Thermal shutdown			145		°C
	Thermal shutdown hysteresis			10		°C
OUTPUT OUTP						
V_{POS}	Positive output voltage regulation	V_{IN} = 2.3V to 5.5V, Iload=0mA to 150mA	–1%	4.63	1%	V
I_{outP}	Output current OUTP		200			mA
$R_{DS(ON)}$	SWP MOSFET on-resistance	V_{IN} = 3.7 V, Isw = 200 mA		300		mΩ
	SWP MOSFET rectifier on-resistance	V_{IN} = 3.7 V, Isw = 200 mA		350		
I_{leak}	Leakage current into OUTP	CTRL = GND, V_{OUTP}= 4.6V; TPS65137A		17	25	uA
I_{SWP}	SWP switch current limit	V_{IN} = 2.9 V	0.9	1.1		A
V_{drop}	LDO Dropout voltage	Iout = 100 mA		300		mV
	Line regulation			0		%/V
	Load regulation			0.001		%/mA
OUTPUT OUTN						
V_{NEG}	Negative output voltage range		–2.2		–5.2	V
V_{NEG}	Negative output voltage regulation	V_{IN} = 2.3V to 5.5V, Iload = 0mA to 150mA; Valid for all voltage steps	–100		+100	mV
$R_{DS(ON)}$	SWN MOSFET on-resistance	V_{IN} = 3.7 V, Isw = 200 mA		400		mΩ
	SWN MOSFET rectifier on-resistance	V_{IN} = 3.7 V, Isw = 200 mA		550		
I_{LKG}	Leakage current out of OUTN	CTRL = GND, V_{OUTN}=-5.2V; TPS65137A		19	30	µA
I_{SWN}	SWN switch current limit	V_{IN} = 2.9 V	1.1	1.35		A
	Line regulation			0		%/V
	Load regulation			0.001		%/mA
CTRL INTERFACE						
V_H	Logic high-level voltage		1.2			V
V_L	Logic low-level voltage				0.4	V
R	Pull down resistor		150	200	860	kΩ
t_{init}	Initialization time			300	400	µs
t_{ss}	Softstart time			1		ms
t_{off}	Shutdown time period		30		80	µs
t_{high}	Pulse high level time period		2	10	25	µs
t_{low}	Pulse low level time period		2	10	25	µs
t_{store}	Data storage/accept time period		30		80	µs
t_{set}	OUTN transition time	C_T = 100 nF		20		ms
R_T	CT pin output impedance		150	250	500	kΩ

DEVICE INFORMATION

10 PIN TQFN PACKAGE
(TOP VIEW



Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
VIN	1	I	Input supply
CT	5	O	Sets the settling time for the voltage on Vneg when programmed to a new value
CB	8	O	Internal boost converter bypass capacitor
GND	6		Analog ground
PGND	10		Power Ground
SWN	2		Switch pin of the negative buck boost converter
OUTN	3	O	Output of negative buck boost converter
OUTP	7	O	Output of the boost converter
CTRL	4	I	Combined enable and output voltage program pin
SWP	9		Switch pin of the boost converter
Exposed thermal die			Connect this pad to analog GND.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency versus Output current		Figure 1
Efficiency versus Input voltage		Figure 2
Efficiency versus Negative voltage		Figure 3
Negative output voltage programming		Figure 4
Negative output voltage programming	Device enabled (CTRL = 400µs high), programmed to –3.0V	Figure 5
Light load current operation		Figure 6
Nominal load current operation	V_{IN} = 3.7V	Figure 7
Nominal load current operation	V_{IN} = 4.5V	Figure 8
Line transient response	150mA	Figure 9
Line transient response	100mA	Figure 10
Startup		Figure 11
Shutdown		Figure 12
Short circuit		Figure 13

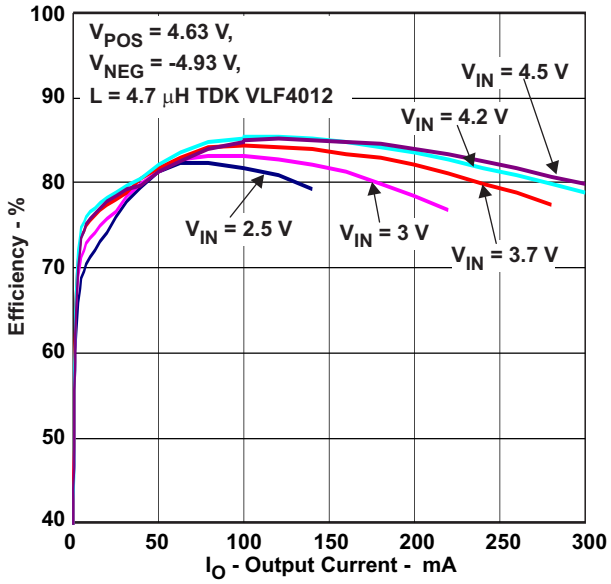


Figure 1. EFFICIENCY

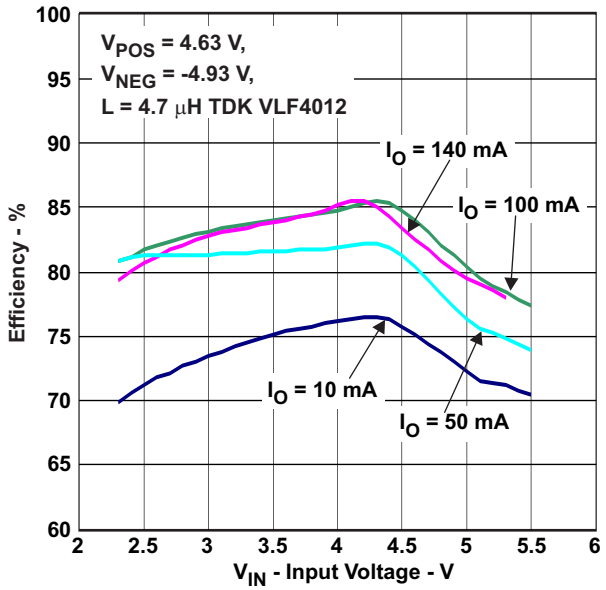


Figure 2. EFFICIENCY

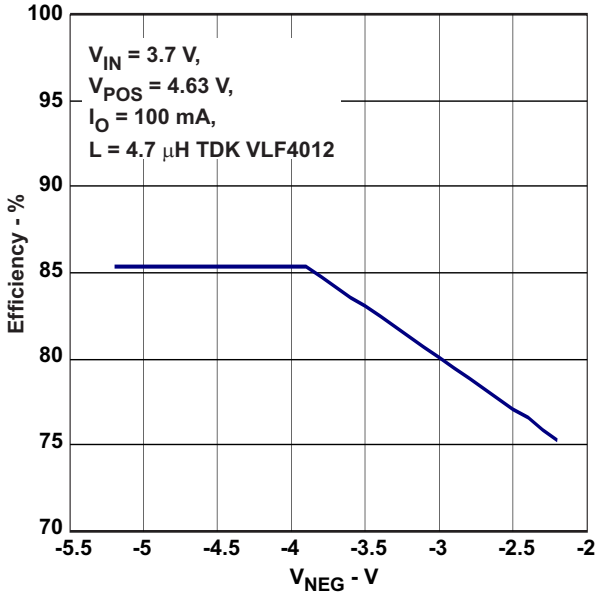


Figure 3. EFFICIENCY

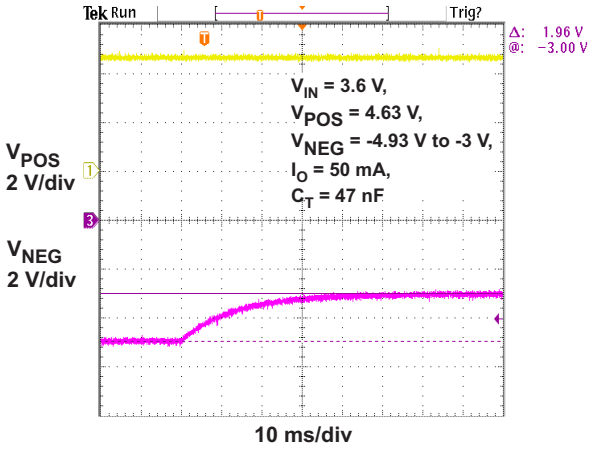


Figure 4. NEGATIVE OUTPUT VOLTAGE PROGRAMMING

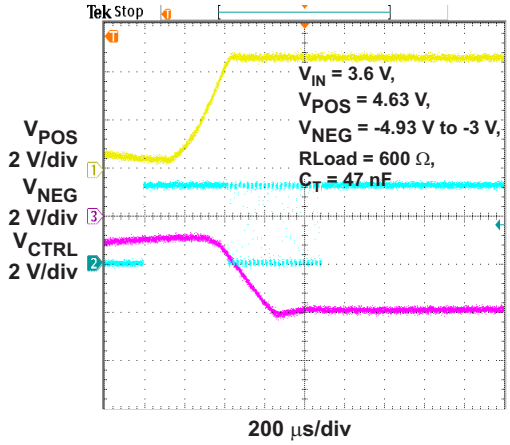


Figure 5. NEGATIVE OUTPUT VOLTAGE PROGRAMMING (Device enabled (CTRL = 400µs high), programmed to –3.0V)

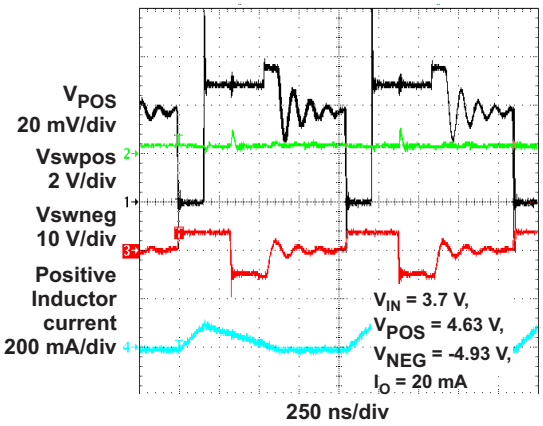


Figure 6. LIGHT LOAD CURRENT OPERATION

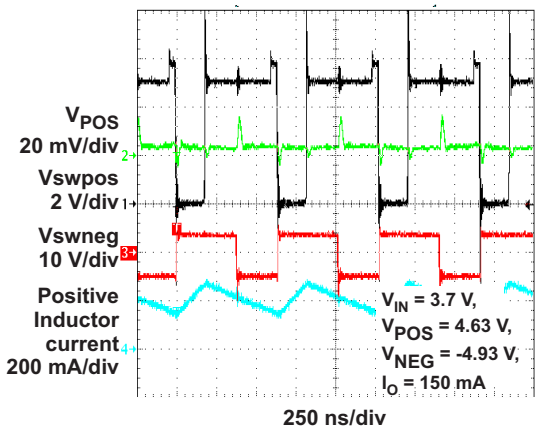


Figure 7. NOMINAL LOAD CURRENT OPERATION (V_{IN} = 3.7V)

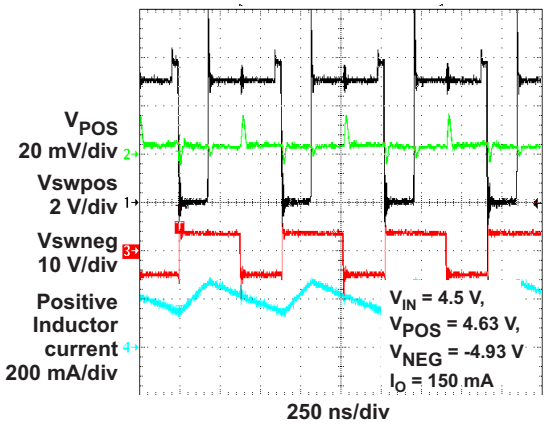


Figure 8. NOMINAL LOAD CURRENT OPERATION (V_{IN} = 4.5V)

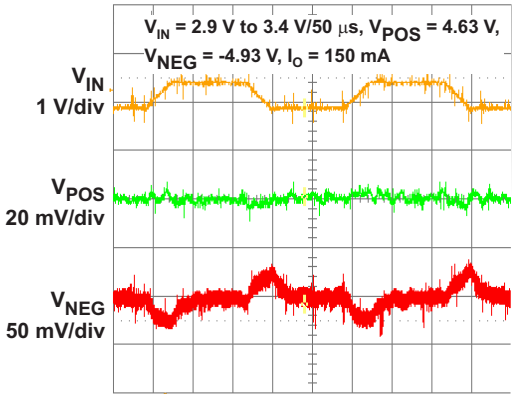


Figure 9. LINE TRANSIENT RESPONSE (150mA)

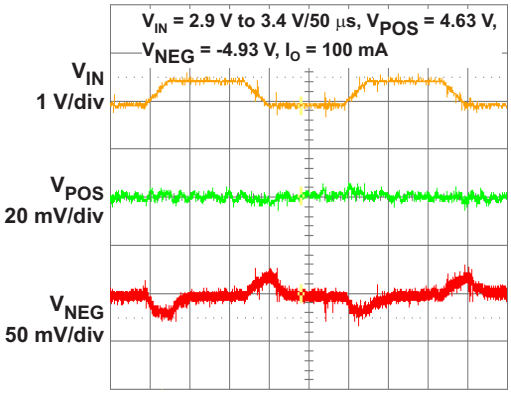


Figure 10. LINE TRANSIENT RESPONSE (100mA)

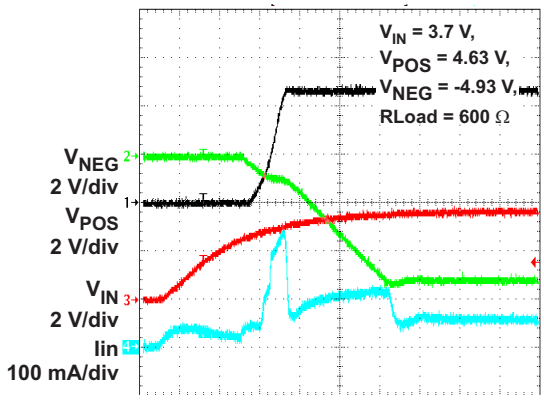


Figure 11. STARTUP

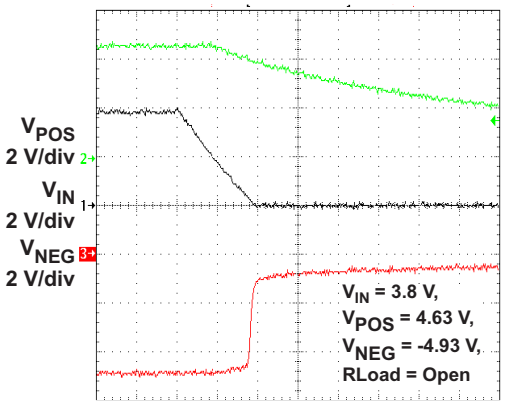


Figure 12. SHUTDOWN

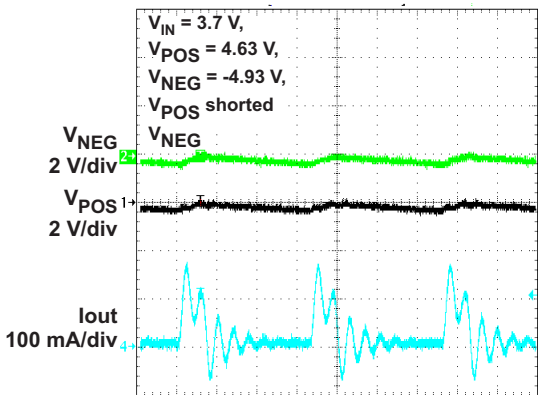
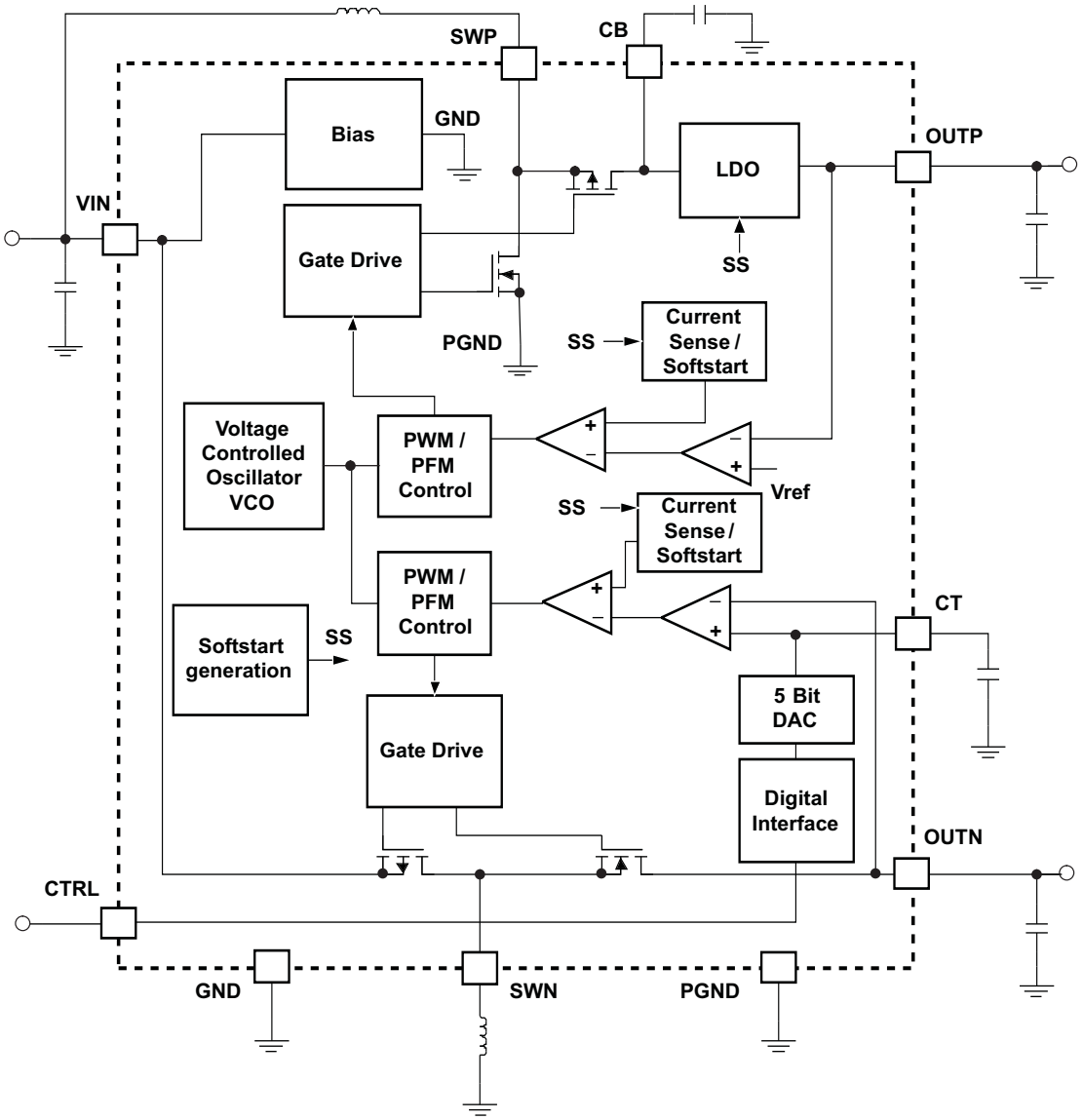


Figure 13. SHORT CIRCUIT

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

The TPS65137 consists of a boost converter using a LDO as post regulator. The output voltage of the boost converter is regulated to operate the internal LDO above its dropout voltage maintaining best line and load regulation of OUTP. The internal LDO disconnects OUTP during shutdown and allows regulation of the output when the input voltage is higher than OUTP. The LDO minimizes the output voltage ripple of OUTP. The negative output uses a buck boost converter topology operating in DCM (Discontinuous Conduction Mode) providing superior line regulation. In order to adjust the output voltage of the negative converter a digital interface can be used to program the output voltage. To achieve high efficiency over the entire load current range the device reduces the switching frequency with the load current using its internal voltage controlled oscillator (VCO). Since the boost converter output CB is post regulated by the integrated LDO (Low Dropout Regulator) the output voltage ripple is minimized and the line transient response is at its best. Because of this topology the operation mode of the boost converter has minimum effect on the output voltage ripple observed on OUTP. The boost converter, as well as the negative converter operate in peak current mode using the VCO (Voltage Controlled Oscillator) while operating in DCM (Discontinuous Conduction Mode). When entering CCM (Continuous Conduction Mode) the converter operates in peak current control using fixed off time control.

POWER SAVE MODE OPERATION

In order to maintain high efficiency over the entire load current range the converter reduces its switching frequency as the load current decreases. To maintain a controlled switching frequency a voltage controlled oscillator (VCO) is used.

SOFT START AND SHORT CIRCUIT PROTECTION

The device has a soft-start implemented limiting inrush current during turn on. The device is also protected against short circuits of the outputs to ground or when the outputs shorted together. This is implemented with two output voltage thresholds determining the device switch current limit and LDO operation shown in Figure 14.

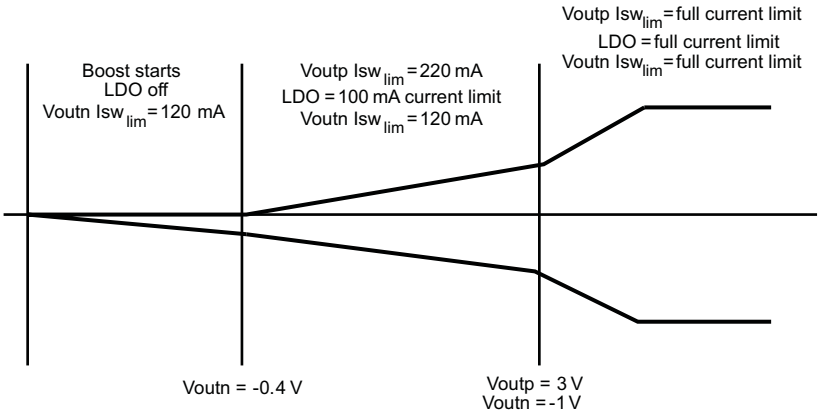


Figure 14. Soft Start and Short Circuit Thresholds

When the device is enabled pulling CTRL pin high then the boost converter and buck converter starts with reduced switch current limit. During this period of time the LDO is turned off. As V_{NEG} reaches –0.4V then the LDO is turned on having a 100mA current limit. The switch current limit of both outputs is increased to 220mA and 120mA. When V_{POS} reaches 3V and V_{NEG} reaches –1V, then both outputs operate with full current limit. This architecture limits the inrush current during start-up and protects the device during short circuits events. When the positive output is shorted to the negative output then the device cycles between the first and second section of the start-up sequence. By that, the output current cycles between zero and 100mA. This protects the device and avoids excessive power dissipation during short circuit conditions. With this architecture the device is able to start-into full load current once V_{POS} exceeds 3V and V_{NEG} is lower than –1V.

ENABLE (CTRL pin)

The CTRL pin serves two functions. One is the enable and disable of the device, the other is the output voltage programming of the device. If the digital interface is not required the CTRL pin can be used as a standard enable pin for the device. Pulling CTRL high starts the converter operating with its default output voltage on OUTN of –4.93V.

DIGITAL INTERFACE (CTRL)

The digital interface allows programming the negative output voltage OUTN in digital steps. If the digital output voltage setting is not required then the CTRL pin can also be used as a standard enable pin. In such a case the device will come up with its default output voltage of OUTN of –4.93V.

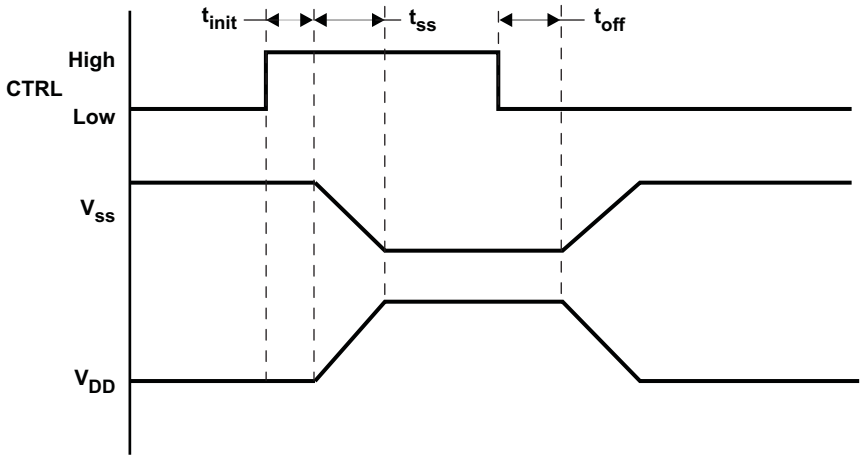


Figure 15. CTRL Used as a Standard Device Enable

The digital output voltage programming of OUTN is implemented by a simple digital interface with the timing shown in Figure 16.

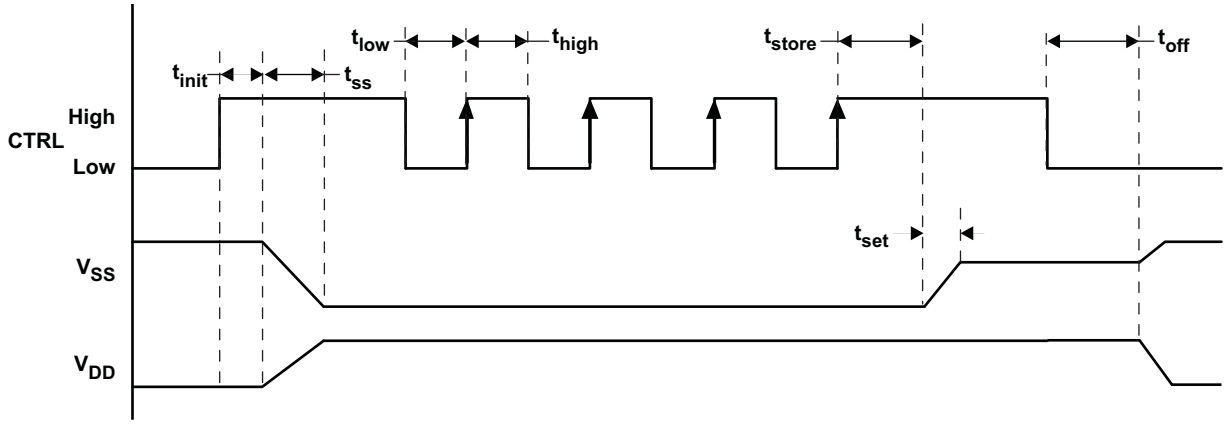


Figure 16. Digital Interface Using CTRL

Once CTRL is pulled high the device will come up with its default voltage of –4.93V. The TPS65137 has a 5 bit DAC implemented with the correspondent output voltage as given in Table 1. The interface counts the rising edges applied to CTRL pin once the device is enable. For example with the timing diagram shown in Figure 16, OUTN is programmed to –4.93V since 4 rising edges are applied. Other output voltages are programmed according to Table 1.

Table 1. Programming Table for OUTN

BIT/RISING EDGES	OUTN (Vss)	DAC VALUE	BIT/RISING EDGES	OUTN(Vss)	DAC VALUE
Default	–4.93 V	00000	16	–3.7 V	10000
1	–5.23 V	00001	17	–3.62 V	10001
2	–5.13 V	00010	18	–3.52 V	10010
3	–5.03 V	00011	19	–3.42 V	10011
4	–4.93 V	00100	20	–3.32 V	10100
5	–4.83 V	00101	21	–3.22 V	10101
6	–4.73 V	00110	22	–3.12 V	10110
7	–4.63 V	00111	23	–3.02 V	10111
8	–4.53 V	01000	24	–2.92 V	11000
9	–4.43 V	01001	25	–2.82 V	11001
10	–4.33 V	01010	26	–2.72 V	11010
11	–4.23 V	01011	27	–2.62 V	11011
12	–4.13 V	01100	28	–2.52 V	11100
13	–4.03 V	01101	29	–2.42 V	11101
14	–3.93 V	01110	30	–2.31 V	11110
15	–3.82 V	01111	31	–2.21 V	11111

V_{neg} Programming Transition Time t_{set} for OUTN (C_T)

The TPS65137 allows setting the transition time t_{set} using an external capacitor connected to pin CT. The transition time is the time period required to move OUTN from one voltage level to the next programmed voltage level. When the CT pin is left open then the shortest possible transition time is programmed. When connecting a capacitor to the CT pin then the transition time is given by the R-C time constant. This is given by the output impedance of the CT pin of typically 250kΩ and the external capacitance. Within one τ the output voltage OUTN has reached 70% of its programmed value. An example is given when using 100nF for C_T.

$\tau \approx t_{set70\%} = 250\ k\Omega \times C_T = 250\ k\Omega \times 100\ nF = 25\ mS$

INPUT CAPACITOR SELECTION

The device typically requires a 4.7µF ceramic input capacitor. Larger values can be used to lower the input voltage ripple.

Table 2. Input Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
4.7 µF/10 V	Taiyo Yuden LMK107BJ475	0603
10 µF/10 V	Taiyo Yuden LMK212BJ106	0805
10 µF/6.3 V	Taiyo Yuden JMK107BJ106	0603

BOOST CONVERTER DESIGN CONSIDERATION, V_{pos}

The positive output consists of a boost converter using a LDO as post regulator. The maximum output current is limited by the minimum current limit of the LDO, of 200mA. The component values and output current are calculated at maximum load current in continuous conduction operation. The typical switching frequency during this operation mode is 1.4MHz.

The boost converter duty cycle is:

$$D = 1 - \frac{V_{IN} \times \eta}{V_{POS}} \quad (1)$$

To calculate the duty cycle, a good estimation for the efficiency, η, is 75% or it can be taken out of the typical curve in **Figure 1**. In order to calculate the maximum output current of the boost converter for a certain input voltage, the following formula is used:

$$Iout = (1 - D)\left(Isw - \frac{V_{IN} \times D}{2 \times fs \times L}\right) \quad (2)$$

The maximum output current is given at the highest switching frequency of typically 1.4MHz and minimum switch current limit of 0.9A. Equation 3 is used to calculate the switch peak current.

$$I_{swpeak} = \frac{V_{IN} \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D} \quad (3)$$

The inductor needs to be rated for this switch peak current to avoid inductor saturation.

The boost converter output capacitor is connected to pin CB and a 4.7µF capacitor is sufficient. A 2.2µF capacitor is used on the output V_{POS}, which is the output of the internal low dropout regulator (LDO).

Table 3. Output Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
4.7 µF/10 V	Taiyo Yuden LMK107BJ475	0603
2.2 µF/10 V	Taiyo Yuden LMK107BJ225	0603

NEGATIVE BUCK BOOST CONVERTER DESIGN CONSIDERATION, V_{neg}

The negative output is generated with a buck boost converter. The component values and output current are calculated at maximum load current in continuous conduction operation. The typical switching frequency during this operation mode is 1.4MHz.

The buck boost converter duty cycle is:

$$D = \frac{|V_{NEG}|}{V_{IN} \times \eta + |V_{NEG}|} \quad (4)$$

To calculate the duty cycle a good estimation for the efficiency, η, is 75% or it can be taken out of the typical curve in Figure 1. In order to calculate the maximum output current of the buck boost converter for a certain input voltage, the following formula is used:

$$Iout = (1 - D)\left(Isw - \frac{V_{IN} \times D}{2 \times fs \times L}\right) \quad (5)$$

The maximum output current is given at the highest switching frequency of typically 1.4MHz and minimum switch current limit of 1.1A. Equation 6 is used to calculate the switch peak current.

$$I_{swpeak} = \frac{V_{IN} \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D} \quad (6)$$

The inductor needs to be rated for this switch peak current to avoid inductor saturation. Refer to Table 4 for possible inductors for this application. A 4.7µF output capacitor is used on the output V_{NEG}. Larger capacitor values can be used to minimize the output voltage ripple. Refer to Table 3 for output capacitor selection.

INDUCTOR SELECTION

The device is optimized to operate with 4.7uH inductors. Different inductor values will change the converter efficiency and output voltage ripple. A 2.2uH inductor is also a possible solution. Any other inductor values will degrade device performance and stability which is not recommended for this device.

Table 4. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	Isat/DCR
4.7 µH	TDK VLF4012	3.7 × 3.5 × 1.2	1.1A/140mΩ

APPLICATION INFORMATION

PCB LAYOUT

The layout for his device is important to keep the output voltage ripple and output voltage accuracy as low and accurate as possible. The following layout guidelines apply for this device:

- Keep the switch note pad for the boost converter and inverter switch as small as possible to avoid coupling into the output.
- The ground connection for the inductor of the negative converter needs to be as wide as possible to avoid noise generated by inductor ground currents.
- The ground connection of the timing capacitor on pin CT needs to be isolated and directly routed to the GND pin of the device. This is important to avoid noise being coupled into the error amplifier which is internally connected to the CT pin.
- Having the ground connection of the boost converter output capacitor and LDO output capacitor in a close connection to the device ground and power pad connection achieves best load regulation.

REVISION HISTORY

Changes from Original (May 2010) to Revision A **Page**

- Changed Features 6, 7 and 8 from 4.6V to 4.63V, -5.2V to -5.23V and -4.9V to -4.93V 1
- Changed TYPICAL APPLICATION V_{POS} from 4.6V/200mA to 4.63V/200mA 1
- Changed ELECTRICAL CHARACTERISTICS conditions from OUTP=4.6V to OUTP=4.63V and OUTN= -4.9V to -4.93V 4
- Changed ELECTRICAL CHARACTERISTICS OUTPUT OUTP V_{POS}, TYP column from 4.6 to 4.63 4
- Changed V_{POS} from 4.6V to 4.63V and V_{NEG} from -4.9V -4.93V in graphs 6
- Changed Figure 9 waveform 7
- Changed Figure 10 waveform 7
- Changed -4.9V. to -4.93V in Digital Interface (CTRL) section 11
- Changed values in Table 1 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65137ADSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PTTI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

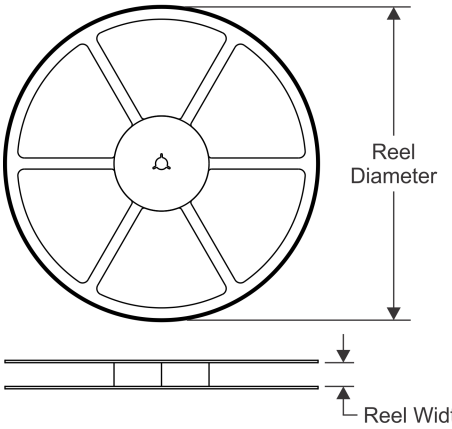
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

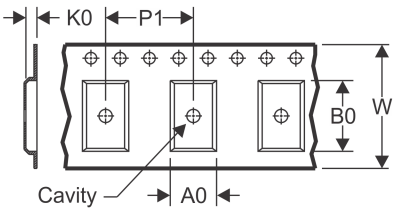
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

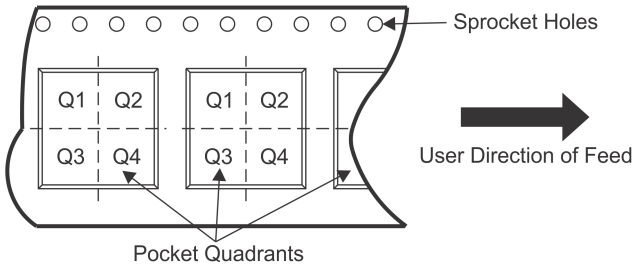


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

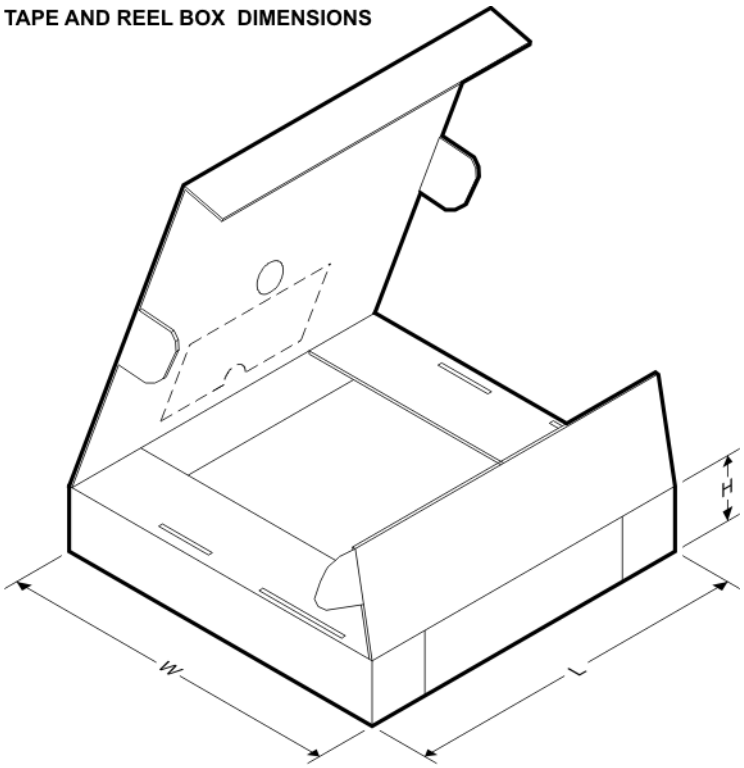
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65137ADSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65137ADSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

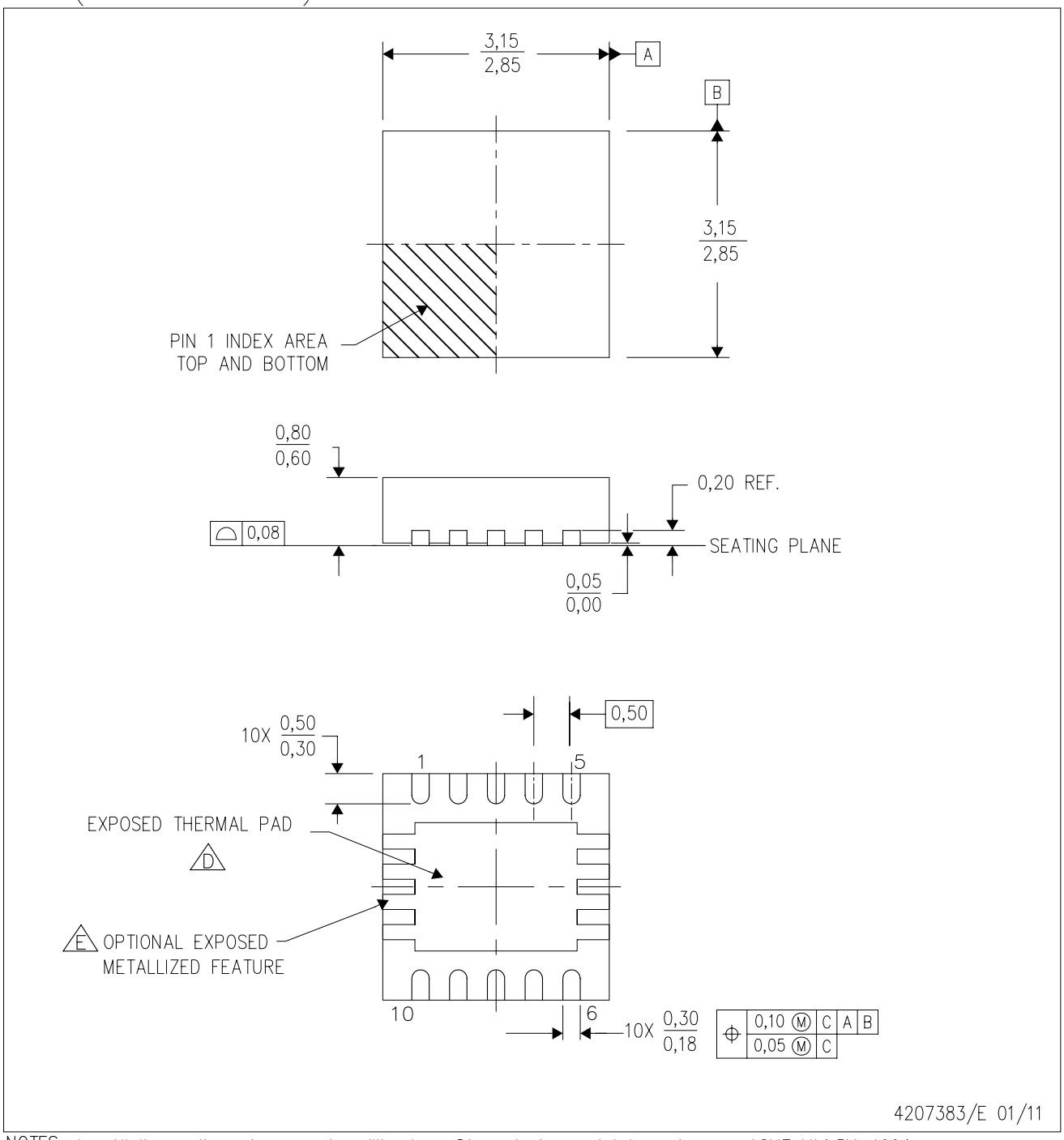
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65137ADSCR	WSON	DSC	10	3000	367.0	367.0	35.0
TPS65137ADSCR	WSON	DSC	10	3000	367.0	367.0	35.0

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

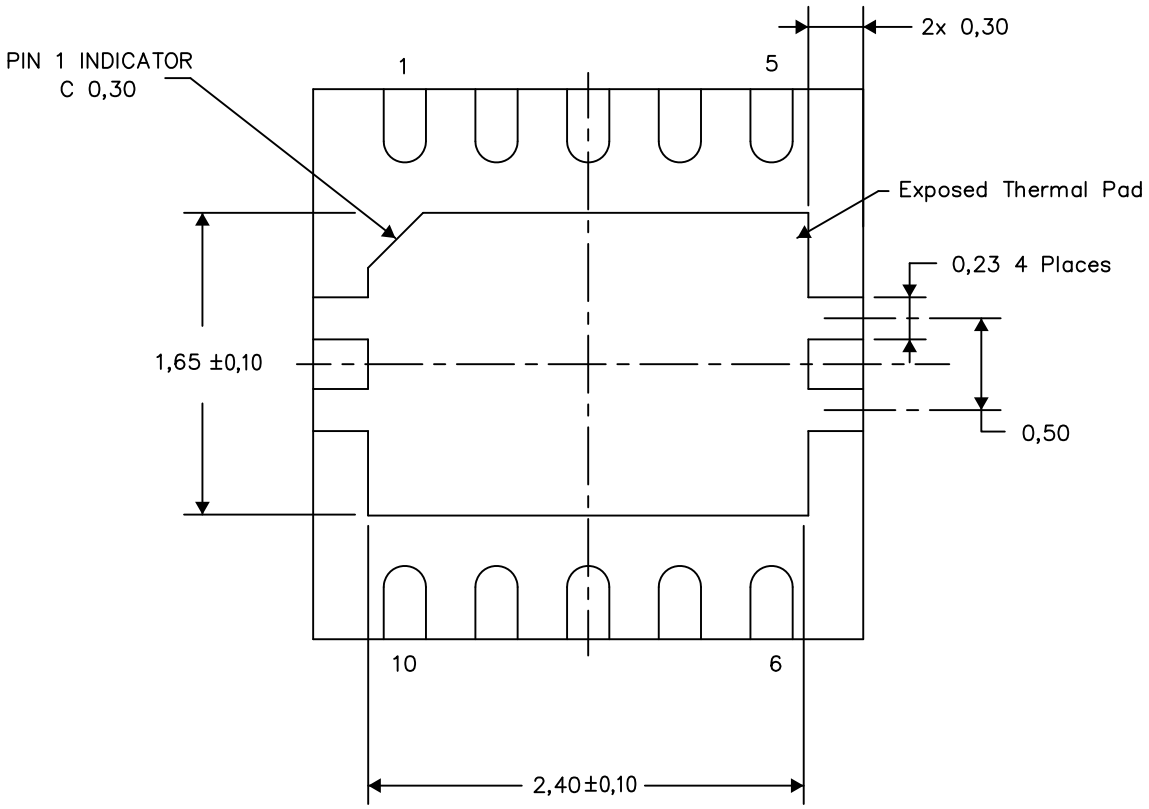
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



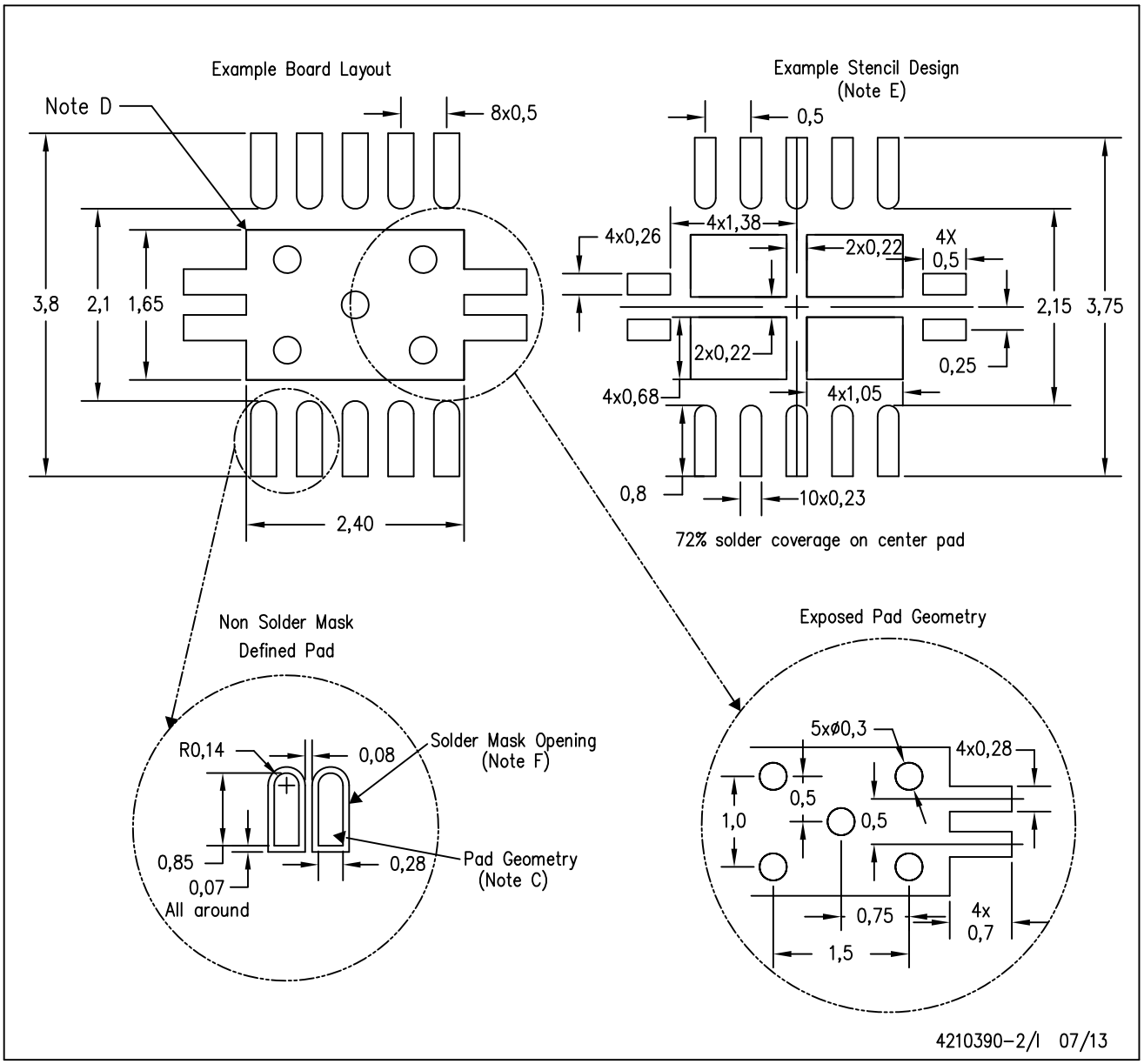
Bottom View

Exposed Thermal Pad Dimensions

4210391–2/M 08/13

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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