±5 V, 250 mA Dual Output Power Supply

FEATURES

- 2.9 V to 5.0 V Input Voltage Range
- Fixed 5.0 V V_{POS} Output Voltage
  - 1% Output Voltage Accuracy
- Fixed 5.0 V V_{NEG} Output Voltage
  - 1% Output Voltage Accuracy
- Up to 250 mA Output Current from V_{POS} and V_{NEG}
- Excellent Line and Load Transient Response
- Operates in CCM Mode for Noise Free Output Voltage
- Boost Converter Able to Operate in "Down Mode" (VIN close to or above V_{POS})
- High Converter Efficiency
- Short Circuit Protection
- Thermal Shutdown
- 3×3 mm 12 Pin QFN Package

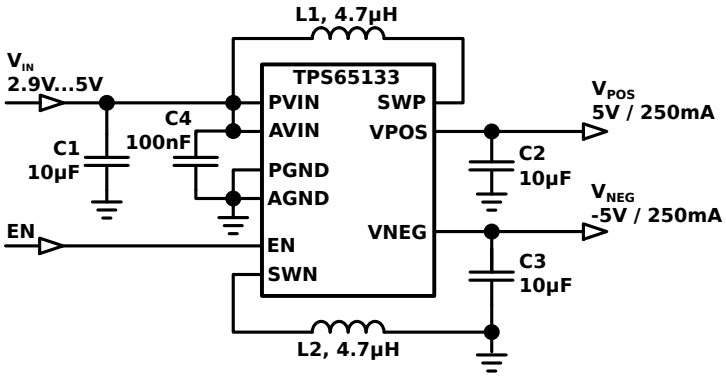
APPLICATIONS

- LCD Bias
- Active Matrix OLED
- Operational Amplifier Supply
- General ±5 V Power Supply

DESCRIPTION

The TPS65133 is designed to drive LCD displays requiring a positive and negative supply rail. It may also be used as a general ±5 V supply for operational amplifiers or other devices requiring similar positive and negative supplies. The device integrates a boost converter and an inverting buck-boost converter suitable for battery operated products.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1) (2)

T_A	PACKAGE	ORDERING P/N	TOP-SIDE MARKING
–40°C to 85°C	12-Pin 3x3 QFN	TPS65133DPDR	SHY

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range(2)	SWP, VPOS, PVIN, AVIN, EN	-0.3	6.0	V
	VNEG	-6.5	0.3	
	SWN	-6.5	5.5	
ESD rating	HBM		2	kV
	MM		200	V
	CDM		500	V
Operating junction temperature range	T_J	-40	150	°C
Operating ambient temperature range	T_A	-40	85	°C
Storage temperature range	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) With respect to GND pin.

THERMAL INFORMATION

THERMAL METRIC(1)		QFN (12 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	51.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	25.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9	3.7	5	V
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

(1) Refer to application section for further information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, EN = V_{IN}, V_{POS} = 5V, V_{NEG} = -5V, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT AND THERMAL PROTECTION						
V_{IN}	Input voltage range		2.9		5	V
I_{SD}	Shutdown current into V_{IN}	EN = GND		0.1	15	µA
UVLO	Under-voltage lockout threshold	V_{IN} falling			2.1	V
		V_{IN} rising			2.5	
T_{SD}	Thermal shutdown temperature			135		°C
LOGIC SIGNALS						
V_H	Logic high-level voltage		1.2			V
V_L	Logic low-level voltage				0.4	V
BOOST CONVERTER (V_{POS})						
V_{POS}	Positive output voltage		4.95	5	5.05	V
$R_{DS(ON)}$	SWP MOSFET on-resistance	I_{SWP} = 200mA		250		mΩ
	SWP MOSFET rectifier on-resistance			350		
f_{SWP}	SWP switching frequency	I_{POS} = 200mA	1.2	1.7	2.2	MHz
I_{SWP}	SWP switch current limit	Inductor valley current	0.8	1.1		A
$V_{P(SCP)}$	Short circuit threshold in operation	V_{POS} falling		4.1		V
$t_{P(SCP)}$	Short circuit detection time in operation		1	3	5	ms
$R_{P(DCG)}$	V_{POS} Discharge resistance	EN = GND, I_{POS} = 1mA	15	30	60	Ω
	Line regulation	I_{POS} = 100 mA		.02		%/V
	Load regulation	VIN = 3.7 V		.24		%/A
BUCK-BOOST CONVERTER (V_{NEG})						
V_{NEG}	Negative output voltage default		-5.05	-5	-4.95	V
$R_{DS(ON)}$	SWN MOSFET on-resistance	I_{SWN} = 200mA		250		mΩ
	SWN MOSFET rectifier on-resistance			350		
f_{SWN}	SWN switching frequency	I_{NEG} = 200mA	1	1.7	2.4	MHz
I_{SWN}	SWN switch current limit	Inductor valley current	1.5	2.2		A
$V_{N(SCP)}$	Short circuit threshold in operation			-4.5		V
$t_{N(SCP)}$	Short circuit detection time in operation		1	3	5	ms
$R_{N(DCG)}$	V_{NEG} Discharge resistance	EN = GND, I_{NEG} = 1mA	100	150	200	Ω
$t_{N(DLY)}$	Start-up delay time after V_{POS} reaches target output to when V_{NEG} will begin startup			2		ms
	Line regulation	I_{NEG} = 100 mA		.01		%/V
	Load regulation	VIN = 3.7 V		.16		%/A

DEVICE INFORMATION

10 PIN TQFN PACKAGE
(TOP VIEW)

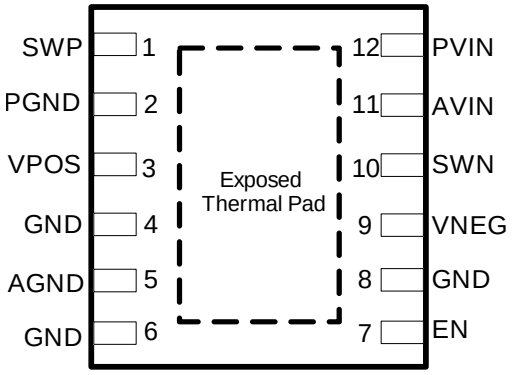
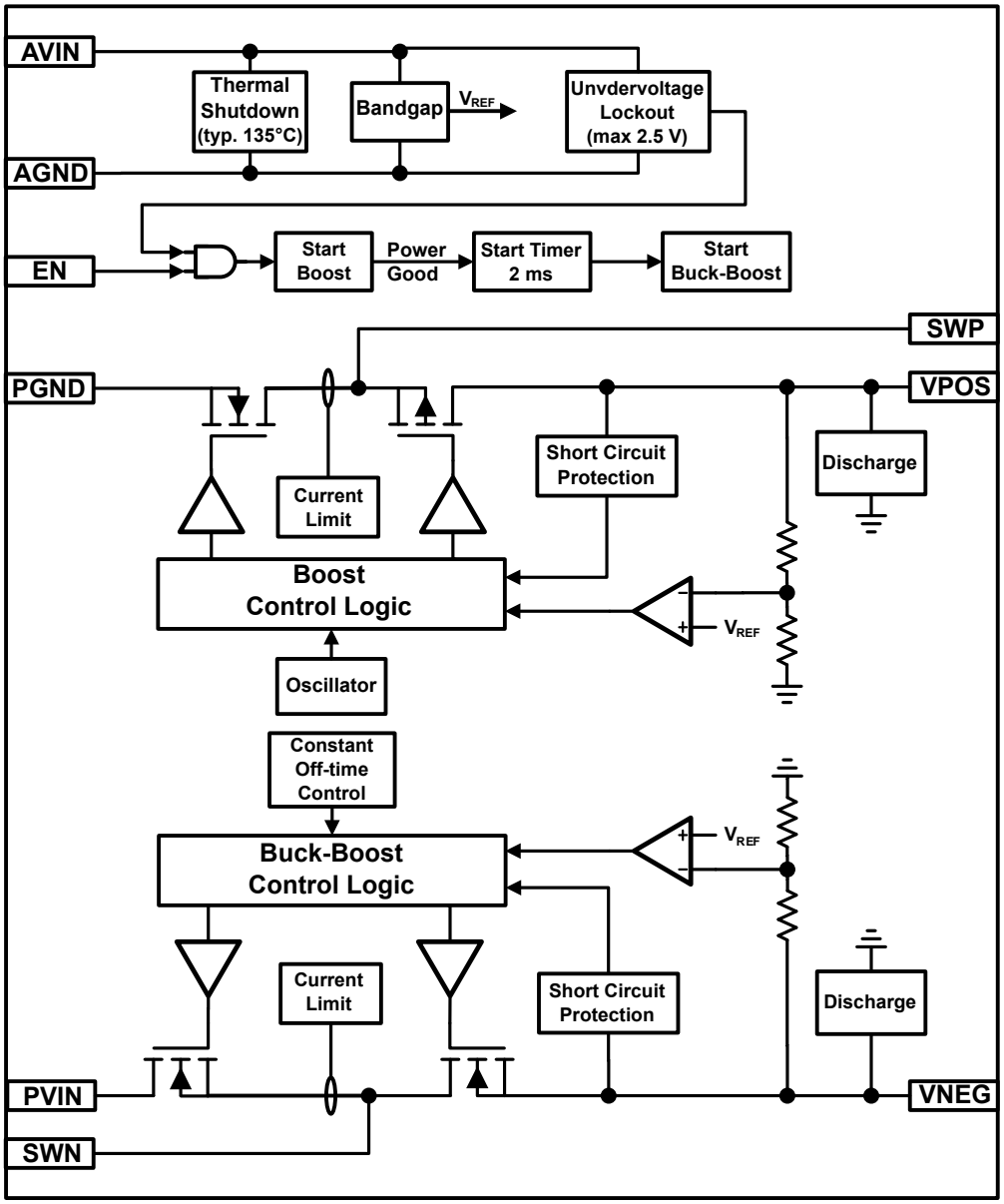


Table 1. Pin Functions

NO.	NAME	TYPE(1)	DESCRIPTION
1	SWP	I	Switch pin of the boost converter
2	PGND	G	Power ground of the boost converter
3	VPOS	O	Output of the boost converter (V_{POS}), place a capacitor close to this pin.
4	GND	G	Ground
5	AGND	G	Analog ground
6	GND	G	Ground
7	EN	I	Enable of boost and buck boost converter
8	GND	G	Ground
9	VNEG	O	Output of the negative buck boost converter (V_{NEG}), place a capacitor close to this pin
10	SWN	I	Switch pin of the negative buck boost converter
11	AVIN	I	Internal logic supply pin
12	PVIN	I	Supply pin for the negative buck boost converter. Place a capacitor close to this pin
—	Exposed thermal pad	G	Connect this pad to all GND pins

(1) G = Ground, I = Input, O = Output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

		FIGURE
Efficiency vs. Output current	V_{POS} = 5 V, V_{NEG} = -5 V $I_{OUT} = I_{POS} + I_{NEG}$, $I_{POS} = I_{NEG}$	Figure 1
Line Regulation	V_{POS} = 5 V, VIN = 2.9 V to 5.0 V	Figure 2
	V_{NEG} = -5 V, VIN = 2.9 V to 5.0 V	Figure 3
Startup	V_{POS} Boost and V_{NEG} Buck-Boost	Figure 4
Switch pin, inductor current and output waveform	V_{POS} Boost, V_{POS} = 5 V, I_{OUT} = 100 mA	Figure 5
	V_{POS} Boost, V_{POS} = 5 V, I_{OUT} = 250 mA	Figure 6
	V_{NEG} Buck-Boost, V_{NEG} = -5 V, I_{OUT} = 100 mA	Figure 7
	V_{NEG} Buck-Boost, V_{NEG} = -5 V, I_{OUT} = 250 mA	Figure 8
Load Transient	VIN = 3.7 V, I_{POS} = 50 mA to 200 mA	Figure 9
	VIN = 3.7 V, I_{NEG} = 50 mA to 200 mA	Figure 10

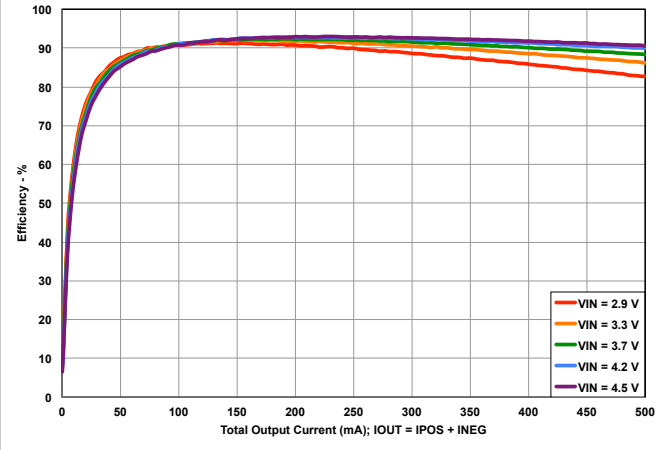


Figure 1. EFFICIENCY vs. OUTPUT CURRENT
V_{POS} = 5 V, V_{NEG} = -5 V
$I_{OUT} = I_{POS} + I_{NEG}$, $I_{POS} = I_{NEG}$

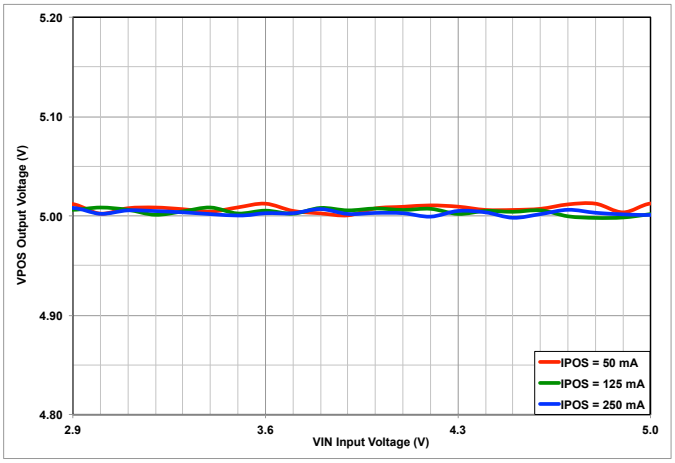


Figure 2. V_{POS} OUTPUT VOLTAGE vs. INPUT VOLTAGE
V_{POS} = 5 V, VIN = 2.9 V to 5.0 V

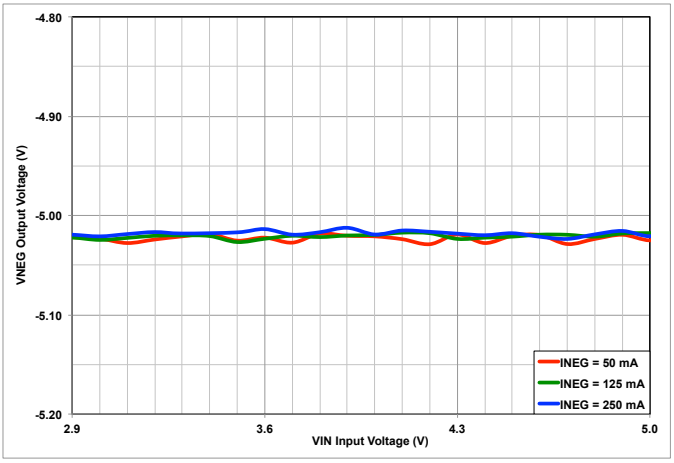


Figure 3. V_{NEG} OUTPUT VOLTAGE vs. INPUT VOLTAGE
V_{NEG} = -5 V, VIN = 2.9 V to 5.0 V

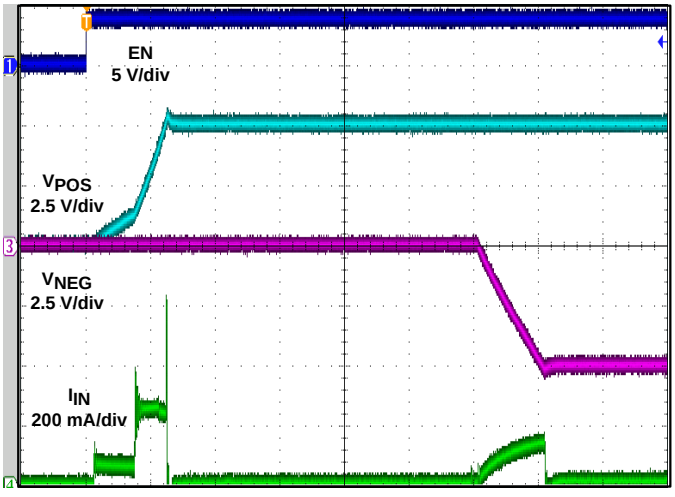


Figure 4. START UP
V_{POS} BOOST and V_{NEG} BUCK-BOOST

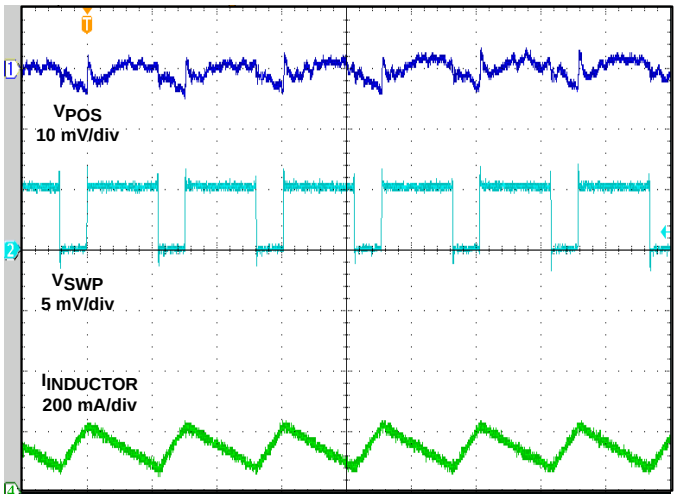


Figure 5. SWITCH PIN, INDUCTOR CURRENT and OUTPUT V_{POS} BOOST, V_{POS} = 5 V, I_{OUT} = 100 mA

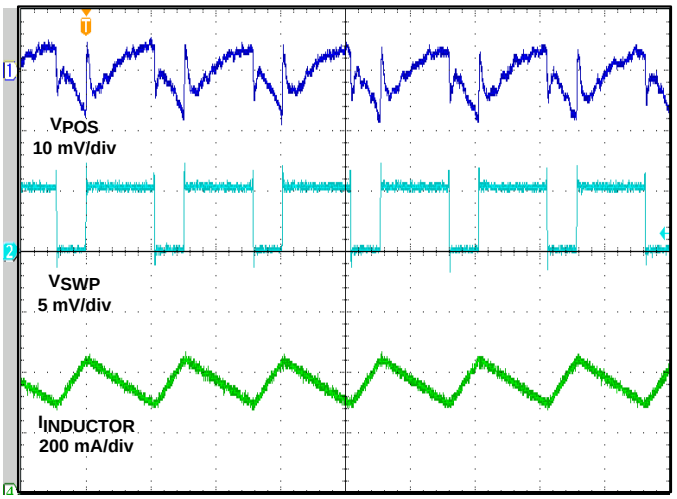


Figure 6. SWITCH PIN, INDUCTOR CURRENT and OUTPUT V_{POS} BOOST, V_{POS} = 5 V, I_{OUT} = 250 mA

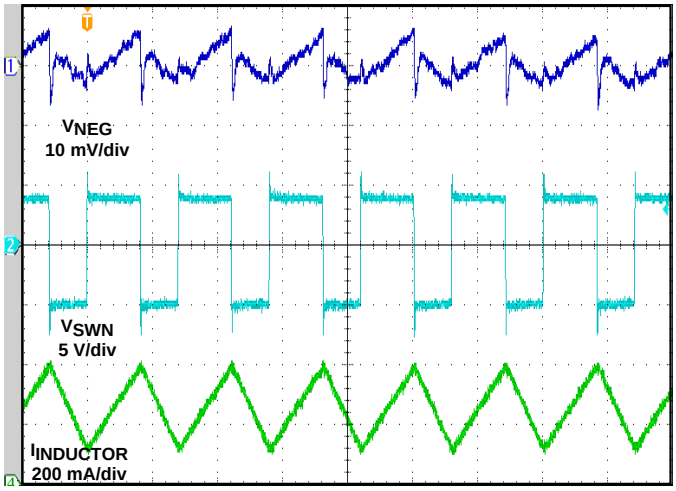


Figure 7. SWITCH PIN, INDUCTOR CURRENT and OUTPUT V_{NEG} BOOST, V_{NEG} = –5 V, I_{OUT} = 100 mA

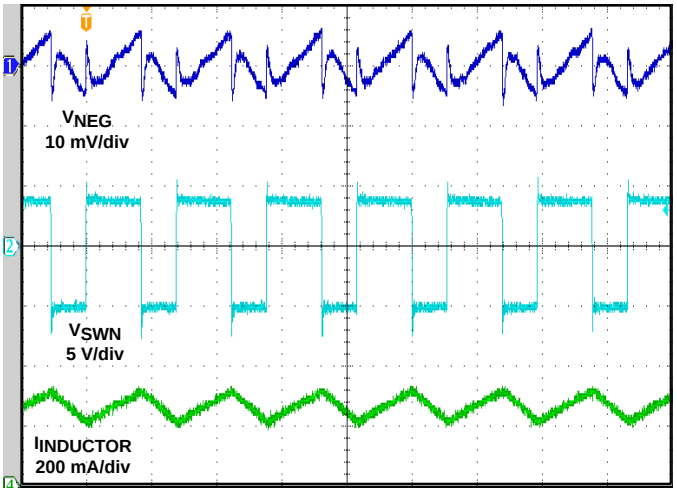


Figure 8. SWITCH PIN, INDUCTOR CURRENT and OUTPUT V_{NEG} BOOST, V_{NEG} = –5 V, I_{OUT} = 250 mA

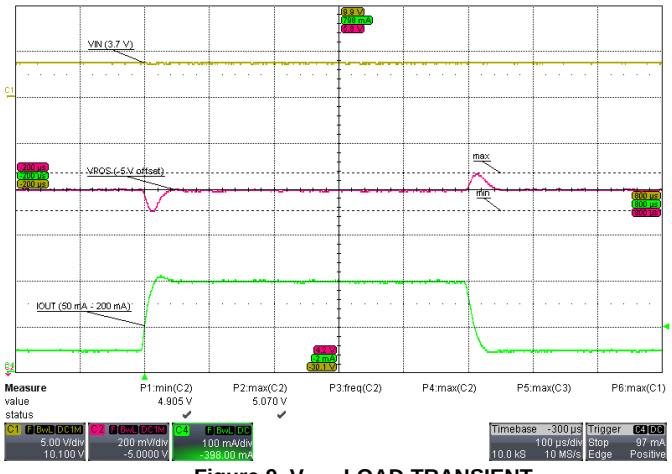


Figure 9. V_{POS} LOAD TRANSIENT VIN = 3.7 V, I_{POS} = 50 mA to 200 mA

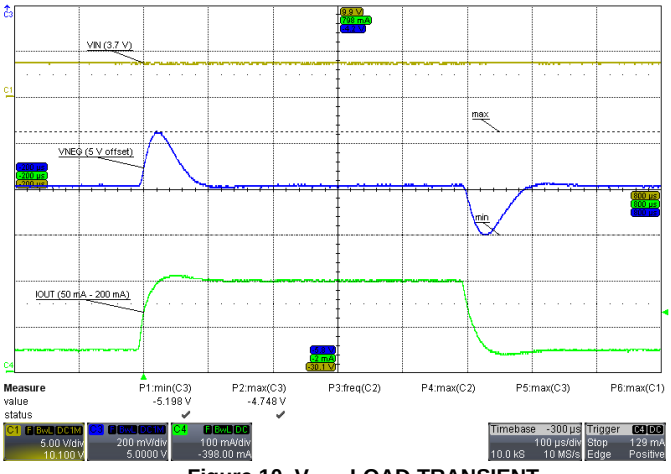


Figure 10. V_{NEG} LOAD TRANSIENT VIN = 3.7 V, I_{NEG} = 50 mA to 200 mA

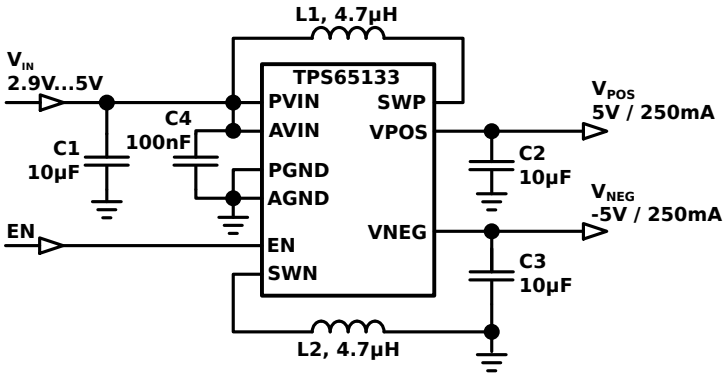


Figure 11. Application for Typical Characteristics

Table 3. Bill of Materials for Typical Characteristics

COMPONENT	VALUE	PART NUMBER	MANUFACTURER
C1, C2, C3	10µF	GRM219R61A106KE44	Murata
L1, L2	4.7µH	1239AS-H-4R7M (DFE 252012C)	TOKO

DETAILED DESCRIPTION

The TPS65133 integrates a boost converter and an inverting buck-boost converter. The positive output is fixed at 5 V and negative output is fixed at –5 V.

ENABLE (EN PIN)

The EN pin enables the boost and buck-boost converters. When EN is pulled high the device is enabled and both rails will startup according to the start-up sequence. When EN is pulled low the device is disabled and both outputs are discharged to ground.

START-UP AND SHUT-DOWN SEQUENCE

The device is enabled by EN pin going high, the boost converter (V_{POS}) will first start. Typically 2 ms after V_{POS} is in regulation, the buck-boost converter (V_{NEG}) starts. To reduce the inrush current, the switch current limit during start-up is reduced (soft-start). The start-up times depend on the output capacitances and the load currents.

During shut-down (EN = low) the outputs are actively discharged to GND, as long as V_{IN} > 1.5 V (typ). The discharge time depends on the output capacitance and the load current. The V_{POS} discharge circuit is stronger than the V_{NEG} discharge circuit, that means for the same output capacitance and load V_{POS} is discharged faster. The start-up and shut-down sequence for the typical application with 10 µF output capacitance is shown in Figure 12.

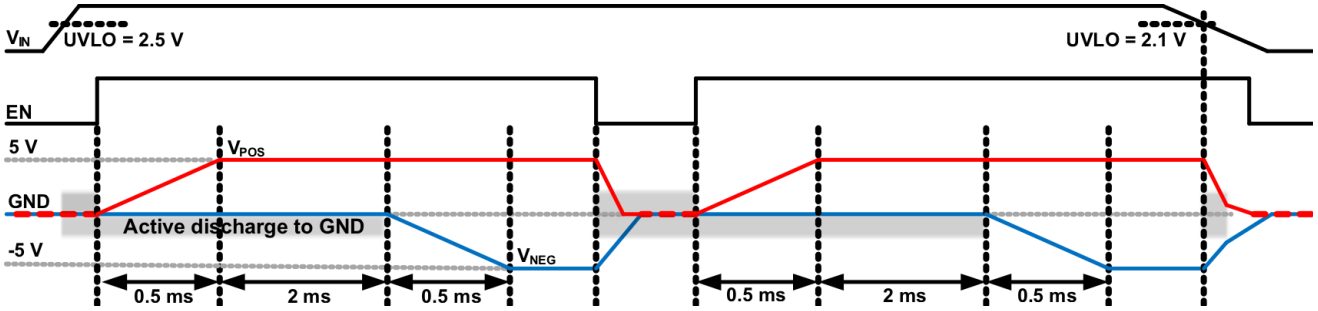


Figure 12. Start-up Sequence

INPUT VOLTAGE OPERATING RANGE

The TPS65133 is designed to work optimally over an input voltage range of 2.9V to 5V. However, as the input voltage drops below 2.9V and approaches the UVLO falling threshold (typically 2.1V), the device will continue to operate. The device is also able to function as the input voltage approaches the target output voltage of the switching converters; that is to say, as VIN approaches and reaches 5V, the VPOS and VNEG rails will continue to output +5V and -5V. The device is able to operate in a 'down' mode similar to an LDO in this condition as VIN approaches and reaches 5V.

OUTPUT DISCHARGE

The device actively discharges V_{POS} and V_{NEG} to GND when the device is disabled (see Figure 12 shaded area).

SHORT CIRCUIT PROTECTION

The device is protected against short circuits of V_{POS} and V_{NEG} to GND.

Short Before Power-up:

When a short-circuit is present before power-up, the output current is limited until the short is removed.

Short During Operation:

A short-circuit is detected if V_{POS} falls below 4.1 V for longer than 3 ms or V_{NEG} is pulled above –4.5V longer than 3 ms. In either case, the device goes into shutdown and this state is latched. Input and outputs are disconnected. To resume normal operation, V_{IN} must cycle below UVLO or EN has to toggle from low to high.

THERMAL SHUTDOWN

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically 135°C is exceeded the device goes into shutdown. To resume normal operation, V_{IN} must cycle below UVLO or EN has to toggle from low to high.

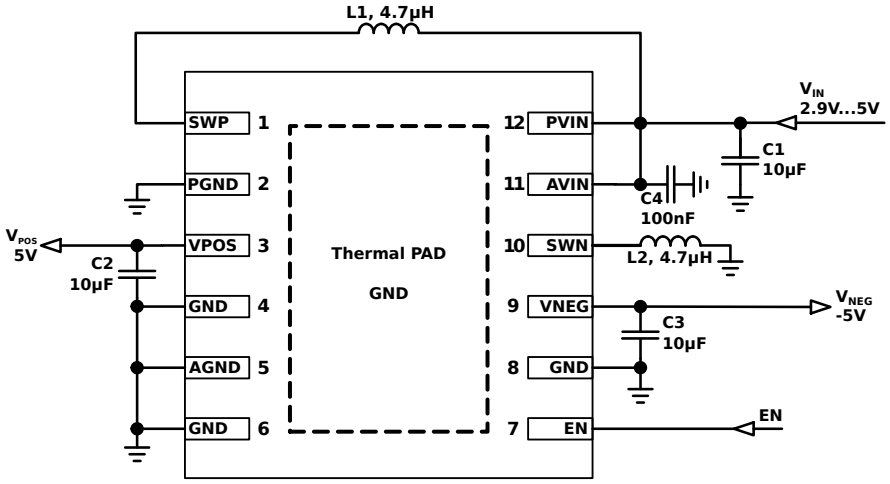


Figure 13. Typical Application Circuit

PCB LAYOUT

1. Place the input capacitor on PVIN and the output capacitor on VNEG as close as possible to device. Use short and wide traces to connect the input capacitor on PVIN and the output capacitor on VNEG.
2. Place the output capacitor on VPOS as close as possible to the device. Use short and wide traces to connect the output capacitor on VPOS.
3. Connect the ground of AVIN capacitor with AGND.
4. Connect input ground and output ground on the same board layer, not through via hole.
5. Connect AGND, PGND and GND with exposed thermal pad.

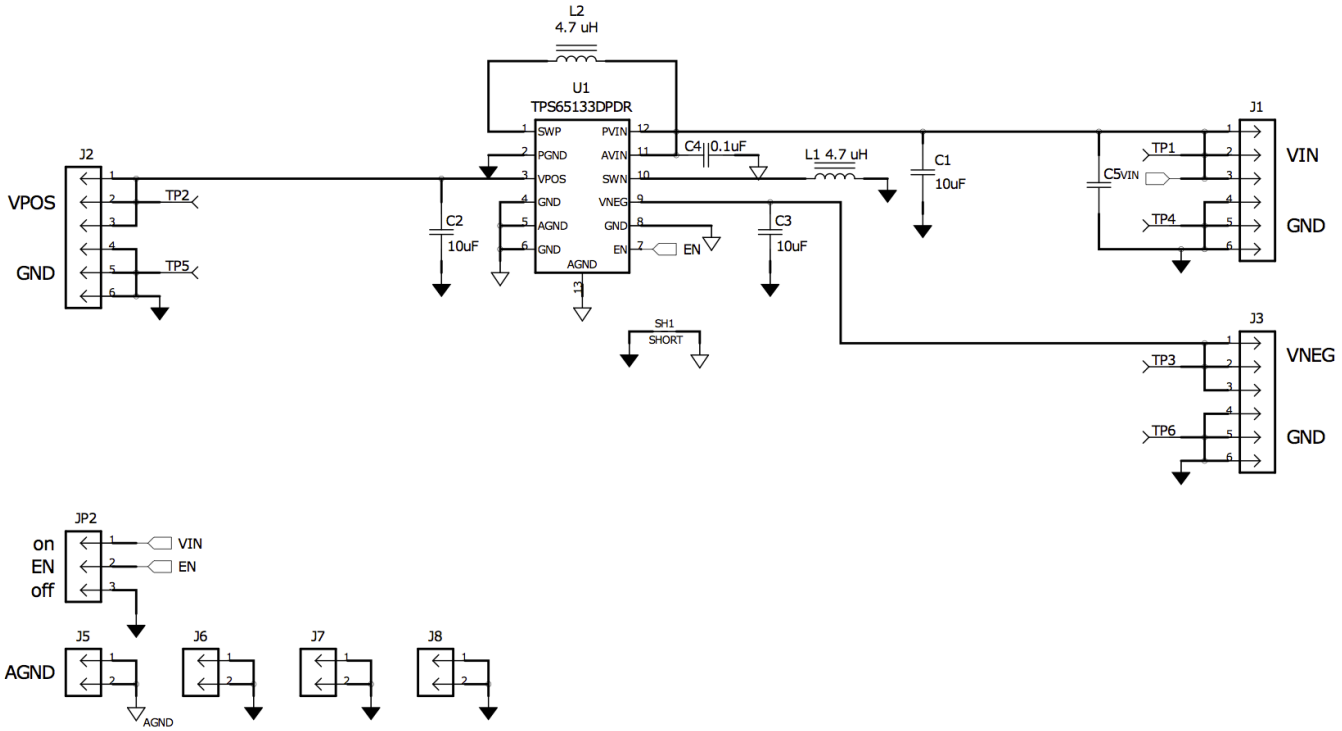


Figure 14. TPS65133 EVM Schematic

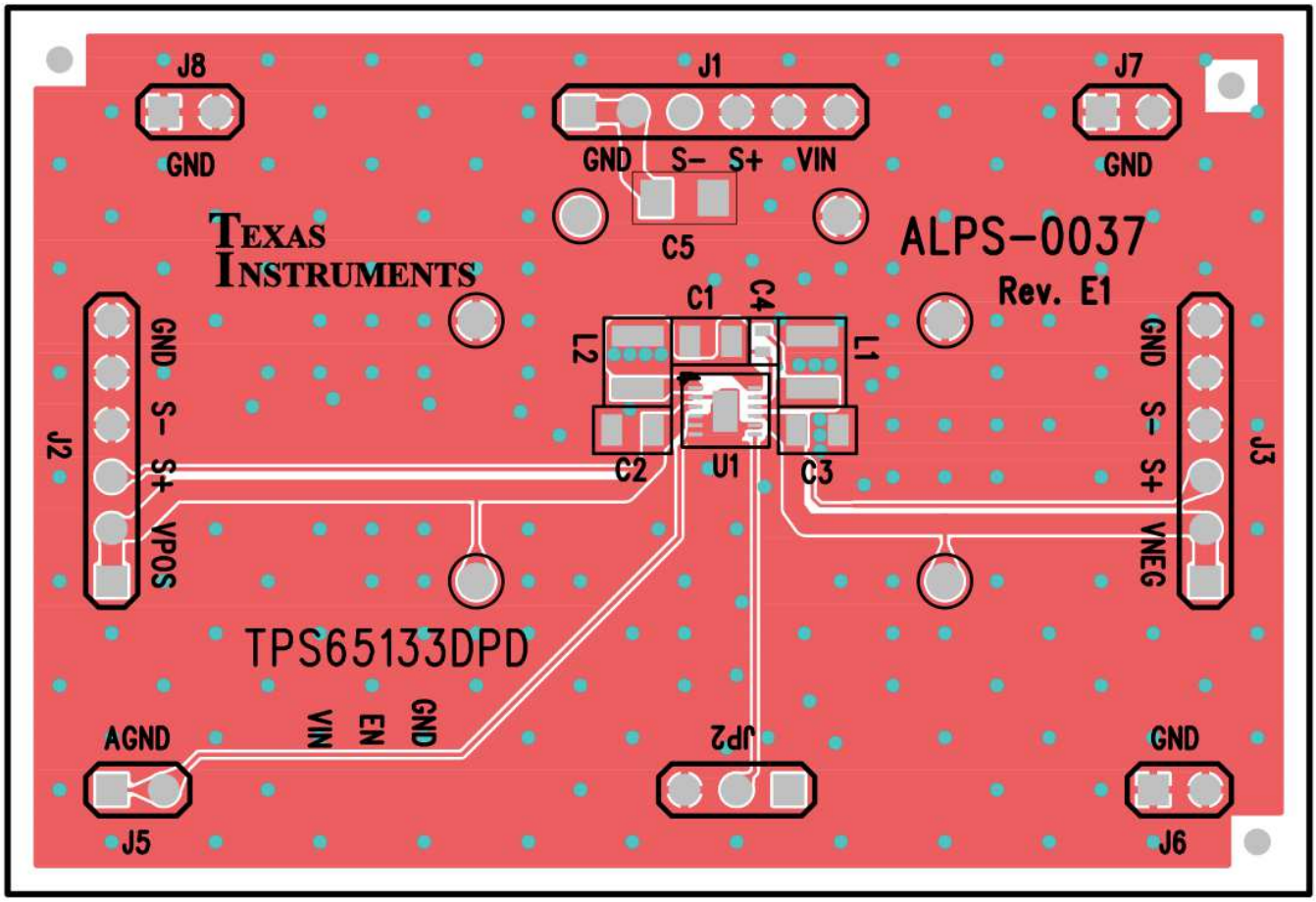


Figure 15. TPS65133 EVM Layout, Top Layer

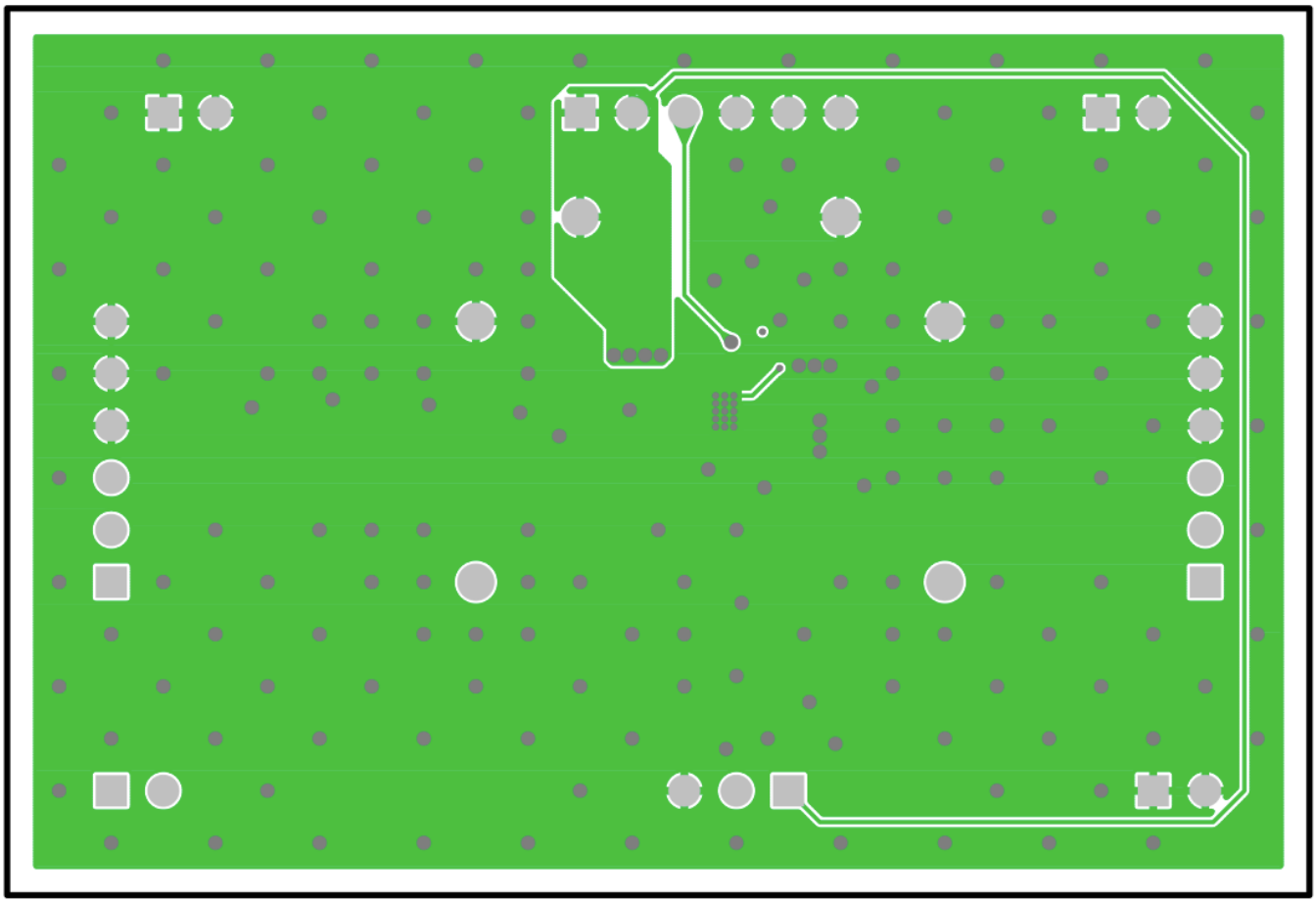


Figure 16. TPS65133 EVM Layout, Bottom Layer

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65133DPDR	ACTIVE	WSON	DPD	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SHY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

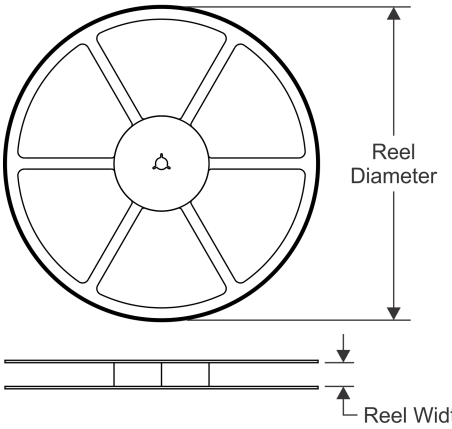
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

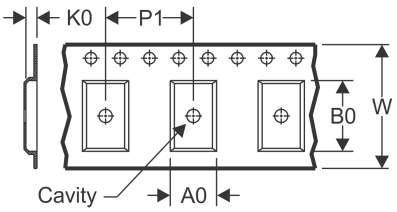
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

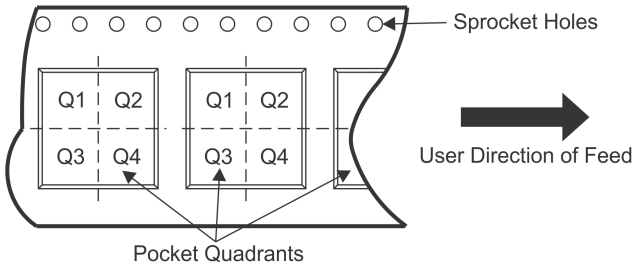


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

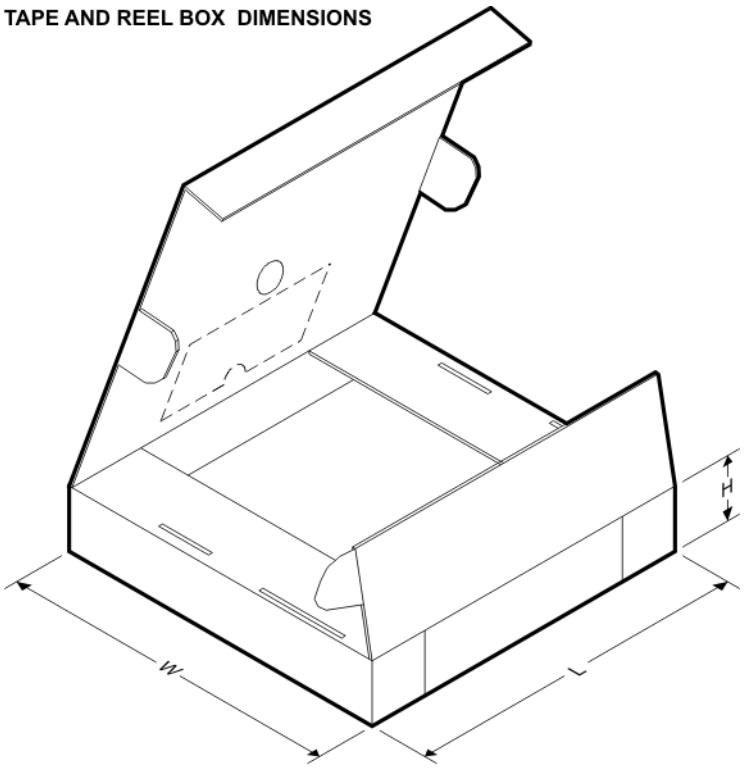
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65133DPDR	WSON	DPD	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

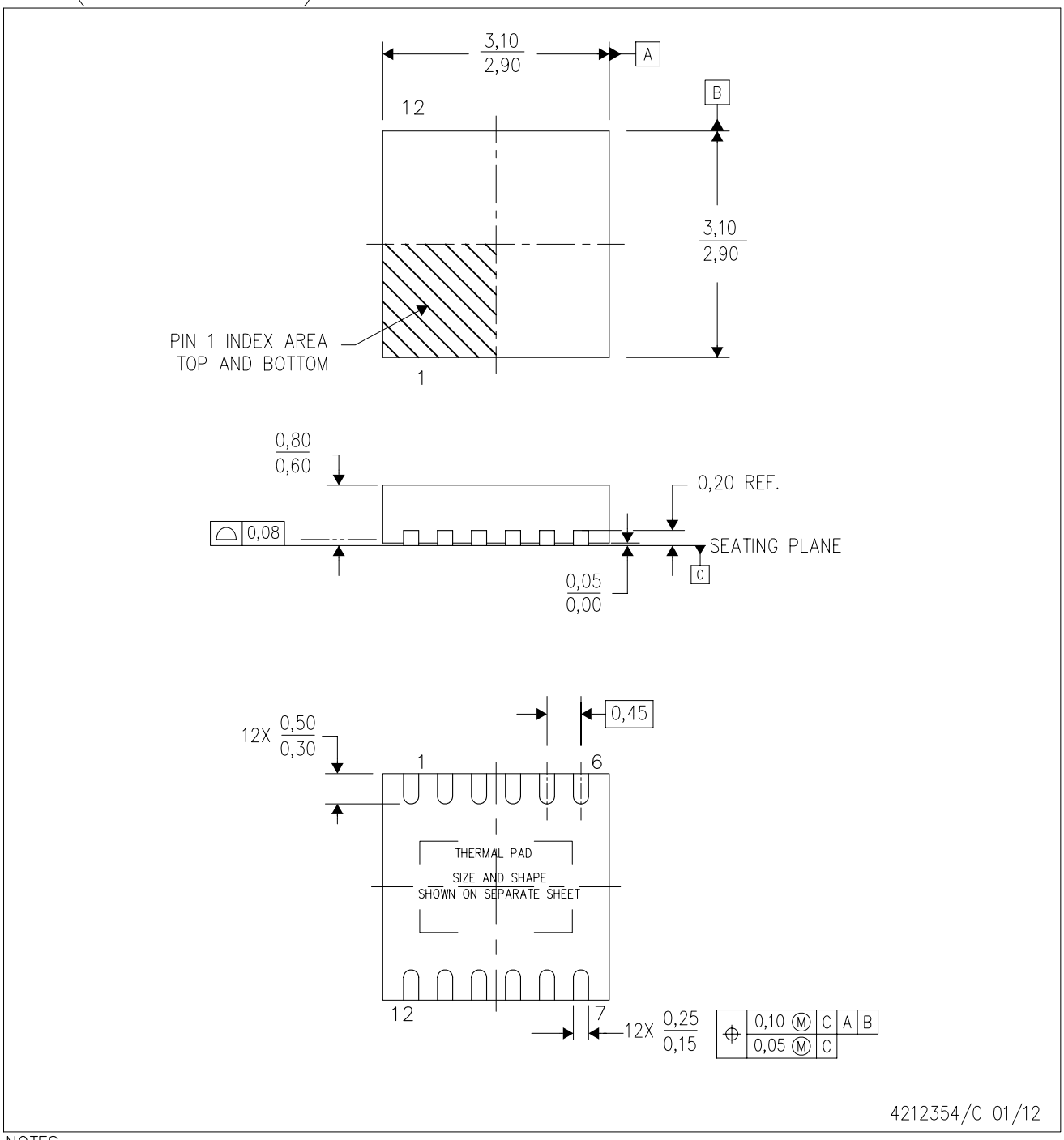
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65133DPDR	WSON	DPD	12	3000	367.0	367.0	35.0

DPD (S–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

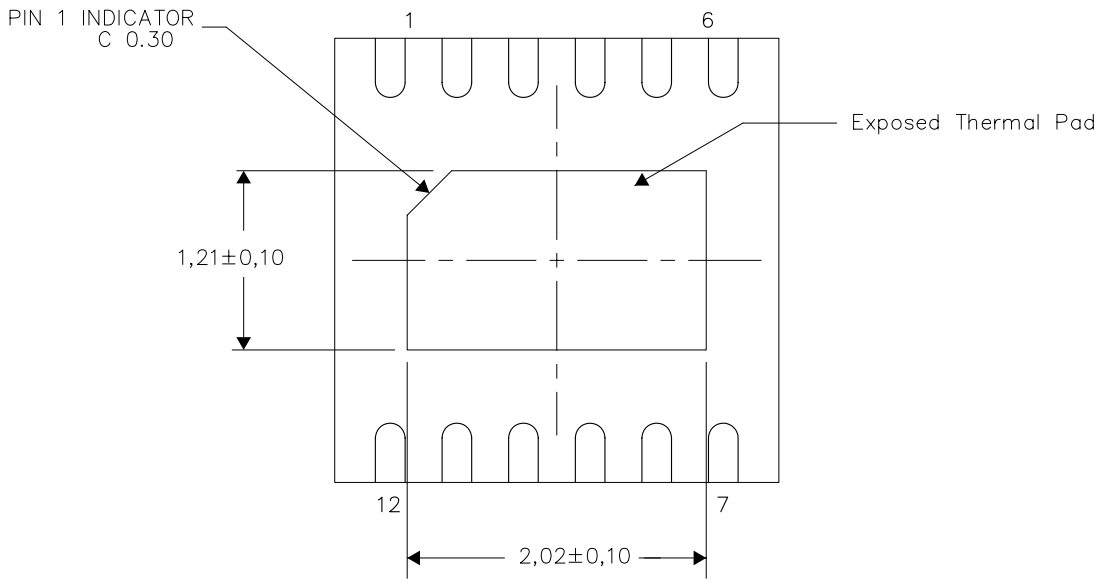
DPD (S–PUSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212468/A 02/12

NOTE: All linear dimensions are in millimeters

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