POWER MANAGEMENT IC FOR LI-ION POWERED SYSTEMS

FEATURES

- **1.2 A, 97% Efficient Step-Down Converter for System Voltage (VDCDC1)**
- **1 A, Up to 95% Efficient Step-Down Converter for Memory Voltage (VDCDC2)**
- **800 mA, 90% Efficient Step-Down Converter for Processor Core (VDCDC3)**
- **20 mA LDO/Switch for Real Time Clock (VRTC)**
- **2 × 50 mA LDO for SRAM and PLL**
- **Dynamic Voltage Management for Processor Core**
- **Externally Adjustable Reset Delay Time**
- **Battery Backup Functionality**
- **Separate Enable Pins for Inductive Converters**
- **I^2C™ Compatible Serial Interface**
- **85-µA Quiescent Current**
- **Low Ripple PFM Mode**
- **Thermal Shutdown Protection**
- **Push Button I/O**

APPLICATIONS

- **PDA**
- **Cellular/Smart Phone**
- **Internet Audio Player**
- **Digital Still Camera**
- **Digital Radio Player**
- **Split Supply DSP and µP Solutions: OMAP1610, OMAP1710, OMAP330**
- **Intel PXA270, etc.**

DESCRIPTION

The TPS65020 is an integrated Power Management IC for applications powered by one Li-Ion or Li-Polymer cell, and which require multiple power rails. The TPS65020 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O and memory rails in a processor based system. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. The TPS65020 also integrates two 50 mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the main battery. The two 50-mA LDO voltage regulators are intended for use with the SDRAM and PLL power supply in a Intel PXA270 based system. The serial interface is used for dynamic voltage scaling of the core voltage, masking interrupts, or for dis/enabling and setting the LDO output voltages. The interface is compatible with the Fast/Standard mode I^2C™ specification, allowing transfers at up to 400 kHz.

The TPS65020 incorporates a push button debounced input and latched output for implementation of a push-button turn-on feature, typically required in smartphones or wireless PDAs.

PowerPAD is a trademark of Texas Instruments.
I^2C is a trademark of Philips Electronics.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER(1)
–40°C to 85°C	40 pin QFN (RHA)	TPS65020RHA

(1) The RHA package is available in tape and reel. Add the R suffix (TPS65020RHAR) to order quantities of 2500 parts per reel. Add the T suffix (TPS65020RHAT) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_I	Input voltage range on all pins except AGND and PGND pins with respect to AGND	–0.3 to 7	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3	2000	mA
	Peak Current at all other pins	1000	mA
	Continuous total power dissipation	See Dissipation Rating Table	
T_A	Operating free-air temperature	–40 to 85	°C
T_J	Maximum junction temperature	125	°C
T_{stg}	Storage temperature	–65 to 150	°C
	Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RHA(1)(2)	2.85 W	28 mW/°C	1.57 W	1.4 W

(1) The thermal resistance junction to ambient of the RHA package is 32°C/W measured on a high K board.
(2) The thermal resistance junction to case (exposed pad) of the RHA package is 5°C/W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input voltage range step-down convertors (VINDCDC1, VINDCDC2, VINDCDC3)	2.5		6	V
V_O	Output voltage range for VDCDC1 step-down convertor(1)	0.6		VINDCDC1	V
	Output voltage range for VDCDC2 step-down convertor(1)	0.6		VINDCDC2	
	Output voltage range for VDCDC3 (core) step-down convertor(1)	0.6		VINDCDC3	
V_I	Input voltage range for LDOs (VINLDO1, VINLDO2)	1.5		6.5	V
V_O	Output voltage range for LDOs (VLDO1, VLDO2)	1		VINLDO1-2	V
$I_{O(DCDC1)}$	Output current at L1			1200	mA
	Inductor at L1(2)	2.2	3.3		µH
$C_{I(DCDC1)}$	Input Capacitor at $V_{I(DCDC1)}$(2)	10			µF
$C_{O(DCDC1)}$	Output Capacitor at VDCDC1 (2)	10	22		µF
$I_{O(DCDC2)}$	Output current at L2			1000	mA
	Inductor at L2 (2)	2.2	3.3		µH

(1) When using an external resistor divider at DEFDCDC3, DEFDCDC2, DEFDCDC1
(2) See applications section for more information.

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$C_{I(DCDC2)}$	Input Capacitor at $V_{I(DCDC2)}$ (2)	10			µF
$C_{O(DCDC2)}$	Output Capacitor at VDCDC2 (2)	10	22		µF
$I_{O(DCDC3)}$	Output current at L3			800	mA
	Inductor at L3 (2)	2.2	3.3		µH
$C_{I(DCDC3)}$	Input Capacitor at $V_{I(DCDC3)}$ (2)	10			µF
$C_{O(DCDC3)}$	Output Capacitor at VDCDC3 (2)	10	22		µF
$C_{I(VCC)}$	Input Capacitor at VCC (2)	1			µF
$C_{i(VINLDO)}$	Input Capacitor at VINLDO (2)	1			µF
$C_{O(VLDO1-2)}$	Output Capacitor at VLDO1, VLDO2 (2)	2.2			µF
$I_{O(VLDO1-2)}$	Output current at VLDO1, VLDO2			50	mA
$C_{O(VRTC)}$	Output Capacitor at VRTC (2)	4.7			µF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C
	Resistor from VINDCDC3, VINDCDC2, VINDCDC1 to VCC used for filtering (3)		1	10	Ω

(3) Up to 3 mA can flow into VCC when all 3 converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS : SCLK, SDAT (input), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN						
V_{IH}	High level input voltage	Rpullup = 4.7 kR, pulled to VRTC	1.3		VCC	V
V_{IL}	Low level input voltage	Rpullup = 4.7 kR, pulled to VRTC	0		0.4	V
I_H	Input bias current			0.01	0.1	µA
CONTROL SIGNALS : $\overline{\text{HOT\_RESET}}$						
V_{IH}	High level input voltage		1.3		VCC	V
V_{IL}	Low level input voltage		0		0.4	V
	Pull up resistor at /HOT_RESET, connected to VCC			1000		kΩ
t_{glitch}	Deglitch time at $\overline{\text{HOT\_RESET}}$		25	30	35	ms
CONTROL SIGNALS : $\overline{\text{LOWBAT}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (output)						
V_{OH}	High level output voltage				6	V
V_{OL}	Low level output voltage	I_{IL} = 5 mA	0		0.3	V
	Duration of low pulse at $\overline{\text{RESPWRON}}$	External capacitor 1 nF		100		ms
	Resetpwron threshold VRTC falling		–3%	2.4	3%	V
	Resetpwron threshold VRTC rising		–3%	2.52	3%	V

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3							
$I_{(qPFM)}$	Operating quiescent current, PFM	All 3 DCDC converters enabled, zero load and no switching, LDOs enabled	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		85	100	µA
		All 3 DCDC converters enabled, zero load and no switching, LDOs enabled	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		78	90	
		DCDC1 and DCDC2 converters enabled, zero load and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		57	70	
		DCDC1 converter enabled, zero load & no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		43	55	
I_I	Current into VCC; PWM	All 3 DCDC converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		2	3	mA
		DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		1.5	2.5	
		DCDC1 converter enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		0.85	2	
$I_{(q)}$	Quiescent current	All converters disabled, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		23	33	µA
		All converters disabled, LDOs off	VCC = 2.6 V, VBACKUP = 3 V; VVSYSIN = 0 V		3.5	5	µA
		All converters disabled, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; VVSYSIN = 0 V			43	µA

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY PINS: VCACKUP, VSYSIN, VRTC						
$I_{(q)}$	Operating quiescent current	VBACKUP = 3 V, VSYSIN = 0 V; VCC = 2.6 V, current into VBACKUP		20	33	µA
$I_{(SD)}$	Operating quiescent current	VBACKUP < V_VBACKUP, current into VBACKUP		2	3	µA
	VRTC LDO output voltage	VSYSIN = VBACKUP = 0 V, I_O = 0 mA		3		V
I_O	Output current for VRTC	VSYSIN < 2.57 V and VBACKUP < 2.57 V			20	mA
	VRTC short-circuit current limit	VRTC = GND; VSYSIN = VBACKUP = 0 V			100	mA
	Maximum output current at VRTC for $\overline{\text{RESPWRON}}$ = 1	VRTC > 2.6 V, V_{CC} = 3 V; VSYSIN = VBACKUP = 0 V	30			mA
V_O	Output voltage accuracy for VRTC	VSYSIN = VBACKUP = 0 V; Io = 0 mA			± 1%	
	Line regulation for VRTC	VCC = VRTC + 0.5 V to 6.5 V, I_O = 5 mA			±1%	
	Load regulation VRTC	I_O = 1 mA to 20 mA; VSYSIN = VBACKUP = 0 V			±2%	
	Regulation time for VRTC	Load change from 10% to 90%		10		µs
I_{lkg}	Input leakage current at VSYSIN	VSYSIN < V_VSYSIN			2	µA
	$r_{DS(on)}$ of VSYSIN switch				12.5	Ω
	$r_{DS(on)}$ of VBACKUP switch				12.5	Ω
	Input voltage range at VBACKUP (1)		2.73		3.75	V
	Input voltage range at VSYSIN (1)		2.73		3.75	V
	VSYSIN threshold	VSYSIN falling	–3%	2.55	3%	V
	VSYSIN threshold	VSYSIN rising	–3%	2.65	3%	V
	VBACKUP threshold	VBACKUP falling	–3%	2.55	3%	V
	VBACKUP threshold	VBACKUP falling	-3%	2.65	3%	V
SUPPLY PIN: VINLDO						
$I_{(q)}$	Operating quiescent current	Current per LDO into VINLDO		16	30	µA
$I_{(SD)}$	Shutdown current	Total current for both LDOs into VINLDO, VLDO = 0 V		0.1	1	µA

(1) Based on the requirements for the Intel PXA270 processor.

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC1			2.5		6.0	V
I_O	Maximum output current			1200			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC1		DCDC1_EN = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC1 = $V_{(GS)}$ = 3.6 V		125	261	mΩ
I_{lkg}	P-channel leakage current		VINDCDC1 = 6 V			2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC1 = $V_{(GS)}$ = 3.6 V		130	260	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
	Forward current limit (P- and N-channel)		2.5 V < $V_{I(MAIN)}$ < 6 V	1.55	1.75	1.95	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz
	Fixed output voltage FPWMDCDC1=0	3 V	VINDCDC1 = 3.3 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
		3.3 V	VINDCDC1 = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
	Fixed output voltage FPWMDCDC1=1	3 V	VINDCDC1 = 3.3 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
		3.3 V	VINDCDC1 = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC1 FPWMDCDC1=0		VINDCDC1 = VDCDC1 +0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=1		VINDCDC1 = VDCDC1 +0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
	Line Regulation		VINDCDC1 = VDCDC1 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 1200 mA		0.25		%/A
	Soft start ramp time		VDCDC1 ramping from 5% to 95% of target value		750		µs
	Internal resistance from L1 to GND				1		MΩ
	VDCDC1 discharge resistance				300		Ω

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC2 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC2			2.5		6	V
I_O	Maximum output current			1000			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC2		DCDC2_EN = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC2 = $V_{(GS)}$ = 3.6 V		140	300	mΩ
I_{lkg}	P-channel leakage current		VINDCDC2 = 6 V			2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC2 = $V_{(GS)}$ = 3.6 V		150	297	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel)		2.5 V < VINDCDC2 < 6 V	1.40	1.55	1.70	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz
	Fixed output voltage FPWMDCDC2=0	1.8 V	VINDCDC2 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.0 A	–2%		2%	
		2.5 V	VINDCDC2 = 2.8 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
	Fixed output voltage FPWMDCDC2=1	1.8 V	VINDCDC2 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
		2.5 V	VINDCDC2 = 2.8 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC2 FPWMDCDC2=0		VINDCDC2 = VDCDC2 +0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.0 A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC2; FPWMDCDC2=1		VINDCDC2 = VDCDC2 +0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.0 A	–1%		1%	
	Line Regulation		VINDCDC2 = VDCDC2 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 1 mA		0.25		%/A
	Soft start ramp time		VDCDC2 ramping from 5% to 95% of target value		750		µs
	Internal resistance from L2 to GND				1		MΩ
	VDCDC2 discharge resistance				300		Ω

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC3 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC3			2.5		6	V
I_O	Maximum output current			800			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC3		DCDC3_EN = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC3 = $V_{(GS)}$ = 3.6 V		310	698	mΩ
I_{lkg}	P-channel leakage current		VINDCDC3 = 6 V		0.1	2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC3 = $V_{(GS)}$ = 3.6 V		220	503	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
	Forward current limit (P- and N-channel)		2.5 V < VINDCDC3 < 6 V	1.05	1.2	1.35	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz
	Fixed output voltage FPWMDCDC3=0	All VDCDC3	VINDCDC3 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 600 mA	–2%		2%	
	Fixed output voltage FPWMDCDC3=1		VINDCDC3 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 600 mA	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC3 FPWMDCDC3=0		VINDCDC3 = VDCDC3 +0.4 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 600 mA	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC3; FPWMDCDC3=1		VINDCDC3 = VDCDC3 +0.4 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 600 mA	–1%		1%	
	Line Regulation		VINDCDC3 = VDCDC3 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0.0		%/V
	Load Regulation		I_O = 10 mA to 400 mA		0.25		%/A
	Soft start ramp time		VDCDC3 ramping from 5% to 95% of target value		750		µs
	Internal resistance from L3 to GND				1		MΩ
	VDCDC3 discharge resistance				300		Ω

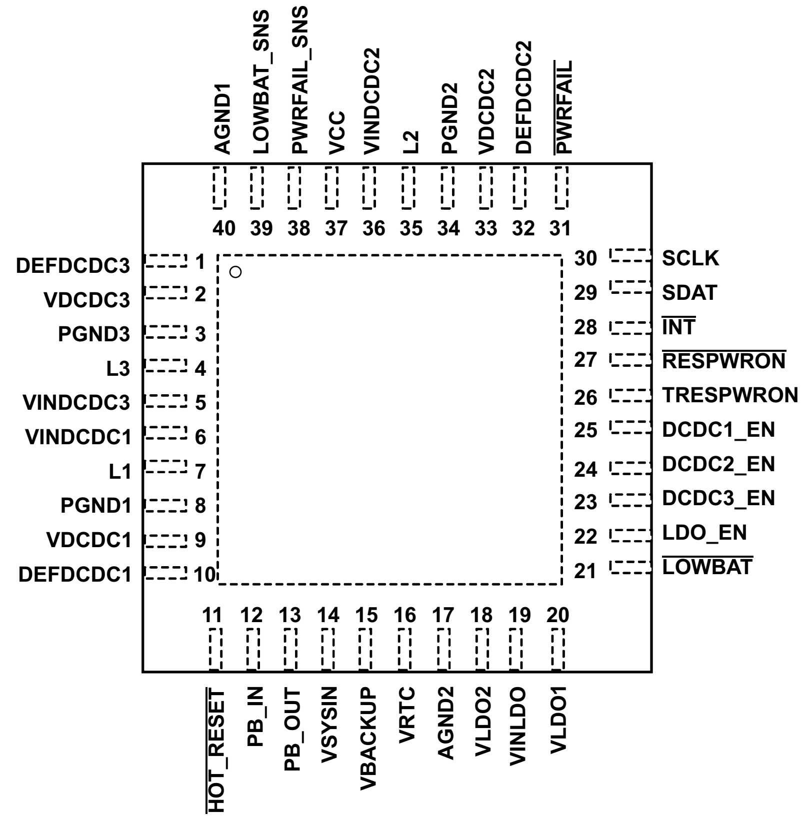
ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1 and VLDO2 LOW DROPOUT REGULATORS						
V_I	Input voltage range for LDO1, 2		1.5		6.5	V
V_O	LDO1 output voltage range		1		3.3	V
V_O	LDO2 output voltage range		1.0		3.3	V
I_O	Maximum output current for LDO1, LDO2		50			mA
$I_{(SC)}$	LDO1 and LDO2 short circuit current limit	VLDO1 = GND, VLDO2 = GND			400	mA
	Minimum voltage drop at LDO1, LDO2	I_O = 50 mA, VINLDO = 1.8 V			120	mV
	Minimum voltage drop at LDO1, LDO2	I_O = 50 mA, VINLDO = 1.5 V		65	150	mV
	Output voltage accuracy for LDO1, LDO2	I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2	VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2	I_O = 0 mA to 50 mA	–1%		1%	
	Regulation time for LDO1, LDO2	Load change from 10% to 90%		10		µs
ANALOGIC SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3						
V_{IH}	High level input voltage		1.3		VCC	V
V_{IL}	Low level input voltage		0		0.4	V
I_H	Input bias current			0.001	0.05	µA
LOGIC SIGNALS PB_IN; PB_OUT						
V_{OL}	Low level output voltage at PB_OUT	I_{OL} = 20 mA			0.5	V
V_{OH}	High level output voltage PB_OUT				6	V
V_{IL}	Low level input voltage PB_IN				0.4	V
V_{IH}	High level input voltage PB_IN		1.3		Vcc(1)	V
	II Input leakage current PB_IN				1	µA
THERMAL SHUTDOWN						
$T_{(SD)}$	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shudown hysteresis	Decreasing junction temperature		20		°C
INTERNAL UNDER VOLTAGE LOCK OUT						
UVLO	Internal UVLO	VCC falling	–2%	2.35	2%	V
$V_{(UVLO\_HYST)}$	Internal UVLO comparator hysteresis			120		mV
VOLTAGE DETECTOR COMPARATORS						
	Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS)	Falling threshold	–1%	1.0	1%	V
	Hysteresis		40	50	60	mV
	Propagation delay	25 mV overdrive			10	µs
POWER GOOD						
$V_{(PGOODF)}$		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, decreasing	–12%	–10%	–8%	
$V_{(PGOODR)}$		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, increasing	–7%	–5%	–3%	

(1) The input voltage can go as high as 6 V. If the input voltage exceeds VCC, an input current of ($V_{(PB\_IN)}$ - 0.7 V - VCC) / 10 kR flows.

PIN ASSIGNMENT
(TOP VIEW)



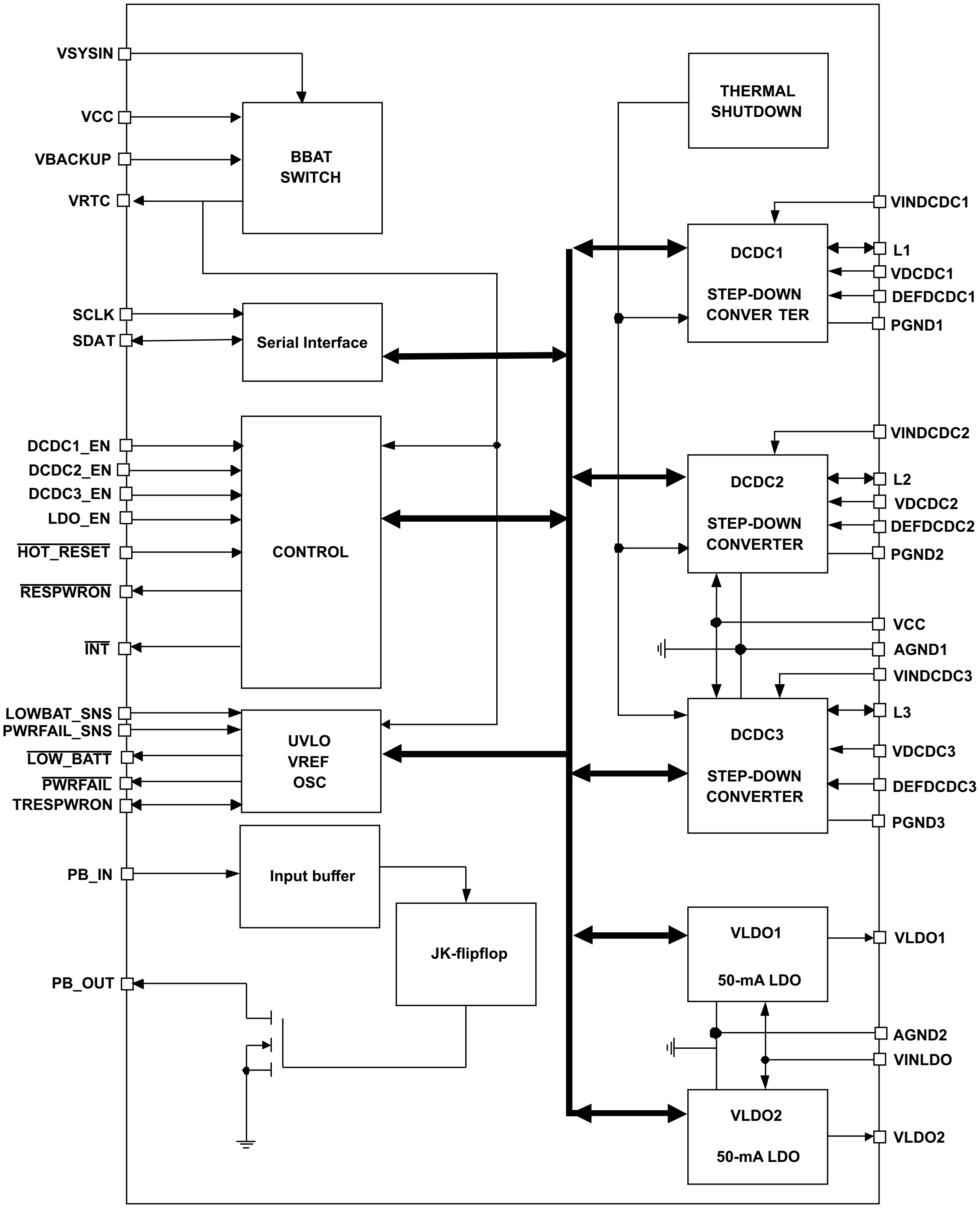
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
SWITCHING REGULATOR SECTION			
AGND1	40		Analog ground connection. All analog ground pins are connected internally on the chip.
AGND2	17		Analog ground connection. All analog ground pins are connected internally on the chip.
PowerPAD™	–		Connect the power pad to analog ground.
VINDCDC1	6	I	Input voltage for VDCDC1 step-down converter. This must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC.
L1	7		Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
VDCDC1	9	I	VDCDC1 feedback voltage sense input, connect directly to VDCDC1
PGND1	8		Power ground for VDCDC1 converter
VINDCDC2	36	I	Input voltage for VDCDC2 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC3, and VCC.
L2	35		Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
VDCDC2	33	I	VDCDC2 feedback voltage sense input, connect directly to VDCDC2
PGND2	34		Power ground for VDCDC2 converter
VINDCDC3	5	I	Input voltage for VDCDC3 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC.
L3	4		Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
VDCDC3	2	I	VDCDC3 feedback voltage sense input, connect directly to VDCDC3
PGND3	3		Power ground for VDCDC3 converter
VCC	37	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 dc-dc converters. This must be connected to the same voltage supply as VINDCDC3, VINDCDC1, and VINDCDC2. Also supplies serial interface block

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
DEFDCDC1	10	I	Input signal indicating default VDCDC1 voltage, 0 = 3 V, 1 = 3.3 V This pin can also be connected to a resistor divider between VDCDC1 and GND. If the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V
DEFDCDC2	32	I	Input signal indicating default VDCDC2 voltage, 0 = 1.8 V, 1 = 2.5 V This pin can also be connected to a resistor divider between VDCDC2 and GND. If the output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V
DEFDCDC3	1	I	Input signal indicating default VDCDC3 voltage, 0 = 1.3 V, 1 = 1.55 V This pin can also be connected to a resistor divider between VDCDC3 and GND. If the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V
DCDC1_EN	25	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC2_EN	24	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC3_EN	23	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
LDO REGULATOR SECTION			
VINLDO	19	I	I Input voltage for LDO1 and LDO2
VLDO1	20	O	Output voltage of LDO1
VLDO2	18	O	Output voltage of LDO2
LDO_EN	22	I	Enable input for LDO1 and LDO2. Logic high enables the LDOs, logic low disables the LDOs
VBACKUP	15	I	Connect the backup battery to this input pin.
VRTC	16	O	Output voltage of the LDO/switch for the real time clock
VSYSIN	14	I	Input of system voltage for VRTC switch
CONTROL AND I^{2}C SECTION			
$\overline{\text{HOT\_RESET}}$	11	I	Push button input used to reboot or wake-up processor via $\overline{\text{RESPWRON}}$ output pin
TRESPWRON	26	I	Connect the timing capacitor to this pin to set the reset delay time: 1 nF → 100 ms
$\overline{\text{RESPWRON}}$	27	O	Open drain System reset output
$\overline{\text{PWRFAIL}}$	31	O	Open drain output. Active low when $\overline{\text{PWRFAIL}}$ comparator indicates low VBAT condition.
$\overline{\text{LOW\_BAT}}$	21	O	Open drain output of LOW_BAT comparator
$\overline{\text{INT}}$	28	O	Open drain output
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
PWRFAIL_SNS	38	I	Input for the comparator driving the $\overline{\text{PWRFAIL}}$ output
LOWBAT_SNS	39	I	Input for the comparator driving the $\overline{\text{LOW\_BAT}}$ output
PB_IN	12	I/O	Push button input debounced and output fed to latch at PB_OUT
PB_OUT	13	I/O	Open drain output of latch driven by PB_IN. Low after power up.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Graphs were taken using the EVM with the following inductor/output capacitor combinations:

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
VDCDC1	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC2	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC3	VLF4012AT-2R2M1R5	C2012X5R0J106M	2 × 10 μF

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current	1, 2, 3, 4, 5, 6, 7
	Line transient response		8, 9, 10
	Load transient response		11, 12, 13
	VDCDC2 PFM operation		14
	VDCDC2 low ripple PFM operation		15
	VDCDC2 PWM operation		16
	Startup VDCDC1, VDCDC2 and VDCDC3		17
	Startup LDO1 and LDO2		18
	Line transient response		19, 20, 21
	Load transient response		22, 23, 24

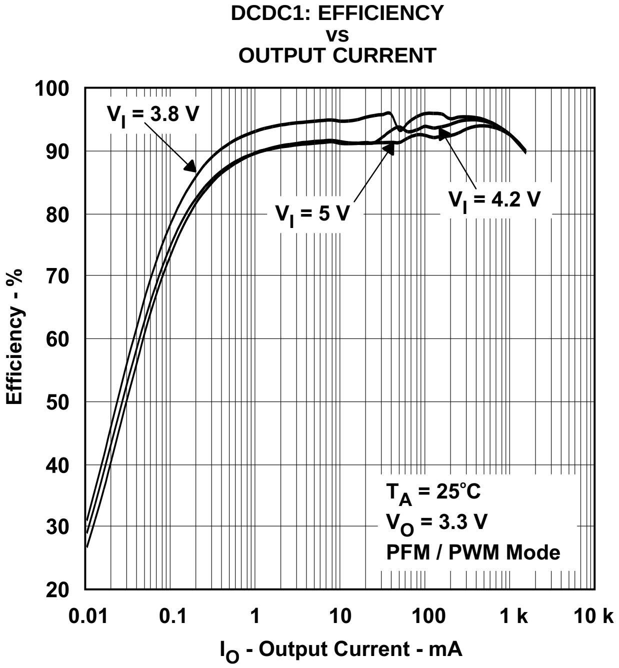


Figure 1.

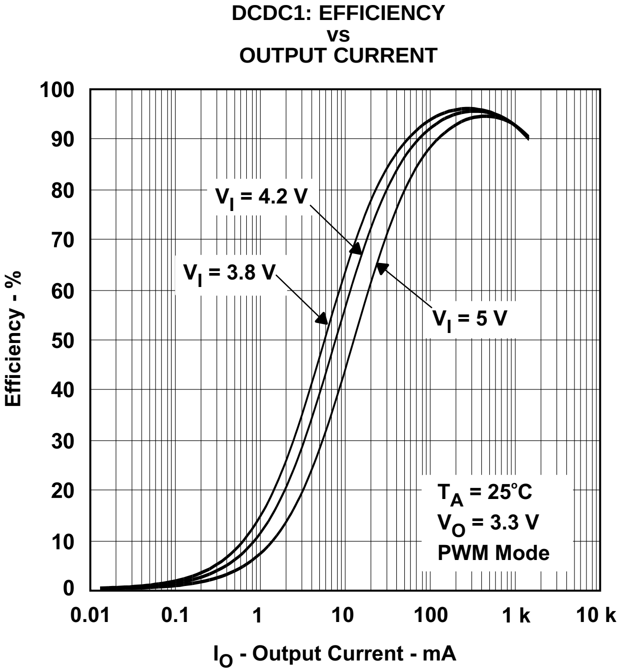


Figure 2.

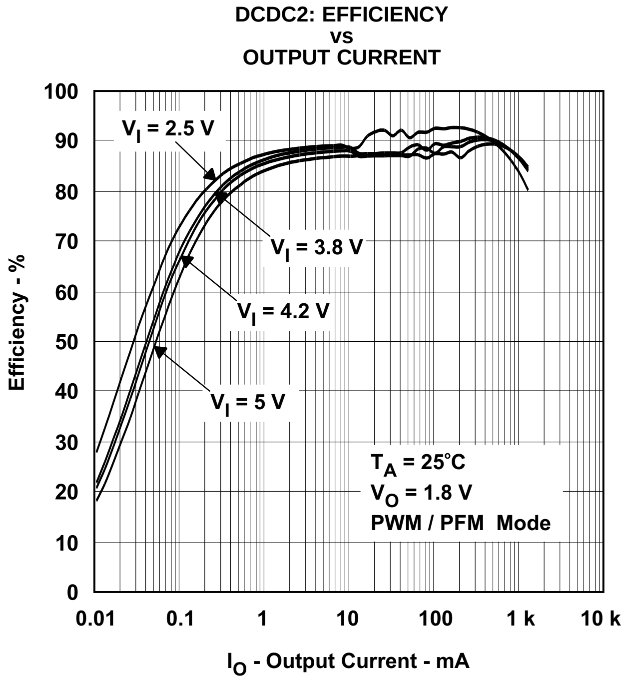

DCDC2: EFFICIENCY vs OUTPUT CURRENT

Figure 3.

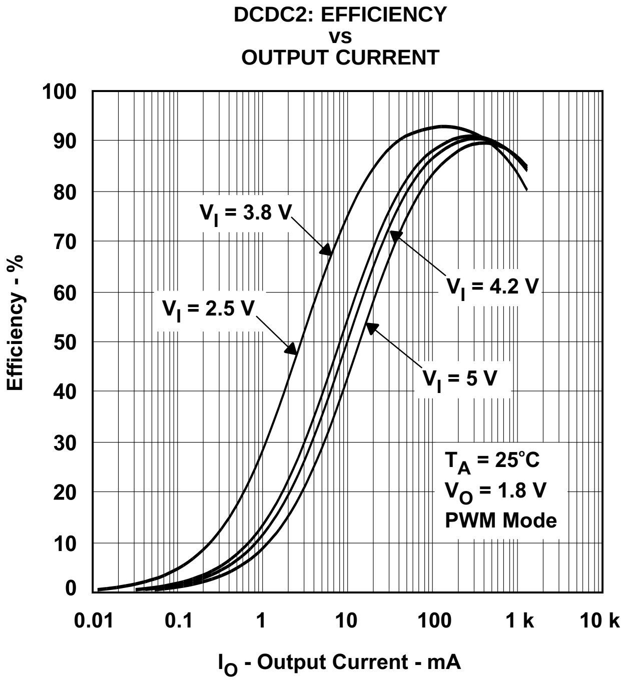

DCDC2: EFFICIENCY vs OUTPUT CURRENT

Figure 4.

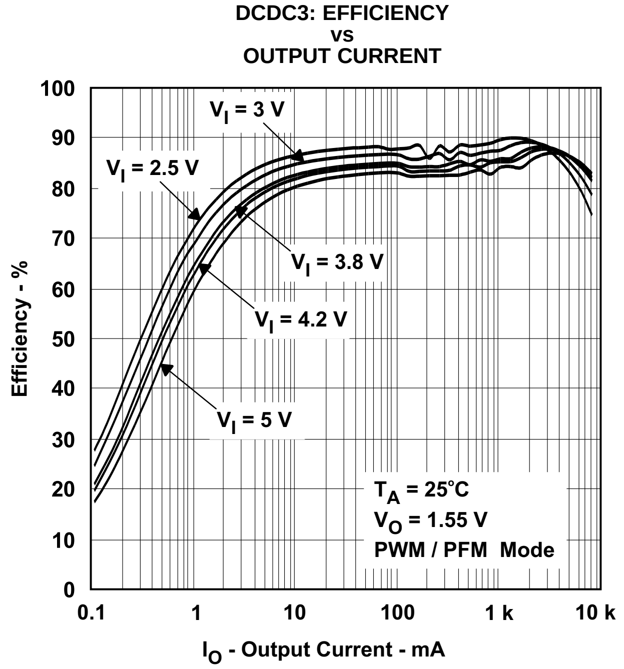

DCDC3: EFFICIENCY vs OUTPUT CURRENT

Figure 5.

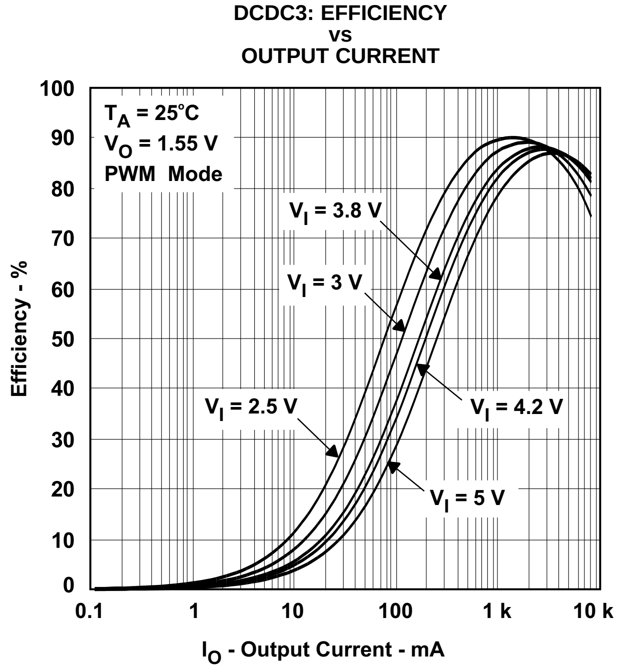

DCDC3: EFFICIENCY vs OUTPUT CURRENT

Figure 6.

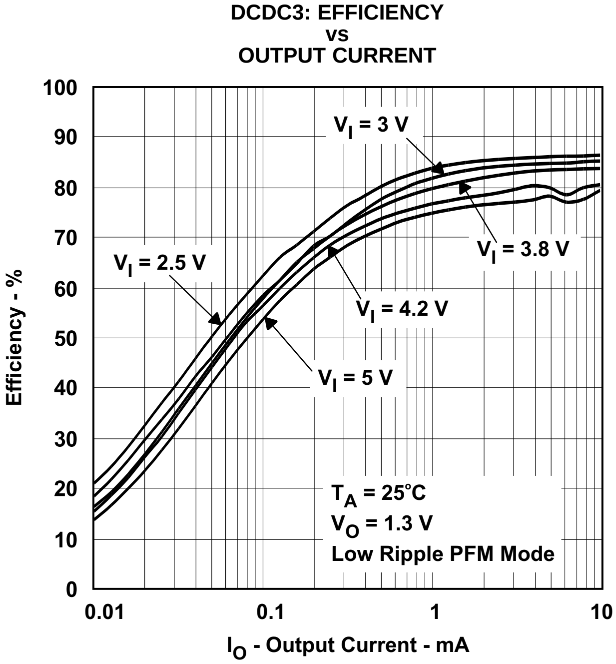


Figure 7.

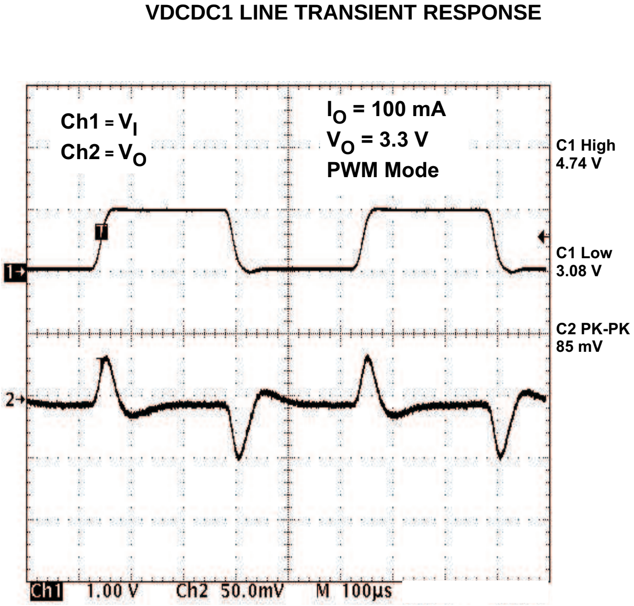


Figure 8.

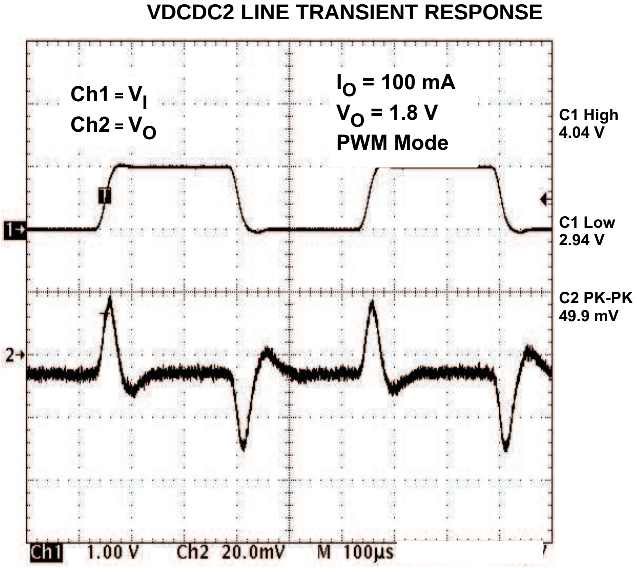


Figure 9.

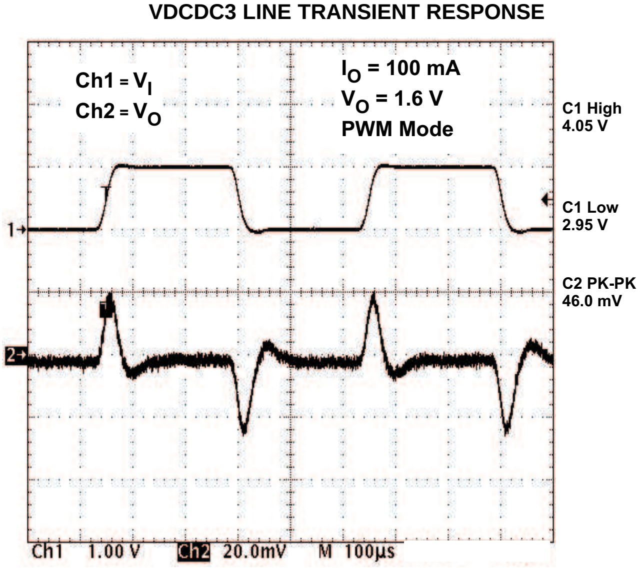


Figure 10.

VDCDC1 LOAD TRANSIENT RESPONSE

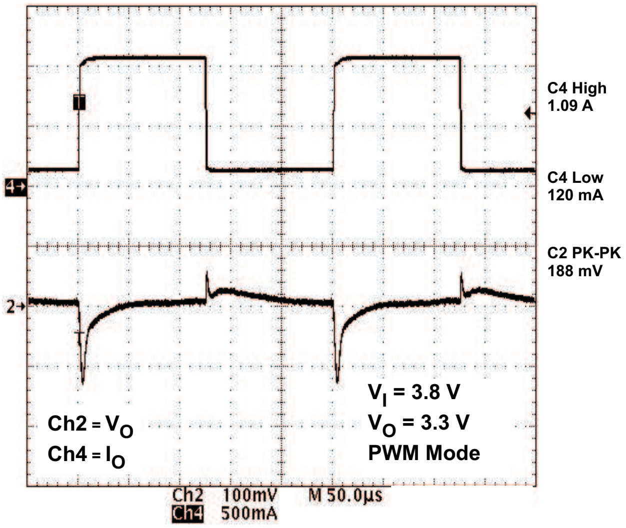


Figure 11.

VDCDC2 LOAD TRANSIENT RESPONSE

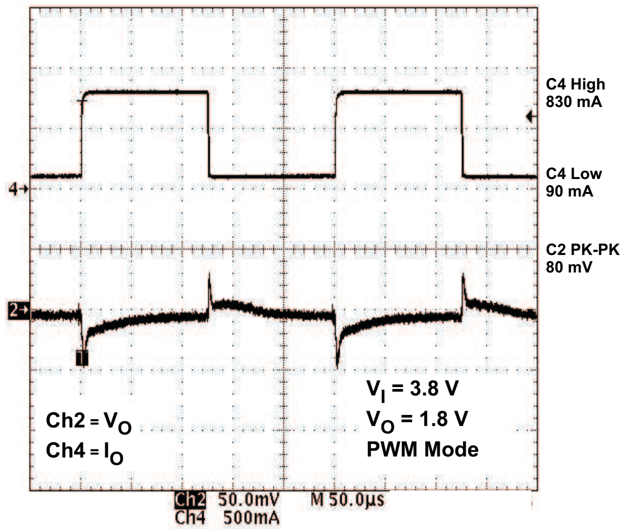


Figure 12.

VDCDC3 LOAD TRANSIENT RESPONSE

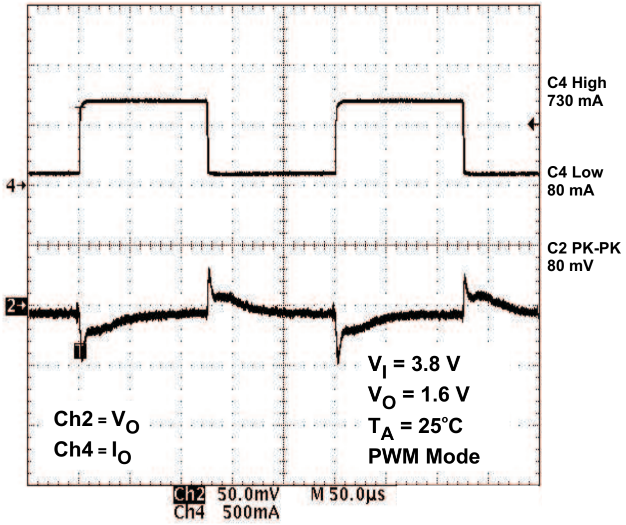


Figure 13.

VDCDC2 OUTPUT VOLTAGE RIPPLE

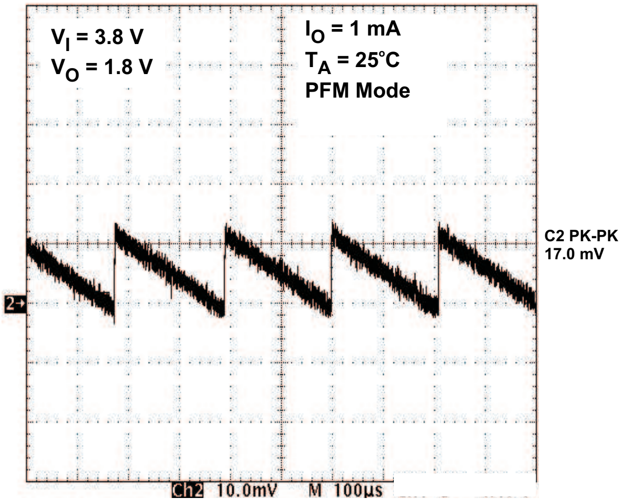


Figure 14.

VDCDC2 OUTPUT VOLTAGE RIPPLE

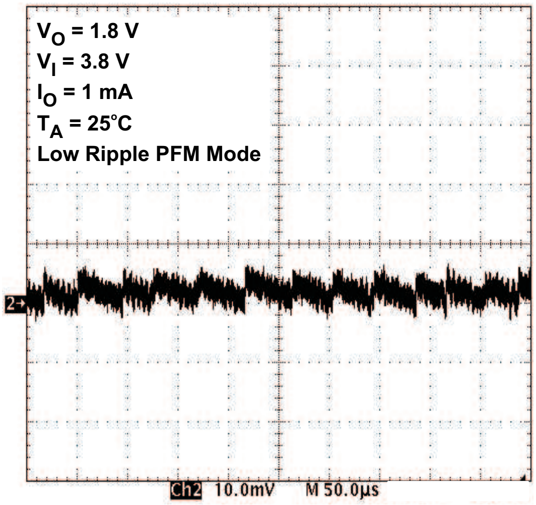


Figure 15.

VDCDC2 OUTPUT VOLTAGE RIPPLE

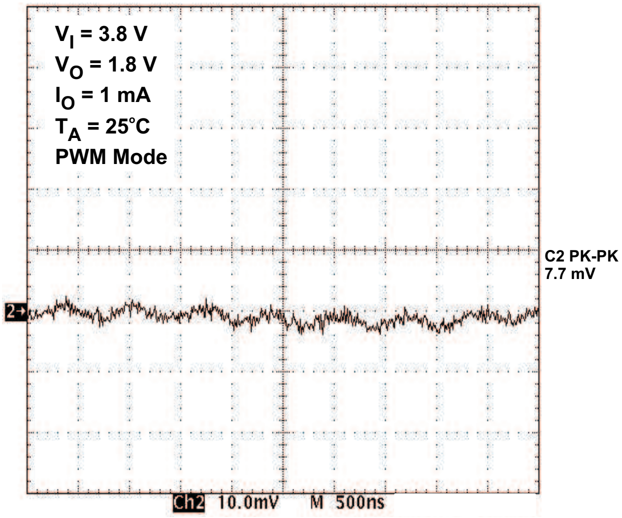


Figure 16.

STARTUP VDCDC1, VDCDC2, AND VDCDC3

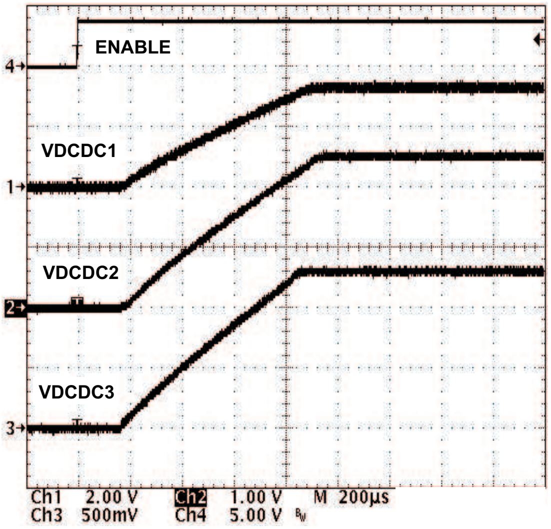


Figure 17.

STARTUP LDO1 AND LDO2

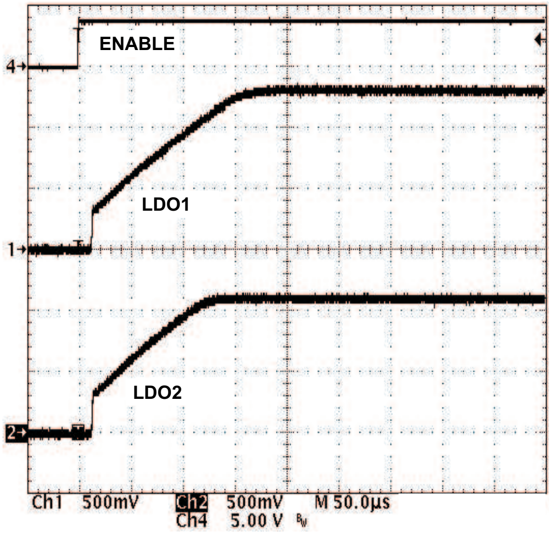


Figure 18.

LDO1 LINE TRANSIENT RESPONSE

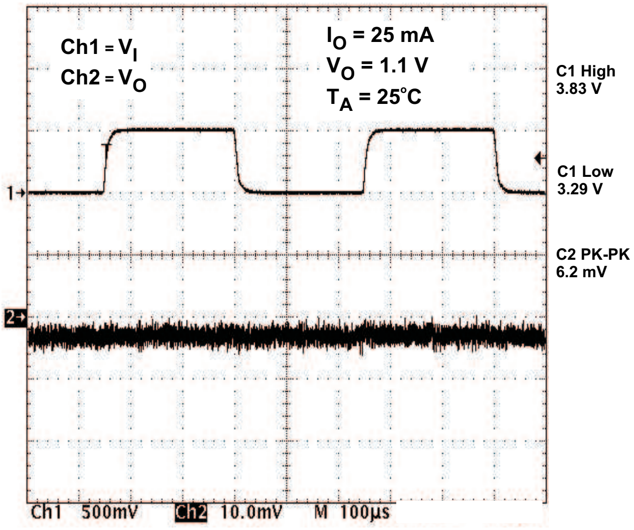


Figure 19.

LDO2 LINE TRANSIENT RESPONSE

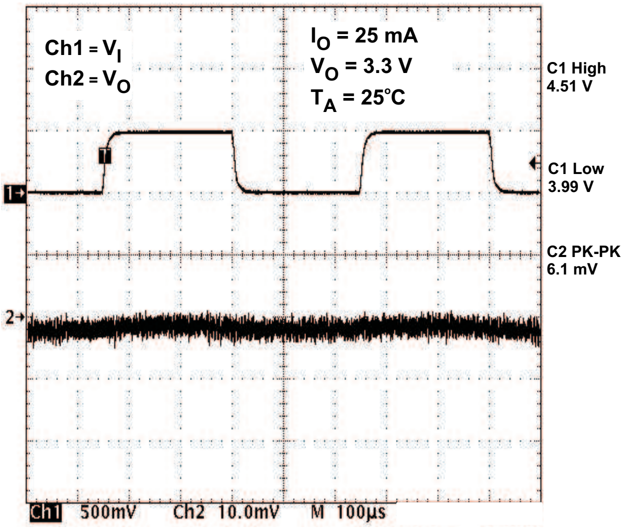


Figure 20.

VRTC LINE TRANSIENT RESPONSE

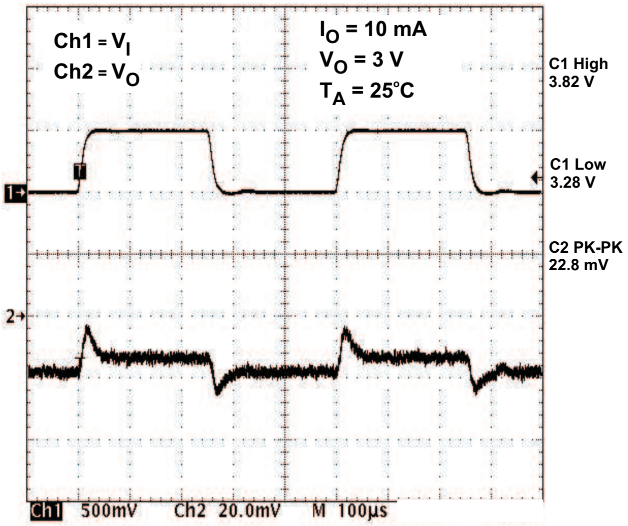


Figure 21.

LDO1 LOAD TRANSIENT RESPONSE

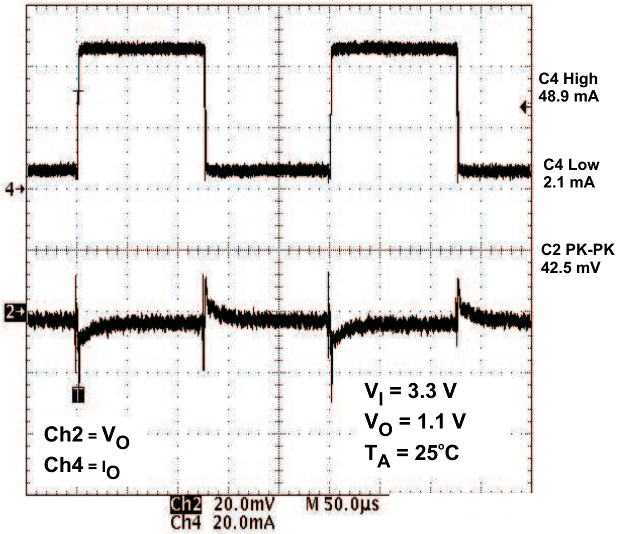


Figure 22.

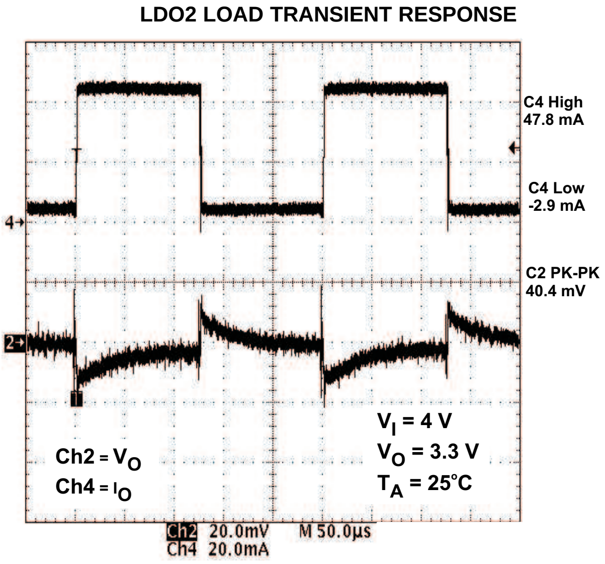

LDO2 LOAD TRANSIENT RESPONSE

Figure 23.

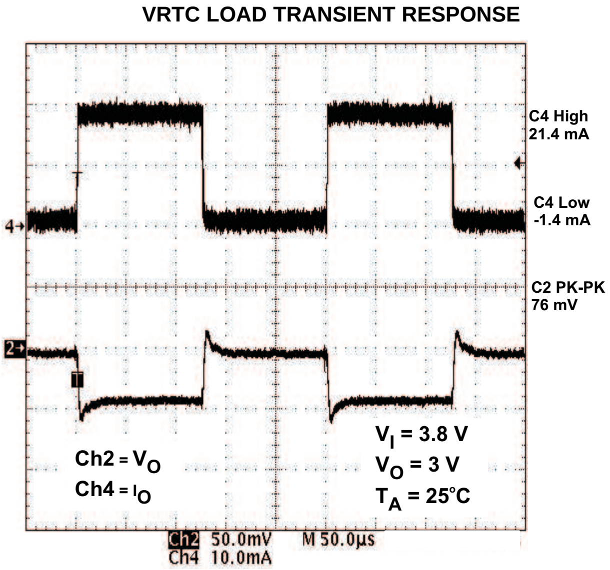

VRTC LOAD TRANSIENT RESPONSE

Figure 24.

DETAILED DESCRIPTION

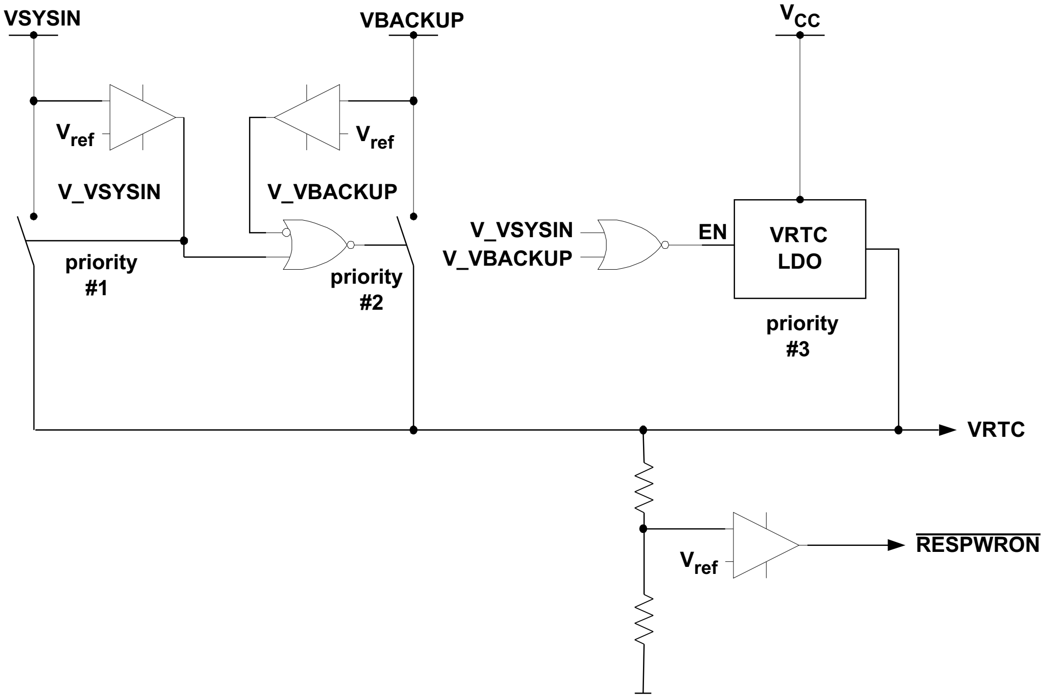
VRTC OUTPUT AND OPERATION WITH OR WITHOUT BACKUP BATTERY

The VRTC pin is an always-on output, intended to supply up to 20 mA to a permanently required rail. This is the VCC_BATT rail of the Intel PXA270 processor for example.

In applications using a backup battery, the backup voltage can be either directly connected to the TPS65020 VBACKUP pin if a Li-Ion cell is used, or via a boost converter (e.g. TPS61070) if a single NiMH battery is used. The voltage applied to the VBACKUP pin is fed through a PMOS switch to the VRTC pin. The TPS65020 asserts the $\overline{\text{RESPWRON}}$ signal if VRTC drops below 2.4 V. This, together with 250 mV at 20 mA drop out for the PMOS switch means that the voltage applied at VBACKUP must be greater than 2.65 V for normal system operation.

When the voltage at the VSYSIN pin exceeds 2.65 V, the path from VBACKUP to VRTC is cut, and VRTC is supplied by a similar PMOS switch from the voltage source connected to the VSYSIN input. Typically this is the VDCDC1 converter but can be any voltage source within the appropriate range.

In systems where no backup battery is used, the VBACKUP pin is connected to GND. In this case, a low power LDO is enabled, supplied from VCC and capable of delivering 20 mA to the 3 V output. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V. VRTC is then supplied from the external source connected to this pin as previously described



A. V_VSYSIN, V_VBACKUP thresholds: falling = 2.55 V, rising = 2.65 V ±3%

B. $\overline{\text{RESPWRON}}$ thresholds: falling = 2.4 V, rising = 2.52 V ±3%

Figure 25.

STEP-DOWN CONVERTERS, VDCDC1, VDCDC2, and VDCDC3

The TPS65020 incorporates three synchronous step-down converters operating typically at 1.5 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter the power save mode (PSM), and operate with pulse frequency modulation (PFM). The VDCDC1 converter is capable of delivering 1.2 A output current, the VDCDC2 converter is capable of delivering 1 A and the VDCDC3 converter is capable of delivering up to 800 mA.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The

DETAILED DESCRIPTION (continued)

pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 3 V or 3.3 V depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 3 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. See the application information section for more details.

The VDCDC2 converter defaults to 1.8 V or 2.5 V depending on the DEFDCDC2 configuration pin. If DEFDCDC2 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 2.5 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC2 V.

The VDCDC3 converter defaults to 1.3 V or 1.55 V depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground the default is 1.3 V. If it is tied to VCC, the default is 1.55 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC3 V. The core voltage can be reprogrammed via the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The step-down converter outputs (when enabled) are monitored by power good (PG) comparators, the outputs of which are available via the serial interface. The outputs of the dc-dc converters can be optionally discharged via on-chip 300 Ω resistors when the dc-dc converters are disabled. This feature can be enabled using the I^2C interface.

During PWM operation, the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on. The inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The three dc-dc converters operate synchronized to each other with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7 V to 3.3 V, the VDCDC2 converter from 3.7 V to 2.5 V, and the VDCDC3 converter from 3.7 V to 1.5 V. The phase of the three converters can be changed using the CON_CTRL register.

POWER SAVE MODE OPERATION

As the load current decreases, the converters enter the power save mode operation. During PSM, the converters operate in a burst mode (PFM mode) with a switching frequency between half of the switching frequency and switching frequency for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load, the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as follows:

DETAILED DESCRIPTION (continued)

$$I_{PFMDCDC1\ enter} = \frac{VINDCDC1}{24}$$

$$I_{PFMDCDC2\ enter} = \frac{VINDCDC2}{26}$$

$$I_{PFMDCDC3\ enter} = \frac{VINDCDC3}{39} \qquad (1)$$

During the PSM the output voltage is monitored with a comparator, and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_O, the P-channel switch turns on and the converter effectively delivers a constant current defined as follows.

$$I_{PFMDCDC1\ leave} = \frac{VINDCDC1}{18}$$

$$I_{PFMDCDC2\ leave} = \frac{VINDCDC2}{20}$$

$$I_{PFMDCDC3\ leave} = \frac{VINDCDC3}{29} \qquad (2)$$

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold again. If the load current is greater than the delivered current, then the output voltage falls until it crosses the COMP LOW threshold, set to 2% below nominal V_O, or the skip burst exceeds 16×1/switching frequency. Power Save Mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current to typically 14 µA per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I^2C interface to force the individual converters to stay in fixed frequency PWM mode.

LOW RIPPLE MODE

Setting Bit 3 in register CON-CTRL to 1 enables the low ripple mode for all of the dc-dc converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

SOFT START

Each of the three converters has an internal soft start circuit that limits the inrush current during start-up. The soft start is realized by using a very low current to initially charge the internal compensation capacitor. The soft start time is typically 750 µs if the output voltage ramps from 5% to 95% of the final target value. If the output is already precharged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170 µs between the converter being enabled and switching activity actually starting. This is to allow the converter to bias itself properly, to recognize if the output is precharged, and if so to prevent discharging of the output while the internal soft start ramp catches up with the output voltage.

DETAILED DESCRIPTION (continued)

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS65020 converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain dc regulation depends on the load current and output voltage. It is calculated as:

$$Vin_{min} = Vout_{min} + Iout_{max} \times \left(r_{DS(on)}max + R_L\right) \quad (3)$$

with:

$Iout_{max}$ = maximum load current (Note: ripple current in the inductor is zero under these conditions)
$r_{DS(on)}max$ = maximum P-channel switch $r_{DS(on)}$
R_L = DC resistance of the inductor
$Vout_{min}$ = nominal output voltage minus 2% tolerance limit

ACTIVE DISCHARGE WHEN DISABLED

When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, EN_x or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled via the CON_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a 300 Ω (typical) load which is active as long as the converters are disabled.

POWER GOOD MONITORING

All three step-down converters and both the LDO1 and LDO2 linear regulators have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register via the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.

LOW DROPOUT VOLTAGE REGULATORS

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 150 mV at rated output current. Each LDO supports a current limit feature. Both LDOs are enabled by the EN_LDO pin, both LDOs can be disabled or programmed via the serial interface using the REG_CTRL and LDO_CTRL registers. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65020 step-down and LDO voltage regulators automatically power down when the VBAT voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit for the five regulators on the TPS65020 prevents the device from malfunctioning at low-input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the VCC pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the dc-dc converters are running, there is an input current at the VCC pin, which is up to 3 mA when all three converters are running in PWM mode. This current needs to be taken into consideration if an external RC filter is used at the VCC pin to remove switching noise from the TPS65020 internal analog circuitry supply.

POWER-UP SEQUENCING

The TPS65020 power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter, and a common enable signal for the LDOs. The relevant control pins are described in Table 2.

DETAILED DESCRIPTION (continued)

Table 2. Control Pins and Status Outputs for DC-DC Converters

PIN NAME	INPUT OUTPUT	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.3 V, DEFDCDC3 = VCC defaults VDCDC3 to 1.55 V.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 2.5 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 3 V, DEFDCDC1 = VCC defaults VDCDC1 to 3.3 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
HOT_RESET	I	The HOT_RESET pin generates a reset (RESPWRON) for the processor.HOT_RESET does not alter any TPS65020 settings except the output voltage of VDCDC3. Activating HOT_RESET sets the voltage of VDCDC3 to its default value defined with the DEFDCDC3 pin. A 1 MΩ pull-up resistor to VCC is integrated in TPS65020. HOT_RESET is internally de-bounced by the TPS65020.
RESPWRON	O	RESPWRON is held low when power is initially applied to the TPS65020. The VRTC voltage is monitored: RESWPRON is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. RESPWRON can also be forced low by activation of the HOT_RESET pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the RESPWRON pin. 1 nF typically gives 100 ms.

SYSTEM RESET + CONTROL SIGNALS

The RESPWRON signal can be used as a global reset for the application. It is an open drain output. The RESPWRON signal is generated according to the power good comparator of VRTC, and remains low for $t_{nrespwron}$ seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis). $t_{nrespwron}$ is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms. RESPWRON is also triggered by the HOT_RESET input. This input is internally debounced, with a filter time of typically 30 ms.

The PWRFAIL and LOW_BAT signals are generated by two voltage detectors using the PWRFAIL_SNS and LOWBAT_SNS input signals. Each input signal is compared to a 1 V threshold (falling edge) with 5% (50 mV) hysteresis.

The VDCDC3 converter is reset to its default output voltage defined by the DEFDCDC3 input, when HOT_RESET is asserted. Other I^2C registers are not affected. Generally, the VDCDC3 converter is set to its default voltage with one of these conditions: HOT_RESET active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, RESPWRON active, both VDCDC3-converter AND VDCDC1-converter disabled. In addition, the voltage of VDCDC3 changes to 1xxx0, if the VDCDC1 converter is disabled. Where xxx is the state before VDCDC1 was disabled.

PB_IN and PB_OUT

In the TPS65020 the PB_IN pin is defined as an input. It is active high and debounces the input signal. For example from a push button, before passing it to a latch associated with PB_OUT (active low). This feature allows the implementation of a push-button on-off-switch. PB_OUT is actively pulled low per default. See the application information section.

Interrupt Management and the INT Pin

The INT pin combines the outputs of the PGOOD comparators from each dc-dc converter and LDOs. The INT pin is used as a POWER_OK pin indicating when all enabled supplies are in regulation. If the PGOODZ register is read via the serial interface, any active bits are then blocked from the INT output pin.

Interrupts can be masked using the MASK register; default operation is not to mask any interrupts since this gives the simple POWER_OK function.

TIMING DIAGRAMS

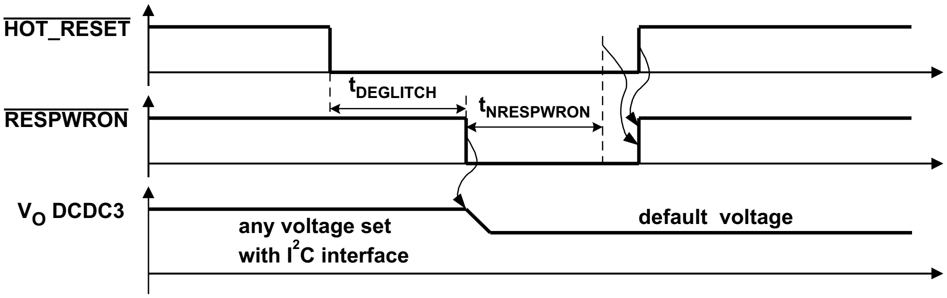


Figure 26. HOT_RESET Timing

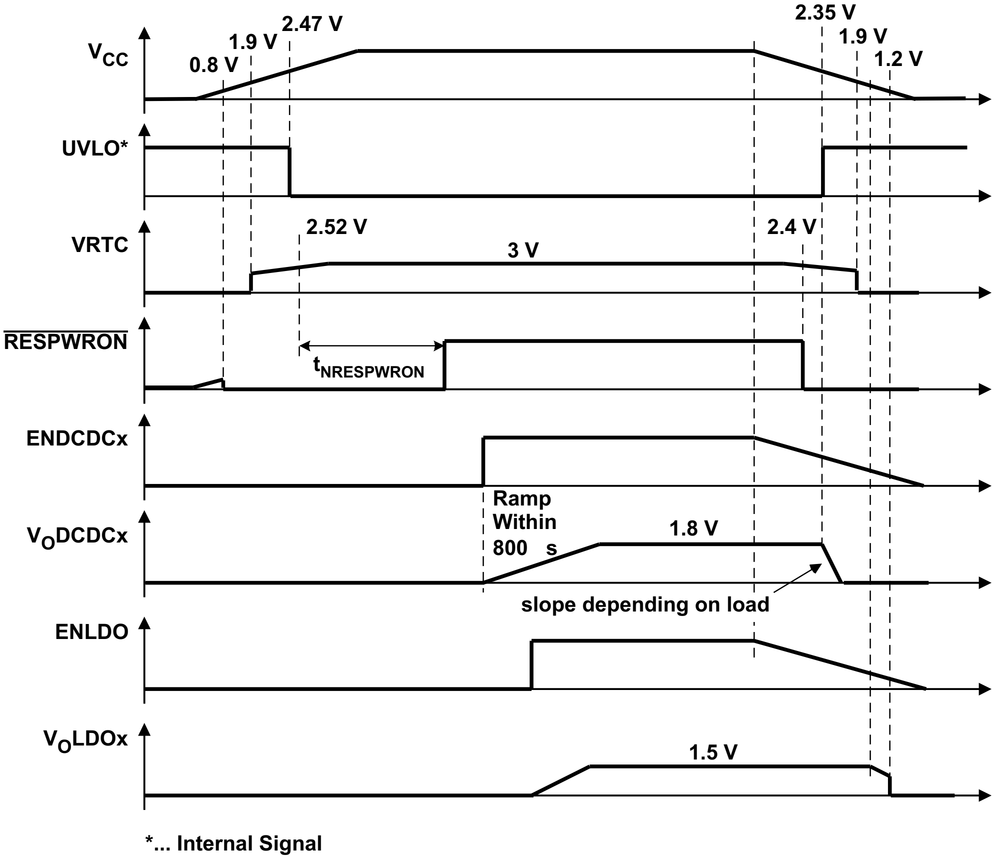


Figure 27. Power-Up and Power-Down Timing

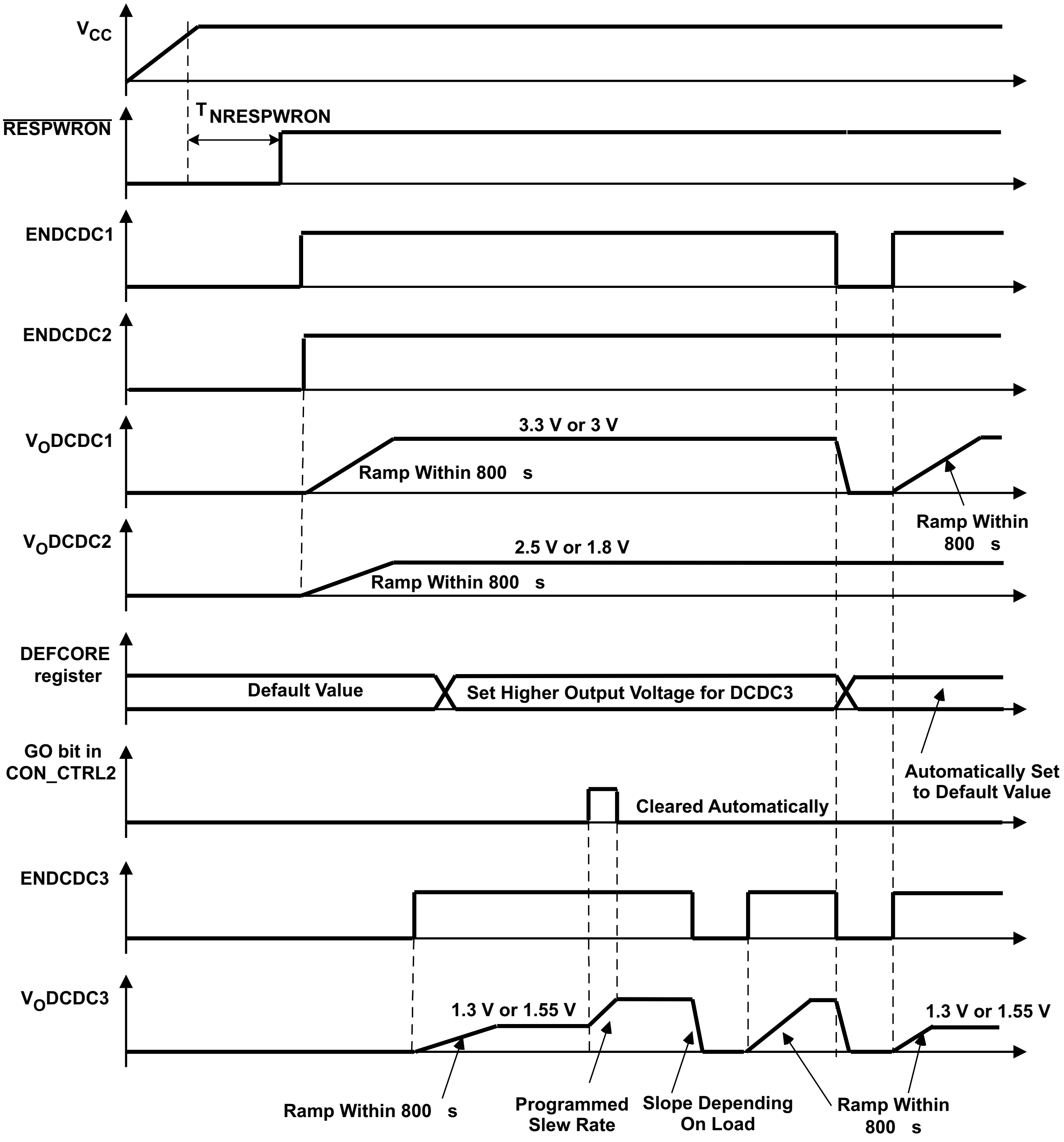


Figure 28. DVS Timing

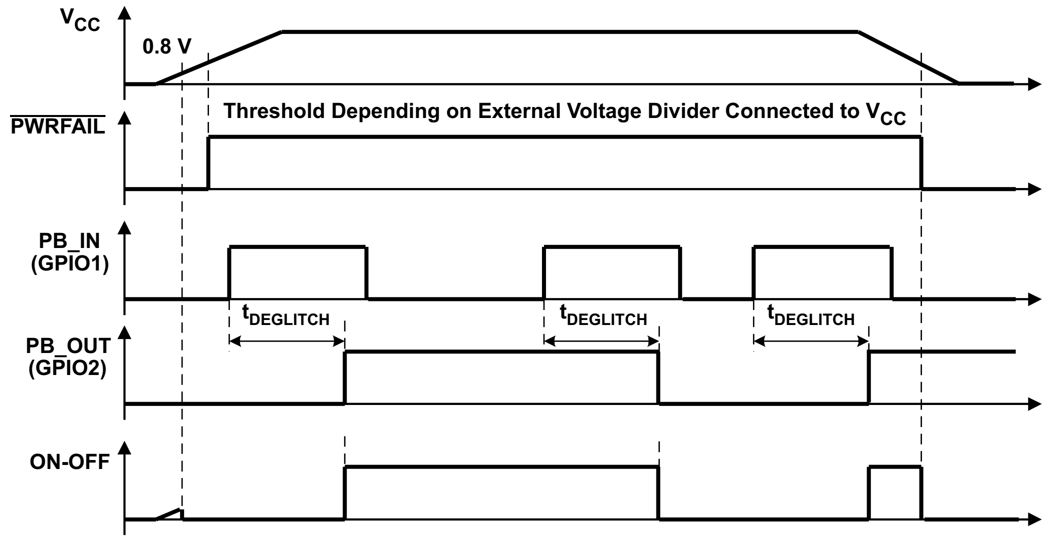


Figure 29. PB-ON-OFF Timing

SERIAL INTERFACE

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above 2 V. The TPS65020 has a 7bit address: 1001000, other addresses are available upon contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65020 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65020 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge–related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65020 device must leave the data line high to enable the master to generate the stop condition

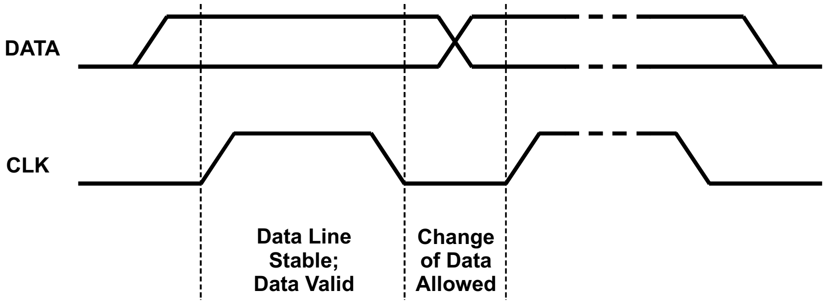


Figure 30. Bit Transfer on the Serial Interface

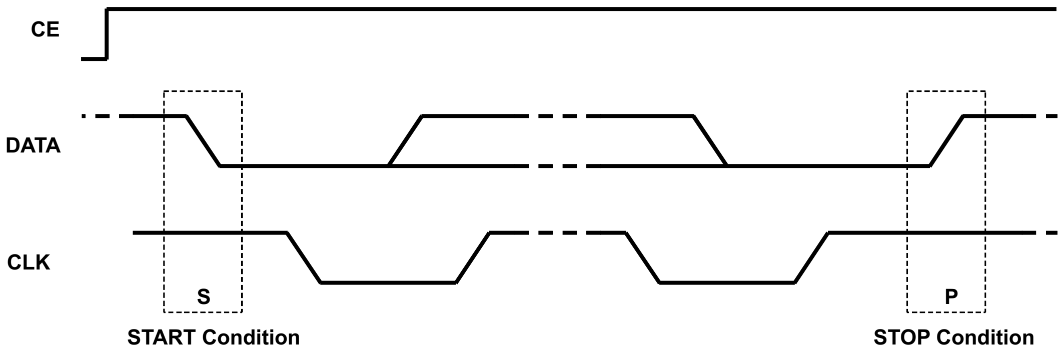
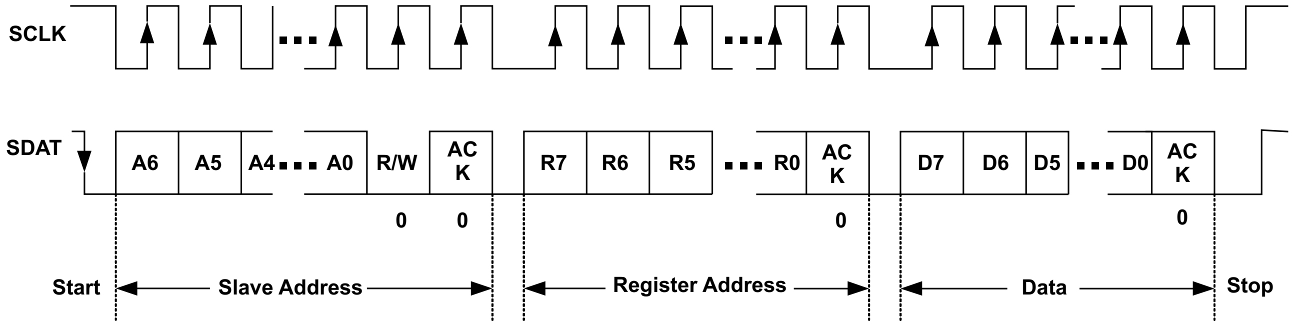
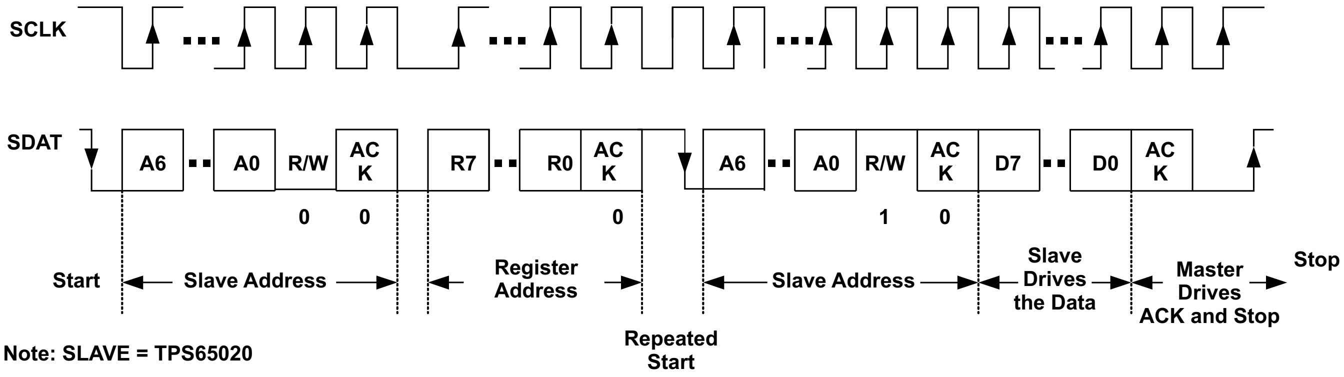


Figure 31. START and STOP Conditions



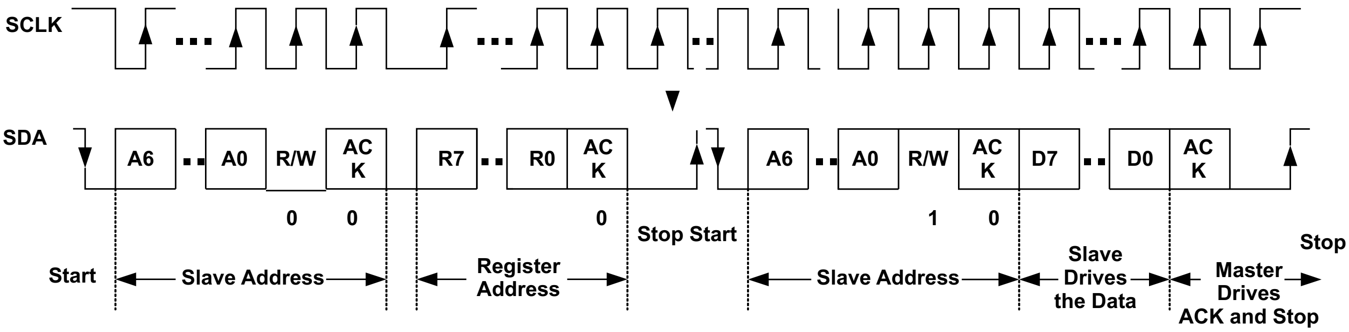
Note: SLAVE = TPS65020

Figure 32. Serial i/f WRITE to TPS65020 Device



Note: SLAVE = TPS65020

Figure 33. Serial i/f READ from TPS65020: Protocol A



Note: SLAVE = TPS65020

Figure 34. Serial i/f READ from TPS65020: Protocol B

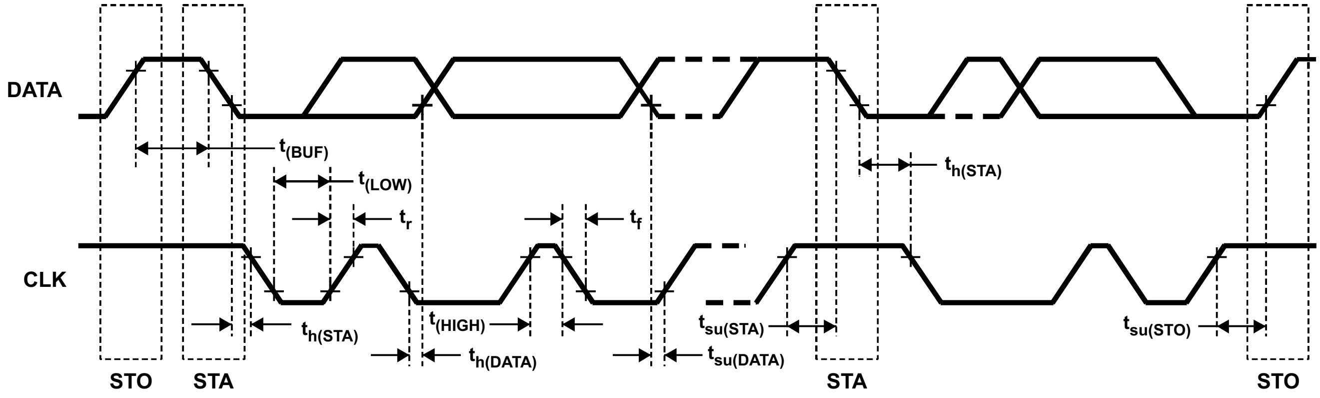


Figure 35. Serial i/f Timing Diagram

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_F	DATA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{h(DATA)}$	Setup time for repeated START condition	600		ns
$t_{h(DATA)}$	Data input hold time	0		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time	1300		ns

VERSION. Register Address: 00h (read only)

VERSION	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	0	0	0	1	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

PGOODZ. Register Address: 01h (read only)

PGOODZ	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	PWRFAILZ	LOWBATTZ	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Set by signal	PWRFAIL	LOWBATT	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Default value loaded by:	PWRFAILZ	LOWBATTZ	PGOOD VDCDC1	PGOOD VDCDC2	PGOOD VDCDC3	PGOOD LDO2	PGOOD LDO1	
Read/Write	R	R	R	R	R	R	R	R

Bit 7 PWRFAILZ:

0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold.

1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold.

Bit 6 LOWBATTZ:

0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold.

1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold.

Bit 5 PGOODZ VDCDC1:

0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled.

1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage

Bit 4 PGOODZ VDCDC2:

0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled.

1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage

Bit 3 PGOODZ VDCDC3: .

0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM controlled output voltage transition

1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage

Bit 2 PGOODZ LDO2:

0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled.

1 = indicates that LDO2 output voltage is below its target regulation voltage

Bit 1 PGOODZ LDO1

0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled.

1 = indicates that the LDO1 output voltage is below its target regulation voltage

The MASK register can be used to mask particular fault conditions from appearing at the $\overline{\text{INT}}$ pin. MASK<n> = 1 masks PGOODZ<n>.

MASK. Register Address: 02h (read/write) Default Value: C0h

MASK	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	MASK PWRFAILZ	MASK LOWBATTZ	MASK VDCDC1	MASK VDCDC2	MASK VDCDC3	MASK LDO2	MASK LDO1	
Default	1	1	0	0	0	0	0	0
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The REG_CTRL register can be used to disable and enable all power supplies via the serial interface. Default is to allow all supplies to be on, providing the relevant enable pin is high. The following tables indicate how the enable pins and the REG_CTRL register are combined. The REG_CTRL bits are automatically reset to default when the corresponding enable pin is low.

REG_CTRL. Register Address: 03h (read/write) Default Value: FFh

REG_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function			VDCDC1 ENABLE	VDCDC2 ENABLE	VDCDC3 ENABLE	LDO2 ENABLE	LDO1 ENABLE	
Default	1	1	1	1	1	1	1	
Set by signal			DCDC1_ENZ	DCDC2_ENZ	DCDC3_ENZ	LDO_ENZ	LDO_ENZ	
Default value loaded by:			UVLO	UVLO	UVLO	UVLO	UVLO	
Read/Write			R/W	R/W	R/W	R/W	R/W	

DCDC1_EN PIN	REG_CTRL<5>	DCDC1 CONVERTER
0	x	disabled
1	0	disabled
1	1	enabled

DCDC2_EN PIN	REG_CTRL<4>	DCDC2 CONVERTER
0	x	disabled
1	0	disabled
1	1	enabled

DCDC3_EN PIN	REG_CTRL<3>	DCDC3 CONVERTER
0	x	disabled
1	0	disabled
1	1	enabled

LDO_EN PIN	REG_CTRL<2>	LDO2
0	x	disabled
1	0	disabled
1	1	enabled

LDO_EN PIN	REG_CTRL<1>	LDO1
0	x	disabled
1	0	disabled
1	1	enabled

The CON_CTRL register is used to force any or all of the converters into forced PWM operation, when low output voltage ripple is vital. It is also used to control the phase shift between the three converters in order to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed zero phase shift.

CON_CTRL. Register Address: 04h (read/write) Default Value: B0h

CON_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name and function	DCDC2 PHASE1	DCDC2 PHASE0	DCDC3 PHASE1	DCDC3 PHASE0	LOW RIPPLE	FPWM DCDC2	FPWM DCDC1	FPWM DCDC3
Default	1	0	1	1	0	0	0	0
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CON_CTRL<7:6>	**DCDC2 CONVERTER DELAYED BY**
00	zero
01	1/4 cylce
10	**½ cycle**
11	3/4 cycle

CON_CTRL<5:4>	**DCDC3 CONVERTER DELAYED BY**
00	zero
01	1/4 cylce
10	½ cycle
11	**3/4 cycle**

Bit 3 LOW RIPPLE:
0 = Skip mode operation optimized for high efficiency for all converters
1 = Skip mode operation optimized for low output voltage ripple for all converters

Bit 2 FPWM DCDC2:
0 = DCDC2 converter operates in PWM / PFM mode
1 = DCDC2 converter is forced into fixed frequency PWM mode

Bit 1 FPWM DCDC1:
0 = DCDC1 converter operates in PWM / PFM mode
1 = DCDC1 converter is forced into fixed frequency PWM mode

Bit 0 FPWM DCDC3:
0 = DCDC3 converter operates in PWM / PFM mode
1 = DCDC3 converter is forced into fixed frequency PWM mode

The CON_CTRL2 register can be used to take control the inductive converters.

CON_CTRL. Register Address: 05h (read/write) Default Value: 40h

CON_CTRL2	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name and function	GO	Core adj allowed				DCDC2 discharge	DCDC1 discharge	DCDC3 discharge
Default	0	1	0	0	0	0	0	0
Default value loaded by:	UVLO + DONE	UVLO				UVLO	UVLO	UVLO
Read/Write	R/W	R/W				R/W	R/W	R/W

Bit 7 GO:

0 = no change in the output voltage for the DCDC3 converter

1 = the output voltage of the DCDC3 converter is changed to the value defined in DEFCORE with the slew rate defined in DEFSLEW. This bit is automatically cleared when the DVM transition is complete. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC3 output voltage is actually in regulation at the desired voltage.

Bit 6 CORE ADJ Allowed:

0 = the output voltage is set with the I^{2}C register

1 = DEFDCDC3 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC3 defaults to 1.3 V or 1.55 V respectively at start-up

Bit 2– 0 0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled

1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load

DEFCORE. Register Address: 06h (read/write Default Value: 14h/1Eh

DEFCORE	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function				CORE4	CORE3	CORE2	CORE1	CORE0
Default	0	0	0	1	DEFDCDC3	1	DEFDCDC3	0
Default value loaded by:				RESET(1)	RESET(1)	RESET(1)	RESET(1)	RESET(1)
Read/Write				R/W	R/W	R/W	R/W	R/W

RESET(1): DEFCORE is reset to its default value by one of these events:

- undervoltage lockout (UVLO)
- DCDC1 AND DCDC3 disabled
- $\overline{\text{HOT\_RESET}}$ pulled low
- $\overline{\text{RESPWRON}}$ active
- VRTC below threshold

CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC3		CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC3
0	0	0	0	0	0.8 V		1	0	0	0	0	1.2 V
0	0	0	0	1	0.825 V		1	0	0	0	1	1.225 V
0	0	0	1	0	0.85 V		1	0	0	1	0	1.25 V
0	0	0	1	1	0.875 V		1	0	0	1	1	1.275 V
0	0	1	0	0	0.9 V		1	0	1	0	0	1.3 V
0	0	1	0	1	0.925 V		1	0	1	0	1	1.325 V
0	0	1	1	0	0.95 V		1	0	1	1	0	1.35 V
0	0	1	1	1	0.975 V		1	0	1	1	1	1.375 V
0	1	0	0	0	1 V		1	1	0	0	0	1.4 V
0	1	0	0	1	1.025 V		1	1	0	0	1	1.425 V
0	1	0	1	0	1.05 V		1	1	0	1	0	1.45 V
0	1	0	1	1	1.075 V		1	1	0	1	1	1.475 V
0	1	1	0	0	1.1 V		1	1	1	0	0	1.5 V
0	1	1	0	1	1.125 V		1	1	1	0	1	1.525 V
0	1	1	1	0	1.15 V		1	1	1	1	0	1.55 V
0	1	1	1	1	1.175 V		1	1	1	1	1	1.6 V

DEFSLEW. Register Address: 07h (read/write) Default Value: 06h

DEFSLEW	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function						SLEW2	SLEW1	SLEW0
Default						1	1	0
Default value loaded by:						UVLO	UVLO	UVLO
Read/Write						R/W	R/W	R/W

SLEW2	SLEW1	SLEW0	VDCDC3 SLEW RATE
0	0	0	0.15 mV/µs
0	0	1	0.3 mV/µs
0	1	0	0.6 mV/µs
0	1	1	1.2 mV/µs
1	0	0	2.4 mV/µs
1	0	1	4.8 mV/µs
1	**1**	**0**	**9.6 mV/µs**
1	1	1	Immediate

LDO_CTRL. Register Address: 08h (read/write) Default Value: 23h

LDO_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function		LDO2_2	LDO2_1	LDO2_0		LDO1_2	LDO1_1	LDO1_0
Default		0	1	0		0	1	1
Default value loaded by:		UVLO	UVLO	UVLO		UVLO	UVLO	UVLO
Read/Write		R/W	R/W	R/W		R/W	R/W	R/W

The LDO_CTRL registers can be used to set the output voltage of LDO1 and LDO2.

LDO1_2	LDO1_1	LDO1_0	LDO1 OUTPUT VOLTAGE		LDO2_2	LDO2_1	LDO2_0	LDO2 OUTPUT VOLTAGE
0	0	0	1 V		0	0	0	1 V
0	0	1	1.05 V		0	0	1	1.05 V
0	1	0	1.1 V		**0**	**1**	**0**	**1.1 V**
0	**1**	**1**	**1.3 V**		0	1	1	1.3 V
1	0	0	1.8 V		1	0	0	1.8 V
1	0	1	2.5 V		1	0	1	2.5 V
1	1	0	3 V		1	1	0	3 V
1	1	1	3.3 V		1	1	1	3.3 V

DESIGN PROCEDURE

Inductor Selection for the DC-DC Converters

Each of the converters in the TPS65020 typically use a 3.3 μH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

For a fast transient response, a 2.2-μH inductor in combination with a 22-μF output capacitor is recommended.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is needed because during heavy load transient the inductor current rises above the value calculated under Equation 4.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \tag{4}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{5}$$

with:

f = Switching Frequency (1.5 MHz typical)
L = Inductor Value
ΔI_L = Peak-to-Peak inductor ripple current
I_{LMAX} = Maximum Inductor current

The highest inductor current occurs at maximum Vin.

Open core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65020 (2 A for the VDCDC1 and VDCDC2 converters, and 1.3 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

See Table 3 and the typical applications for possible inductors.

Table 3. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC3 converter	3.3 µH	CDRH2D14NP-3R3	Sumida
	3.3 µH	LPS3010-332	Coilcraft
	3.3 µH	VLF4012AT-3R3M1R3	TDK
	2.2 µH	VLF4012AT-2R2M1R5	TDK
	2.2 µH	NR3015T2R2	Taiyo-Yuden
DCDC2 converter	3.3 µH	CDRH2D18/HPNP-3R3	Sumida
	3.3 µH	VLF4012AT-3R3M1R3	TDK
	2.2 µH	VLCF4020-2R2	TDK
DCDC1 converter	3.3 µH	CDRH3D14/HPNP-3R2	Sumida
	3.3 µH	CDRH4D28C-3R2	Sumida
	3.3 µH	MSS5131-332	Coilcraft
	2.2 µH	VLCF4020-2R2	TDK

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the inductive converters implemented in the TPS65020 allow the use of small ceramic capacitors with a typical value of 10 µF for a 3.3-µH inductor for each converter without having large output voltage under and overshoots during heavy load transients.

For a fast transient response a 22-µF capacitor with a 2.2-µH inductor should be used on each converter.

Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 4 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \qquad (6)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$I_{RMSCout} = \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \qquad (7)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each dc-dc converter requires a 10-µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the dc-dc converters. A filter resistor of up to 10R and a 1-µF capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the VCC pin when all converters are running in PWM mode.

Table 4. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic

Output Voltage Selection

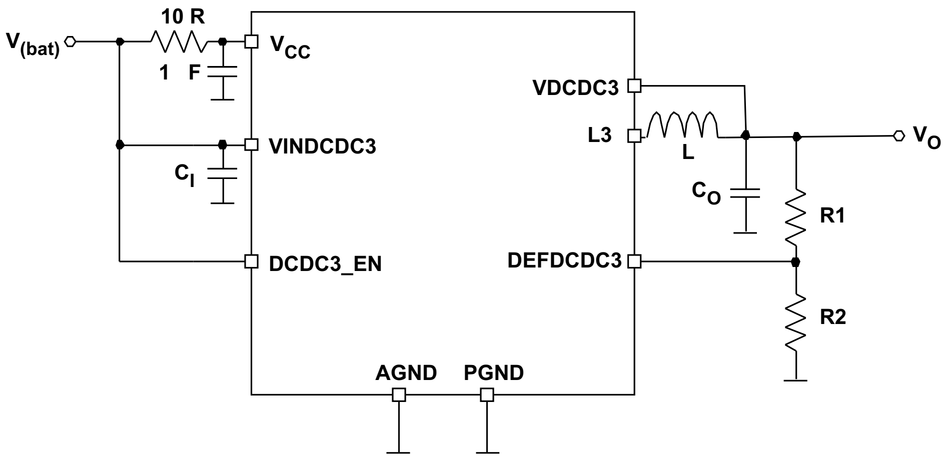
The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See the table for the default voltages if the pins are pulled to GND or to VCC. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in Table 5.

The output voltage of VDCDC3 is set with the I^2C interface. If the voltage is changed from the default, using the DEFCORE register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC3 does not change the voltage set with the register. Bit B6 in the CON_CTRL2 register is used to switch between the internal voltage setting or the voltage set with the external DEFDCDC3 pin for the VDCDC3 converter.

Table 5.

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	3.3 V
	GND	3 V
DEFDCDC2	VCC	2.5 V
	GND	1.8 V
DEFDCDC3	VCC	1.55 V
	GND	1.3 V

Using an external resistor divider at DEFDCDCx:



When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage $V_{(bat)}$. The total resistance (R1+R2) of the voltage divider should be kept in the 1-MR range in order to maintain a high efficiency at light load.

$V_{(DEFDCDCx)} = 0.6\ V$

$$V_{OUT} = V_{DEFDCDC3} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDC3}}\right) - R2 \tag{8}$$

VRTC Output

The VRTC output is typically connected to the Vcc_Batt pin of a Intel PXA270 processor. During power-up of the processor, the TPS65020 internally switches from the LDO or the backup battery to the system voltage connected at the VSYSIN pin (see Figure 25). It is recommended to add a capacitor of 4.7-µF minimum to the VRTC pin.

LDO1 and LDO2

The LDOs default voltage is 1.1 V for LDO2 and 1.3 V for LDO1. They are intended to provide power to VCC_PLL and the VCC_SRAM pin on a PXA270 processor. The minimum output capacitor required is 2.2 µF. The LDOs output voltage is changed to different voltages between 1 V and 3.3 V using the I^2C interface. Therefore, they can also be used as general-purpose LDOs in applications powering processors different from PXA270. The supply voltage for the LDOs needs to be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system, and providing the highest efficiency.

Trespwron

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2 µA between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

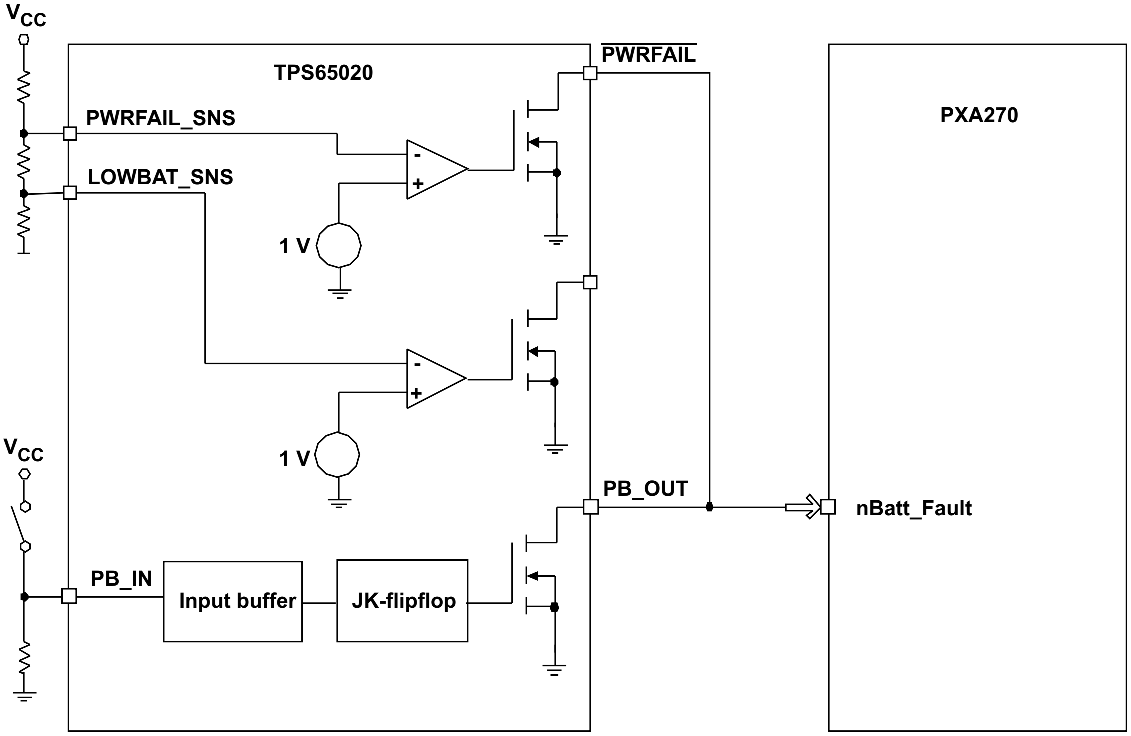
Vcc-Filter

An RC filter connected at the VCC input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 10R and 1 µF is used to filter the switching spikes, generated by the dc-dc converters. A larger resistor than 10R should not be used because the current into VCC of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at VCC internally to switch off too early.

APPLICATION INFORMATION

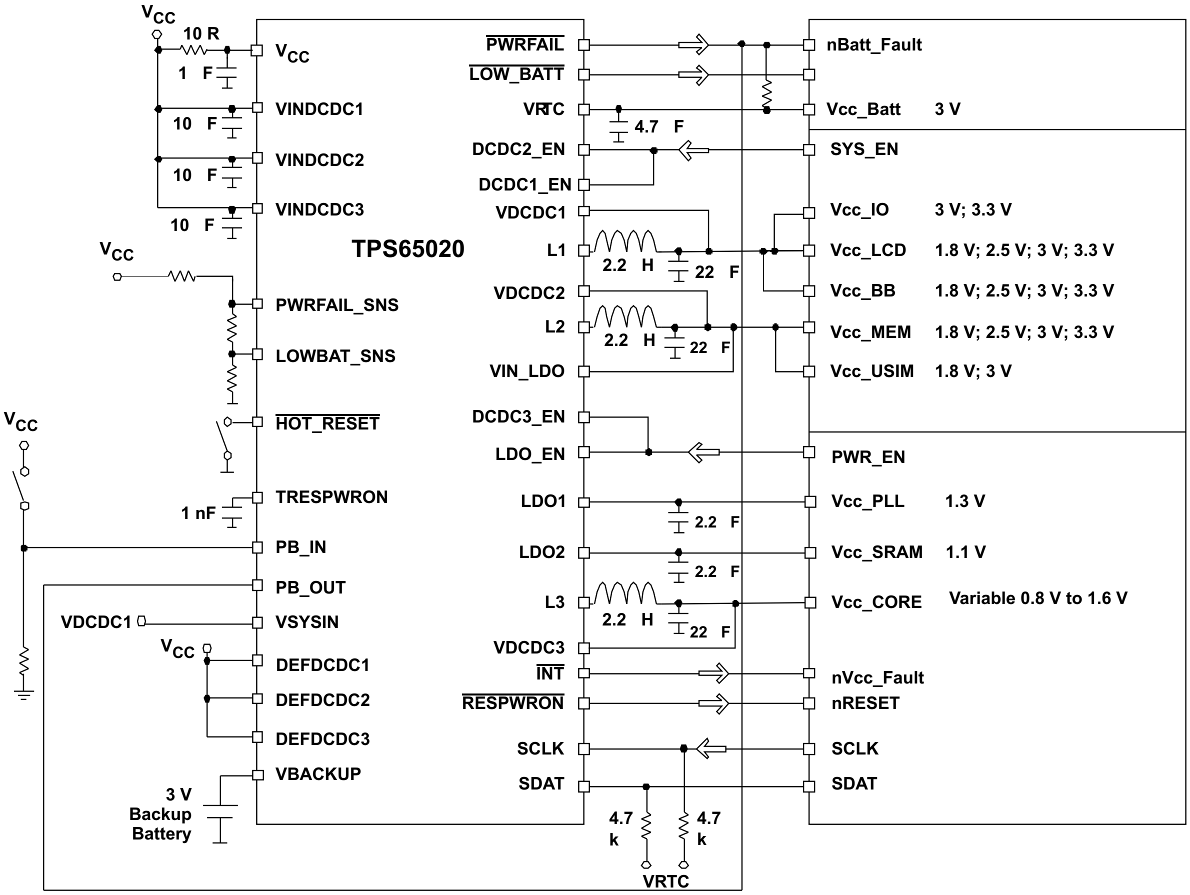
IMPLEMENTING A PUSH-BUTTON ON-OFF FUNCTION USING PB_IN AND PB_OUT

In mobile phone applications, usually the device must not automatically power up when the battery is inserted. Such a function can be implemented using PB_IN and PB_OUT. After the main battery is inserted, the PB_OUT open drain output is low. When this pins is connected with $\overline{\text{PWRFAIL}}$, the signal is pulled low, preventing Intel PXA270 to start up.



APPLICATION INFORMATION (continued)

TYPICAL CONFIGURATION FOR THE Intel Bulverde PROCESSOR

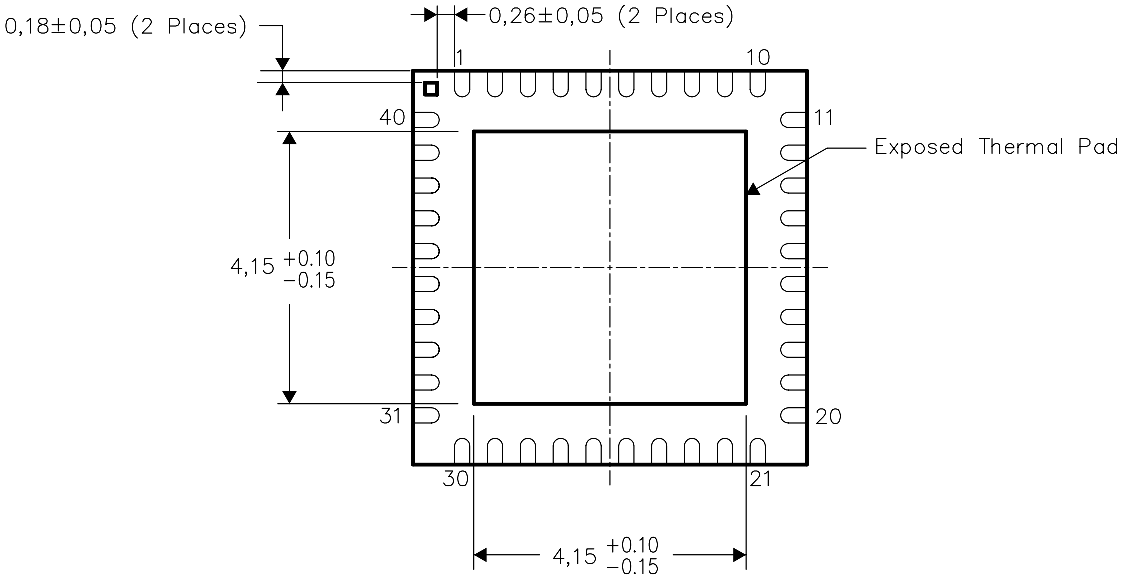


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGE OPTION ADDENDUM

23-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS65020RHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS65020RHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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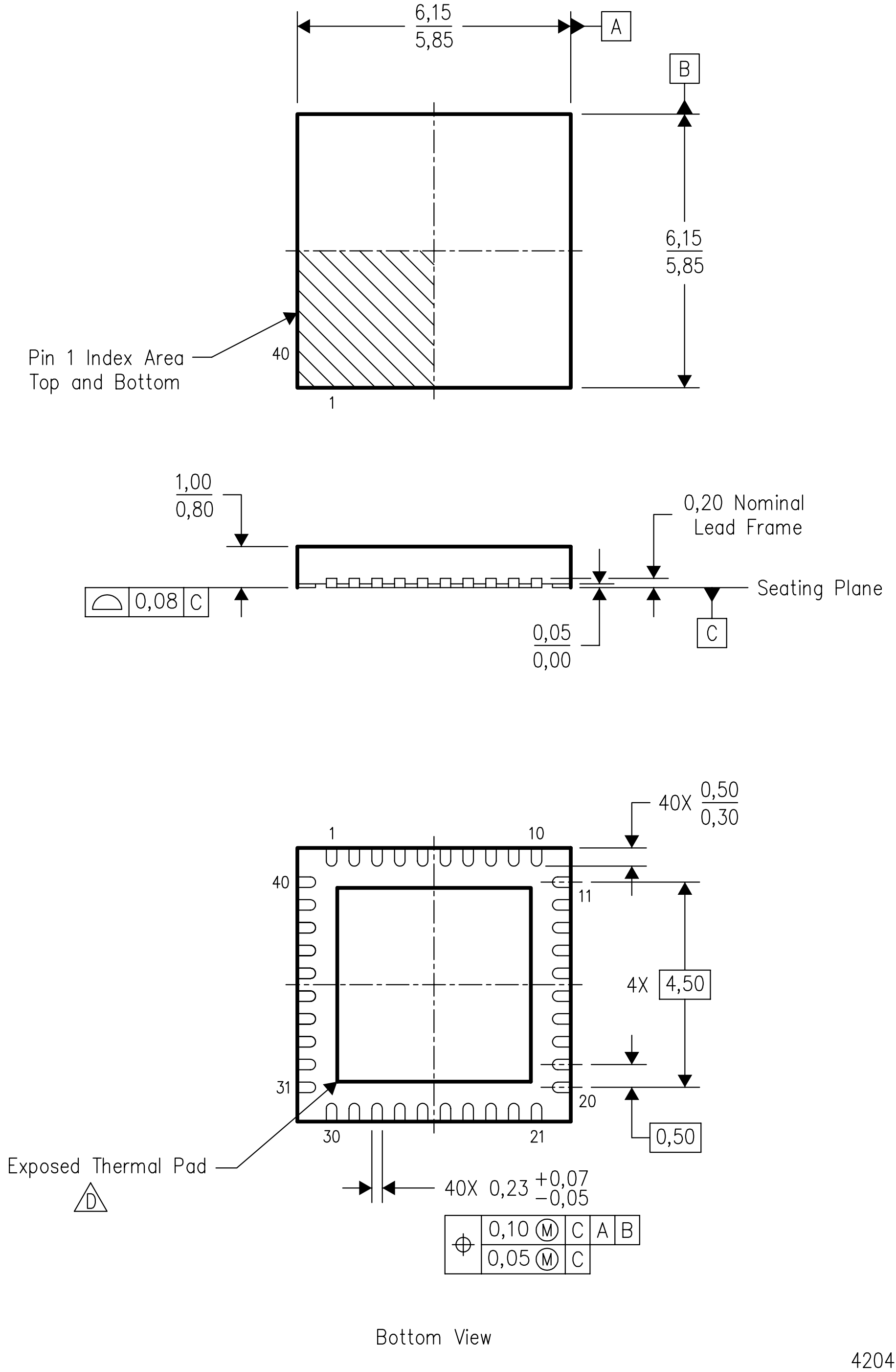
RHA (S-PQFP-N40) PLASTIC QUAD FLATPACK



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No−Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO−220 variation VJJD−2.

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