

TPS6290x Step-Down Converter Evaluation Module User's Guide



ABSTRACT

The TPS6290xEVM-069 (BSR069) facilitates the evaluation of the TPS6290x 1-A, 2-A and 3-A pin-to-pin compatible buck converters in small 1.5-mm by 2-mm QFN packages. The BSR069-003 uses the 3-A TPS62903 to output a 1.2-V output voltage from input voltages between 3 V and 17 V. The BSR069-002 uses the 2-A TPS62902 to output a 1.8-V output voltage from input voltages between 3 V and 17 V. The BSR069-001 uses the 1-A TPS62901 to output a 3.3-V output voltage from input voltages up to 17 V. The TPS6290x is a high-efficiency, low I_Q buck converter for use in a variety of industrial, enterprise, and personal electronics applications, such as factory and building automation, IP network cameras, industrial PC, data center switches, servo drives, mobile and embedded computing, and any application with a 12-V input voltage or a 1-4 cell lithium battery pack.

Table of Contents

1 Introduction	2
1.1 Performance Specification.....	2
1.2 Modifications.....	2
2 Setup	4
2.1 Input/Output Connector Descriptions.....	4
3 Safety Instructions	5
4 Test Results	6
5 Board Layout	7
6 Schematic and Bill of Materials	10
6.1 Schematic.....	10
6.2 Bill of Materials.....	13
7 Revision History	14

List of Figures

Figure 1-1. Loop Response Measurement Modification (Top Layer).....	3
Figure 4-1. Thermal Performance ($V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 3000\text{ mA}$, JP2 open).....	6
Figure 4-2. Loop Response Measurement ($V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 3000\text{ mA}$, JP2 open).....	6
Figure 5-1. Top Assembly.....	7
Figure 5-2. Top Layer.....	7
Figure 5-3. Internal Layer 1.....	8
Figure 5-4. Internal Layer 2.....	8
Figure 5-5. Bottom Layer.....	9
Figure 5-6. Bottom Layer (Mirrored).....	9
Figure 6-1. TPS62903EVM-069 Schematic.....	10
Figure 6-2. TPS62902EVM-069 Schematic.....	11
Figure 6-3. TPS62901EVM-069 Schematic.....	12

List of Tables

Table 1-1. TPS62903EVM-069 Performance Specification Summary.....	2
Table 1-2. TPS62902EVM-069 Performance Specification Summary.....	2
Table 1-3. TPS62901EVM-069 Performance Specification Summary.....	2
Table 6-1. TPS6290xEVM-069 Bill of Materials.....	13

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1 Introduction

The TPS6290x are synchronous, step-down converters in a small 1.5- × 2- × 1-mm QFN package. Three different devices in this family support 1 A, 2 A, or 3 A of output current.

1.1 Performance Specification

Table 1-1, Table 1-2, and Table 1-3 provide a summary of the TPS6290xEVM-069 performance specifications.

Table 1-1. TPS62903EVM-069 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input Voltage		3	12	17	V
Output Voltage Setpoint			1.2		V
Output Current		0		3	A
MODE/S-CONF (R4) Setting	2.5 MHz, Auto PFM/PWM with AEE, external FB, output discharge disabled		7.15		kΩ

Table 1-2. TPS62902EVM-069 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input Voltage		3	12	17	V
Output Voltage Setpoint			1.8		V
Output Current		0		2	A
MODE/S-CONF (R4) Setting	1 MHz, Auto PFM/PWM, external FB, output discharge disabled		16.9		kΩ

Table 1-3. TPS62901EVM-069 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input Voltage		3.4	12	17	V
Output Voltage Setpoint			3.3		V
Output Current		0		1	A
MODE/S-CONF (R4) Setting	1 MHz, Auto PFM/PWM, external FB, output discharge disabled		16.9		kΩ

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. Additional input and output capacitors can be added. Also, the input voltage at which the IC turns on can be adjusted with two resistors, the soft start time can be changed, the output voltage can track an applied voltage, a feed-forward capacitor can be added, and the switching frequency, output discharge setting, MODE setting, and output voltage setting configuration can be changed. Finally, the loop response can be measured. See the [TPS62903, 3-V to 17-V, Low I_Q Buck Converter in 1.5 mm × 2 mm QFN Package data sheet](#) for details of the various settings.

1.2.1 Input and Output Capacitors

C6, C7, and C8 are provided for additional input capacitors. These capacitors are not required for proper operation but can be used to reduce the input voltage ripple.

C9, C10, C11, and C12 are provided for additional bulk output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple. The total output capacitance must remain within the recommended range in the [TPS62903, 3-V to 17-V, Low I_Q Buck Converter in 1.5 mm × 2 mm QFN Package data sheet](#) for proper operation.

1.2.2 Configurable Enable Threshold Voltage

With JP1 removed, R5 and R6 can be installed to set a user-selectable input voltage at which the IC turns on.

1.2.3 SS/TR Capacitor

C3 sets the soft start time. This capacitor can be changed to set other soft start times.

1.2.4 Feedforward Capacitor

C5 is provided as an optional feedforward capacitor (C_{FF}).

1.2.5 MODE/S-CONF Resistor

R4 selects the switching frequency, output discharge, MODE setting, and output voltage setting configuration. When selecting a different switching frequency, the inductor value should also be changed. When using the VSET configuration for setting the output voltage, remove R1 and change the value of R2. See the [TPS62903, 3-V to 17-V, Low \$I_Q\$ Buck Converter in 1.5 mm × 2 mm QFN Package data sheet](#) for details of the various settings.

1.2.6 Loop Response Measurement

The loop response can be measured with simple changes to the circuitry. First, install a 10- Ω resistor across R9's pads on the back of the PCB. The pads are spaced to allow installation of an 0603-sized resistor. Next, cut the short section of trace on the top layer between the via on pin 3 and C2. [Figure 1-1](#) shows this change. With these changes, an AC signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added 10- Ω resistor. [Figure 4-2](#) shows the results of this test.

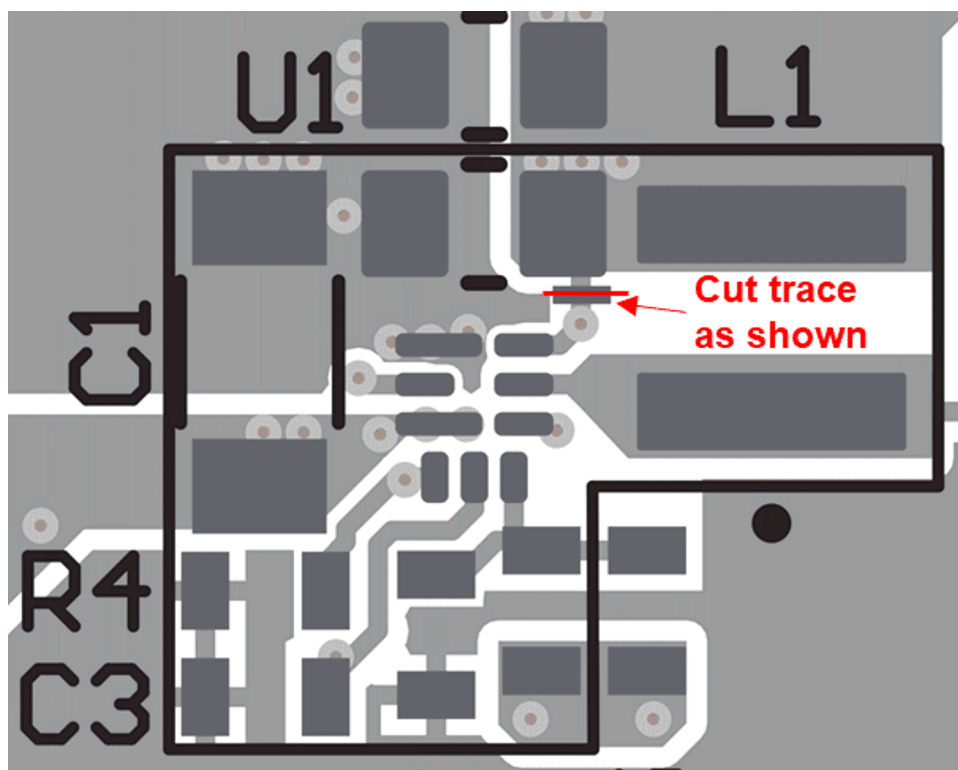


Figure 1-1. Loop Response Measurement Modification (Top Layer)

2 Setup

This section describes how to properly use the EVM.

2.1 Input/Output Connector Descriptions

J1, Pin 1 and 2 – V_{IN}	Positive input connection from the input supply for the EVM.
J1, Pin 3 and 4 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J1, Pin 5 and 6 – GND	Return connection from the input supply for the EVM.
J2, Pin 1 and 2 – V_{OUT}	Output voltage connection
J2, Pin 3 and 4 – S+/S-	Output voltage sense connections. Measure the output voltage at this point.
J2, Pin 5 and 6 – GND	Output return connection
J3 – PG/GND	The PG output is on pin 1 of this header with a convenient ground on pin 2.
J4 – TRACK-IN/SS/TR/GND	By removing C3, the IC tracks an externally applied voltage. Apply the voltage on pin 1 to scale the applied voltage through R7 and R8. The SS/TR voltage can be measured on pin 2.
J5 – SW/GND	This header is not installed. Use the holes in the PCB to measure the SW node on pin 2 with a convenient GND on pin 1.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC. Remove the jumper to set a configurable enable threshold voltage with R5 and R6.
JP2 – MODE/S-CONF	MODE/S-CONF pin input jumper. Place the supplied jumper across PWM and MODE/S-CONF to operate the IC in forced PWM mode. Place the jumper across PFM/PWM and MODE/S-CONF to operate the IC in Auto PFM/PWM mode. Remove the jumper to operate the IC with the MODE/S-CONF settings set by R4.
Note	
If it is desired to change between PWM and PFM/PWM modes during operation, JP2 must be set to either PWM or PFM/PWM before enabling the IC.	
JP3 – PG Pull-up Voltage	PG pin pull-up voltage jumper. Place the supplied jumper on JP3 to connect the PG pin pull-up resistor to V _{OUT} . Alternatively, the jumper can be removed and a different voltage can be supplied on pin 1 to pull up the PG pin to a different level. This externally applied voltage must remain below 18 V.

3 Safety Instructions



WARNING

Hot surface. Contact may cause burns. Do not touch.

4 Test Results

The TPS6290xEVM-069 was used to take all the data in the [TPS62903, 3-V to 17-V, Low I_Q Buck Converter in 1.5 mm × 2 mm QFN Package data sheet](#). See the device data sheet for the performance of this EVM.

Figure 4-1 shows the thermal performance of the EVM. "Spot" shows the temperature of the PCB. Figure 4-2 shows the loop response measurement.

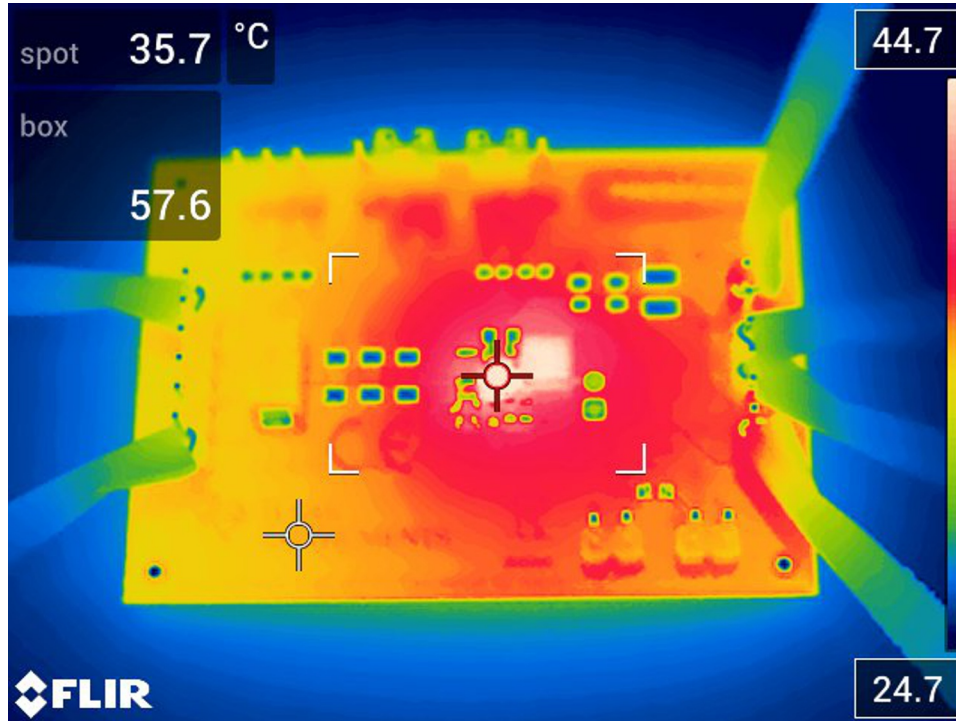


Figure 4-1. Thermal Performance ($V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 3000\text{ mA}$, JP2 open)

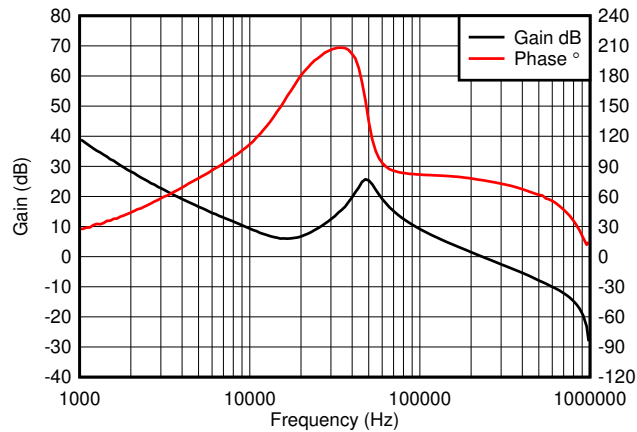


Figure 4-2. Loop Response Measurement ($V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 3000\text{ mA}$, JP2 open)

5 Board Layout

This section provides the EVM board layout and illustrations in [Figure 5-1](#) through [Figure 5-6](#). The Gerbers are available on the [EVM product page](#).

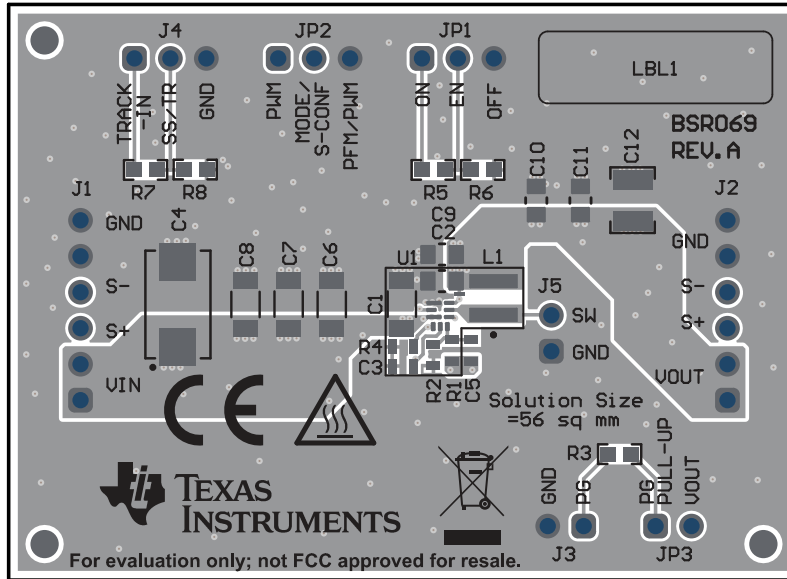


Figure 5-1. Top Assembly

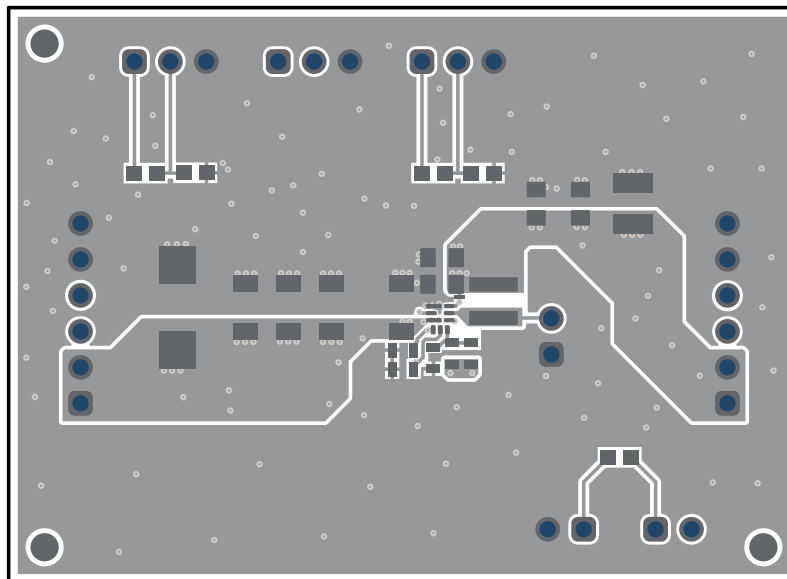


Figure 5-2. Top Layer

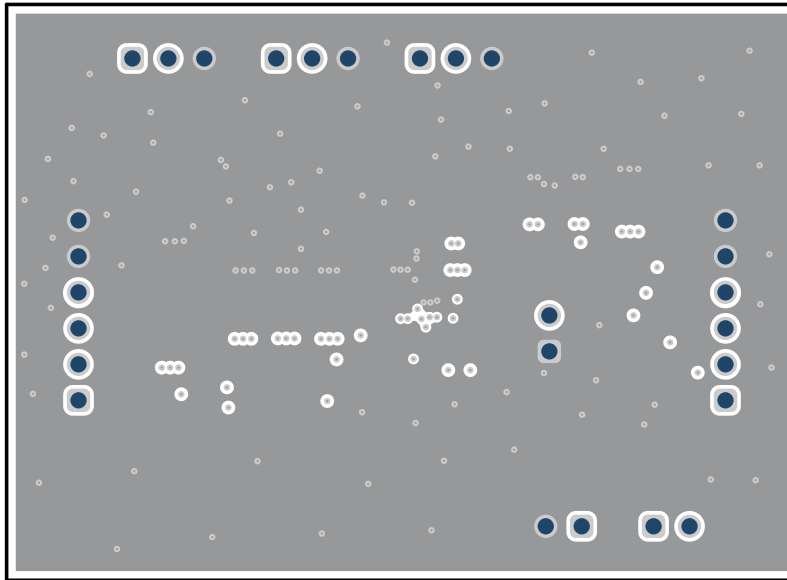


Figure 5-3. Internal Layer 1

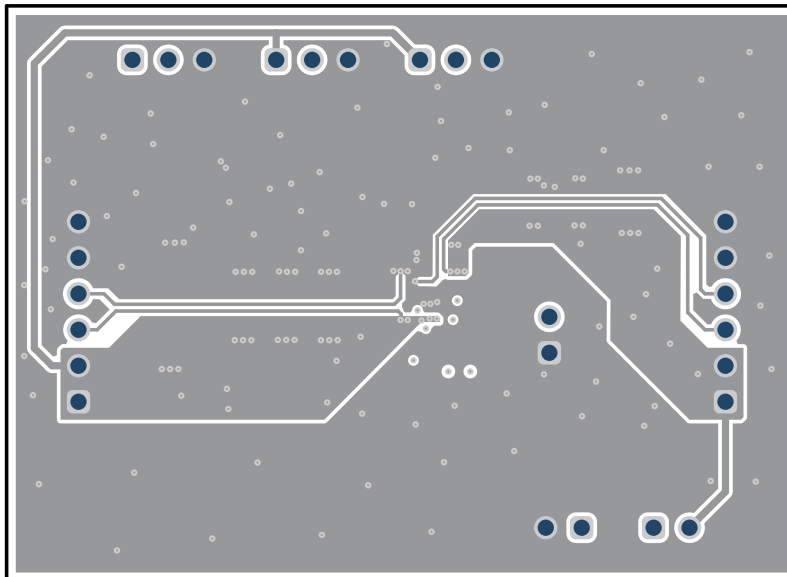


Figure 5-4. Internal Layer 2

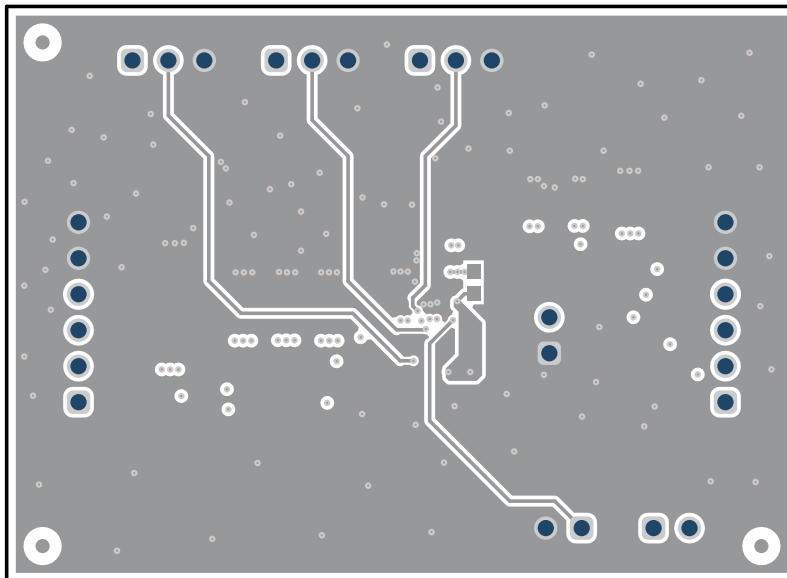


Figure 5-5. Bottom Layer

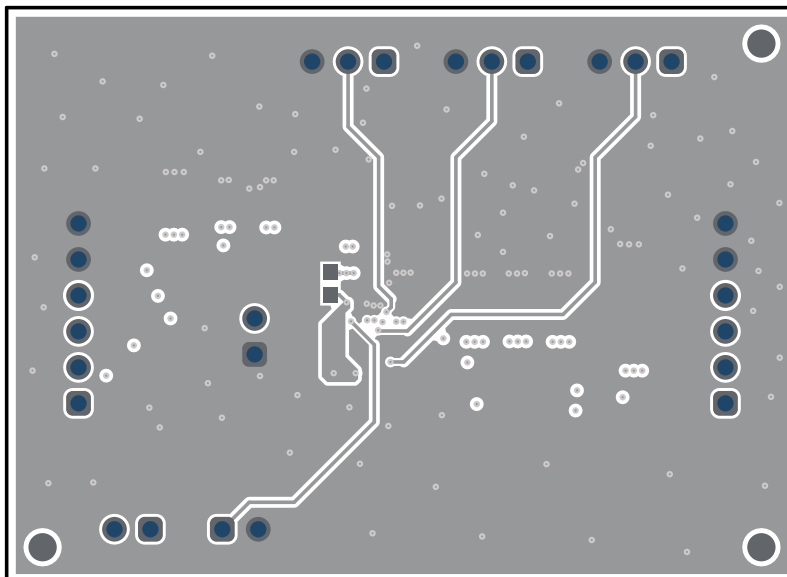


Figure 5-6. Bottom Layer (Mirrored)

6 Schematic and Bill of Materials

This section provides the EVM schematic and bill of materials (BOM).

6.1 Schematic

Figure 6-1, Figure 6-2, and Figure 6-3 illustrate the EVM schematics.

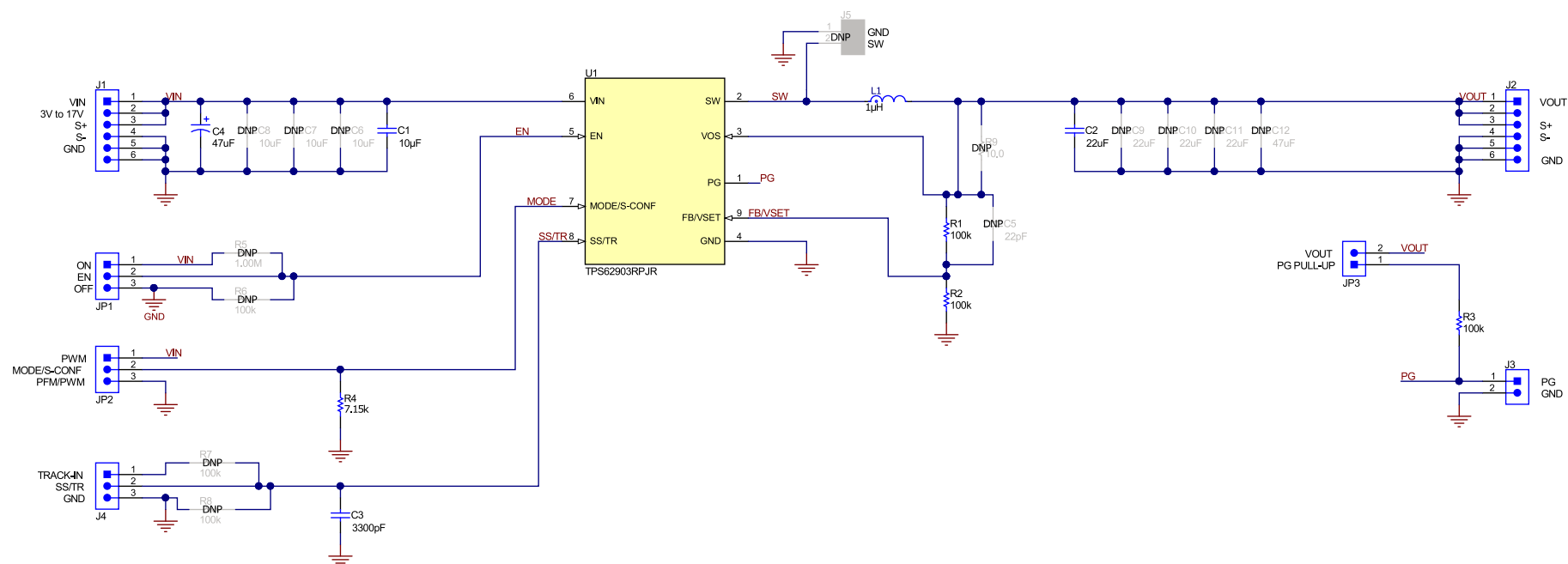


Figure 6-1. TPS62903EVM-069 Schematic

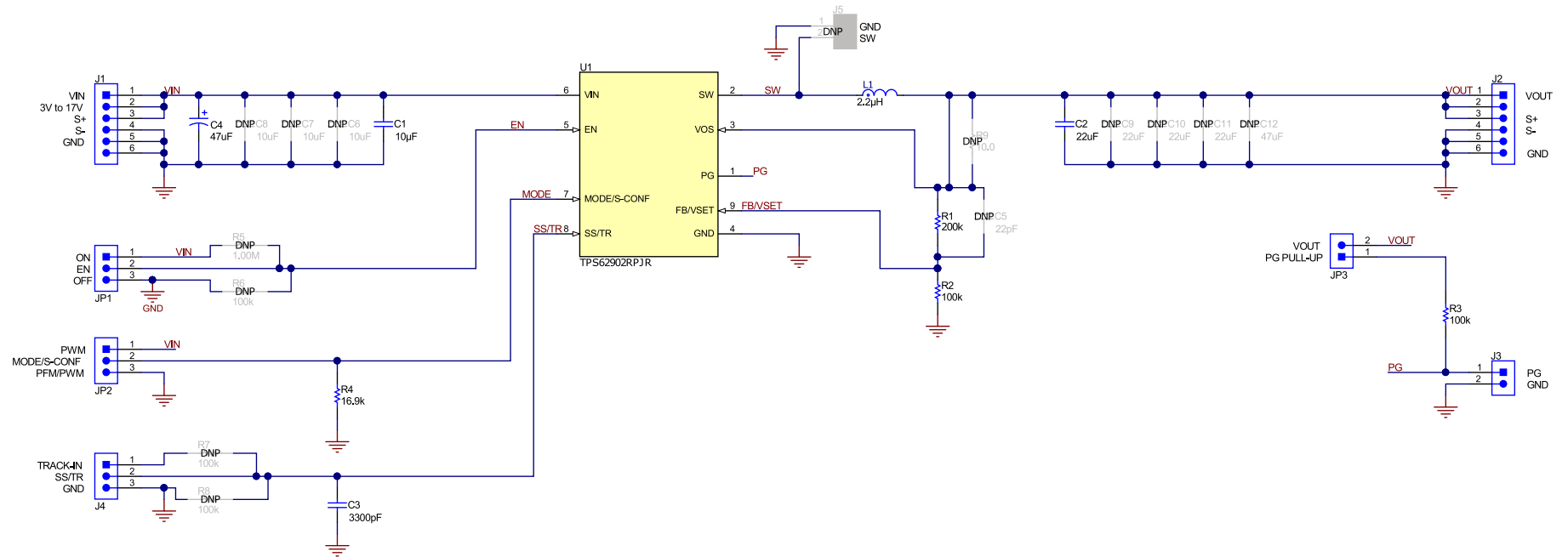


Figure 6-2. TPS62902EVM-069 Schematic

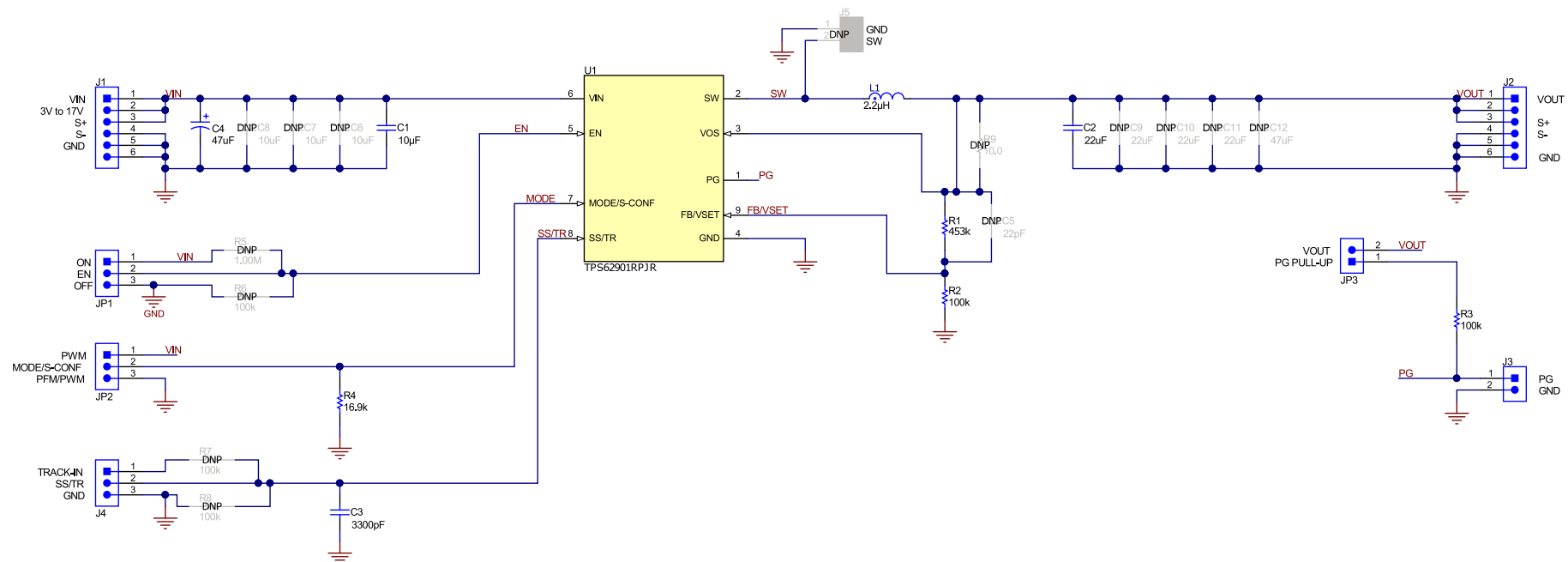


Figure 6-3. TPS62901EVM-069 Schematic

6.2 Bill of Materials

Table 6-1 lists the BOM for this EVM.

Table 6-1. TPS6290xEVM-069 Bill of Materials

-001	-002	-003	Reference Designator	Value	Description	Package	Part Number	Manufacturer
1	1	1	C1	10 μ F	CAP, CERM, 10 μ F, 25 V, +/- 10%, X7R	1206	C3216X7R1E106K160AB	TDK
1	1	1	C2	22 μ F	CAP, CERM, 22 μ F, 10 V, +/- 20%, X7S	0805	C2012X7S1A226M125AC	TDK
1	1	1	C3	3300pF	CAP, CERM, 3300 pF, 50 V, +/- 5%, COG/NPO	0603	GRM1885C1H332JA01D	muRata
1	1	1	C4	47 μ F	CAP, TA, 47 μ F, 35 V, +/- 10%, 0.3 Ω	7343-43	T495X476K035ATE300	Kemet
0	0	1	L1	1 μ H	Inductor Power Shielded Wirewound 1 μ H 20% Composite 8.8A 8.2m Ω DCR	4 x 4 mm	XGL4020-102MEC	Coilcraft
1	1	0	L1	2.2 μ H	Inductor Power Shielded Wirewound 2.2 μ H 20% Composite 6.2A 19.5m Ω DCR	4 x 4 mm	XGL4020-222MEC	Coilcraft
1	0	0	R1	453k Ω	RES, 453 k Ω , 1%, 0.1 W	0603	Std	Std
0	1	0	R1	200k Ω	RES, 200 k Ω , 1%, 0.1 W	0603	Std	Std
0	0	1	R1	100k Ω	RES, 100 k Ω , 1%, 0.1 W	0603	Std	Std
2	2	2	R2, R3	100k Ω	RES, 100 k Ω , 1%, 0.1 W	0603	Std	Std
1	1	0	R4	16.9k Ω	RES, 16.9 k Ω , 1%, 0.1 W	0603	Std	Std
0	0	1	R4	7.15k Ω	RES, 7.15 k Ω , 1%, 0.1 W	0603	Std	Std
1	0	0	U1	TPS62901 ¹	3-V to 17-V, Low I _Q Buck Converter in 1.5 mm x 2 mm QFN Package	1.5 x 2 mm	TPS62901RPJR	Texas Instruments
0	1	0	U1	TPS62902 ¹	3-V to 17-V, Low I _Q Buck Converter in 1.5 mm x 2 mm QFN Package	1.5 x 2 mm	TPS62902RPJR	Texas Instruments
0	0	1	U1	TPS62903 ¹	3-V to 17-V, Low I _Q Buck Converter in 1.5 mm x 2 mm QFN Package	1.5 x 2 mm	TPS62903RPJR	Texas Instruments

1. The TPS6290xEVM-069 may be populated with TPS6290x (U1) devices that do not contain the correct top-side markings on the top of the device itself. These devices are still fully-tested TPS6290x devices.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2021) to Revision A (May 2021)	Page
• Updated user's guide title.....	2

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