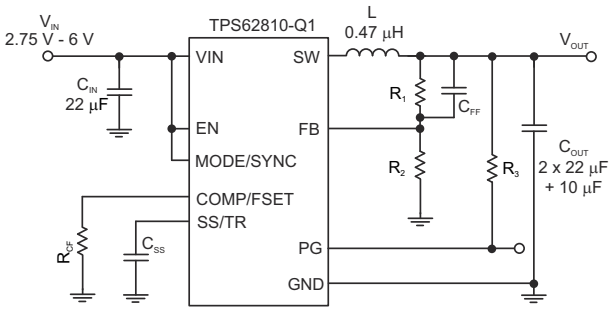
TPS6281x-Q1 2.75-V to 6-V Adjustable-Frequency Step-Down Converter

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 2.75 V to 6 V
- Family of 1 A, 2 A, 3 A and 4 A
- Quiescent current 15-µA typical
- Output voltage from 0.6 V to 5.5 V
- Output voltage accuracy ±1% (PWM operation)
- Adjustable soft start
- Forced PWM or PWM and PFM operation
- Adjustable switching frequency of 1.8 MHz to 4 MHz
- Precise ENABLE input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Spread spectrum clocking - optional
- Power-good output with window comparator
- Package with wettable flanks

2 Applications

- Infotainment head unit
- Hybrid and reconfigurable cluster
- Telematics control unit
- Surround view ECU, ADAS sensor fusion
- External amplifier



Simplified Schematic

3 Description

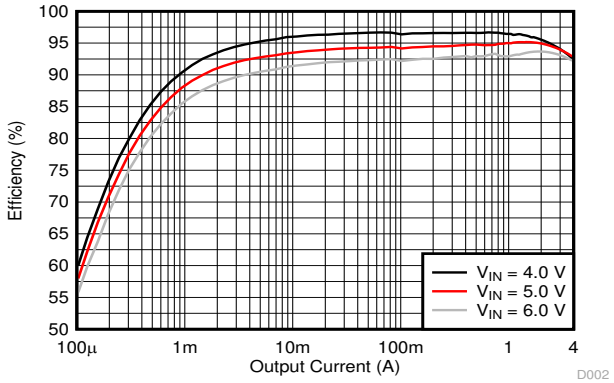
The TPS6281x-Q1 is family of pin-to-pin 1-A, 2-A, 3-A, and 4-A synchronous step-down DC/DC converters. All devices offer high efficiency and ease of use. The TPS6281x-Q1 family is based on a peak current mode control topology. The TPS6281x-Q1 is designed for automotive applications such as infotainment and advanced driver assistance systems. Low resistive switches allow up to 4-A continuous output current at high ambient temperature. The switching frequency is externally adjustable from 1.8 MHz to 4 MHz and can also be synchronized to an external clock in the same frequency range. In PWM/PFM mode, the TPS6281x-Q1 automatically enter power save mode at light loads to maintain high efficiency across the whole load range. The TPS6281x-Q1 provide 1% output voltage accuracy in PWM mode which helps design a power supply with high output voltage accuracy. The SS/TR pin allows setting the start-up time or forming tracking of the output voltage to an external source. This feature allows external sequencing of different supply rails and limiting the inrush current during start-up.

The TPS6281x-Q1 is available in a 3-mm × 2-mm VQFN package with wettable flanks.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS62810-Q1	RWY (VQFN, 9)	3.00 mm × 2.00 mm
TPS62811-Q1		
TPS62812-Q1		
TPS62813-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency vs Output Current; V_{OUT} = 3.3 V; PWM/PFM; f_S = 2.25 MHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (December 2021) to Revision J (March 2023)	Page
• Added planned device spins to *Device Comparison Table*	3

Changes from Revision H (April 2021) to Revision I (December 2021)	Page
• Added planned device spins to *Device Comparison Table*	3
• Added feedback voltage for fixed voltage version TPS628122A, TPS6281006	6

Changes from Revision G (March 2021) to Revision H (April 2021)	Page
• Added device version to *Device Comparison Table*	3

5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	Vout DISCHARGE	FOLDBACK CURRENT LIMIT	SPREAD SPECTRUM CLOCKING (SSC)	OUTPUT VOLTAGE
TPS62811QWRWYRQ1	1 A	ON	OFF	OFF	adjustable
TPS6281120QWRWYRQ1	1 A	ON	OFF	ON	adjustable
TPS6281126QWRWYRQ1	1 A	ON	OFF	ON	fixed 1.0 V
TPS6281109QWRWYRQ1	1 A	ON	OFF	OFF	fixed 1.15 V
TPS628110AQWRWYRQ1	1 A	ON	OFF	OFF	fixed 1.2 V
TPS628112AQWRWYRQ1	1 A	ON	OFF	ON	fixed 1.2 V
TPS628112MQWRWYRQ1	1 A	ON	OFF	ON	fixed 1.8 V
TPS628113HQWRWYRQ1	1 A	ON	OFF	ON	fixed 3.3 V
TPS62812QWRWYRQ1	2 A	ON	OFF	OFF	adjustable
TPS6281220QWRWYRQ1	2 A	ON	OFF	ON	adjustable
TPS6281240QWRWYRQ1	2 A	OFF	OFF	ON	adjustable
TPS6281206QWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.0 V
TPS6281208QWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.1 V
TPS6281228QWRWYRQ1	2 A	ON	OFF	ON	fixed 1.1 V
TPS628122AQWRWYRQ1	2A	ON	OFF	ON	fixed 1.2 V
TPS628122GQWRWYRQ1	2 A	ON	OFF	ON	fixed 1.5 V
TPS628120MQWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.8 V
TPS62813QWRWYRQ1	3 A	ON	OFF	OFF	adjustable
TPS6281320QWRWYRQ1	3 A	ON	OFF	ON	adjustable
TPS6281326QWRWYRQ1	3 A	ON	OFF	ON	fixed 1.0 V
TPS628132DQWRWYRQ1	3 A	ON	OFF	ON	fixed 1.35 V
TPS628132MQWRWYRQ1	3 A	ON	OFF	ON	fixed 1.8 V
TPS628130AQWRWYRQ1	3 A	ON	OFF	OFF	fixed 1.2 V
TPS6281302QWRWYRQ1	3 A	ON	OFF	OFF	fixed 0.8 V
TPS62810QWRWYRQ1	4 A	ON	OFF	OFF	adjustable
TPS6281020QWRWYRQ1	4 A	ON	OFF	ON	adjustable
TPS6281006QWRWYRQ1	4A	ON	OFF	OFF	fixed 1.0 V
TPS6281008QWRWYRQ1	4 A	ON	OFF	OFF	fixed 1.1 V
TPS628100MQWRWYRQ1	4 A	ON	OFF	OFF	fixed 1.8 V

6 Pin Configuration and Functions

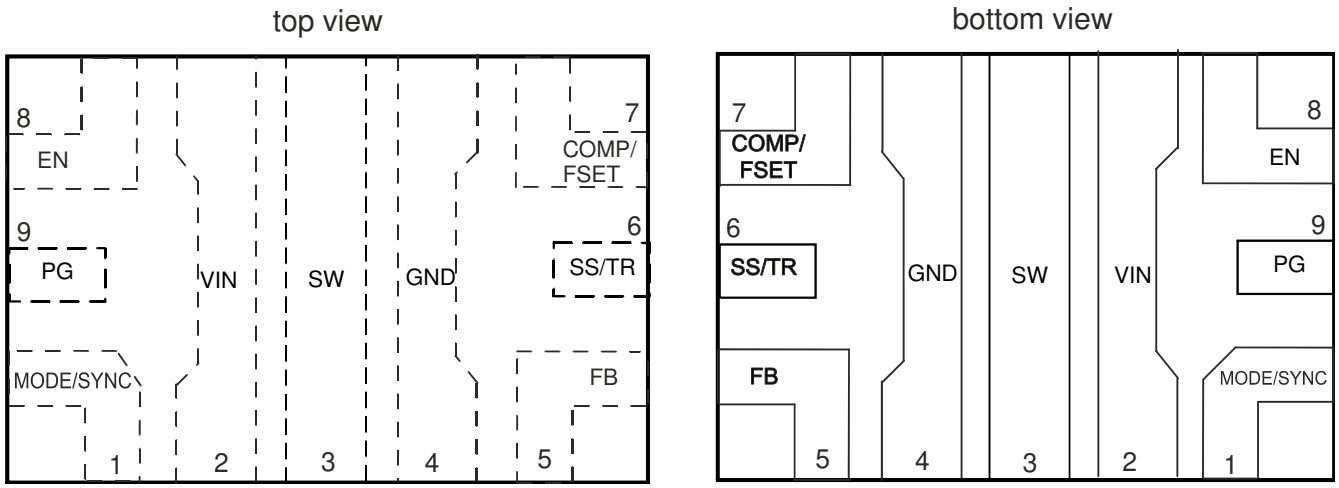


Figure 6-1. RWY Package 9 Pin (VQFN)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input, connect the resistive output voltage divider to this pin. For the fixed voltage versions, connect the FB pin directly to the output voltage.
GND	4		Ground pin
MODE/SYNC	1	I	The device runs in PFM/PWM mode when this pin is pulled low. If the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See the *Section 7* for the detailed specification of the digital signal applied to this pin for external synchronization.
COMP/FSET	7	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. If the pin is tied to GND or VIN, the switching frequency is set to 2.25 MHz. Do not leave this pin unconnected.
PG	9	O	Open drain power good output. Low impedance when not "power good", high impedance when "power good". This pin can be left open or be tied to GND when not used.
SS/TR	6	I	Soft-Start / Tracking pin. A capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing - see the *Soft Start / Tracking (SS/TR)* section.
SW	3		This pin is the switch pin of the converter and is connected to the internal Power MOSFETs.
VIN	2		Power supply input. Connect the input capacitor as close as possible between pin VIN and GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range(1)	VIN	–0.3	6.5	V
	SW	–0.3	V_{IN}+0.3	V
	SW (transient for less than 10 ns)(2)	–3	10	V
	FB	–0.3	4	V
	PG, SS/TR, COMP/FSET	–0.3	V_{IN}+0.3	V
Pin voltage range(1)	EN, MODE/SYNC	–0.3	6.5	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.75		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
L	Effective inductance for a switching frequency of 1.8 MHz to 3.5 MHz	0.32	0.47	0.9	µH
L	Effective inductance for a switching frequency of 3.5 MHz to 4 MHz	0.25	0.33	0.9	µH
C_{OUT}	Effective output capacitance for 1A and 2A version(1)	15	22	470	µF
C_{OUT}	Effective output capacitance for 3A and 4A version (1)	27	47	470	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
R_{CF}		4.5		100	kΩ
T_J	Operating junction temperature	–40		+150	°C

(1) The values given for the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6281x-Q1 RWY 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.1	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS6281x-Q1 RWY 9 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over operating junction temperature (T_J = -40 °C to +150 °C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current	EN = high, I_{OUT}= 0 mA, Device not switching, T_J= 125 °C			21	µA
I_Q	Operating Quiescent Current	EN = high, I_{OUT}= 0 mA, Device not switching		15	30	µA
I_{SD}	Shutdown Current	EN = 0 V, at T_J = 125°C			18	µA
I_{SD}	Shutdown Current	EN = 0 V, Nominal value at T_J= 25°C, Max value at T_J= 150 °C		1.5	26	µA
V_{UVLO}	Undervoltage Lockout Threshold	Rising Input Voltage	2.5	2.6	2.75	V
		Falling Input Voltage	2.25	2.5	2.6	V
T_{SD}	Thermal Shutdown Temperature	Rising Junction Temperature		170		°C
	Thermal Shutdown Hysteresis			15		
CONTROL (EN, SS/TR, PG, MODE/SYNC)						
V_{IH}	High Level Input Voltage for MODE/SYNC Pin		1.1			V
V_{IL}	Low Level Input Voltage for MODE/SYNC Pin				0.3	V
f_{SYNC}	Frequency Range on MODE/ SYNC Pin for Synchronization	requires a resistor from COMP/FSET to GND, see application section	1.8		4	MHz
	Duty Cycle of Synchronization Signal at MODE/SYNC Pin		20%	50%	80%	
	Time to Lock to External Frequency			50		µs
V_{IH}	Input Threshold Voltage for EN pin; Rising Edge		1.06	1.1	1.15	V
V_{IL}	Input Threshold Voltage for EN pin; Falling Edge		0.96	1.0	1.05	V
I_{LKG}	Input Leakage Current for EN, MODE/SYNC	V_{IH} = V_{IN} or V_{IL}= GND			150	nA
	Resistance from COMP/FSET to GND for Logic Low	internal frequency setting with f = 2.25 MHz	0		2.5	kΩ
	voltage on COMP/FSET for logic high	internal frequency setting with f = 2.25 MHz		VIN		V
V_{TH_PG}	UVP Power Good Threshold Voltage; dc Level	Rising (%V_{FB})	92%	95%	98%	
	UVP Power Good Threshold Voltage; dc Level	Falling (%V_{FB})	87%	90%	93%	
	OVP Power Good Threshold; dc Level	Rising (%V_{FB})	107%	110%	113%	
	OVP Power Good Threshold; dc Level	Falling (%V_{FB})	104%	107%	111%	
	Power Good De-glitch Time	for a high level to low level transition on power good		40		µs
V_{OL_PG}	Power Good Output Low Voltage	I_{PG} = 2 mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current (PG)	V_{PG} = 5 V			100	nA

7.5 Electrical Characteristics (continued)

over operating junction temperature (T_J = -40 °C to +150 °C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{SS/TR}$	SS/TR Pin Source Current			2.1	2.5	2.8	µA
	Tracking Gain	V_{FB} / $V_{SS/TR}$ for nominal V_{FB} = 0.6 V			1		
	Tracking Offset	feedback voltage with $V_{SS/TR}$ = 0 V for nominal V_{FB} = 0.6 V			17		mV
POWER SWITCH							
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN} ≥ 5 V			37	60	mΩ
$R_{DS(ON)}$	Low-Side MOSFET ON-Resistance	V_{IN} ≥ 5 V			15	35	mΩ
	High-Side MOSFET leakage current	V_{IN} = 6 V; V(SW) = 0 V				30	µA
	Low-Side MOSFET leakage current	V(SW) = 6 V				55	µA
	SW leakage	V(SW) = 0.6 V; current into SW pin		-0.025		30	µA
I_{LIMH}	High-Side MOSFET Current Limit	dc value, for TPS62810; V_{IN} = 3 V to 6 V		4.8	5.6	6.55	A
I_{LIMH}	High-Side MOSFET Current Limit	dc value, for TPS62813; V_{IN} = 3V to 6 V		3.9	4.5	5.25	A
I_{LIMH}	High-Side MOSFET Current Limit	dc value, for TPS62812; V_{IN} = 3 V to 6 V		2.8	3.4	4.2	A
I_{LIMH}	High-Side MOSFET Current Limit	dc value, for TPS62811; V_{IN} = 3 V to 6 V		2.0	2.6	3.25	A
I_{LIMNEG}	Negative Valley Current Limit	dc value			-1.8		A
f_S	PWM Switching Frequency Range			1.8	2.25	4	MHz
f_S	PWM Switching Frequency	with COMP/FSET tied to VIN or GND		2.025	2.25	2.475	MHz
	PWM Switching Frequency Tolerance	using a resistor from COMP/FSET to GND, fs = 1.8 MHz to 4 MHz		-19%		18%	
$t_{on,min}$	Minimum on-time of HS FET	T_J = –40°C to 125°C, V_{IN} = 3.3 V			50	75	ns
$t_{on,min}$	Minimum on-time of LS FET	V_{IN} = 3.3 V			30		ns
OUTPUT							
V_{FB}	Feedback Voltage	adjustable output voltage versions			0.6		V
V_{FB}	Feedback Voltage	fixed output voltage TPS6281302			0.8		V
V_{FB}	Feedback Voltage	fixed output voltage TPS6281206, TPS6281126, TPS6281326, TPS6281006			1.0		V
V_{FB}	Feedback Voltage	fixed output voltage TPS6281208, TPS6281008, TPS6281228			1.1		V
V_{FB}	Feedback Voltage	fixed output voltage TPS6281109			1.15		V
V_{FB}	Feedback Voltage	fixed output voltage TPS628110A, TPS628112A, TPS628122A, TPS628130A			1.2		V
V_{FB}	Feedback Voltage	fixed output voltage TPS628132D			1.35		V
V_{FB}	Feedback Voltage	fixed output voltage TPS628122G			1.5		V
V_{FB}	Feedback Voltage	fixed output voltage TPS628112M, TPS628120M, TPS628132D, TPS628100M, TPS628132M			1.8		V
V_{FB}	Feedback VoltageVoltage	fixed output voltage TPS628113H			3.3		V
I_{LKG_FB}	FB Input Leakage Current for Adjustable Voltage Versions	V_{FB} = 0.6 V			1	70	nA

7.5 Electrical Characteristics (continued)

over operating junction temperature (T_J = -40 °C to +150 °C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{LKG_FB}	FB Input Current for Fixed Voltage Versions	V_{FB} voltage at target output voltage			1		µA
V_{FB}	Feedback Voltage Accuracy for Adjustable Voltage Versions	$V_{IN} \geq V_{OUT}$ + 1 V	PWM mode	-1%		1%	
V_{FB}	Feedback Voltage Accuracy for Fixed Voltage Versions	$V_{IN} \geq V_{OUT}$ + 1 V	PWM mode, Tj = –40°C to 125°C	-1%		1%	
V_{FB}	Feedback Voltage Accuracy for Fixed Voltage Versions	$V_{IN} \geq V_{OUT}$ + 1 V	PWM mode	-1%		1.3%	
V_{FB}	Feedback Voltage Accuracy	$V_{IN} \geq V_{OUT}$ + 1 V; $V_{OUT} \geq$ 1.5 V	PFM mode; Co,eff ≥ 22 µF, L = 0.47 µH	-1%		2%	
V_{FB}	Feedback Voltage Accuracy	1 V ≤ V_{OUT} < 1.5 V	PFM mode; Co,eff ≥ 47 µF, L = 0.47 µH	-1%		2.5%	
V_{FB}	Feedback Voltage Accuracy with Voltage Tracking	$V_{IN} \geq V_{OUT}$ + 1 V; $V_{SS/TR}$ = 0.3 V	PWM mode	-1%		7%	
	Load Regulation	PWM mode operation			0.05		%/A
	Line Regulation	PWM mode operation, I_{OUT}= 1 A, $V_{IN} \geq V_{OUT}$ + 1 V			0.02		%/V
	Output Discharge Resistance					50	Ω
t_{delay}	Start-up Delay Time	I_{OUT} = 0 mA, Time from EN=high to start switching; V_{IN} applied already		135	250	470	µs
t_{ramp}	Ramp time; SS/TR Pin Open	I_{OUT} = 0 mA, Time from first switching pulse until 95% of nominal output voltage; device not in current limit		100	150	200	µs

7.6 Typical Characteristics

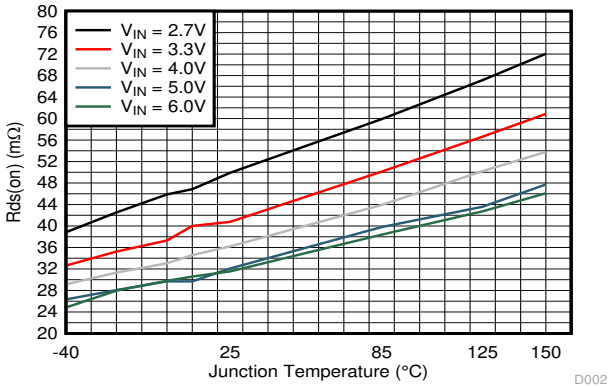


Figure 7-1. $R_{ds(on)}$ of High-side Switch

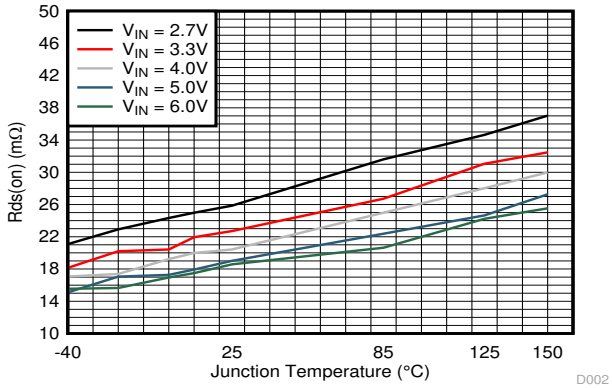


Figure 7-2. $R_{ds(on)}$ of Low-side Switch

8 Parameter Measurement Information

8.1 Schematic

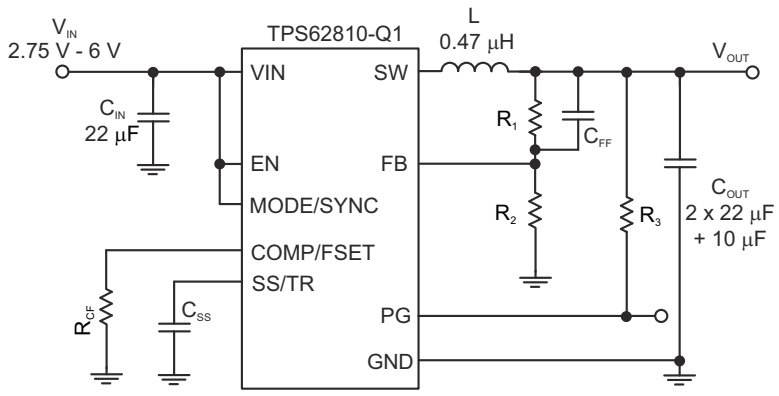


Figure 8-1. Measurement Setup for TPS62810-Q1 and TPS62813-Q1

Table 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPS62810-Q1 or TPS62813-Q1	Texas Instruments
L	0.47-µH inductor; XEL4030-471MEB	Coilcraft
C_{IN}	22 µF / 10 V; GCM31CR71A226KE02L	Murata
C_{OUT}	2 × 22 µF / 10 V; GCM31CR71A226KE02L + 1 x×10 µF 6.3 V; GCM188D70J106ME36	Murata
C_{SS}	4.7 nF (equal to 1-ms start-up ramp)	Any
R_{CF}	8.06 kΩ	Any
C_{FF}	10 pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

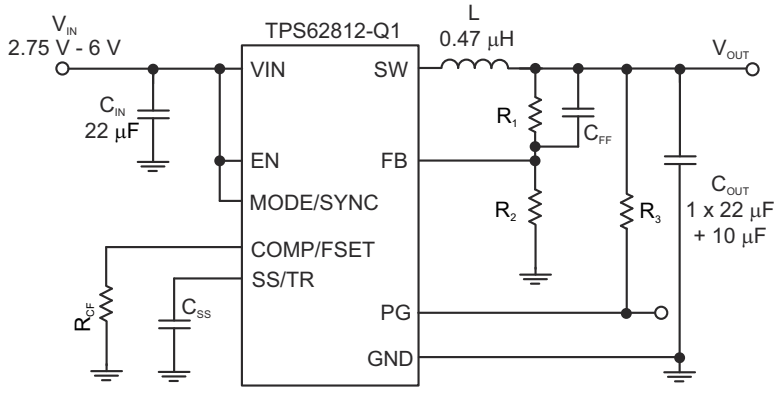


Figure 8-2. Measurement Setup for TPS62812-Q1 and TPS62811-Q1

Table 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPS62812-Q1 or TPS62811-Q1	Texas Instruments
L	0.56-µH inductor; XEL4020-561MEB	Coilcraft
C_{IN}	22 µF / 10 V; GCM31CR71A226KE02L	Murata
C_{OUT}	1 × 22 µF / 10 V; GCM31CR71A226KE02L + 1 × 10 µF 6.3 V; GCM188D70J106ME36	Murata
C_{SS}	4.7 nF (equal to 1-ms start-up ramp)	Any
R_{CF}	8.06 kΩ	Any
C_{FF}	10 pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

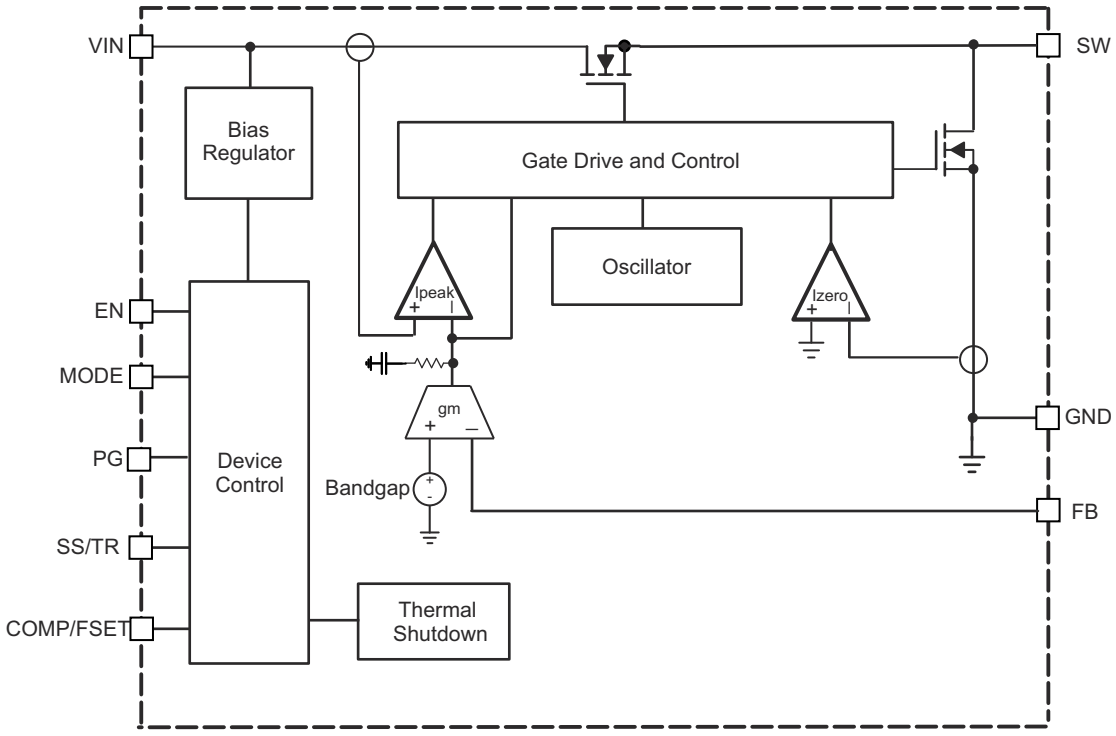
9 Detailed Description

9.1 Overview

The TPS6281x-Q1 synchronous switch mode DC/DC converters are based on a peak current mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with TPS6281x-Q1, one of three internal compensation settings can be selected. See *Section 9.3.2*. The compensation setting is selected either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low ESR ceramic output capacitors. The device can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN, or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. External synchronization is only possible if a resistor from COMP/FSET to GND is used. If COMP/FSET is directly tied to GND or VIN, the TPS6281x-Q1 cannot be synchronized externally. An internal PLL allows to change from internal clock to external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Precise Enable

The voltage applied at the Enable pin of the TPS6281x-Q1 is compared to a fixed threshold of 1.1 V for a rising voltage. This allows to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS6281x-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 1 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

9.3.2 COMP/FSET

This pin allows to set two different parameters independently:

- Internal compensation settings for the control loop
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows you to adapt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency / compensation. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on-time and minimum off-time.

For example: V_{IN} = 5 V, V_{OUT} = 1 V --> duty cycle (DC) = 1 V / 5 V = 0.2

- with t_{on} = DC × T --> $t_{on,min}$ = 1 / $f_{s,max}$ × DC
- --> $f_{s,max}$ = 1 / $t_{on,min}$ × DC = 1 / 0.075 µs · 0.2 = 2.67 MHz

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1 and Table 9-2, up to the maximum of 470 µF in all of the three compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1:

$$R_{CF}(k\Omega) = \frac{18MHz \cdot k\Omega}{f_S(MHz)} \quad (1)$$

For compensation (comp) setting 2:

$$R_{CF}(k\Omega) = \frac{60MHz \cdot k\Omega}{f_S(MHz)} \quad (2)$$

For compensation (comp) setting 3:

$$R_{CF}(k\Omega) = \frac{180MHz \cdot k\Omega}{f_S(MHz)} \quad (3)$$

Table 9-1. Switching Frequency and Compensation for TPS62810-Q1 (4 A) and TPS62813-Q1 (3 A)

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ VOUT < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3 V
for smallest output capacitance (comp setting 1)	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to Equation 1	53 µF	32 µF	27 µF
for medium output capacitance (comp setting 2)	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to Equation 2	100 µF	60 µF	50 µF
for large output capacitance (comp setting 3)	100 kΩ ... 45 kΩ	1.8 MHz (100 kΩ) ... 4 MHz (45 kΩ) according to Equation 3	200 µF	120 µF	100 µF
for smallest output capacitance (comp setting 1)	tied to GND	internally fixed 2.25 MHz	53 µF	32 µF	27 µF
for large output capacitance (comp setting 3)	tied to V_{IN}	internally fixed 2.25 MHz	200 µF	120 µF	100 µF

Table 9-2. Switching Frequency and Compensation for TPS62812-Q1 (2 A) and TPS62811-Q1 (1 A)

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ VOUT < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3 V
for smallest output capacitance (comp setting 1)	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to Equation 1	30 µF	18 µF	15 µF
for medium output capacitance (comp setting 2)	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to Equation 2	60 µF	36 µF	30 µF
for large output capacitance (comp setting 3)	100 kΩ ... 45 kΩ	1.8MHz (100 kΩ) ...4 MHz (45 kΩ) according to Equation 3	130 µF	80 µF	68 µF
for smallest output capacitance (comp setting 1)	tied to GND	internally fixed 2.25 MHz	30 µF	18 µF	15 µF
for large output capacitance (comp setting 3)	tied to V_{IN}	internally fixed 2.25 MHz	130 µF	80 µF	68 µF

Refer to *Section 10.1.3.2* for further details on the output capacitance required depending on the output voltage.

A too high resistor value for R_{CF} is decoded as "tied to V_{IN}", a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in Table 9-1 and Table 9-2 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required. All values are effective capacitance, including all tolerances, aging, dc bias effect, and so forth.

9.3.3 MODE / SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows to force PWM mode when set high. The pin also allows you to apply an external

clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. Similar to COMP/FSET, the specifications for the minimum on-time and minimum off-time have to be taken into account when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by R_{CF} to a similar value than the externally applied clock. This ensures a fast settling to the external clock and, if the external clock fails, the switching frequency stays in the same range and the compensation settings are still valid. When there is no resistor from COMP/FSET to GND but the pin is pulled high or low, external synchronization is not possible.

9.3.4 Spread Spectrum Clocking (SSC)

For device versions with SSC enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS6281x-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.6 Power Good Output (PG)

Power good is an open-drain output driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout, and in thermal shutdown. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

Table 9-3. PG Status

EN	DEVICE STATUS	PG STATE
X	V_{IN} < 2 V	undefined
low	V_{IN} ≥ 2 V	low
high	2 V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} not in regulation	low
high	V_{OUT} in regulation	high impedance

9.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases by the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9 µs to detect a too high junction temperature. If the PFM burst is shorter than this delay, the device does not detect a too high junction temperature.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

TPS6281x-Q1 has two operating modes: Forced PWM mode (discussed in this section) and PWM/PFM (discussed in *Section 9.4.2*).

With the MODE/SYNC pin set to high, the TPS6281x-Q1 operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock is applied to MODE/SYNC, the TPS6281x-Q1 follows the frequency applied to the pin. To maintain regulation, the frequency must be in a range the TPS6281x-Q1 can operate at, taking the minimum on-time into account.

9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.2 A. When the peak inductor current

drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = VOUT / VIN. The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 30 ns is reached, the TPS6281x-Q1 skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

9.4.4 Current Limit and Short Circuit Protection

The TPS6281x-Q1 is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low-side switch has decreased below the low-side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

- I_{LIMH} is the static current limit as specified in the electrical characteristics
- L is the effective inductance at the peak current
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \quad (5)$$

9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to typically 1.8 A. Foldback current limit is left when the current limit indication goes away. For the case that device operation continues in current limit, it can, after 3072 switching cycles, try again full current limit for again 1024 switching cycles.

9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after TPS6281x-Q1 has been enabled at least once because the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

9.4.7 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after

a delay of about 200 µs then the internal reference and hence V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving the SS/TR pin un-connected provides the fastest startup ramp with 150 µs typically. A capacitor connected from SS/TR to GND is charged with 2.5 µA by an internal current source during soft start until it reaches the reference voltage of 0.6 V. The capacitance required to set a certain ramp-time (t_{ramp}) therefore is:

$$C_{SS}\left[nF\right] = \frac{2.5\mu A \cdot t_{ramp}\left[ms\right]}{0.6V} \tag{6}$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to ensure a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin must not be connected to the SS/TR pin of other devices. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6 V). TI recommends to set the target for the external voltage on SS/TR slightly above the feedback voltage. Given the tolerances of the resistor divider R_5 and R_6 on SS/TR, this ensures the device "switches" to the internal reference voltage when the power-up sequencing is finished. See Figure 10-58.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS6281x-Q1 is adjustable. The output voltage can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 7. TI recommends to choose resistor values which allow a current of at least 2 µA, meaning the value of R_2 must not exceed 400 kΩ. TI recommends lower resistor values for highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{7}$$

10.1.2 External Component Selection

10.1.2.1 Inductor Selection

The TPS6281x-Q1 is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See *Recommended Operating Conditions* for details.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 8 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{8}$$

$$\Delta I_{L(\max)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{L \min} \cdot \frac{1}{f_{SW}} \tag{9}$$

where

- $I_{L(max)}$ is the maximum inductor current
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current
- Lmin is the minimum inductance at the operating point

Table 10-1. Typical Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A] (1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxBxH] mm	MANUFACTURER (2)
XFL4015-471ME	0.47 µH, ±20%	3.5	TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 ×1.6	Coilcraft

Table 10-1. Typical Inductors (continued)

TYPE	INDUCTANCE [µH]	CURRENT [A] (1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxBxH] mm	MANUFACTURER(2)
XEL4020-561ME	0.56 µH, ±20%	9.9	TPS62810-Q1, TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 × 2.1	Coilcraft
XEL4030-471ME	0.47 µH, ±20%	12.3	TPS62810-Q1, TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 × 3.1	Coilcraft
XEL3515-561ME	0.56 µH, ±20%	4.5	TPS62813-Q1, TPS62812-Q1	2.25 MHz	3.5 × 3.2 × 1.5	Coilcraft
XFL3012-331MEB	0.33 µH, ±20%	2.6	TPS62811-Q1 TPS62812-Q1	≥ 3.5 MHz	3 × 3 × 1.3	Coilcraft
XPL2010-681ML	0.68 µH, ±20%	1.5	TPS62811-Q1	2.25 MHz	2 x 1.9 x 1	Coilcraft
DFE252012PD-R47M	0.47 µH, ±20%	see data sheet	TPS62812-Q1, TPS62813-Q1	2.25 MHz	2.5 × 2 × 1.2	Murata

(1) Lower of I_{RMS} at 20°C rise or I_{SAT} at 20% drop.
(2) See the *Third-party Products Disclaimer*.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends a margin of about 20% to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

10.1.3 Capacitor Selection

10.1.3.1 Input Capacitor

For most applications, 22 µF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

10.1.3.2 Output Capacitor

The architecture of the TPS6281x-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use dielectric X7R, X7T, or an equivalent. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 470 µF in any of the compensation settings.

The minimum capacitance required on the output depends on the compensation setting as well as on the current rating of the device. TPS62810-Q1 and TPS62813-Q1 require a minimum output capacitance of 27 µF while the lower current versionsTPS62812-Q1and TPS62811-Q1 requires 15 µF at minimum. The required output capacitance also changes with the output voltage.

For output voltages below 1 V, the minimum increases linearly from 32 µF at 1 V to 53 µF at 0.6 V for the TPS62810-Q1, the TPS62813-Q1 with the compensation setting for smallest output capacitance. Other compensation ranges for TPS62811-Q1 and TPS62812-Q1 , or both are equivalent. See Table 9-1 and Table 9-2 for details.

10.2 Typical Application

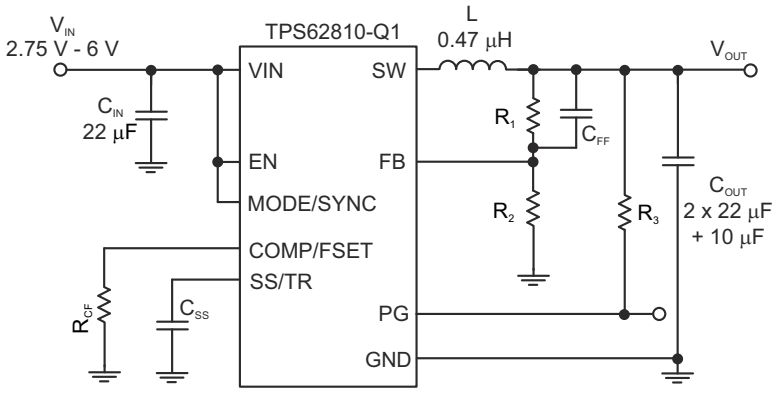


Figure 10-1. Typical Application

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{10}$$

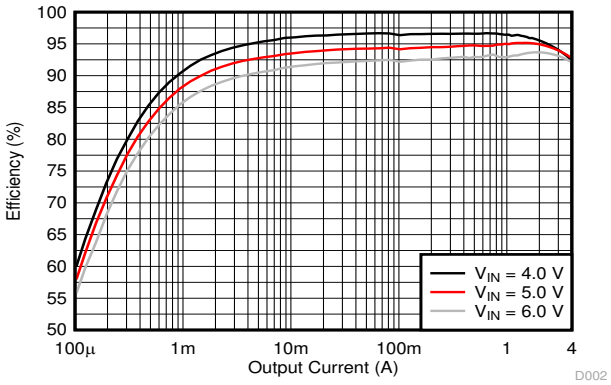
With V_{FB} = 0.6 V:

Table 10-2. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	10 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	10 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	10 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	10 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	10 pF	3.315 V

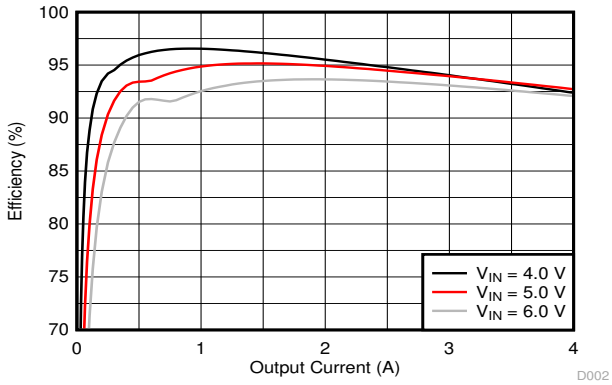
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to Table 8-1.



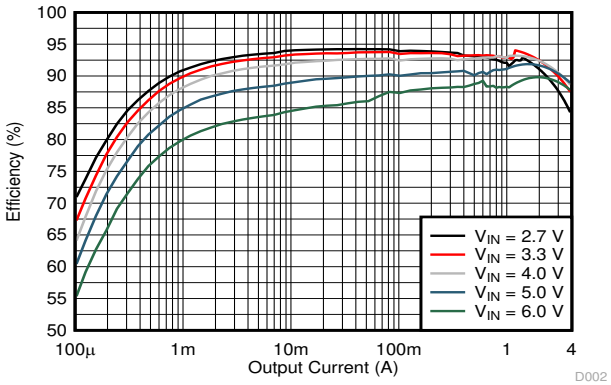
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-2. Efficiency versus Output Current



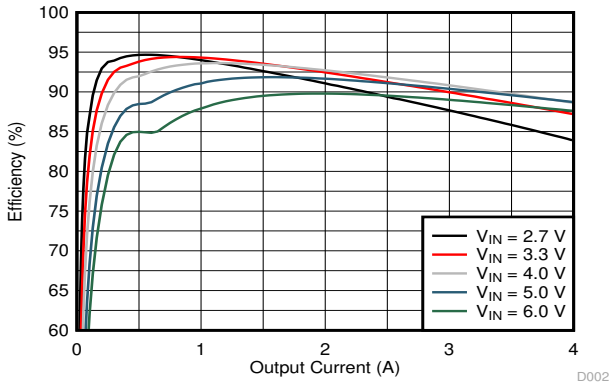
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-3. Efficiency versus Output Current



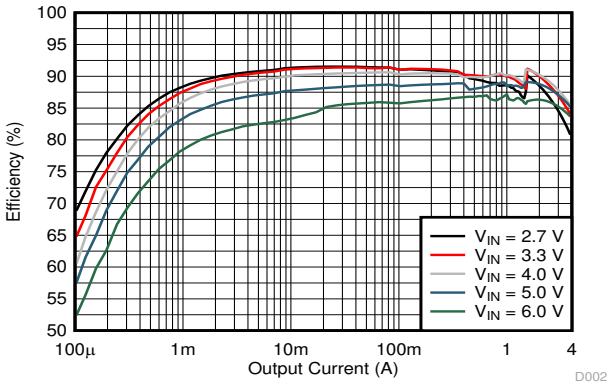
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-4. Efficiency versus Output Current



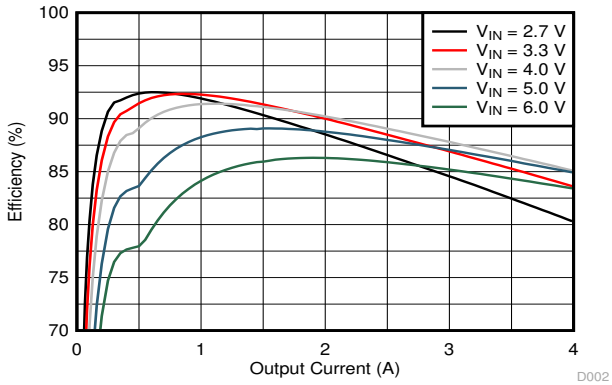
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-5. Efficiency versus Output Current



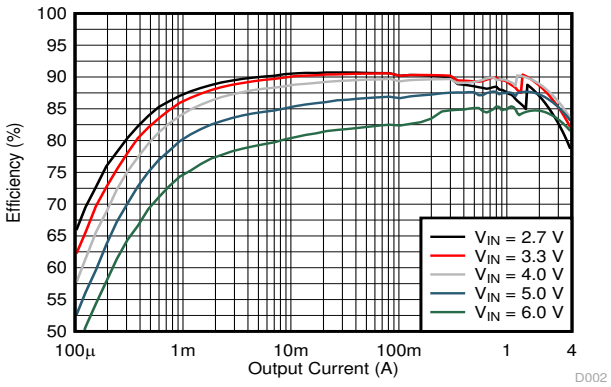
V_{OUT} = 1.2 V PFM T_A = 25°C

Figure 10-6. Efficiency versus Output Current



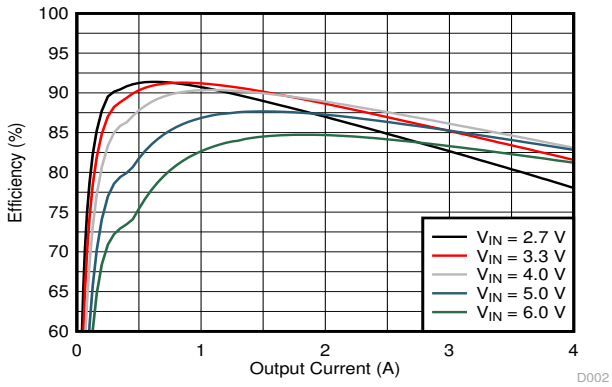
V_{OUT} = 1.2 V PWM T_A = 25°C

Figure 10-7. Efficiency versus Output Current



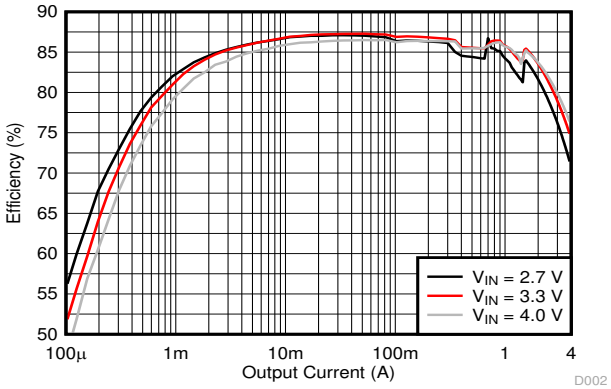
V_{OUT} = 1.0 V PFM T_A = 25°C

Figure 10-8. Efficiency versus Output Current



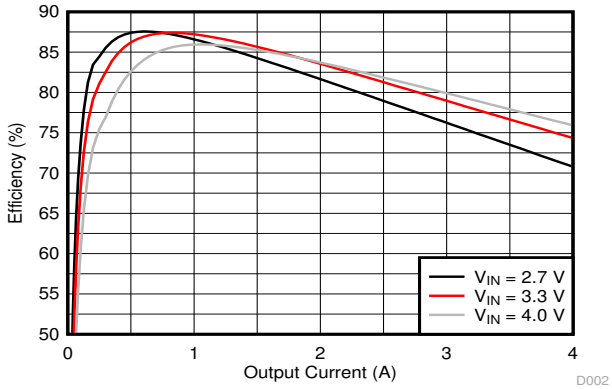
V_{OUT} = 1.0 V PWM T_A = 25°C

Figure 10-9. Efficiency versus Output Current



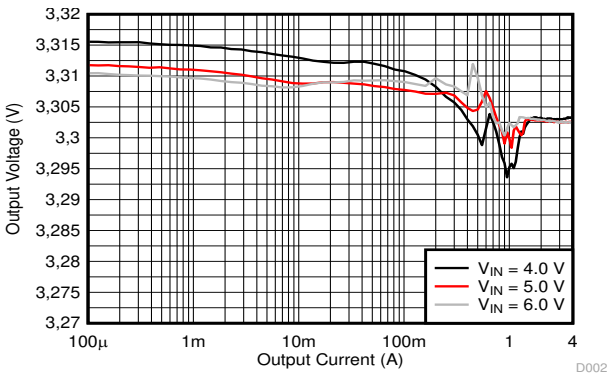
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-10. Efficiency versus Output Current



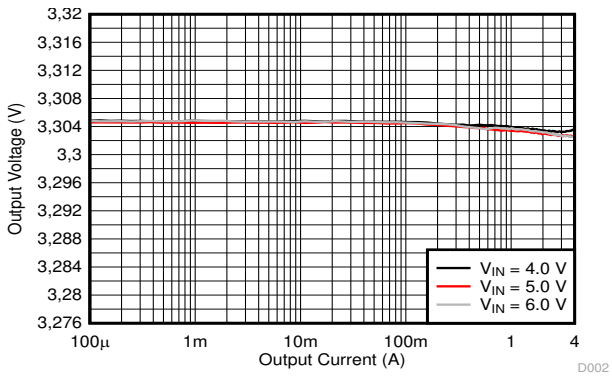
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-11. Efficiency versus Output Current



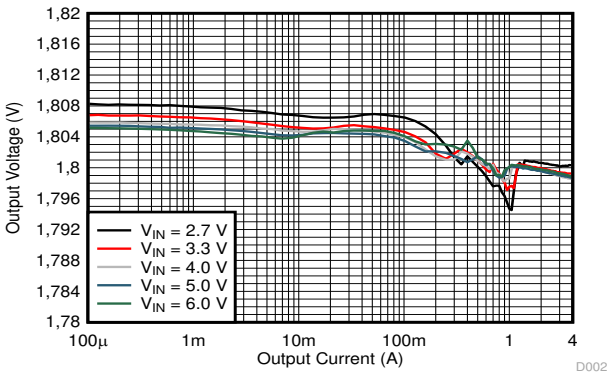
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-12. Output Voltage versus Output Current



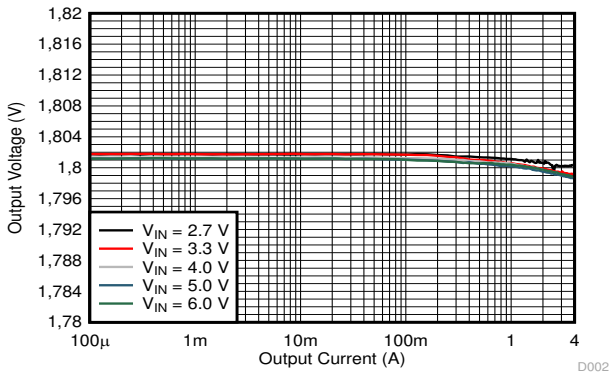
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-13. Output Voltage versus Output Current



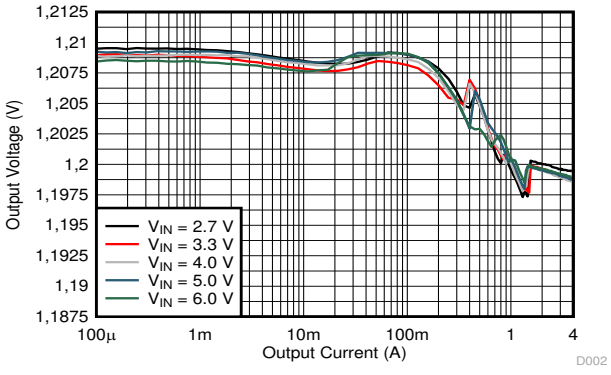
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-14. Output Voltage versus Output Current



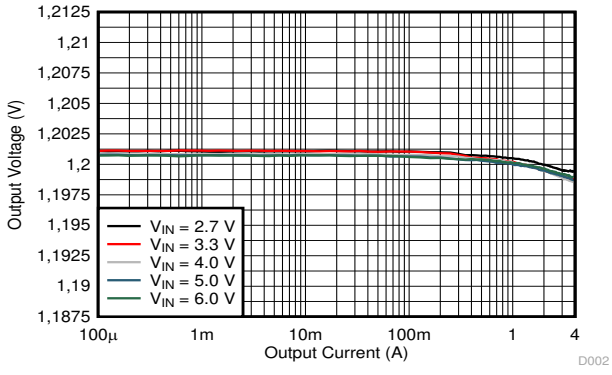
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-15. Output Voltage versus Output Current



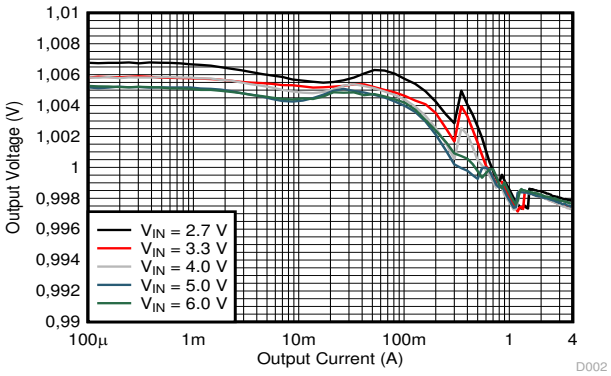
V_{OUT} = 1.2 V PFM T_A = 25°C

Figure 10-16. Output Voltage versus Output Current



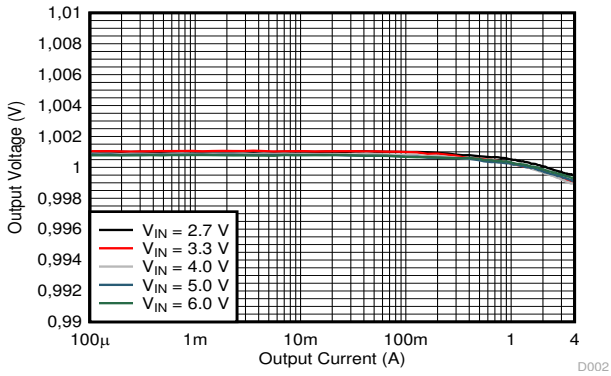
V_{OUT} = 1.2 V PWM T_A = 25°C

Figure 10-17. Output Voltage versus Output Current



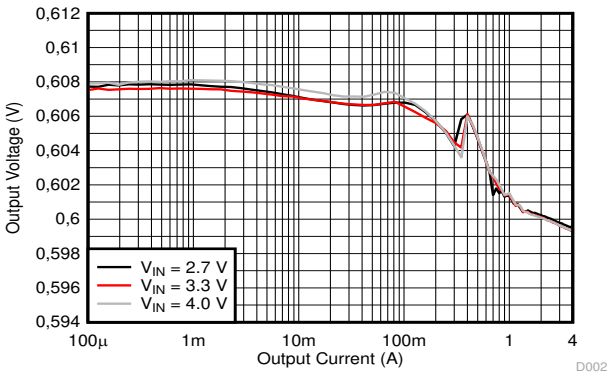
V_{OUT} = 1.0 V PFM T_A = 25°C

Figure 10-18. Output Voltage versus Output Current



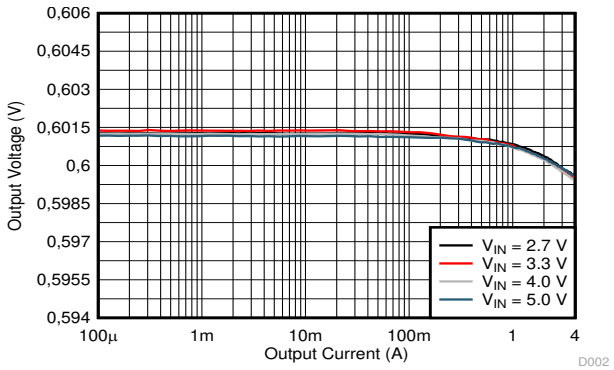
V_{OUT} = 1.0 V PWM T_A = 25°C

Figure 10-19. Output Voltage versus Output Current



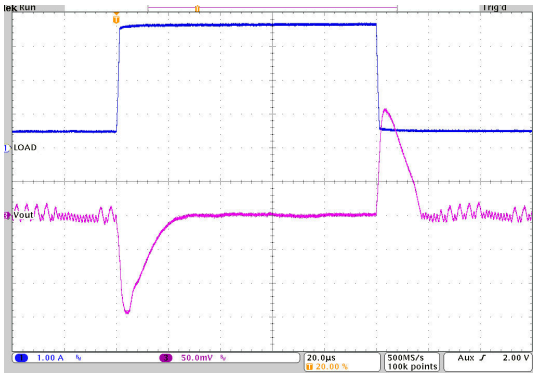
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-20. Output Voltage versus Output Current



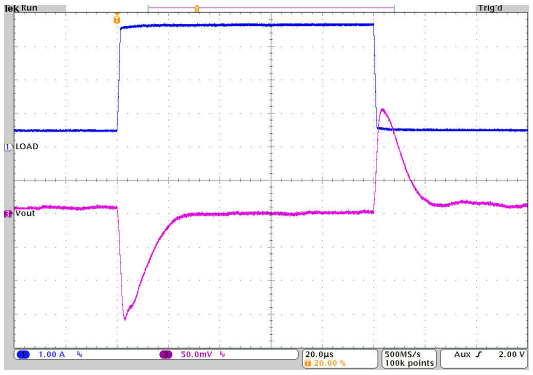
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-21. Output Voltage versus Output Current



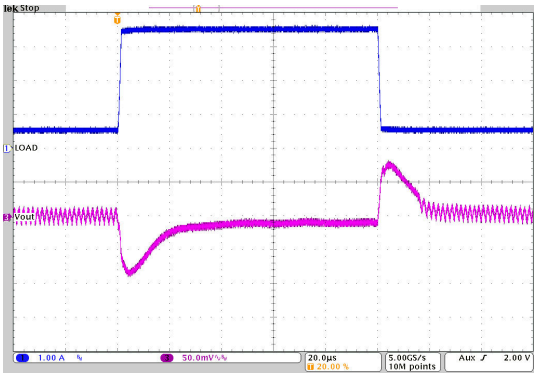
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-22. Load Transient Response



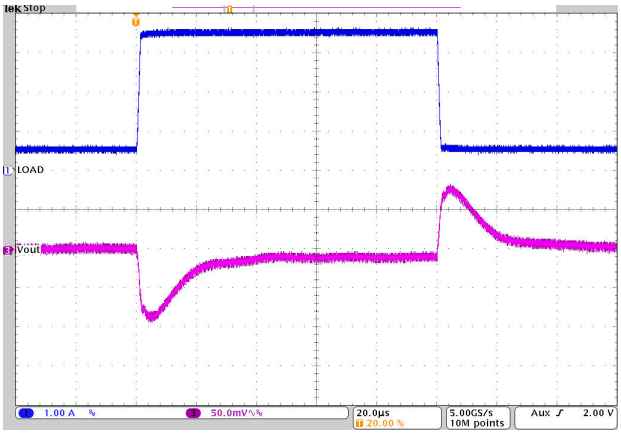
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-23. Load Transient Response



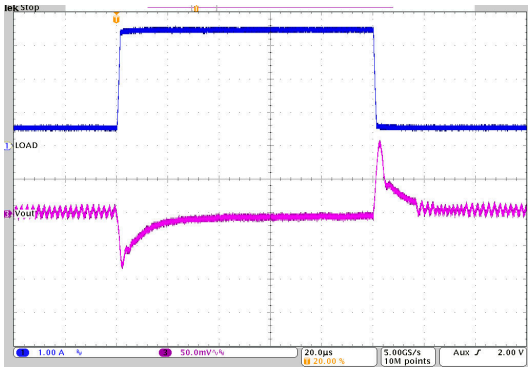
V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-24. Load Transient Response



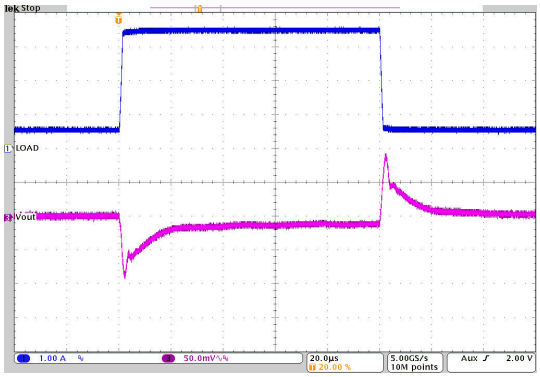
V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-25. Load Transient Response



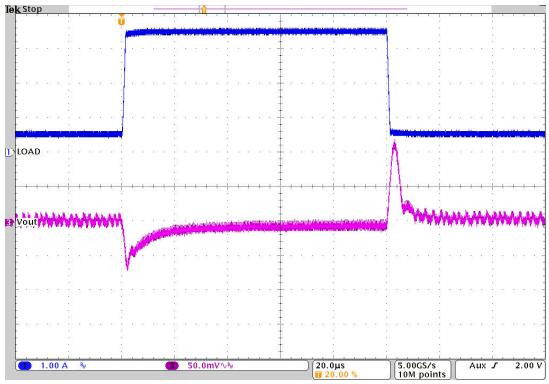
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-26. Load Transient Response



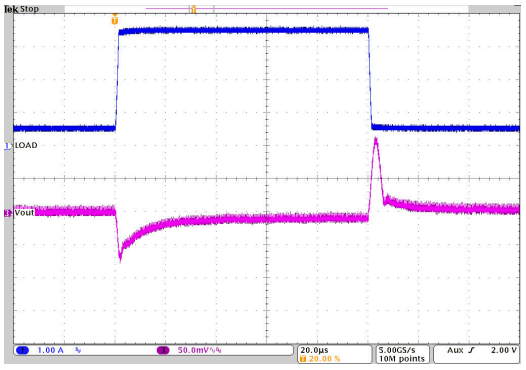
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-27. Load Transient Response



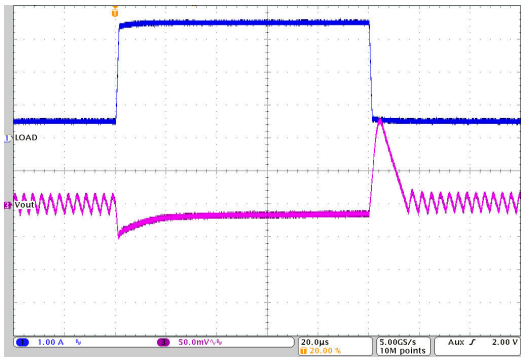
V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-28. Load Transient Response



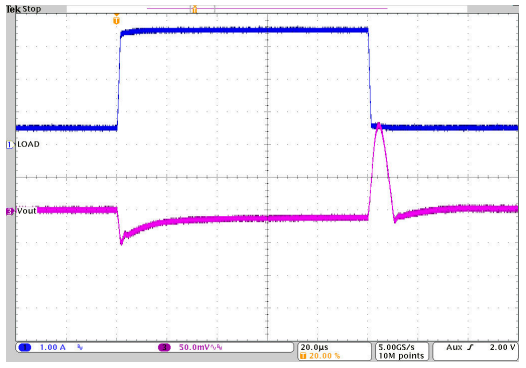
V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-29. Load Transient Response



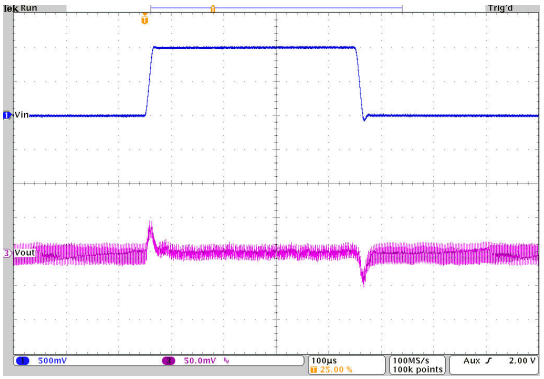
V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-30. Load Transient Response



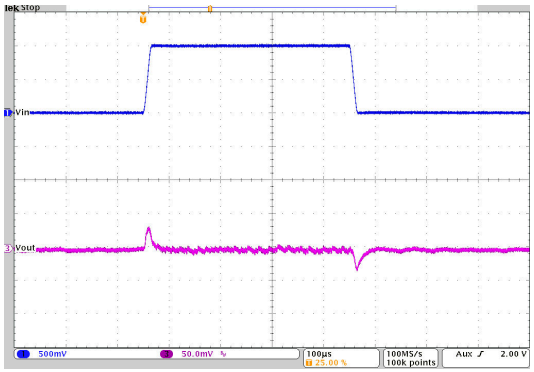
V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.4 A to 3.6 A to 0.4 A

Figure 10-31. Load Transient Response



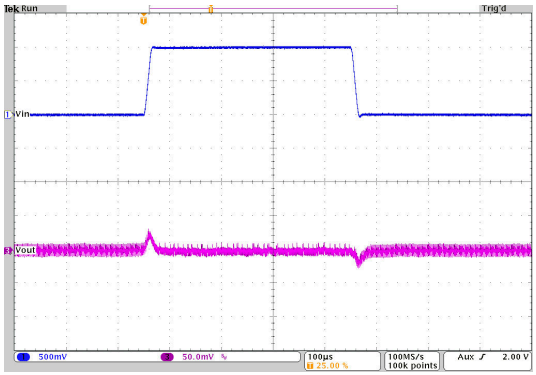
V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-32. Line Transient Response



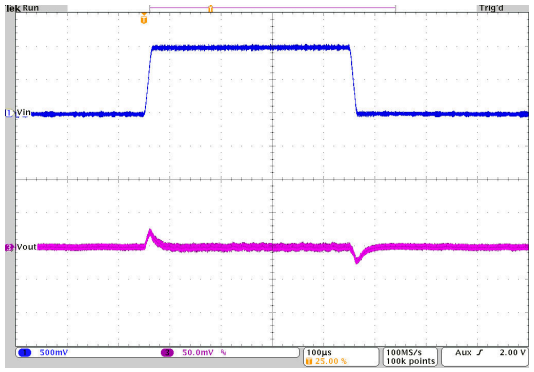
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-33. Line Transient Response



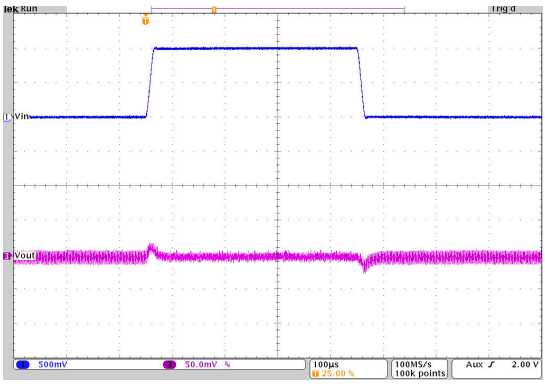
V_{OUT} = 1.8 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-34. Line Transient Response



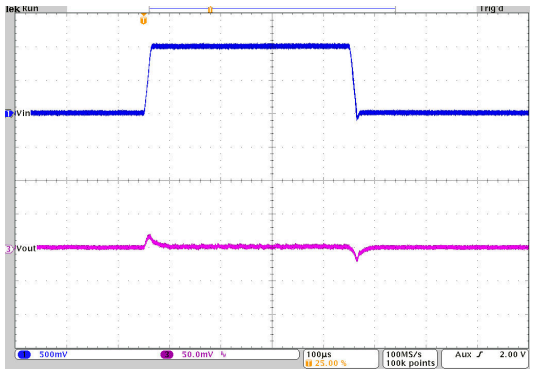
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-35. Line Transient Response



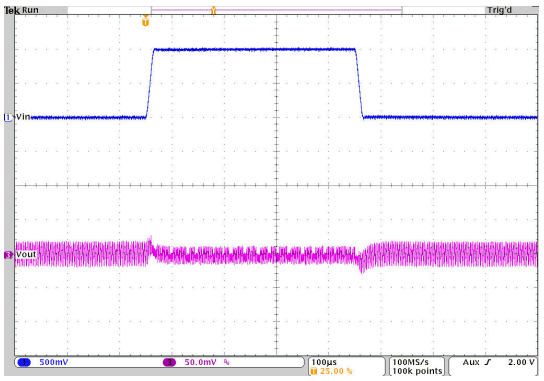
V_{OUT} = 1.2 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-36. Line Transient Response



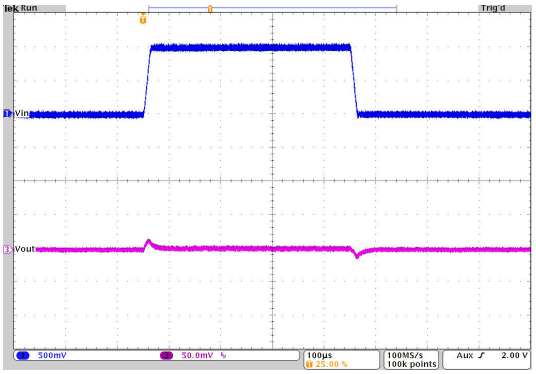
V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-37. Line Transient Response



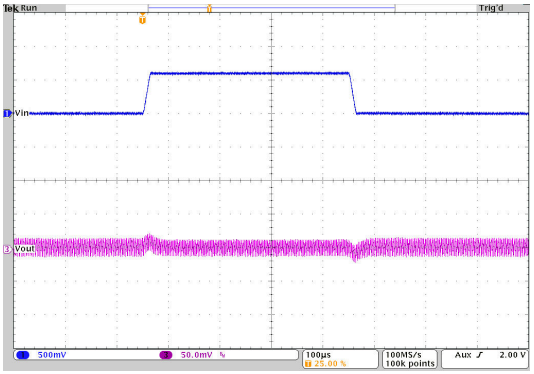
V_{OUT} = 1.0 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-38. Line Transient Response



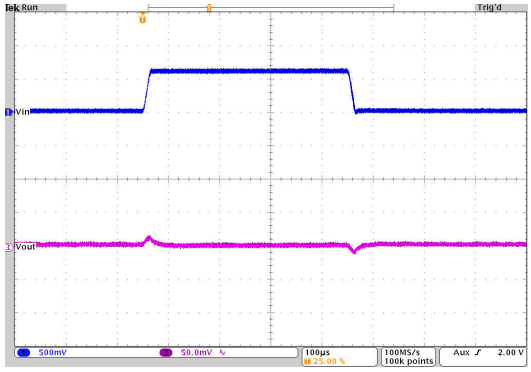
V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-39. Line Transient Response



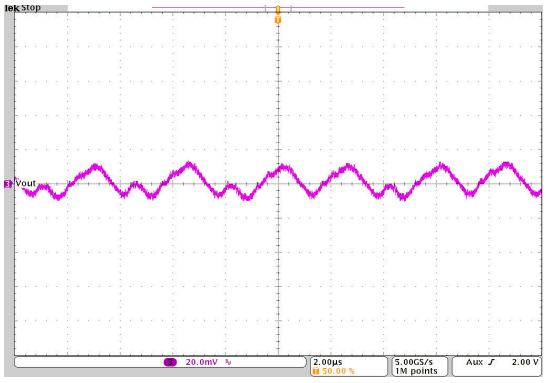
V_{OUT} = 0.6 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-40. Line Transient Response



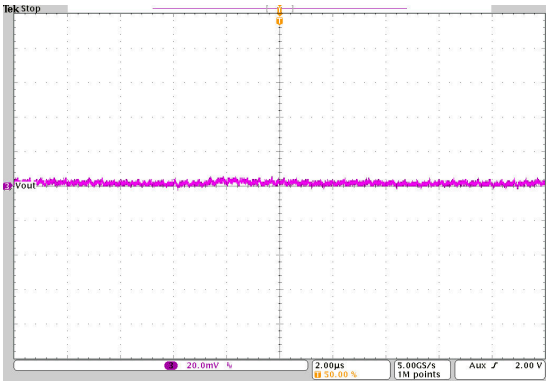
V_{OUT} = 0.6 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-41. Line Transient Response



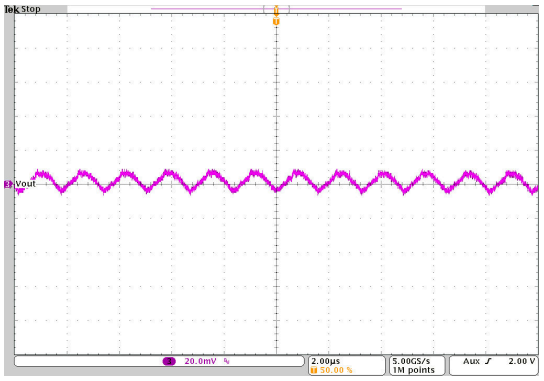
V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-42. Output Voltage Ripple



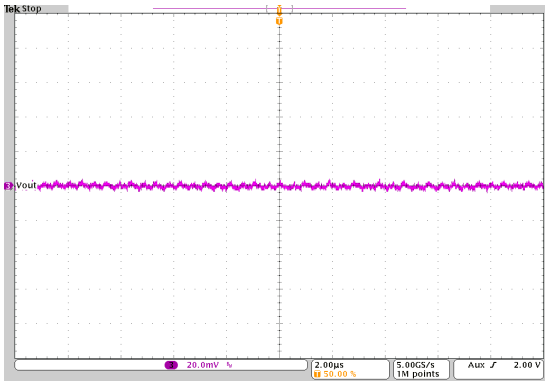
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-43. Output Voltage Ripple



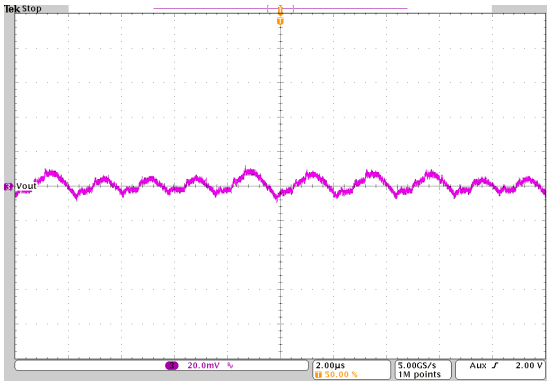
V_{OUT} = 1.8 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-44. Output Voltage Ripple



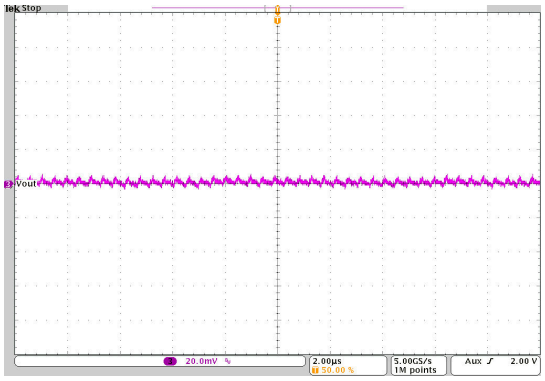
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-45. Output Voltage Ripple



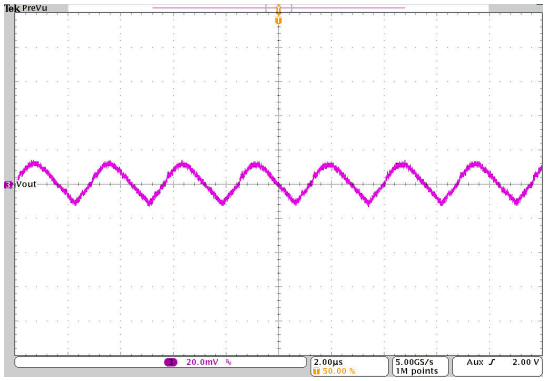
V_{OUT} = 1.2 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-46. Output Voltage Ripple



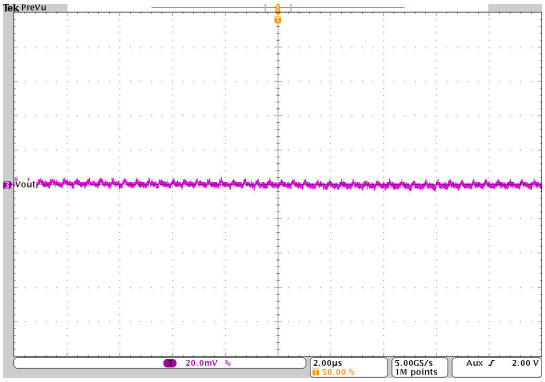
V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-47. Output Voltage Ripple



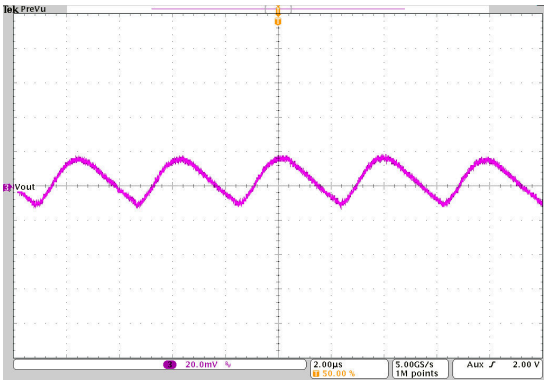
V_{OUT} = 1.0 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-48. Output Voltage Ripple



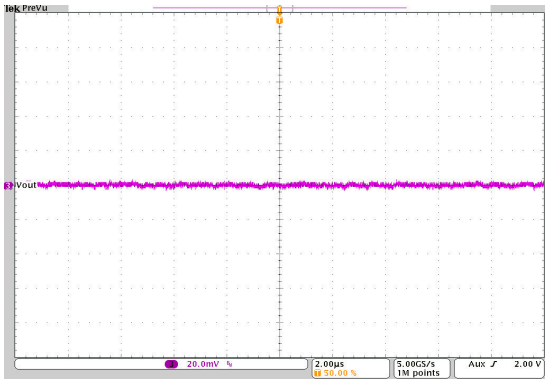
V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-49. Output Voltage Ripple



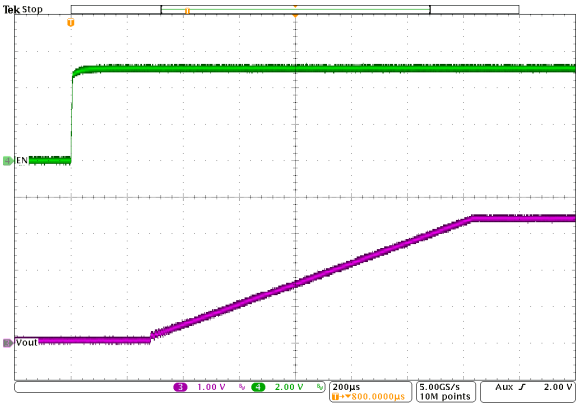
V_{OUT} = 0.6 V PFM T_A = 25°C
I_{OUT} = 0.5 A V_{IN} = 3.3 V BW = 20 MHz

Figure 10-50. Output Voltage Ripple



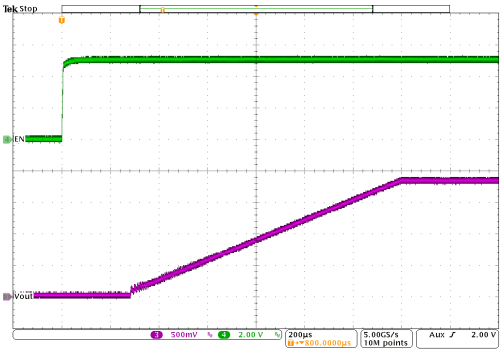
V_{OUT} = 0.6 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 3.3 V BW = 20 MHz

Figure 10-51. Output Voltage Ripple



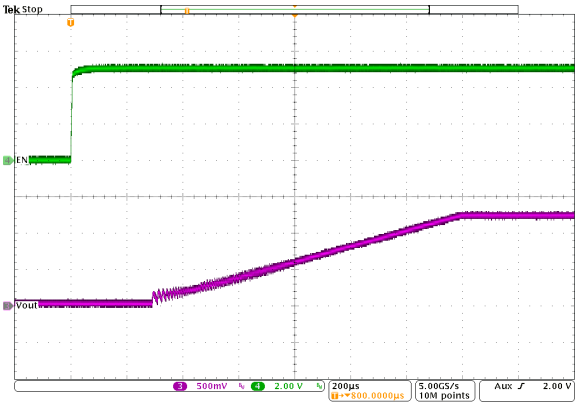
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5 V C_{SS} = 4.7 nF

Figure 10-52. Start-Up Timing



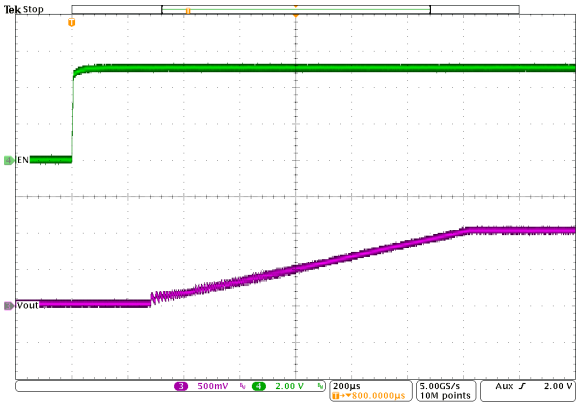
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5 V C_{SS} = 4.7 nF

Figure 10-53. Start-Up Timing



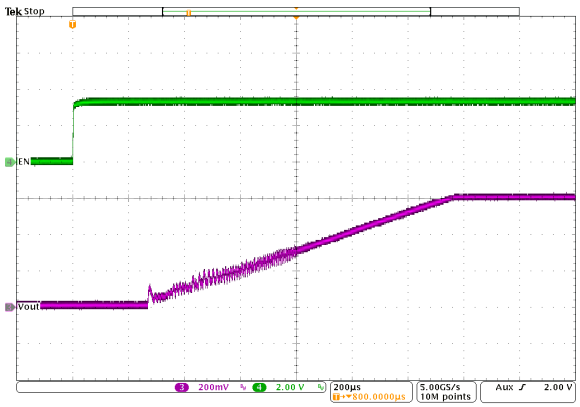
V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5 V C_{SS} = 4.7 nF

Figure 10-54. Start-Up Timing



V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5 V C_{SS} = 4.7 nF

Figure 10-55. Start-Up Timing



V_{OUT} = 0.6 V	PWM	T_A = 25°C
I_{OUT} = 4 A	V_{IN} = 3.3 V	C_{SS} = 4.7 nF

Figure 10-56. Start-up Timing

10.3 System Examples

10.3.1 Fixed Output Voltage Versions

Versions with an internally fixed output voltage allow you to remove the external feedback voltage divider. This not only allows you to reduce the total solution size but also provides higher accuracy as there is no additional error caused by the external resistor divider. The FB pin must be tied to the output voltage directly as shown in Figure 10-57. Independent of that, the application shown runs with an internally defined switching frequency of 2.25 MHz by connecting COMP/FSET to GND.

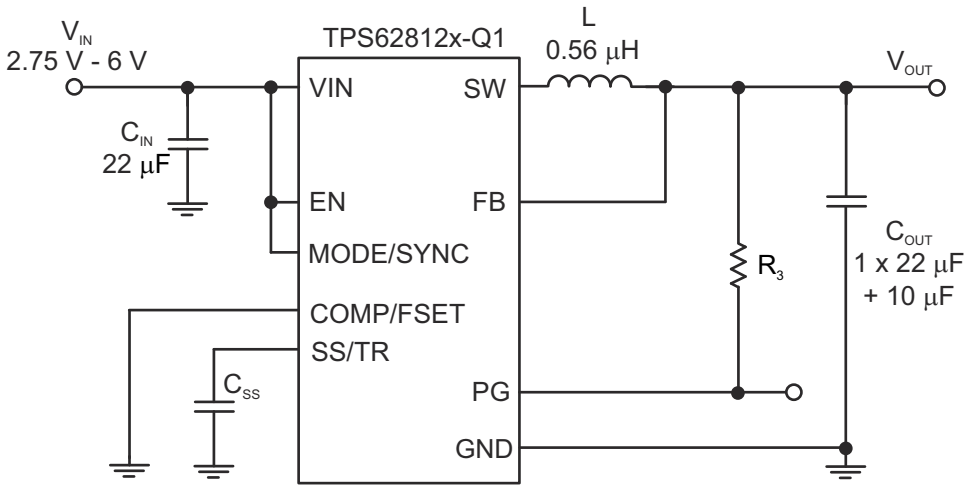


Figure 10-57. Schematic for Fixed Output Voltage Versions

10.3.2 Voltage Tracking

The TPS6281x-Q1 follows the voltage applied to the SS/TR pin. A voltage ramp on SS/TR to 0.6 V ramps the output voltage according to the 0.6 V feedback voltage.

Tracking the 3.3 V of device 1, such that both rails reach their target voltage at the same time, requires a resistor divider on SS/TR of device 2 equal to the output voltage divider of device 1. The output current of 2.5 µA on the SS/TR pin causes an offset voltage on the resistor divider formed by R_5 and R_6. The equivalent resistance of R_5 // R_6, so it must be kept below 15 kΩ. The current from SS/TR causes a slightly higher voltage across R6 than 0.6 V, which is desired because device 2 switches to its internal reference as soon as the voltage at SS/TR is higher than 0.6 V.

In case both devices must run in forced PWM mode, TI recommends to tie the MODE pin of device 2 to the output voltage or the power good signal of device 1, the master device. The TPS6281x-Q1 has a duty cycle limitation defined by the minimum on-time. For tracking down to low output voltages, device 2 cannot follow after the minimum duty cycle is reached. Enabling PFM mode while tracking is in progress allows you to ramp down the output voltage close to 0 V.

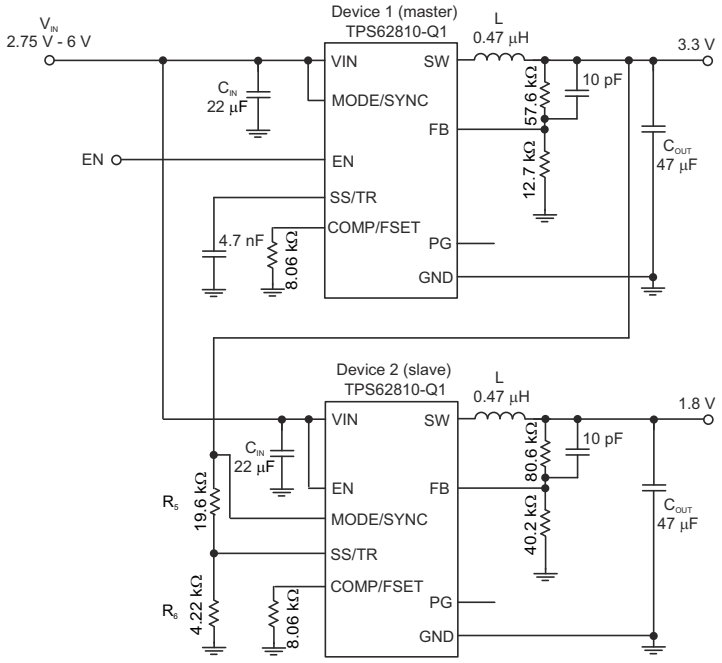


Figure 10-58. Schematic for Output Voltage Tracking

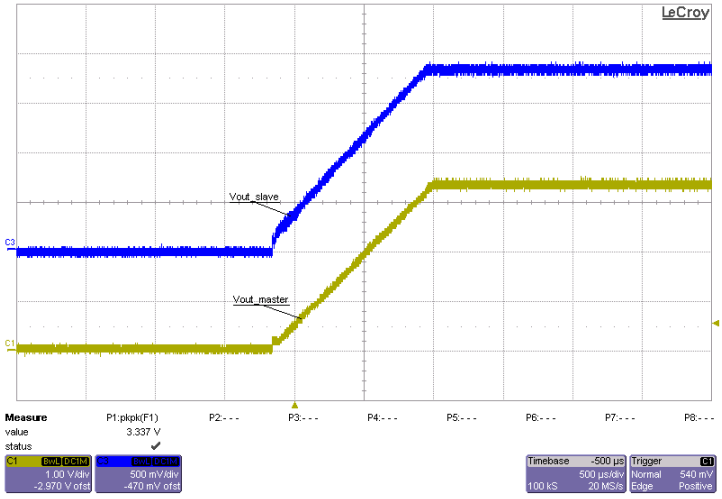


Figure 10-59. Scope Plot for Output Voltage Tracking

10.3.3 Synchronizing to an External Clock

The TPS6281x-Q1 can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied / removed during operation, allowing you to switch from an externally-defined fixed frequency to power-save mode or to internal fixed frequency operation. The value of the R_{CF} resistor must be chosen so that the internally defined frequency and the externally applied frequency are close to each other. This ensures a smooth transition from internal to external frequency and vice versa.

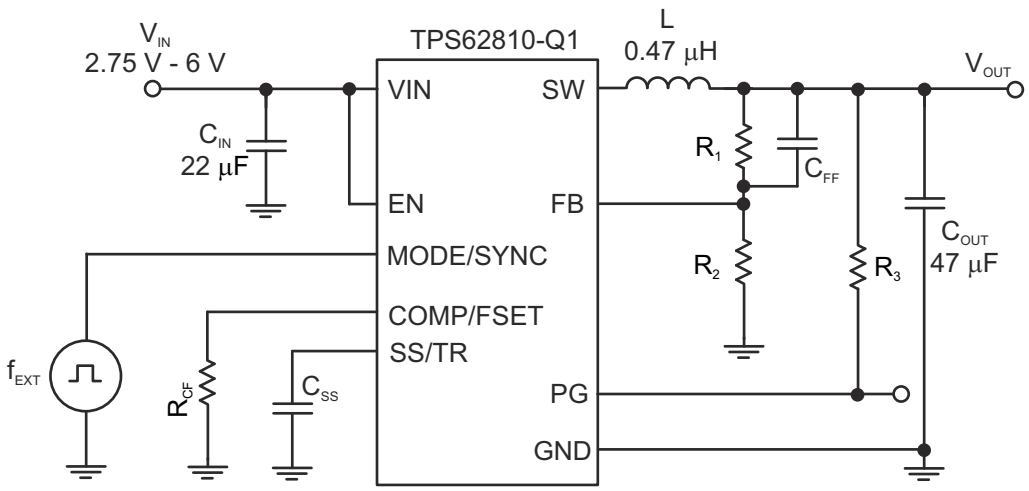
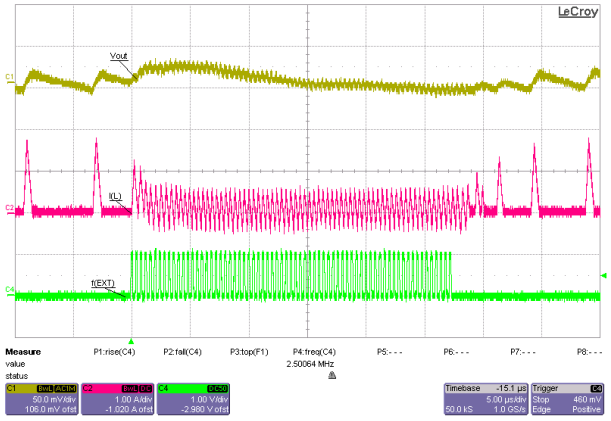
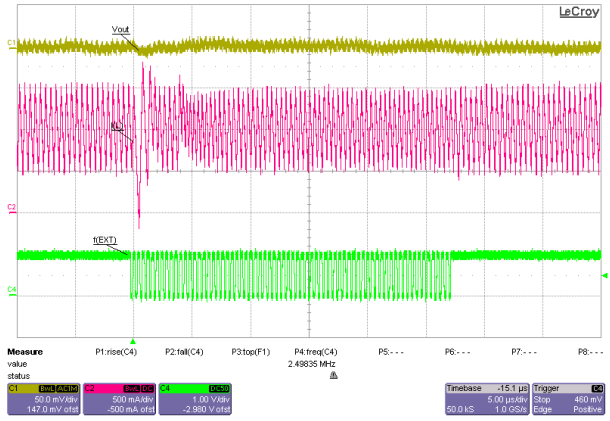


Figure 10-60. Schematic Using External Synchronization



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 0.1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-61. Switching from External Synchronization to Power-Save Mode (PFM)



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-62. Switching from External Synchronization to Internal Fixed Frequency

10.4 Power Supply Recommendations

The TPS6281x-Q1 device family has no special requirements for its input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6281x-Q1.

10.5 Layout

10.5.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6281x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses increased EMI radiation and noise sensitivity.

See *Layout Example* for the recommended layout of the TPS6281x-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC

pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB must be connected with short wires and not nearby high dv/dt signals (for example SW). Because they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R_1 and R_2, must be kept close to the IC and connect directly to those pins and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help spread the heat into the pcb.

The recommended layout is implemented on the EVM and shown in the *TPS62810EVM-015 Evaluation Module user's guide*.

10.5.2 Layout Example

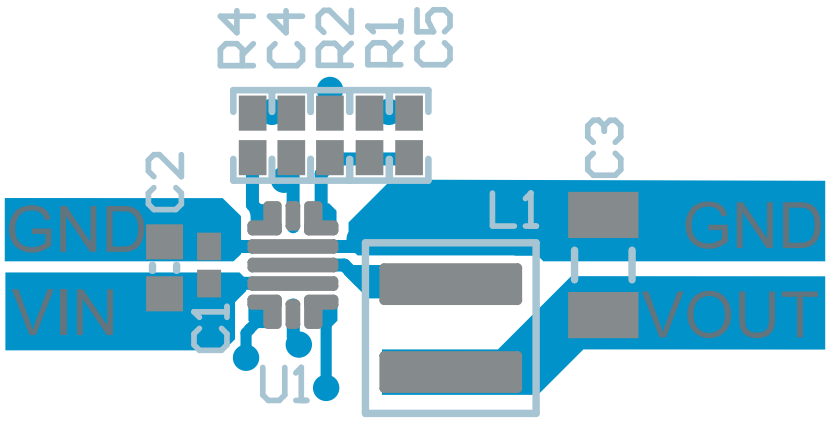


Figure 10-63. Example Layout

11 Device and Documentation Support

11.1 Device Support

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS62810EVM-015 Evaluation Module* user's guide

11.3 Receiving Notification of Documentation Updates

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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