2.25 MHz 600 mA Step Down Converter in 2x2SON/TSOT-23 Package

FEATURES

- **High Efficiency Step Down Converter**
- **Output Current up to 600 mA**
- **Wide V_{IN} Range from 2 V to 6 V for Li-Ion Batteries with Extended Voltage Range**
- **2.25 MHz Fixed Frequency Operation**
- **Power Save Mode at Light Load Currents**
- **Output Voltage Accuracy in PWM mode ±1.5%**
- **Typ. 15 µA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Soft Start**
- **Voltage Positioning at Light Loads**
- **Available in a small 2×2×0,8mm SON and TSOT-23 package**
- **Allows <1mm Solution Height**

APPLICATIONS

- **PDAs, Pocket PCs**
- **Low Power DSP Supply**
- **Portable Media Players**
- **POL applications**

DESCRIPTION

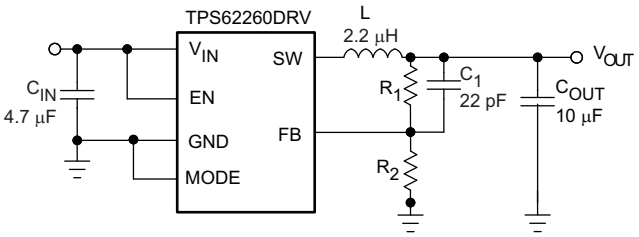
The TPS62260 device is a high efficient synchronous step down dc-dc converter optimized for battery powered applications. It provides up to 600-mA output current from a single Li-Ion cell and is ideal to power mobile phones and other portable applications.

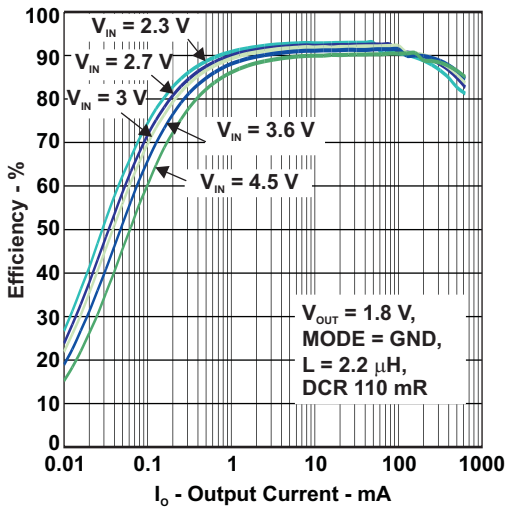
With an wide input voltage range of 2 V to 6 V, the device supports applications powered by Li-Ion batteries with extended voltage range, two and three cell alkaline batteries, 3.3 V and 5 V input voltage rails.

The TPS62260 operates at 2.25 MHz fixed switching frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range.

The Power Save Mode is optimized for low output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1µA. TPS62260 allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62260 is available in a very small 2×2 6 pin SON and TSOT-23 5 pin package.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER(1)	OUTPUT VOLTAGE(2)	PACKAGE(3)	PACKAGE DESIGNATOR	ORDERING	PACKAGE MARKING
–40°C to 85°C	TPS62260	adjustable	SON 2x2-6	DRV	TPS62260DRV	BYK
			TSOT-23 5	DDC	TPS62260DDC	BYP
	TPS62261	1.8V fix	SON 2x2-6	DRV	TPS62261DRV	BYL
	TPS62262	1.2V fix	SON 2x2-6	DRV	TPS62262DRV	BYM

(1) The DRV (2x2-6 SON) and DDC (TSOT-23-5) packages are available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.
(2) Contact TI for other fixed output voltage options
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range(2)		–0.3 to 7	V
	Voltage range at EN, MODE		–0.3 to V_{IN} +0.3, ≤ 7	V
	Voltage on SW		–0.3 to 7	V
	Peak output current		Internally limited	A
	ESD rating(3)	HBM Human body model	2	kV
		CDM Charge device model	1	
		Machine model	200	V
T_J	Maximum operating junction temperature		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DRV	76°C/W	1300 mW	13 mW/°C
DDC	250/°C	400 mW	4 mW/°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2		6	V
	Output voltage range for adjustable voltage	0.6		VIN	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

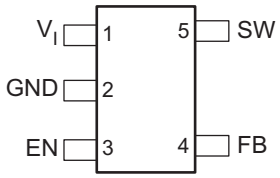
Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 4.7µF 0603, C_{OUT} = 10µF 0603, L = 2.2µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6	V
I_{OUT}	Output current	V_{IN} 2.5 V to 6 V			600	mA
		V_{IN} 2.3 V to 2.5 V			300	
		V_{IN} 2 V to 2.3 V			150	
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device not switching		15		µA
		I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device switching, V_{OUT} = 1.8 V, See (1)		18.5		
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	1		VIN	V
V_{IL}	Low level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or VIN		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		240	480	mΩ
	Low side MOSFET on-resistance			185	380	
I_{LIMF}	Forward current limit MOSFET high-side and low side	V_{IN} = V_{GS} = 3.6 V	0.8	1	1.2	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN}≤ 6 V	2	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable output voltage range		0.6		V_{IN}	V
V_{ref}	Reference voltage			600		mV
V_{FB}	Feedback voltage PWM Mode	MODE = V_{IN}, PWM operation, for fixed output voltage versions V_{FB} = V_{OUT}, 2.5 V ≤ V_{IN} ≤ 6 V, 0 mA ≤ I_{OUT} ≤ 600 mA, See (2)	–1.5%	0%	1.5%	
	Feedback voltage PFM mode	MODE = GND, device in PFM mode, voltage positioning active, See (1)		1%		
	Load regulation	PWM Mode		-0.5		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, See (3)		0.1	1	µA

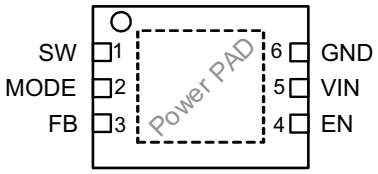
(1) In PFM mode, the internal reference voltage is set to typ. 1.01×V_{ref}. See the parameter measurement information.
(2) For V_{IN} = V_O + 0.6 V
(3) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

PIN ASSIGNMENTS

DDC PACKAGE
(TOP VIEW)



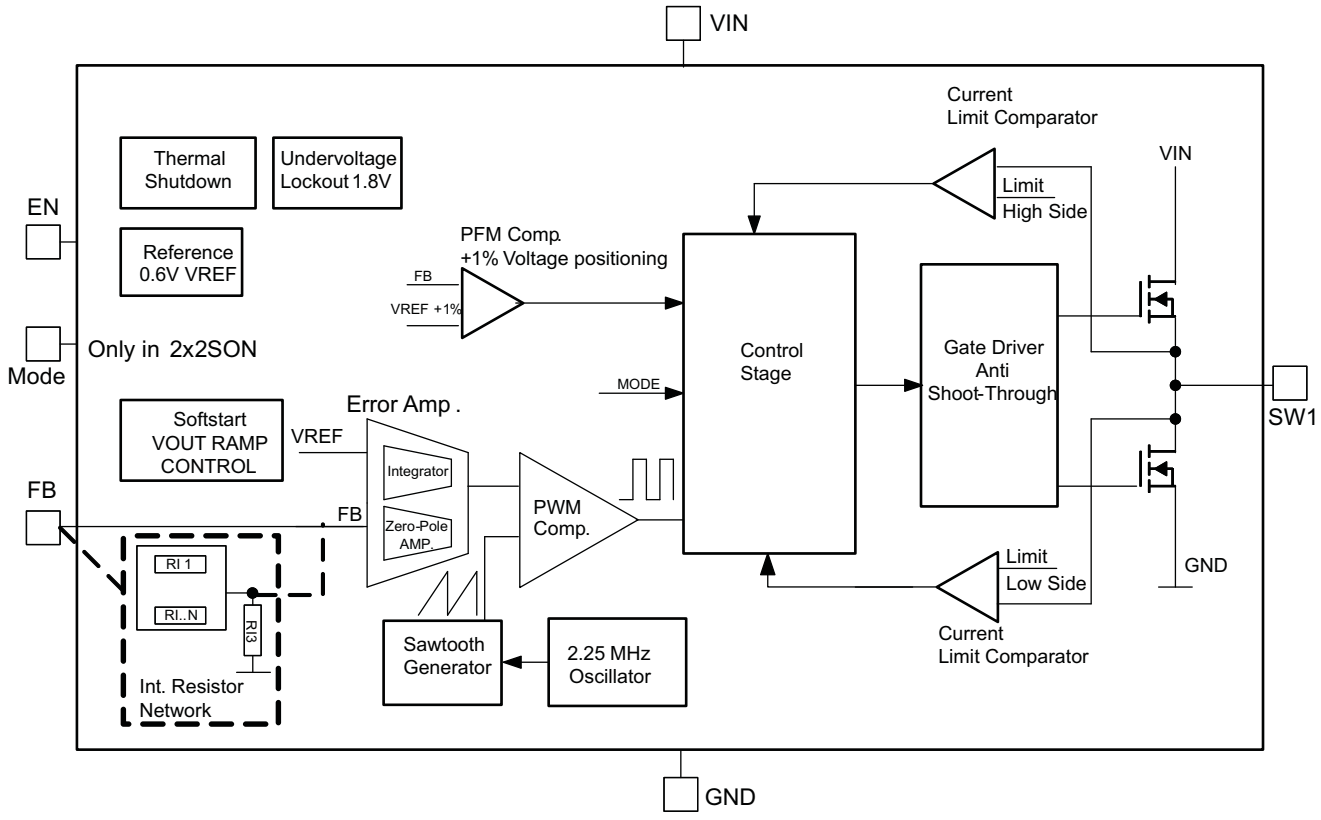
DRV PACKAGE
(TOP VIEW)



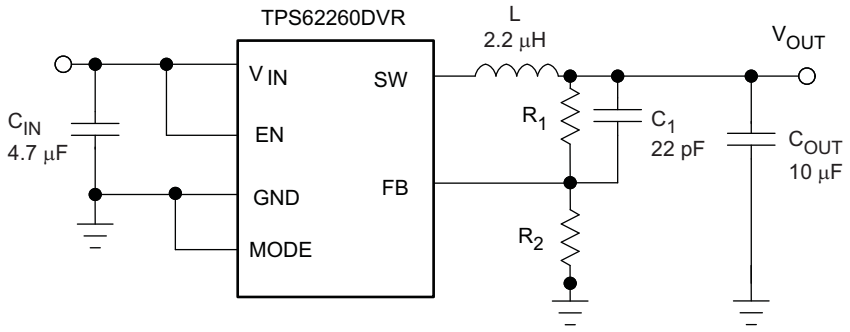
TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO. SON 2x2-6	NO. TSOT23-5		
V_{IN}	5	1	PWR	VIN power supply pin.
GND	6	2	PWR	GND supply pin
EN	4	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	4	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
FB	3	5	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	2		I	This pin is only available at SON package option. MODE pin = high forces the device to operate in fixed frequency PWM mode. MODE pin = low enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: LPS3015 2.2 µH, 110 µΩ
C_{IN} GRM188R60J475K 4.7 µF Murata 0603 size
C_{OUT} GRM188R60J106M 10 µF Murata 0603 size

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
η Efficiency	Output Current V_{OUT} = 1.8 V, Power Save Mode, MODE = GND	Figure 1
	Output Current V_{OUT} = 1.8 V, PWM Mode, MODE = V_{IN}	Figure 2
	Output Current V_{OUT} = 3.3 V, PWM Mode, MODE = V_{IN}	Figure 3
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	Output Current	Figure 5
	Output Current	Figure 6
Output Voltage Accuracy	at 25°C, V_{OUT} = 1.8 V, Power Save Mode, MODE = GND	Figure 7
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	at 85°C, V_{OUT} = 1.8 V, Power Save Mode, MODE = GND	Figure 9
	at 25°C, V_{OUT} = 1.8 V, PWM Mode, MODE = V_{IN}	Figure 10
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Load Transient	Forced PWM Mode , V_{OUT} = 1.5 V, 50 mA to 200 mA	Figure 17
	Forced PWM Mode , V_{OUT} = 1.5 V, 200 mA to 400 mA	Figure 18
	PFM Mode to PWM Mode, V_{OUT} = 1.5 V, 150 µA to 400 mA	Figure 19
	PWM Mode to PFM Mode, V_{OUT} = 1.5 V, 400 mA to 150 µA	Figure 20
	PFM Mode, V_{OUT} = 1.5 V, 1.5 mA to 50 mA	Figure 21
	PFM Mode, V_{OUT} = 1.5 V, 50 mA to 1.5 mA	Figure 22
	PFM Mode to PWM Mode, V_{OUT} = 1.8 V, 50 mA to 250 mA	Figure 23
	PFM Mode to PWM Mode, V_{OUT} = 1.5 V, 50 mA to 400 mA	Figure 24
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Line Transient	PFM Mode, V_{OUT} = 1.8 V, 50 mA	Figure 26
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TYPICAL CHARACTERISTICS (continued)

Table of Graphs (continued)

		FIGURE
Typical Operation	PFM V_{OUT} Ripple, V_{OUT} = 1.8 V, 10 mA, L = 2.2µH, C_{OUT} = 10µF	Figure 28
	PFM V_{OUT} Ripple, V_{OUT} = 1.8 V, 10 mA, L = 4.7µH, C_{OUT} = 10µF	Figure 29
Shutdown Current into VIN	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = -40°C)	Figure 30
Quiescent Current	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = -40°C)	Figure 31
Static Drain Source On-State Resistance	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = -40°C)	Figure 32
		Figure 33

EFFICIENCY (Power Save Mode) vs OUTPUT CURRENT

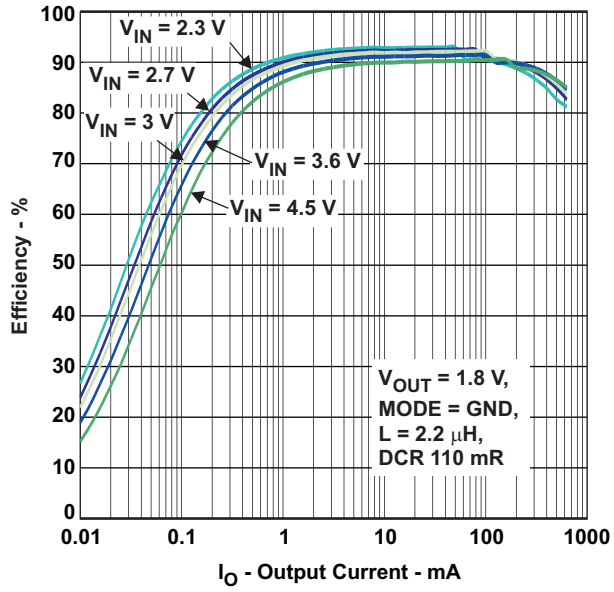

Figure 1.

EFFICIENCY (PWM Mode) vs OUTPUT CURRENT

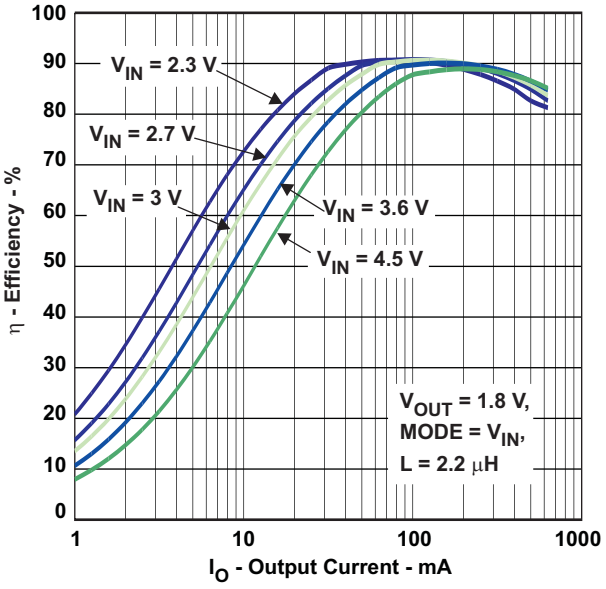

Figure 2.

EFFICIENCY (PWM Mode)
vs
OUTPUT CURRENT

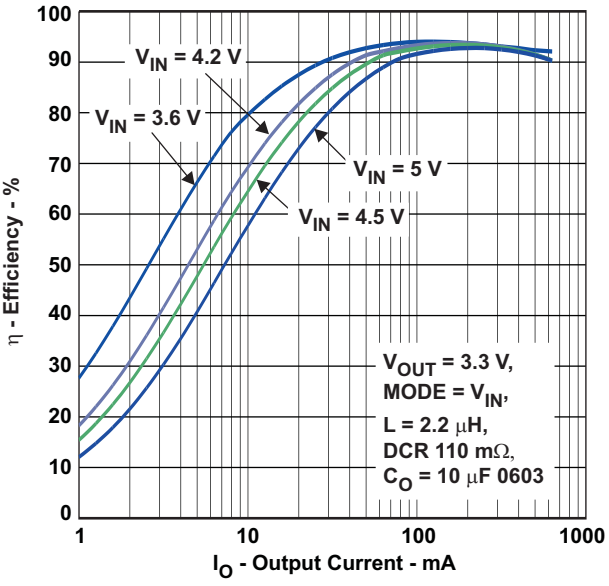

Figure 3.

EFFICIENCY (Power Save Mode)
vs
OUTPUT CURRENT

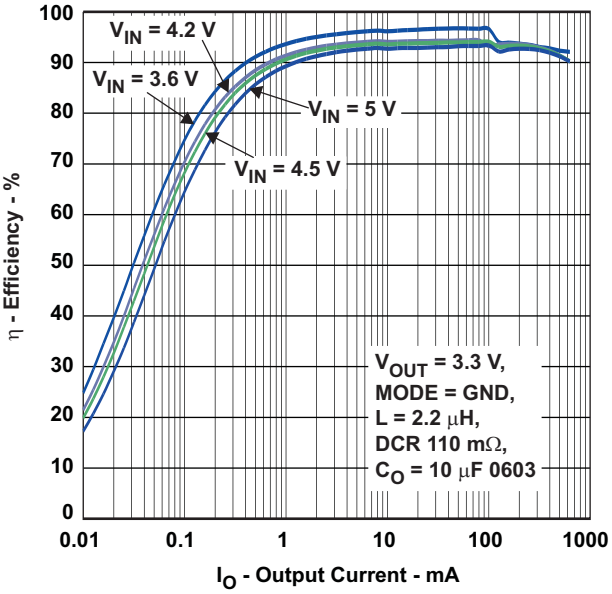

Figure 4.

EFFICIENCY
vs
OUTPUT CURRENT

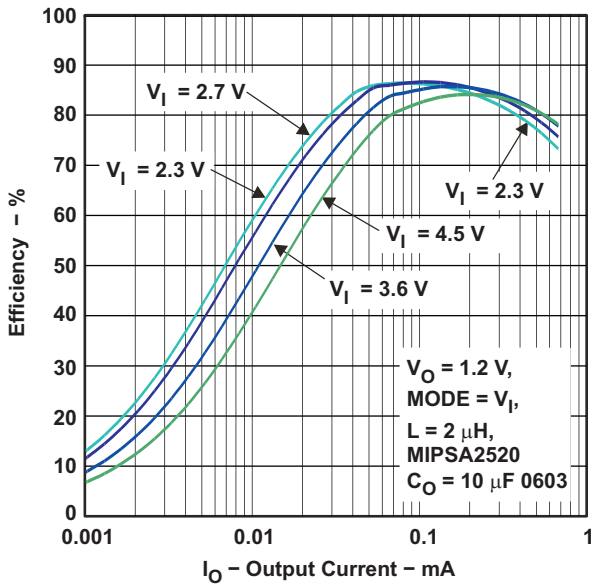

Figure 5.

EFFICIENCY
vs
OUTPUT CURRENT

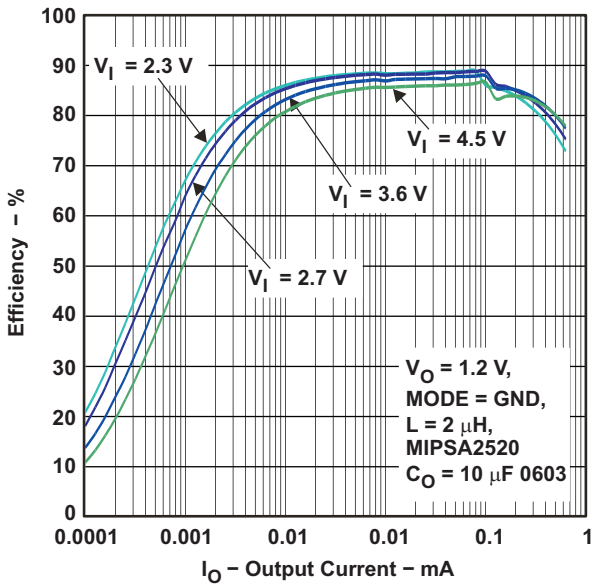

Figure 6.

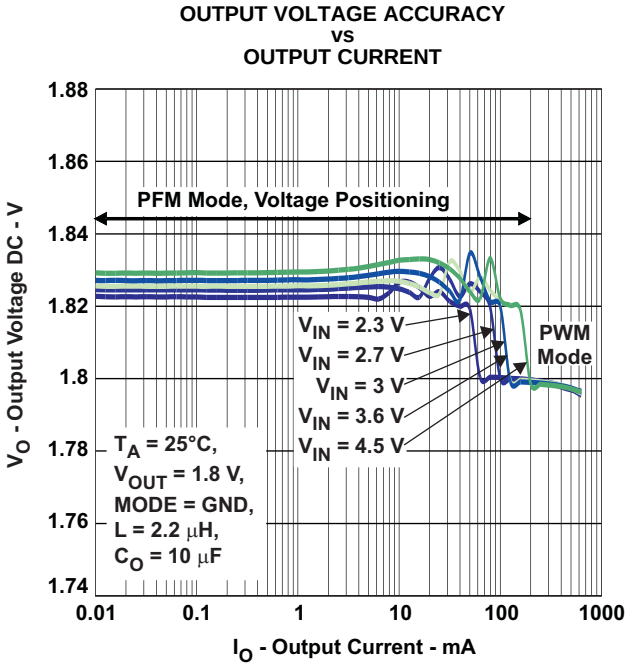

Figure 7.

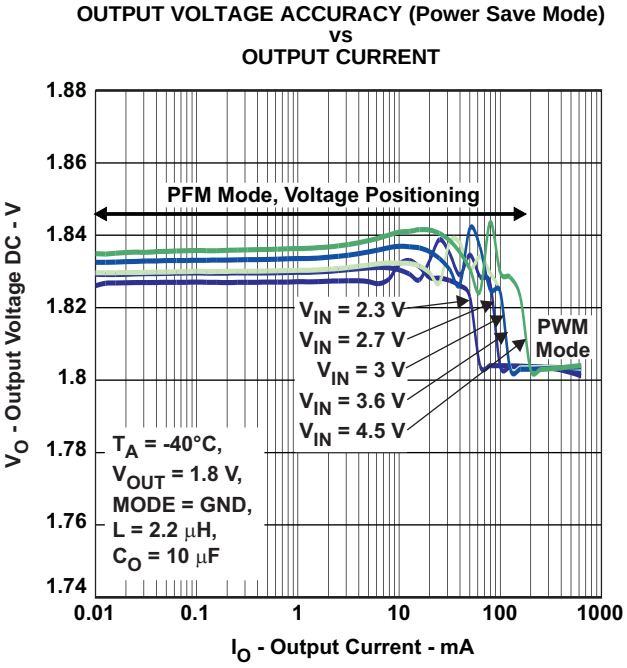

Figure 8.

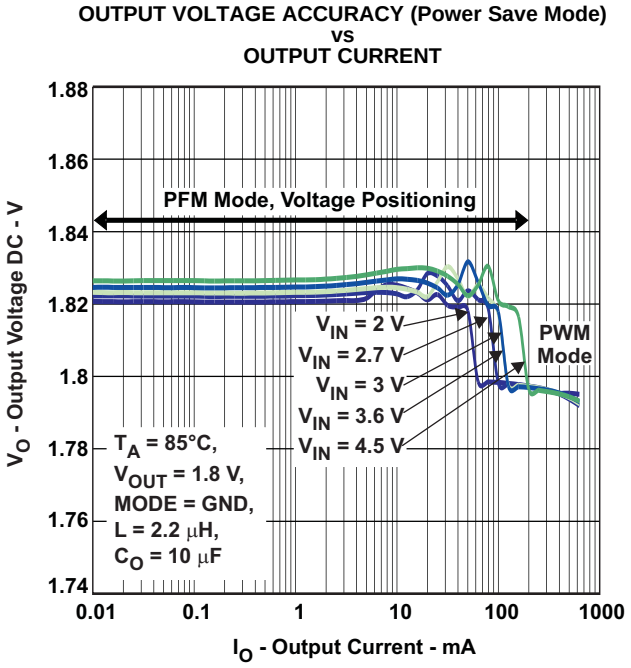

Figure 9.

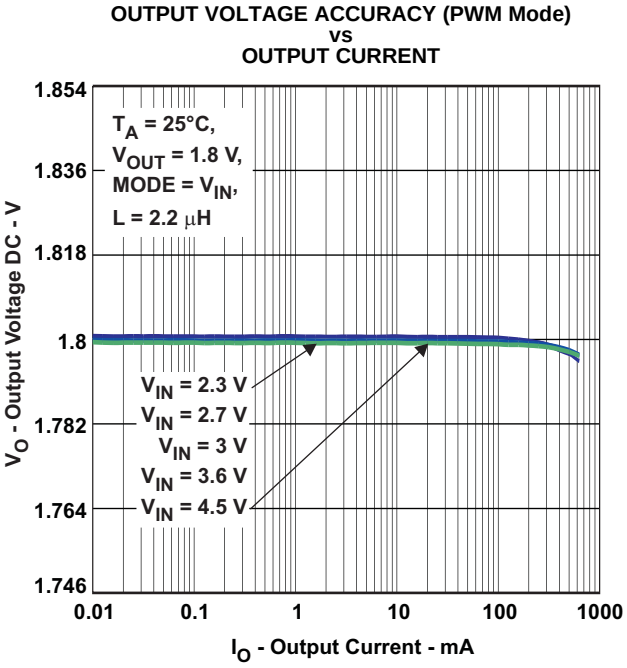

Figure 10.

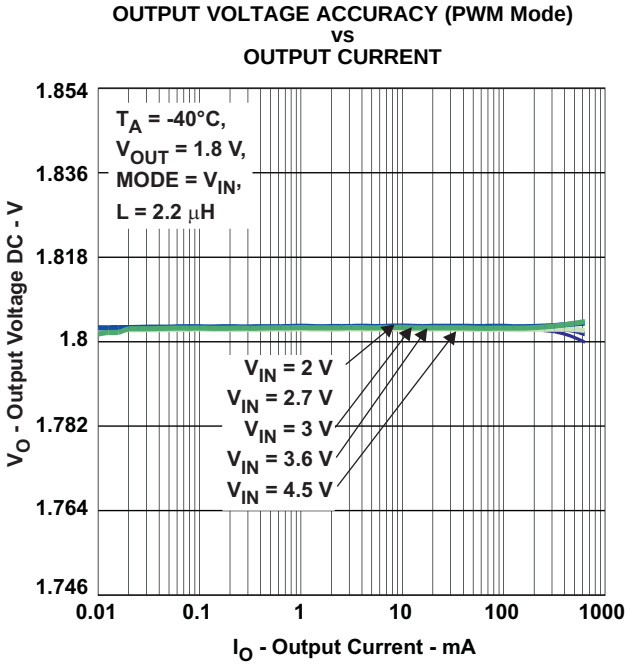

Figure 11.

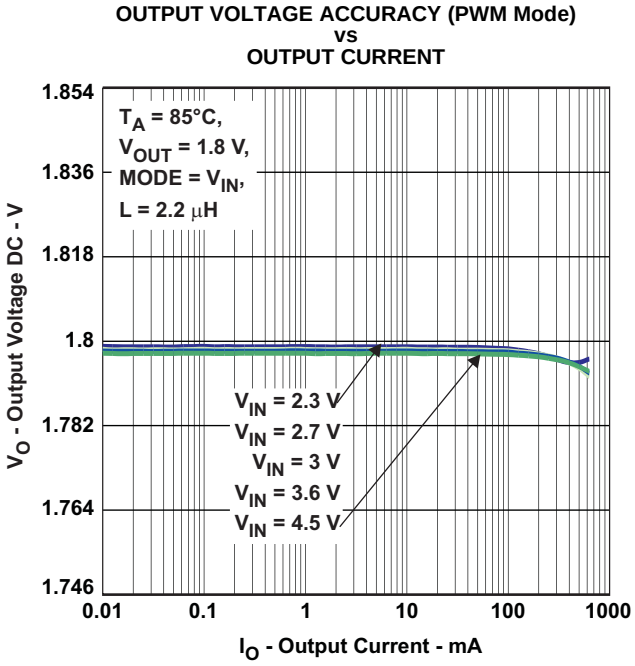

Figure 12.

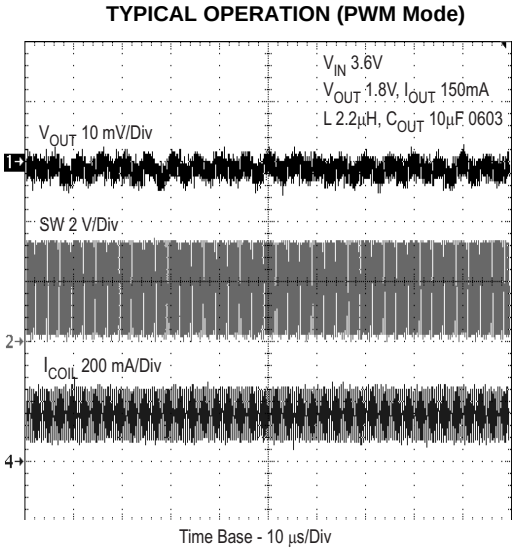

Figure 13.

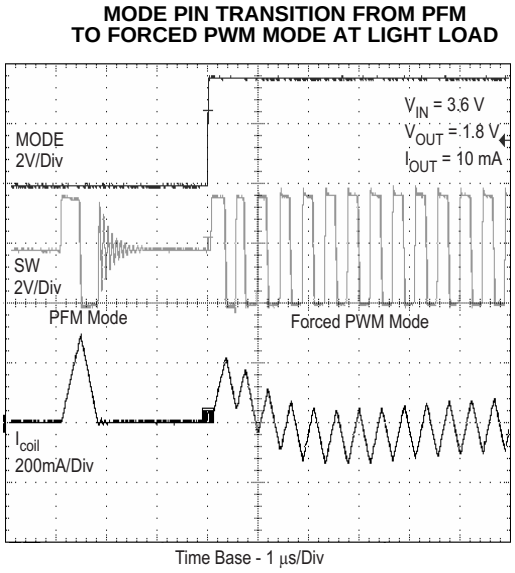

Figure 14.

MODE PIN TRANSITION FROM PWM TO PFM MODE AT LIGHT LOAD

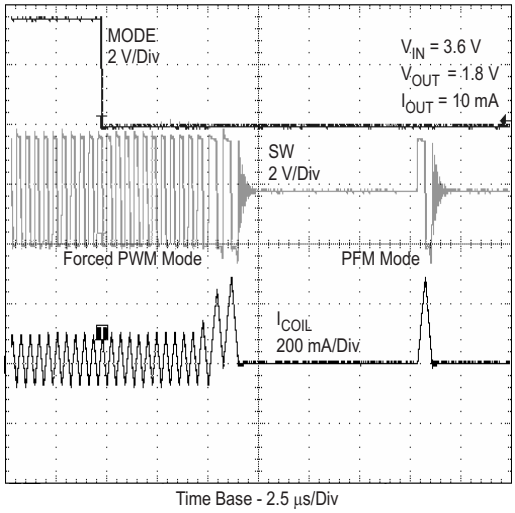

Figure 15.

START-UP TIMING

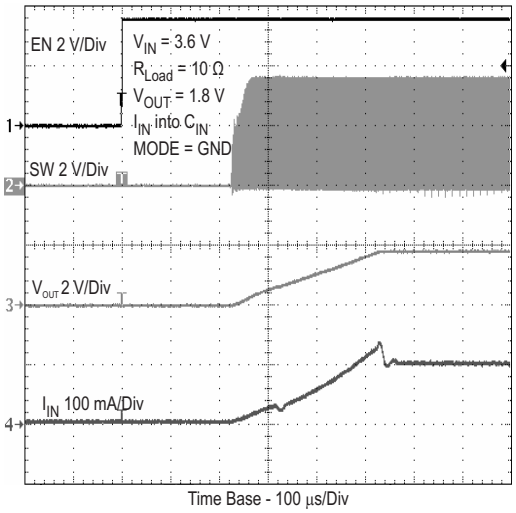

Figure 16.

LOAD TRANSIENT (Forced PWM Mode)

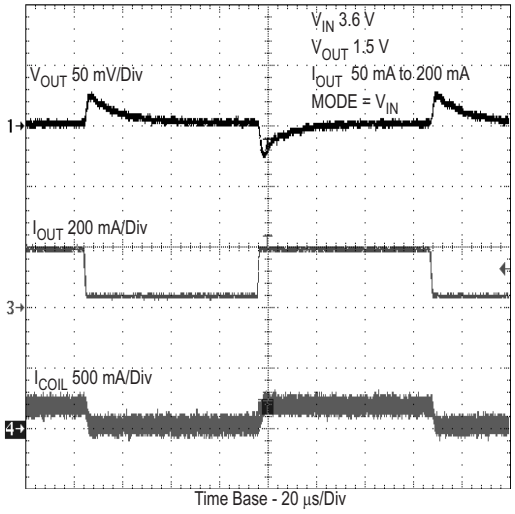

Figure 17.

LOAD TRANSIENT (Forced PWM Mode)

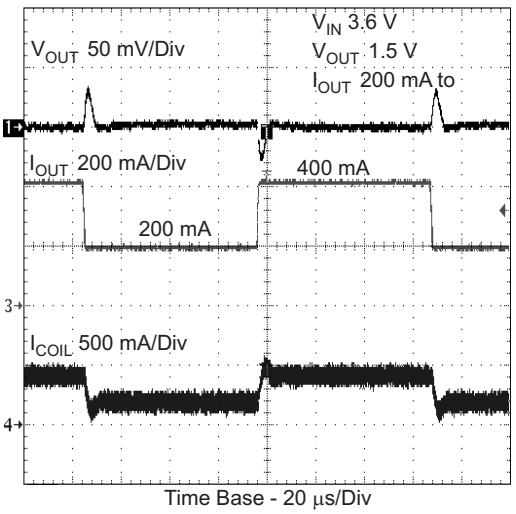

Figure 18.

LOAD TRANSIENT
(Forced PFM Mode To PWM Mode)

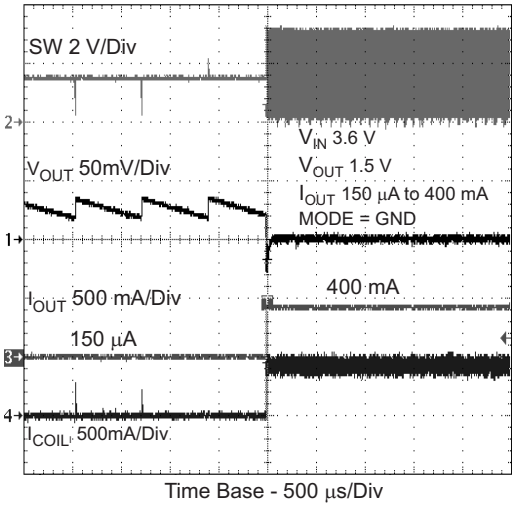

Figure 19.

LOAD TRANSIENT
(Forced PWM Mode To PFM Mode)

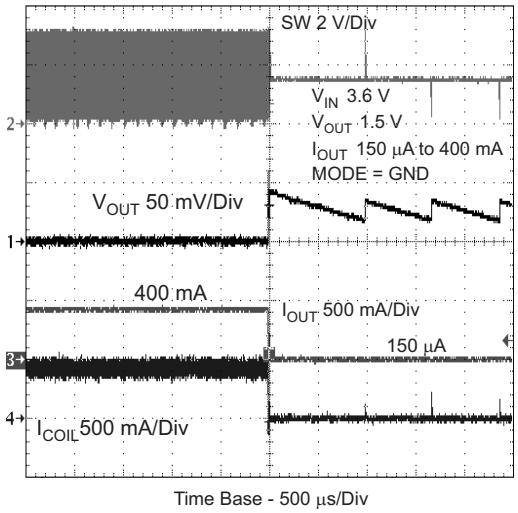

Figure 20.

LOAD TRANSIENT (PFM Mode)

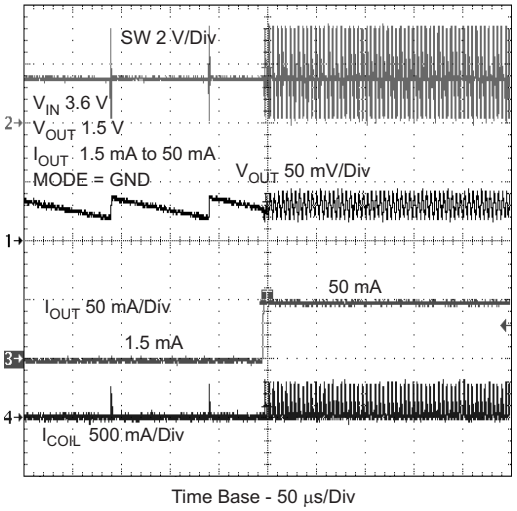

Figure 21.

LOAD TRANSIENT (PFM Mode)

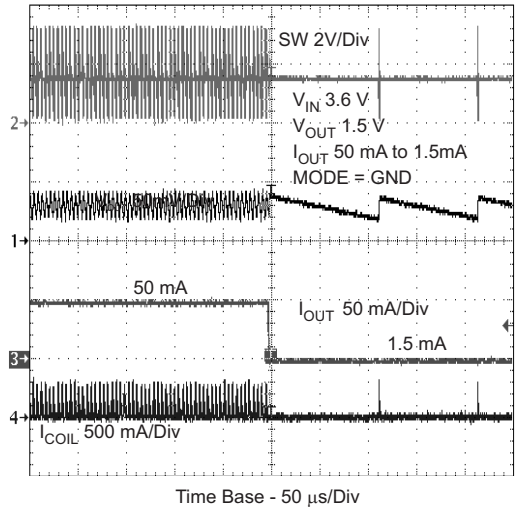

Figure 22.

LOAD TRANSIENT (PFM Mode To PWM Mode)

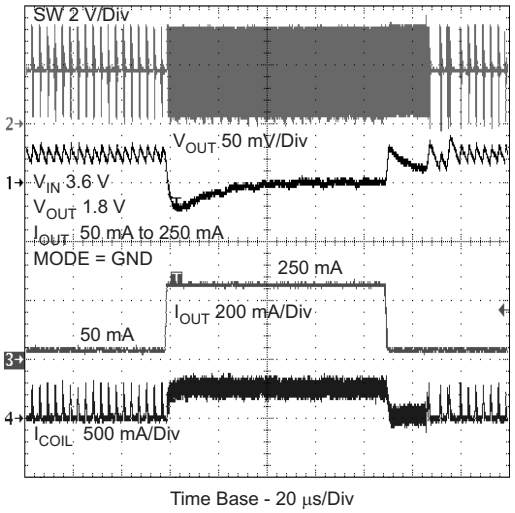

Figure 23.

LOAD TRANSIENT (PFM Mode To PWM Mode)

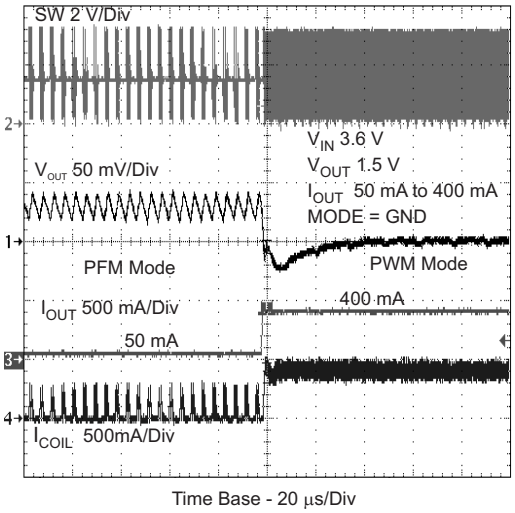

Figure 24.

LOAD TRANSIENT (PWM Mode To PFM Mode)

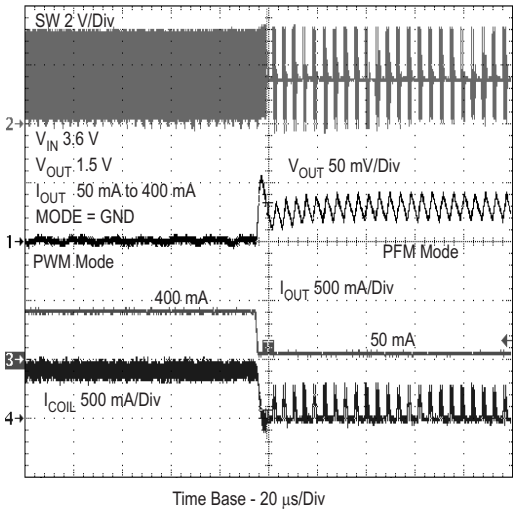

Figure 25.

LINE TRANSIENT (PFM Mode)

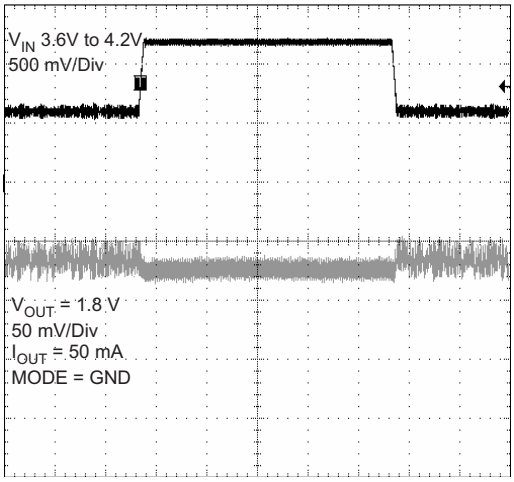

Figure 26.

LINE TRANSIENT (PWM Mode)

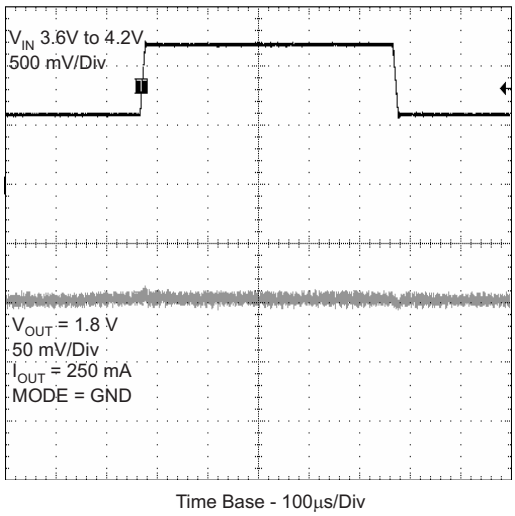

Figure 27.

TYPICAL OPERATION (PFM Mode)

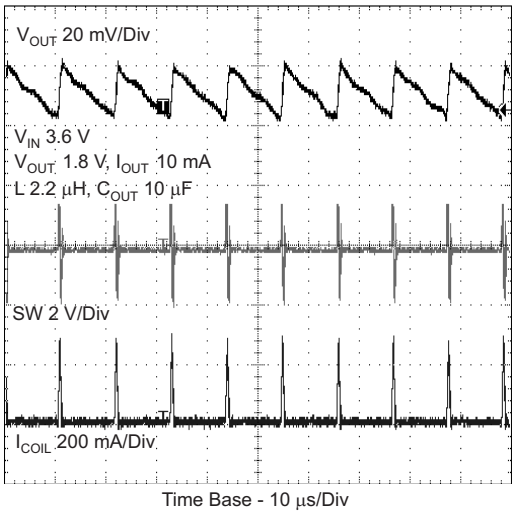

Figure 28.

TYPICAL OPERATION (PFM Mode)

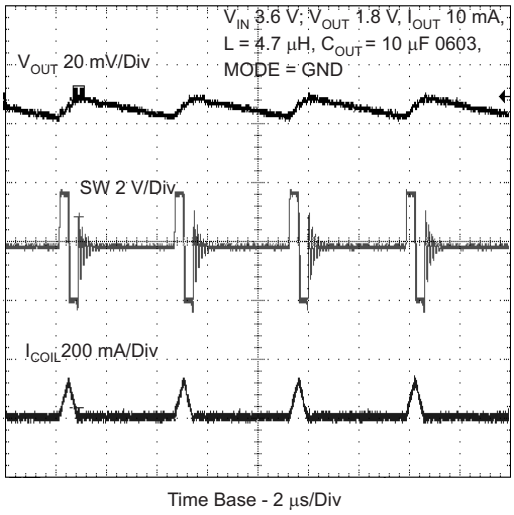

Figure 29.

SHUTDOWN CURRENT INTO VIN vs INPUT VOLTAGE

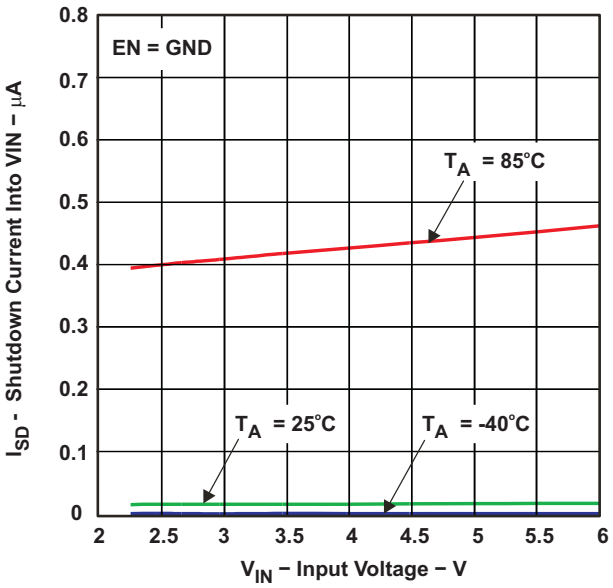

Figure 30.

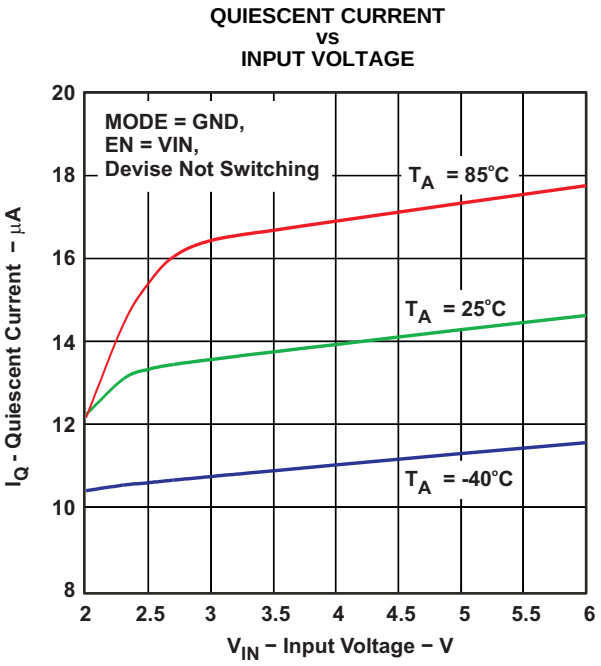

Figure 31.

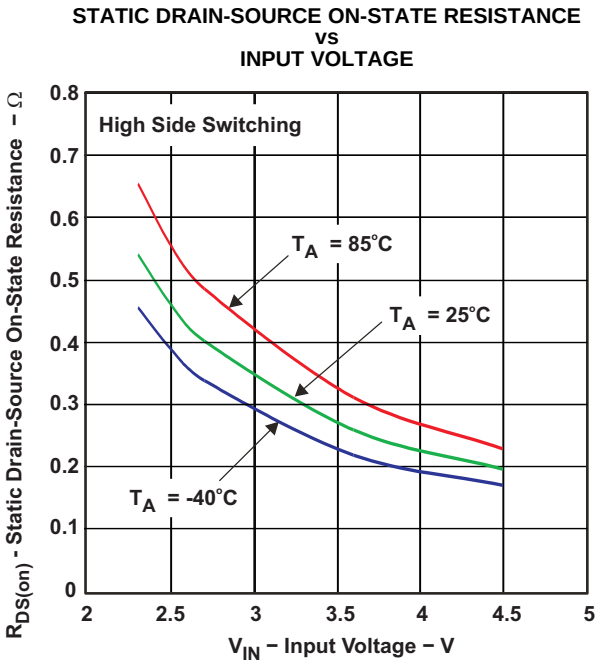

Figure 32.

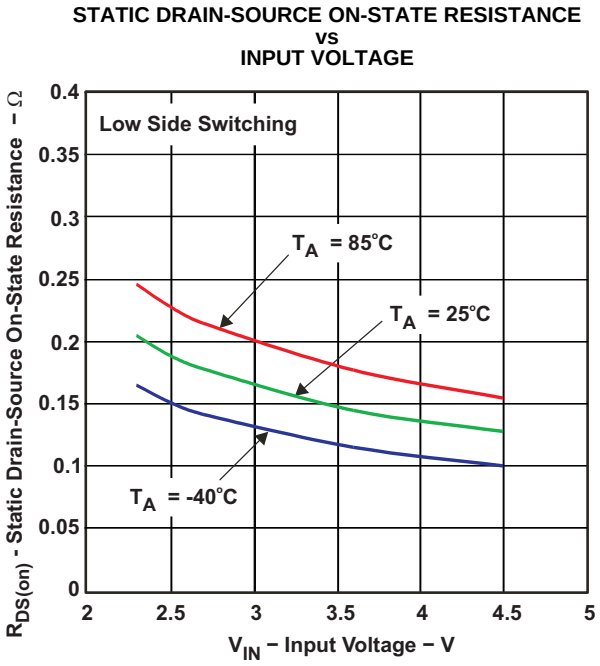

Figure 33.

DETAILED DESCRIPTION

OPERATION

The TPS62260 step down converter operates with typically 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation the converter use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After a dead time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch.

POWER SAVE MODE

The Power Save Mode is enabled with MODE Pin set to low level. If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal +1%, the device starts a PFM current pulse. The High Side MOSFET switch will turn on, and the inductor current ramps up. After the On-time expires, the switch is turned off and the Low Side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15μA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM Pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode. The Power Save Mode can be disabled through the MODE pin set to high. The converter will then operate in fixed frequency PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

DETAILED DESCRIPTION (continued)

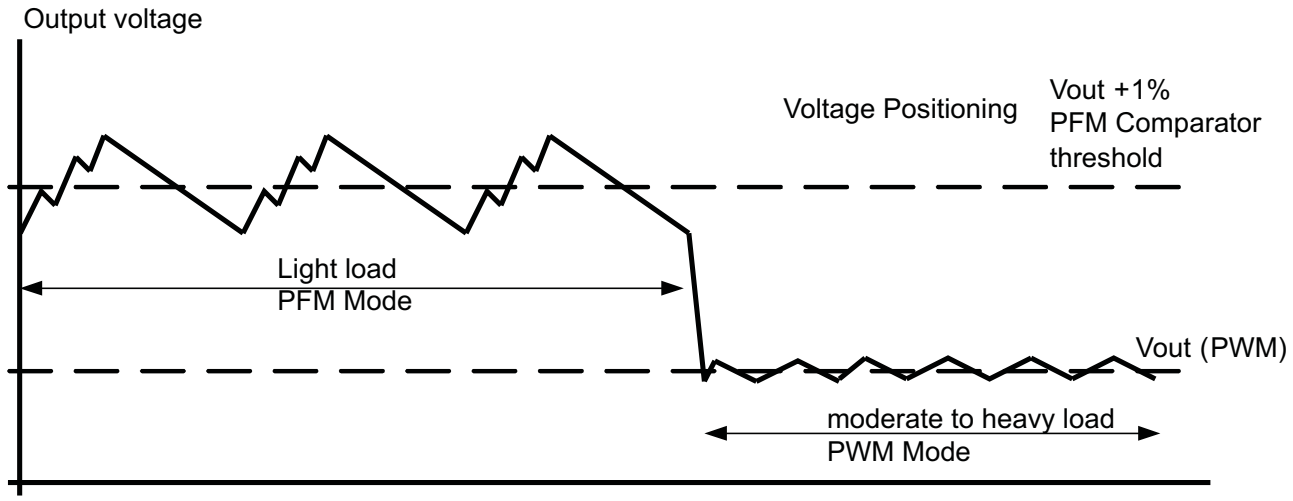

Figure 34. Power Save Mode Operation with automatic Mode transition

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High Side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN the High Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$V_{IN}min = V_Omax + I_Omax \times (R_{DS(on)}max + R_L)$

With:

I_Omax = maximum output current plus inductor ripple current

$R_{DS(on)}max$ = maximum P-channel switch RDSon.

R_L = DC resistance of the inductor

V_Omax = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85V with falling V_{IN}.

MODE SELECTION

The MODE pin allows mode selection between forced PWM mode and Power Save Mode.

Connecting this pin to GND enables the Power Save Mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

DETAILED DESCRIPTION (continued)

ENABLE

The device is enabled setting EN pin to high. During the start up time $t_{Start\ Up}$ the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode in which all internal circuits are disabled. In fixed output voltage versions, the internal resistor divider network is then disconnected from FB pin.

SOFT START

The TPS62260 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled within the start up time $t_{Start\ Up}$.

SHORT-CIRCUIT PROTECTION

The High Side and Low Side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the High Side MOSFET switch exceeds the threshold of it's current limit comparator, it turns off and the Low Side MOSFET switch is activated to ramp down the current in the inductor and High Side MOSFET switch. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has decreased below the threshold of its current limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

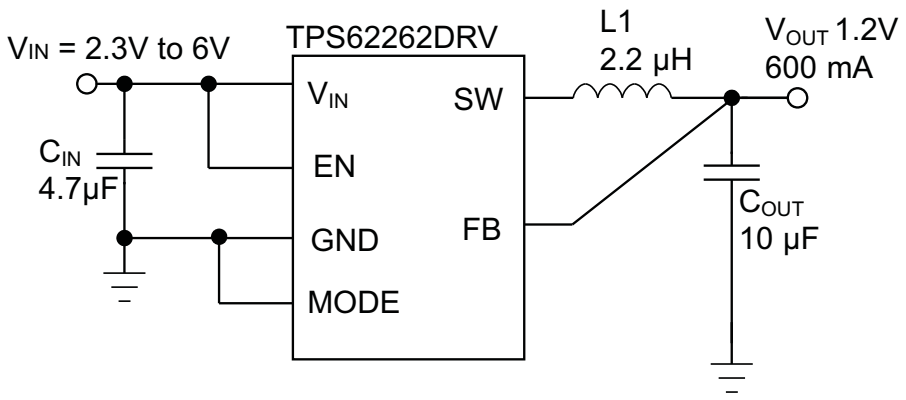

Figure 35. TPS62260 Fixed 1.2-V Output

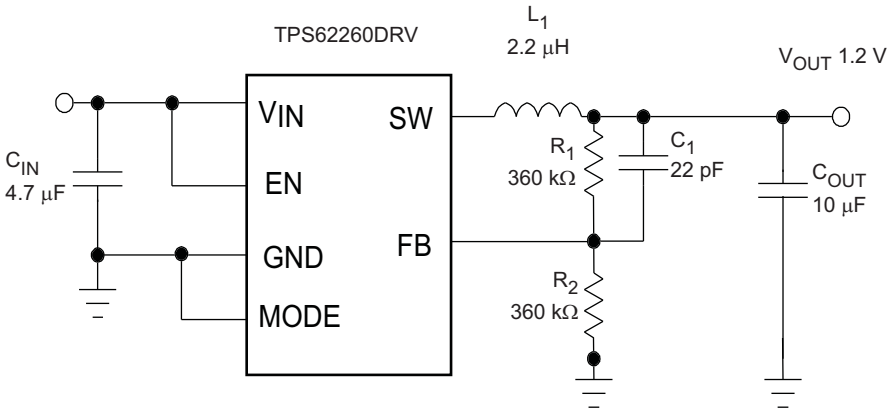

Figure 36. TPS62260DRV Adjustable 1.2-V Output

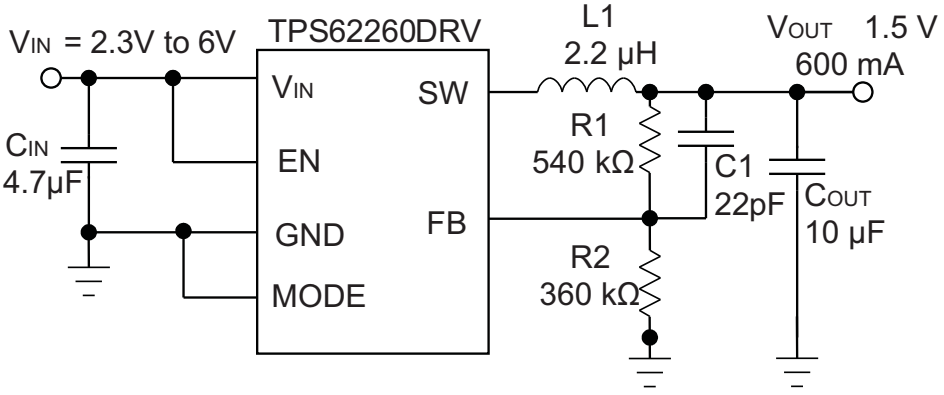

Figure 37. TPS62260 Fixed 1.5-V Output

APPLICATION INFORMATION (continued)

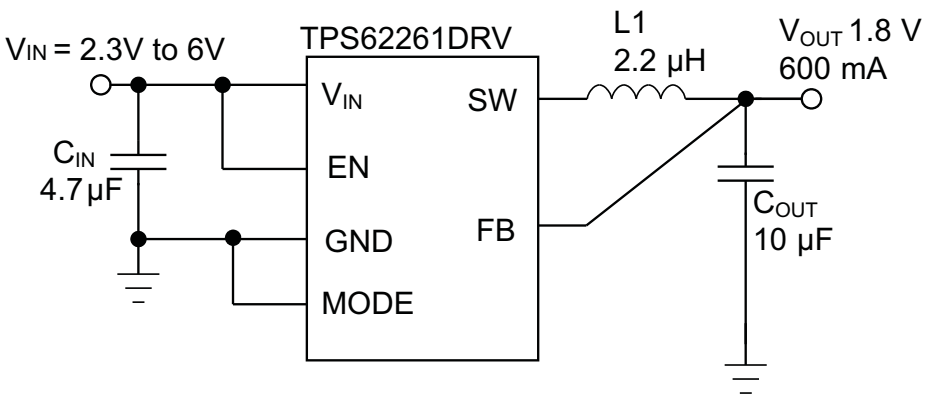

Figure 38. TPS62261 Fixed 1.8-V Output

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$ with an internal reference voltage V_{REF} typical 0.6V.

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1MΩ, to keep the network robust against noise. An external feed forward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range between 22pF and 33pF.

Route the FB line away from noise sources, such as the inductor or the SW line.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62260 is designed to operate with inductors in the range of 1.5µH to 4.7µH and with output capacitors in the range of 4.7µF to 22µF. The part is optimized for operation with a 2.2µH inductor and 10µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1µH effective inductance and 3.5µF effective capacitance.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection has also impact on the output voltage ripple in PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

APPLICATION INFORMATION (continued)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency (2.25MHz typical)

L = Inductor Value

ΔI_L = Peak to Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List of Inductors

DIMENSIONS [mm³]	Inductance µH	INDUCTOR TYPE	SUPPLIER
2.5x2.0x1.0max	2.0	MIPS2520D2R2	FDK
2.5x2.0x1.2max	2.0	MIPSA2520D2R2	FDK
2.5x2.0x1.0max	2.2	KSLI-252010AG2R2	Htachi Metals
2.5x2.0x1.2max	2.2	LQM2HPN2R2MJ0L	Murata
3x3x1.5max	2.2	LPS3015 2R2	Coilcraft

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62260 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (4)$$

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

Input Capacitor Selection

An input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7µF to 10µF ceramic capacitor is recommended. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10µF input capacitors be used for input voltages > 4.5V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7µF	GRM188R60J475K	0603 1.6x0.8x0.8mm^3	Murata
10µF	GRM188R60J106M69D	0603 1.6x0.8x0.8mm^3	Murata

LAYOUT CONSIDERATIONS

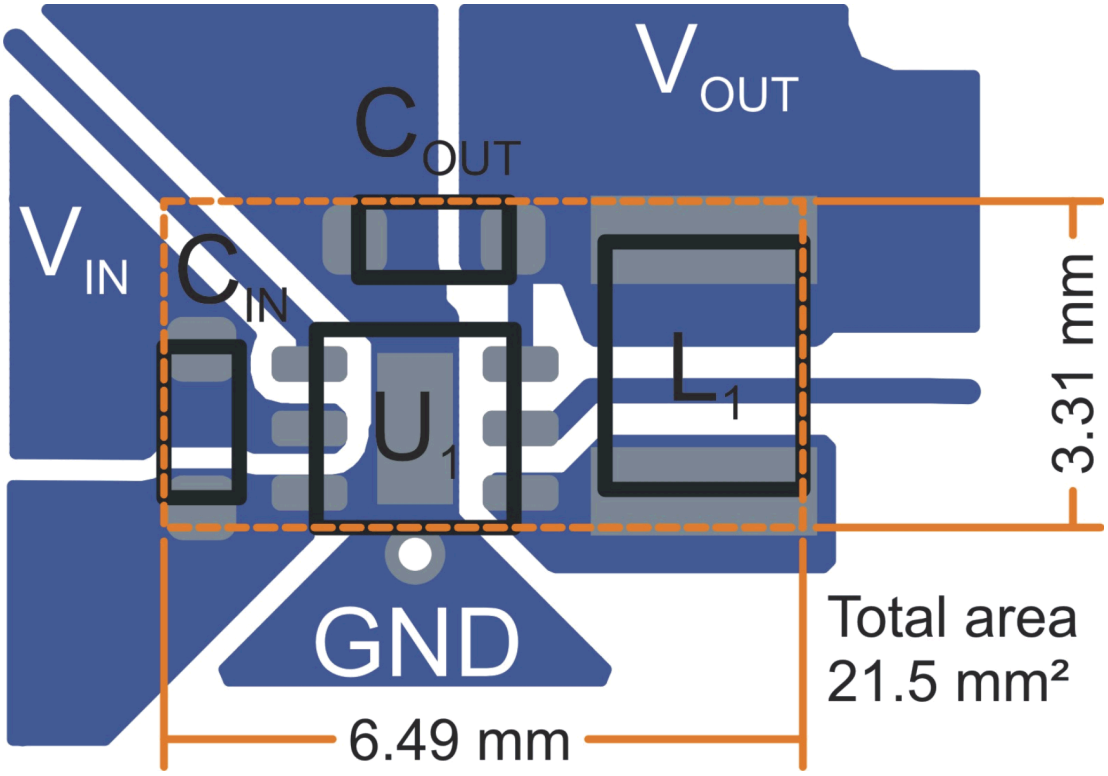

Figure 39. Suggested Layout for Fixed Output Voltage Options

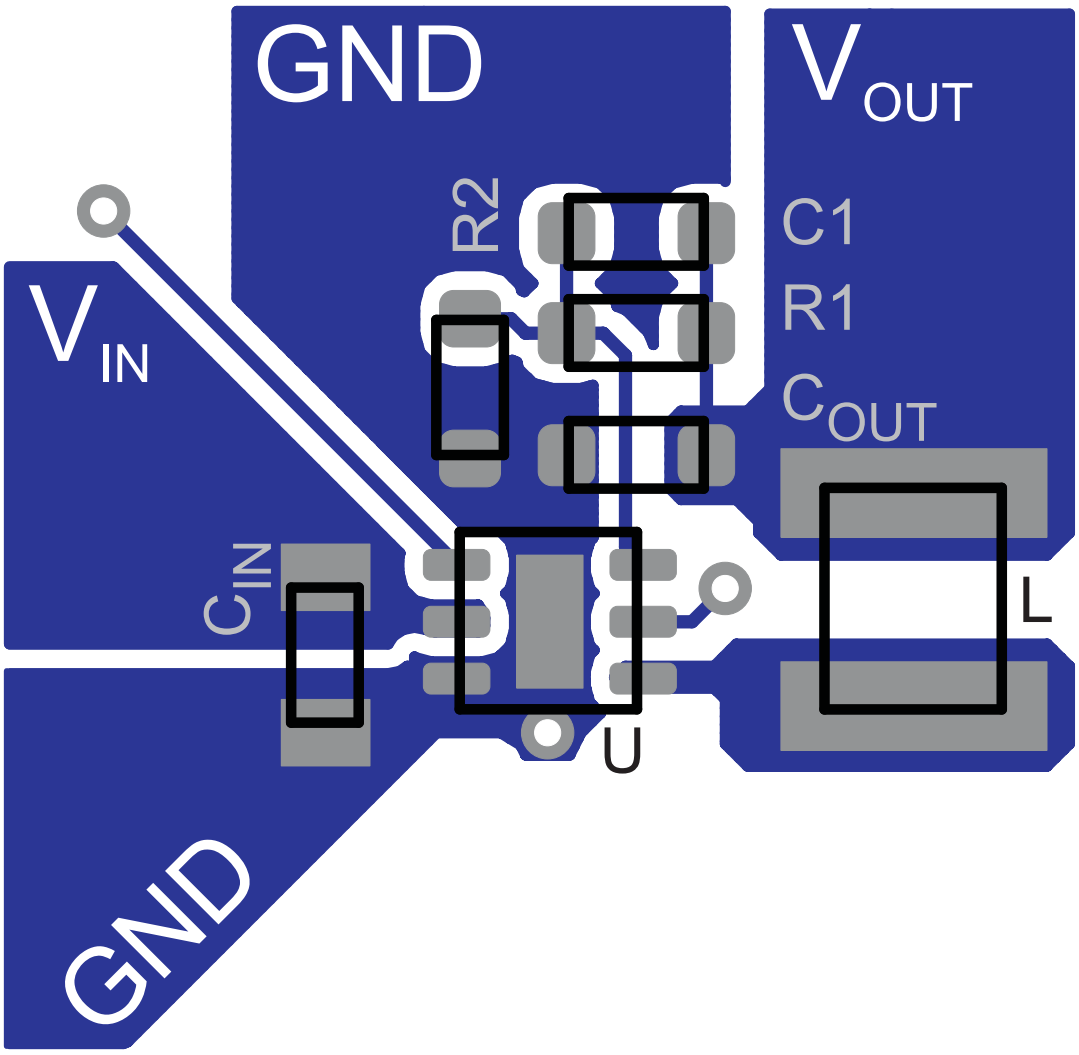

Figure 40. Suggested Layout for Adjustable Output Voltage Version

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND Pin of the device to the PowerPAD™ of the PCB and use this pad as a star point. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line).

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS62260DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DDCTG4	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62260DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62261DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62261DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62261DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62261DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62262DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62262DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62262DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62262DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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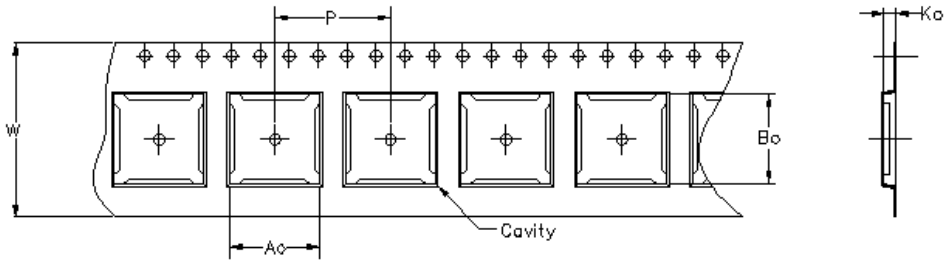
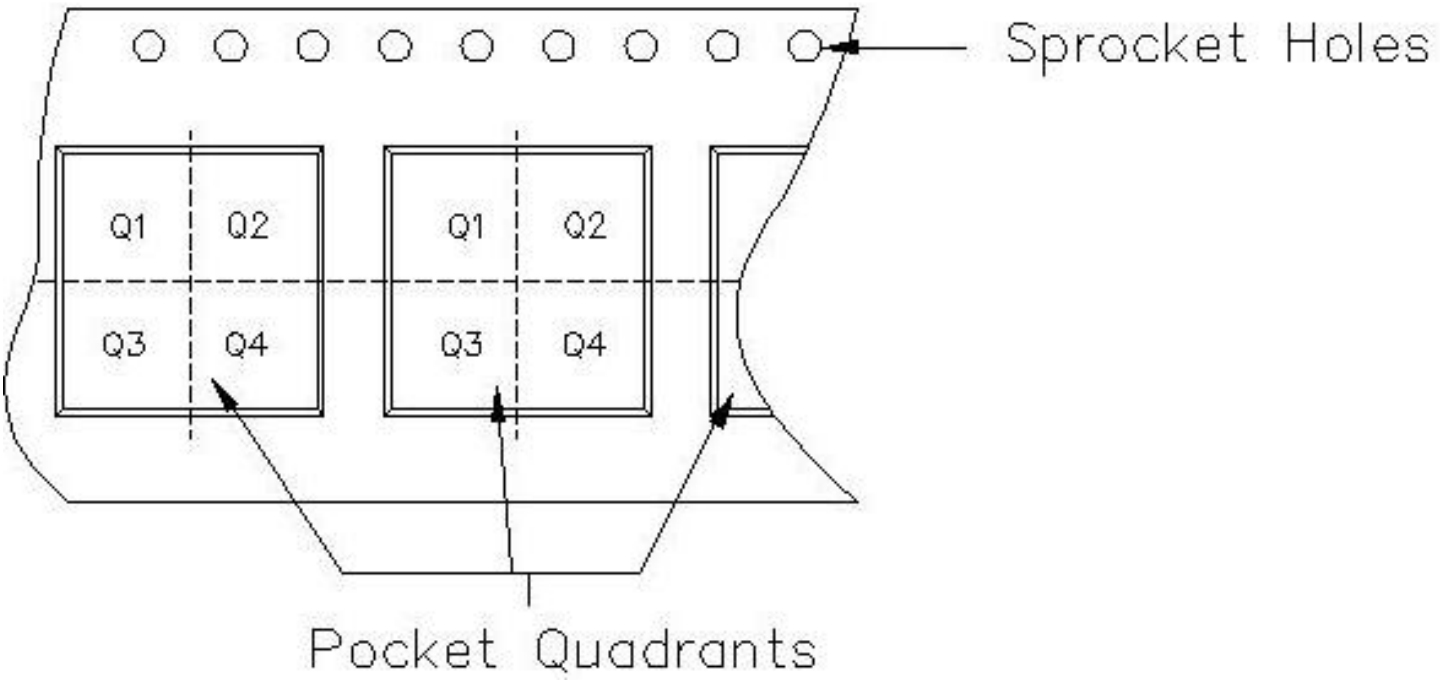


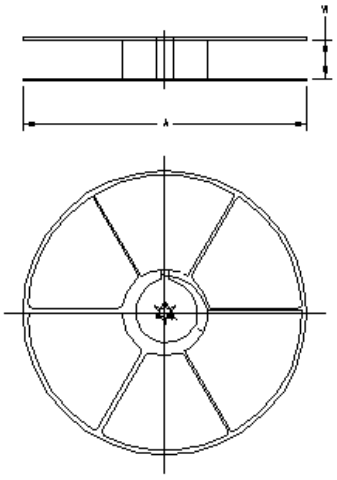
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



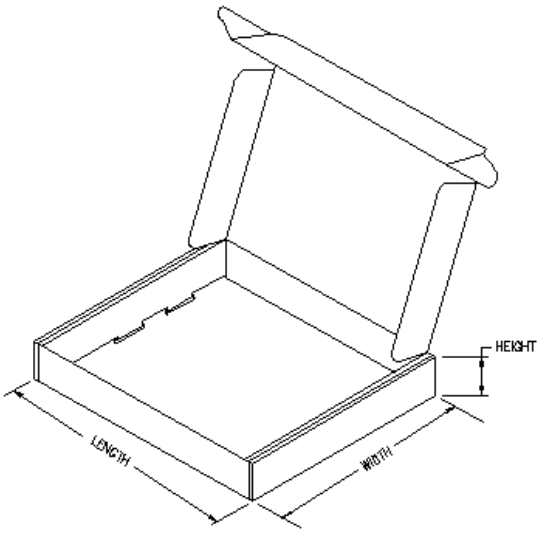
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62260DDCR	DDC	5	NSE	179	8	3.2	3.2	1.4	4	8	Q3
TPS62260DDCT	DDC	5	MLA	179	8	3.2	3.2	1.4	4	8	Q3
TPS62260DDCT	DDC	5	NSE	179	8	3.2	3.2	1.4	4	8	Q3
TPS62260DRVR	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2
TPS62260DRVT	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2
TPS62261DRVR	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2
TPS62261DRVT	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2
TPS62262DRVR	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2
TPS62262DRVT	DRV	6	NSE	179	8	2.2	2.2	1.2	4	8	Q2

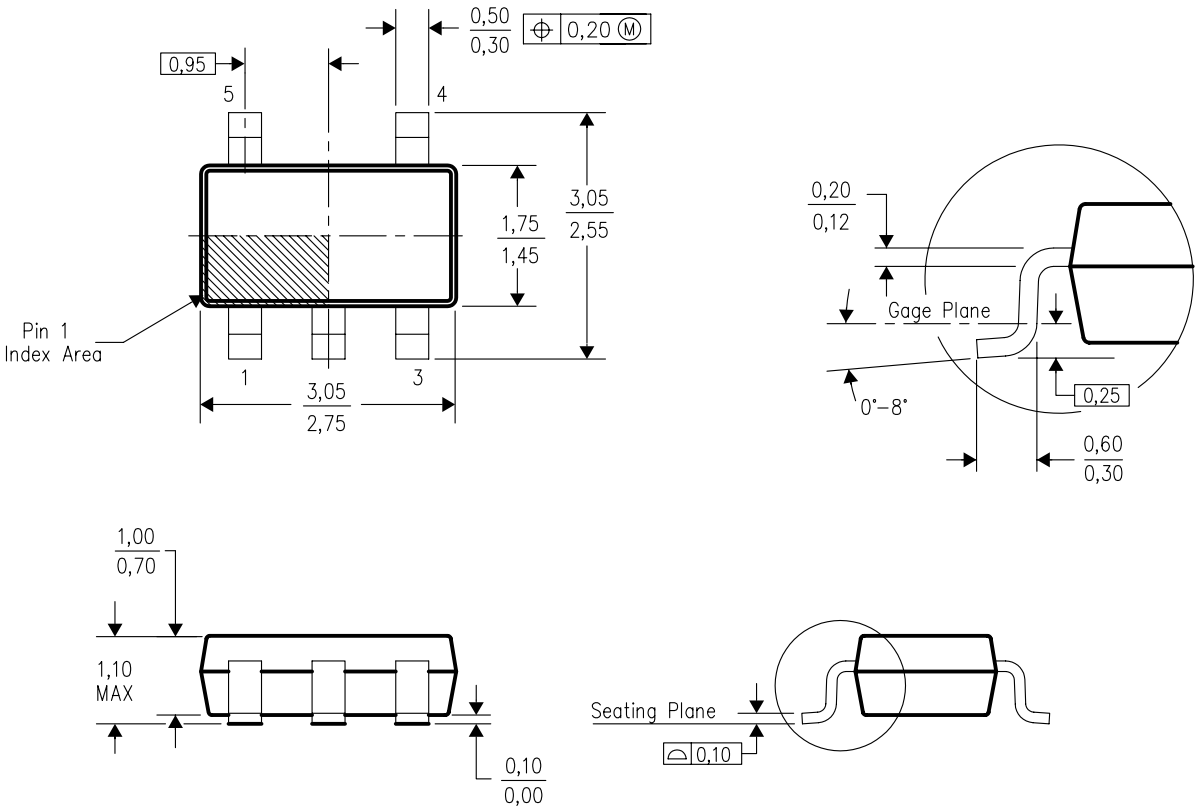


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS62260DDCR	DDC	5	NSE	195.0	200.0	45.0
TPS62260DDCT	DDC	5	MLA	195.0	200.0	45.0
TPS62260DDCT	DDC	5	NSE	195.0	200.0	45.0
TPS62260DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS62260DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS62261DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS62261DRVT	DRV	6	NSE	195.0	200.0	45.0
TPS62262DRVR	DRV	6	NSE	195.0	200.0	45.0
TPS62262DRVT	DRV	6	NSE	195.0	200.0	45.0


HEIGHT
LENGTH
WIDTH

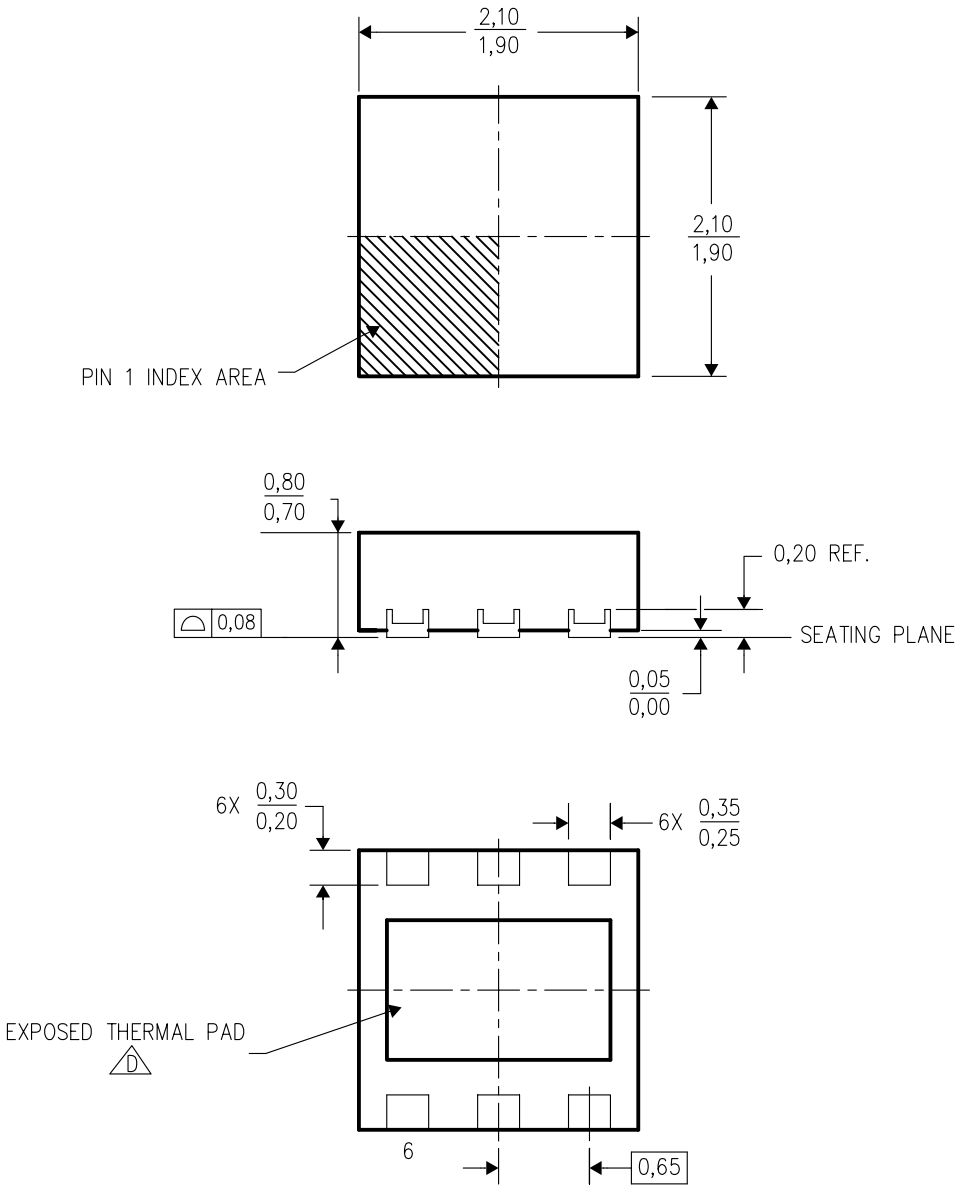
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



4206925/C 01/07

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

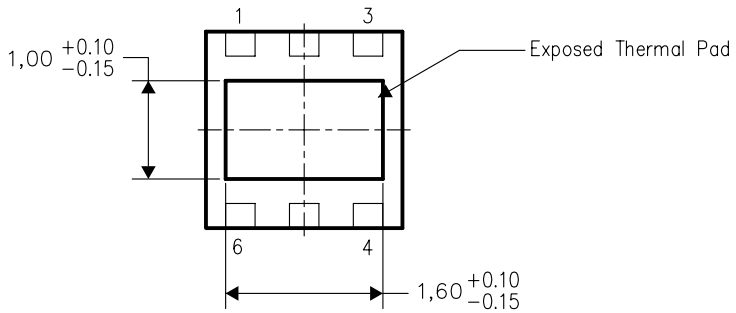
DRV (S–PDSO–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

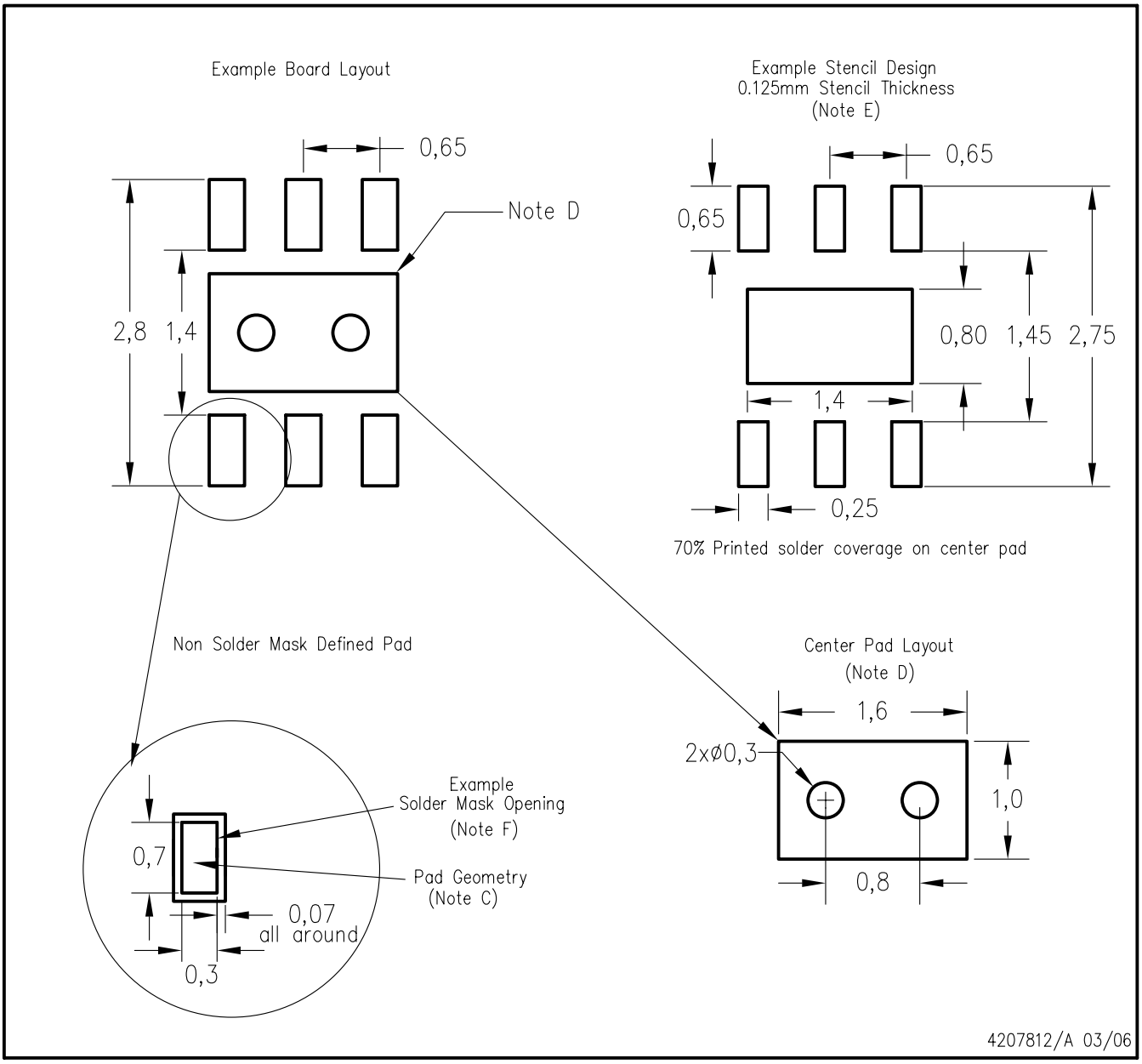


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S–PDSO–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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