TPS61291 Low Iq Boost Converter with Bypass Operation

1 Features

- Input Voltage Range 0.9V to 5V
- Startup Voltage 1.5V at 20mA Load
- Pin Selectable Output Voltages: 3.3V, 3V, 2.5V
- 15nA typical Quiescent Current in Bypass Mode
- 5.7µA typical Quiescent Current in Boost Mode
- Bypass Switch from VIN to VOUT
- I_{OUT} > 200mA at 3.3V V_{OUT}, V_{IN} = 1.8V
- Internal Feedback Divider Disconnect (Bypass Mode)
- Controlled Bypass Transition Prevents Reverse Current into Battery
- Power-Save Mode at Light Loads
- Overtemperature Protection
- Redundant Overvoltage Protection
- Small 2mm x 2mm SON 6-pin package

2 Applications

- Metering (Gas, Water, Smart Meters)
- Remote Controls
- Home Security / Home Automation
- Single 3V Li-MnO_2 or 2 x 1.5V Alkaline Cell Powered Applications

3 Description

The TPS61291 is a boost converter with pin selectable output voltages and an integrated bypass mode. In bypass operation, the device provides a direct path from the input to the system and allows a low power micro controller (MCU) such as the MSP430 to operate directly from a single 3V Li-MnO2 battery or dual alkaline battery cells.

In bypass mode the integrated feedback divider network for boost mode operation is disconnected from the output and the quiescent current consumption drops down to only 15nA (typical).

In boost mode the device provides a minimum output current of 200mA at 3.3V V_{OUT} from 1.8V V_{IN}. The boost mode is used for system components which require a regulated supply voltage and cannot directly operate from the input source. The boost converter is based on a current-mode controller using synchronous rectification to obtain maximum efficiency and consumes typically 5.7uA from the output. During startup of the boost converter, the VSEL pin is read out and the integrated feedback network sets the output voltage to 2.5V, 3V or 3.3V.

Bypass mode or boost mode operation is controlled by the system via the EN/BYP pin.

The device integrates an enhanced bypass mode control to prevent charge, stored in the output capacitor during boost mode operation, from flowing back to the input and charging the battery.

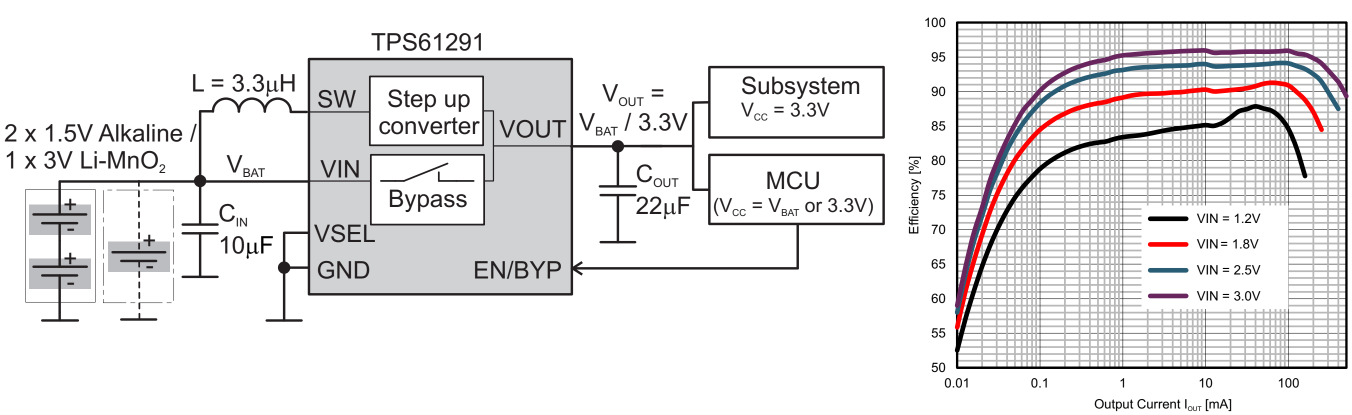
The device is packaged in a small 6-pin SON package (DRV) measuring 2.0mm × 2.0mm x 0.75mm.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61291	SON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic and Efficiency Curves



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4 Revision History

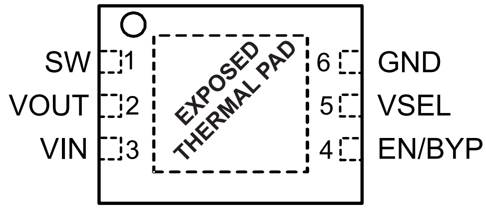
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2014) to Revision A — **Page**

- Changed "Bypass Mode Operation" description 9
- Added sub-section "Controlled Transition into Bypass Mode" 9
- Added NOTE to the "Application and Implementation" section. 10
- Changed "List of Inductors" table 11

5 Pin Configuration and Functions

DRV Package
6 Pin
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1	I	Switch node of the converter. Connect the inductor between this pin and the input capacitor C_{IN}.
VOUT	2	O	Boost converter output. Connect the output capacitor C_{OUT} between this pin and GND close to the device.
VIN	3	PWR	Input voltage supply pin for the boost converter. Connect the input capacitor C_{IN} between this pin and GND as close as possible to the device.
EN/BYP	4	I	Control pin of the device. A high level enables the boost mode operation. A low level disables the boost converter and enables bypass mode operation. EN/BYP must be actively terminated high or low. Usually, this pin is controlled by the MCU in the system.
VSEL	5	I	Output voltage selection pin. The logic level of this pin is read out during startup and internally latched. Connect this pin only to GND, VOUT, or leave it floating.
GND	6	PWR	Ground pin of the device.
EXPOSED THERMAL PAD		NC	Not electrically connected to the IC, but must be soldered to achieve specified thermal performance. Connect this pad to the GND pin and use it as a central GND plane.

Output Voltage Setting

EN/BYP Pin	VSEL Pin at Startup	V_{OUT}	Mode
high	GND	3.3V	Boost Mode Operation
high	VOUT	3.0V	
high	floating	2.5V	
low	GND / VOUT / floating	$V_{OUT} = V_{IN}$ (Bypass Mode)	Bypass Mode Operation

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Pin Voltage Range [2]	VIN	-0.3	5.5	V
	SW	-0.3	7	
	EN/BYP, VOUT	-0.3	5.5	
	VSEL	-0.3	VOUT + 0.3V	
Output Current	In Bypass Operation (EN/BYP = GND)		250	mA
T_J	Maximum Junction Temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) per ANSI/ESDA/JEDEC JS-001, all pins[1]	-2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	-0.5	0.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage for startup	1.5			V
	Supply voltage range (once device has started)	0.9		5	
	Supply voltage range for step up conversion (once device has started)	0.9		V_{OUT}	
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	–40		125	

6.4 Thermal Information

THERMAL METRIC[1]		TPS61291 DRV (2x2 SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	93.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	
ψ_{JT}	Junction-to-top characterization parameter	2.5	
ψ_{JB}	Junction-to-board characterization parameter	41.1	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	11.1	

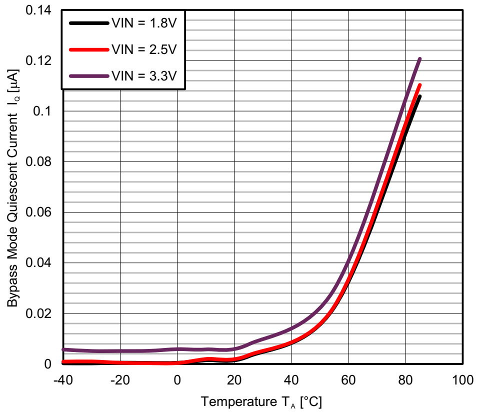
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to 85°C. Typical values are at T_A = 25°C (unless otherwise noted)

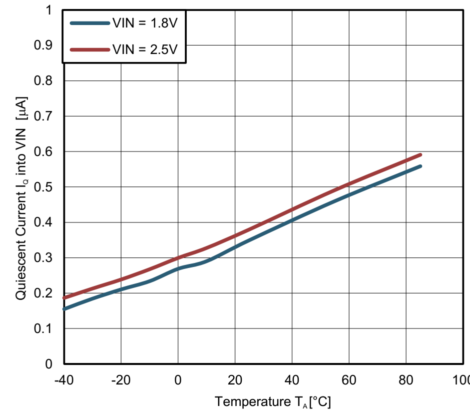
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Startup voltage		V_{OUT} = 3.3V, I_{OUT} = 20mA			1.5	V
	Input voltage range		Operating voltage range	0.9		5	V
I_Q	Quiescent current in boost mode	VIN	I_{OUT} = 0 mA, $V_{EN/BYP}$ = V_{IN} = 1.8 V, V_{OUT} = 3.3V, device not switching		0.4	1.5	µA
		VOUT			5.7	9	µA
	Quiescent current in bypass mode	VIN	$V_{EN/BYP}$ = low, V_{IN} = 3 V, I_{OUT} = 0 mA		0.015	0.5	µA
I_{LkSW}	Leakage current into SW		$V_{EN/BYP}$ = low, V_{IN} = 1.2 V, V_{SW} = 1.2 V		0.01	0.5	µA
V_{UVLO}	Undervoltage lockout threshold		V_{IN} decreasing		0.65	0.9	V
	Overtemperature protection		T_J rising		140		°C
	Overtemperature hysteresis				20		°C
INPUTS							
I_{IN}	EN/BYP, input current		EN/BYP = low or EN/BYP = V_{IN}		0.01	0.1	µA
V_{IL}	EN/BYP, input low voltage		V_{IN} ≤ 1.5 V			0.2 × V_{IN}	V
			5 V > V_{IN} > 1.5 V			0.3	
V_{IH}	EN/BYP, input high voltage		V_{IN} ≤ 1.5 V	0.8 × V_{IN}			V
			5 V > V_{IN} > 1.5 V	1.2			
V_{IL}	VSEL, input low voltage		$V_{EN/BYP}$ = high			0.3	V
V_{IH}	VSEL, input high voltage		$V_{EN/BYP}$ = high	V_{OUT} - 0.3			V
I_{IN}	VSEL, input current		$V_{EN/BYP}$ = high, VSEL = VOUT = 3V		0.01	0.1	µA
POWER SWITCHES							
$R_{DS(ON)}$	Rectifying switch on resistance		V_{OUT} = 3.3 V		0.6		Ω
	Main switch on resistance		V_{OUT} = 3.3 V		0.4		Ω
	Bypass switch on resistance		V_{IN} = 1.8V, I_{OUT} = 50 mA, EN/BYP = low		1.2		Ω
I_{SW}	Switch current limit		V_{OUT} = 3.3V	700	1000	1300	mA
OUTPUT							
V_{OUT}	Output voltage accuracy		V_{IN} = 1.8V, I_{OUT} = 10 mA, V_{OUT} 3.3V, 3.0V, 2.5V, EN/BYP = high	-2	+1	+4	%
	Line regulation		V_{OUT} = 3.3V, V_{IN} = 2V to 3.0V, I_{OUT} = 50 mA, EN/BYP = high		+0.15		%/V
	Load regulation		V_{IN} = 2V, V_{OUT} = 3.3V, I_{OUT} = 1 mA to 200 mA, EN/BYP = high		-0.007		%/mA
V_{OVP}	Output overvoltage protection		V_{OUT} rising, EN/BYP = high		5.4		V

6.6 Typical Characteristics



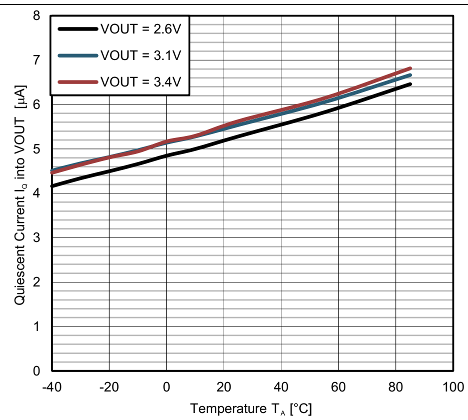
EN/BYP = low VSEL = low IOUT = 0mA

Figure 1. Quiescent Current I_Q into VIN Pin in Bypass Mode



EN/BYP = high Boost mode operation
Device not switching

Figure 2. Quiescent Current I_Q into VIN Pin in Boost Mode



EN/BYP = high Boost mode operation
IOUT = 0mA Device not switching

Figure 3. Quiescent Current I_Q into VOUT Pin in Boost Mode

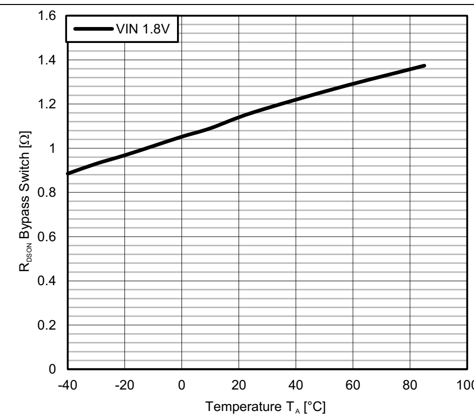
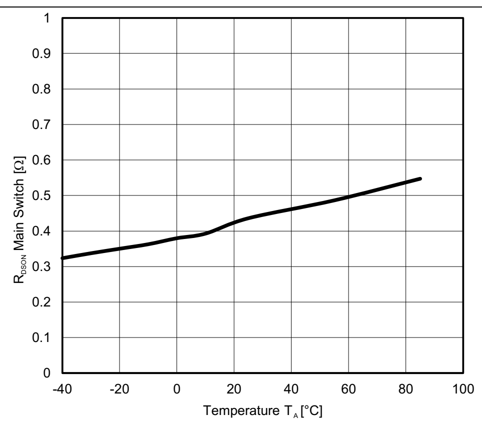
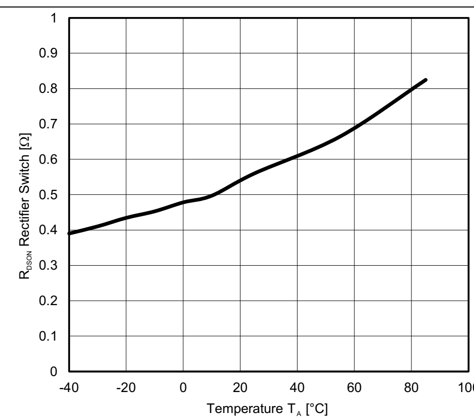


Figure 4. R_{DSON} Bypass Switch



VOUT = 3.3V

Figure 5. R_{DSON} Main Switch



VOUT = 3.3V

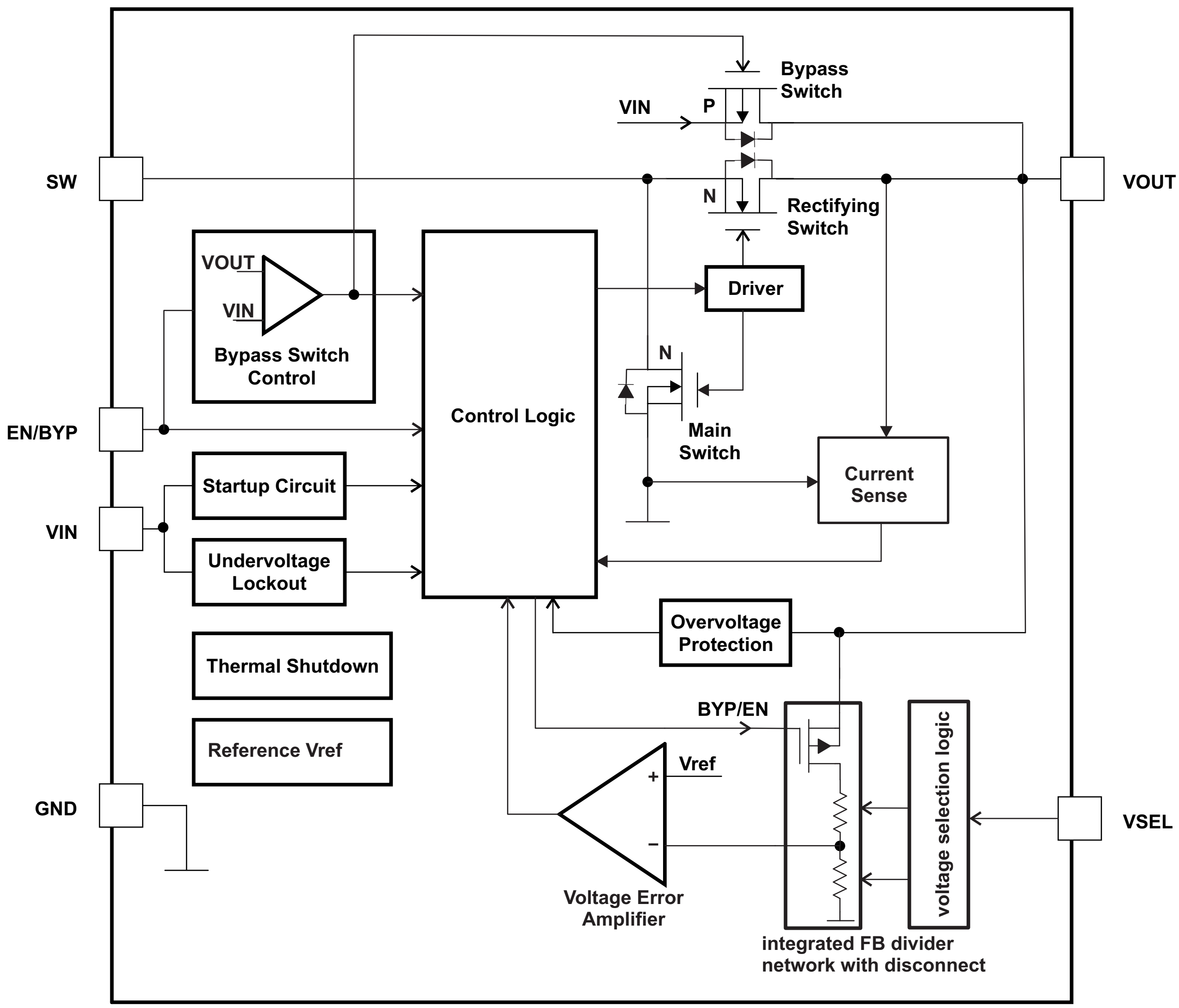
Figure 6. R_{DSON} Rectifier Switch

7 Detailed Description

7.1 Overview

The TPS61291 provides two operating modes: high efficiency boost mode to generate an output voltage higher than the input voltage and bypass mode, which connects the output of the device directly to the input.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bypass / Boost Mode Operation EN/BYP

The EN/BYP pin selects the operating mode of the device. With the EN/BYP pin pulled low, the device operates in bypass mode. With a high level on the EN/BYP pin, the device operates as a boost converter. The EN/BYP pin is usually controlled by an I/O pin of a MCU, powered from the output of the TPS61291 and should not be left floating. See Figure 8. See also sections Boost Mode Operation and Bypass Mode Operation for more detailed descriptions.

Feature Description (continued)

7.3.2 Output Voltage Selection VSEL

In boost mode operation, the device supports three internally set output voltages: 2.5V, 3V and 3.3V. Leaving the VSEL pin open sets the output voltage to 2.5V, VSEL = VOUT to 3.0V and VSEL= GND to 3.3V. The VSEL pin condition is detected during the startup of the boost converter and internally latched. For proper operation, it must be connected to either GND, VOUT or left floating. Depending on the VSEL condition, an integrated feedback divider network is selected. Changing the VSEL pin condition during operation does not change the output voltage.

7.3.3 Feedback Divider Disconnect

In boost mode operation, the integrated feedback divider network, which is required for regulation, is connected to the VOUT pin. To achieve the low quiescent current in bypass mode, the integrated feedback divider network is disconnected from the output pin VOUT.

7.3.4 Undervoltage Lockout

An undervoltage lockout function stops the operation of the boost converter if the input voltage drops below the undervoltage lockout threshold. This function is implemented in order to prevent malfunction of the boost converter. The undervoltage lockout function has no control of the bypass switch.

7.3.5 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal junction temperature in boost mode operation. If the junction temperature exceeds the threshold (140 °C typical), the device stops operating. As soon as the junction temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold. The overtemperature protection is not active in bypass mode operation.

7.3.6 Overvoltage Protection

In boost mode operation (EB/BYP = high), the device features a redundant over voltage protection circuit (OVP), which is independent from the reference, the regulation loop and feedback divider network. The redundant over voltage protection circuit limits the output voltage to typically 5.4V. The over voltage protection can only limit the output voltage in boost mode operation, when the input voltage V_{IN} is smaller than the output voltage V_{OUT}.

7.4 Device Functional Modes

7.4.1 Boost Mode Operation

The device is enabled and operates in boost mode operation when the EN/BYP pin is set high. The bypass switch is turned off once the boost converter has started switching.

In boost mode operation, the device is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 300 mA and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuous to keep the efficiency high at low load conditions. To achieve high efficiency, the power stage is realized as a synchronous boost topology.

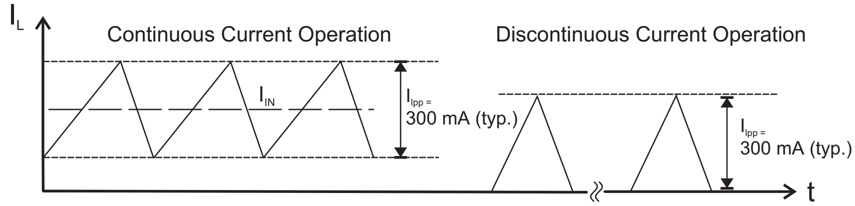


Figure 7. Hysteretic Current Operation

Device Functional Modes (continued)

The output voltage V_{OUT} is monitored via the integrated feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.

The hysteretic current mode architecture allows fast response to load variations.

7.4.2 Bypass Mode Operation

The TPS61291 includes a P-channel MOSFET (Bypass Switch) between the VIN and VOUT pins. When the IC is disabled (EN/BYP = low), bypass mode is activated to provide a direct, low impedance connection from the input voltage (at the VIN pin) to the load (V_{OUT}). The bypass switch is not impacted by undervoltage lockout, or thermal shutdown. The bypass switch is not current-limit controlled. In bypass operation, the OVP circuit is disabled.

7.4.3 Controlled Transition into Bypass Mode

When changing from boost mode into bypass mode, the output capacitor is usually charged up to a higher voltage than the battery voltage V_{BAT}. In order to prevent current flowing from the output capacitor C_{OUT} via the bypass switch into the battery (reverse battery current), the internal bypass control circuit delays the bypass switch activation until the output voltage V_{OUT} has decreased to the input voltage level.

7.4.4 Operation at Output Overload

If the peak inductor current reaches the internal switch current limit threshold in boost mode operation, the main switch is turned off to stop a further increase of the input current. In this case the output voltage will decrease since the device cannot provide sufficient power to maintain the set output voltage. If the output voltage drops below the input voltage, the backgate diode of the rectifying switch gets forward biased and current starts to flow through it. Because this diode cannot be turned off, the load current is only limited by the remaining DC resistance. As soon as the overload condition is removed, the converter automatically resumes normal operation and enters the appropriate soft start mode depending on the operating conditions.

7.4.5 Startup

After the EN/BYP pin is tied high, the device starts to operate. If the input voltage is not high enough to supply the control circuit properly, a startup oscillator starts to operate the switches. During this phase, the switching frequency is controlled by the oscillator and the switch current is limited. As soon as the device has built up the output voltage to about 1.8 V, high enough for supplying the control circuit, the device switches to its normal hysteretic current mode operation.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61291 is a boost converter with pin selectable output voltages and an integrated bypass mode. In bypass operation, the device provides a direct path from the input to the system and allows a low power micro controller (MCU) to operate directly from a single 3V Li-MnO2 battery or dual alkaline battery cells. In bypass mode, the quiescent current consumption is typically only 15nA and supports low power modes of MCUs such as the MSP430. In boost mode operation, the device provides a regulated output voltage (e.g. 3.3V) to supply circuits which require a higher voltage than provided by the battery. See Figure 8.

The device also extends battery life in applications which can run partially directly from the battery, but need a boost conversion to maintain sufficient system voltage when the battery voltage drops due to discharge. In this case, the system runs off the battery in bypass mode operation until the battery voltage trips the minimum system operating voltage. Then the system turns on the boost converter, providing a sufficient output voltage down to the cut off voltage of the battery. See Figure 9 and Figure 26.

8.2 Typical Application

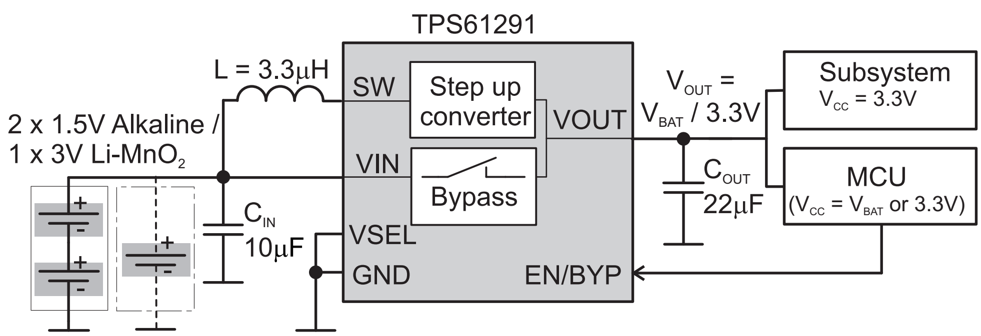


Figure 8. Typical Application Circuit with Regulated 3.3V VOUT / VBAT

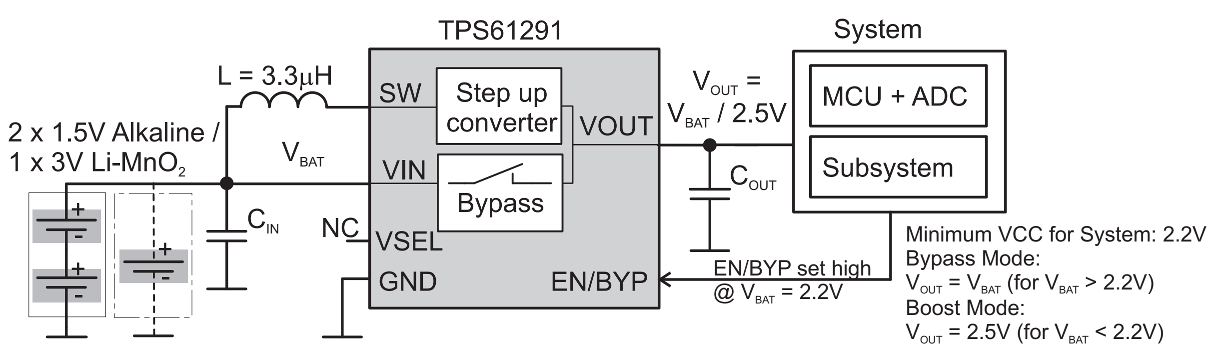


Figure 9. Bypass Mode / Boost Mode Operation to Maintain Sufficient System Voltage

8.2.1 Design Requirements

The TPS61291 is a highly integrated boost converter. The output voltage is set internally via a VSEL pin without any additional components. For operation, only an input capacitor, output capacitor, and an inductor are required. Table 1 shows the components used for the application characteristic curves.

Typical Application (continued)

Table 1. Components for Application Characteristic Curves[1]

Reference	Description	Value	Manufacturer	
TPS61291	Low Iq Boost Converter with Bypass Operation		Texas Instruments	
C_{IN}	Input capacitor	10µF	Murata	GRM219R61A106KE44D
C_{OUT}	Output capacitor	22µF	Murata	GRM21BR60J226ME39L
L	Inductor	3.3µH	Coilcraft	LPS3314 3R3

(1) See the Third-Party Products Disclaimer in the Device Support section.

8.2.2 Detailed Design Procedure

The external components have to fulfill the needs of the application but also the stability criteria of the device's control loop. The TPS61291 is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance must be considered together. The output capacitor sets the corner frequency of the converter while the inductor creates a Right-Half-Plane-Zero degrading the stability of the converter. Consequently with a larger inductor a bigger capacitor has to be used to guarantee a stable loop. Table 2 shows the output filter component selection.

Table 2. Recommended LC Output Filter Combinations

Output voltage [V]	Inductor value [µH][1]	Output capacitor value [µF][2]		
		22	22 + 10	2 x 22
3.3 / 3.0	3.3	√[3]	√	√
	4.7			√
2.5	2.2	√	√	√
	3.3		√[3]	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.1 Inductor Selection

The device is optimized to operate with a 3.3µH inductor value. Other inductor values can be used, per Table 2. The maximum inductor current can be approximated by the I_{LMAX}, from Equation 1. For proper operation, the inductor needs to be rated for a saturation current which is higher than the switch current limit of typically 1A. Table 3 lists inductors that have been tested with the TPS61291.

$$I_{L\,max} := \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN}} + 150\ \text{mA} \quad \text{continuous current operation}$$

$$I_{L\,max} := 300\ \text{mA} \quad \text{discontinuous current operation} \tag{1}$$

Table 3. List of Inductors[1]

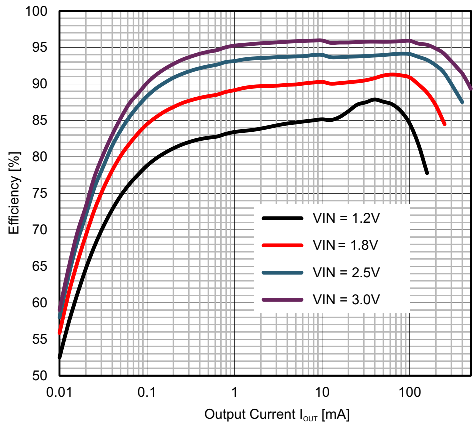
INDUCTANCE	DIMENSIONS [mm³]	TYPE	SUPPLIER
3.3	3.3 x 3.3 x 1.3	LPS3314	Coilcraft
3.3	2.95 x 2.95 x 1.4	LPS3015	
3.3	3 x 2.5 x 1.5	VLF302515	TDK
3.3	2 x 2 x 1.2	MDMK2020T3R3M	Taiyo Yuden
3.3	2.5 x 2.0 x 1.2	DFE252012	Toko
3.3	3.0 x 3.0 x 1.5	74438335033	Würth

(1) See the Third-Party Products Disclaimer in the Device Support section.

8.2.2.2 Input and Output Capacitor Selection

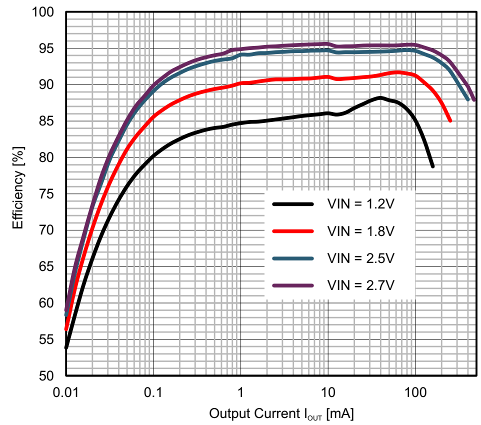
For best output and input voltage filtering, low ESR X5R or X7R ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. At least a 10µF or larger input capacitor is recommended for operation. In applications in which the power source (e.g. certain battery chemistries) shows an internal resistance characteristic, a larger input capacitor might be used to buffer the supply voltage for the TPS61291. The recommended typical output capacitor value is 22 µF and can vary as outlined in the output filter selection Table 2.

8.2.3 Application Curves



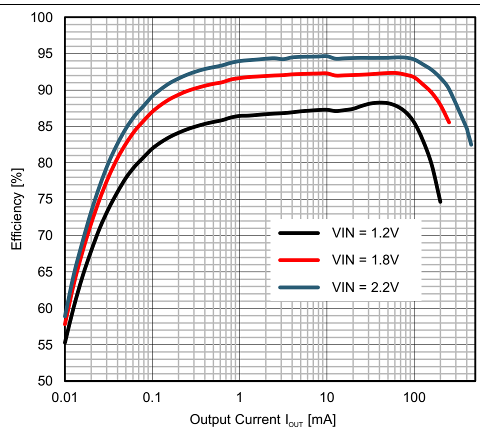
EN/BYP = high L = 3.3µH VSEL = GND

Figure 10. Efficiency vs I_{OUT}, V_{OUT} = 3.3V



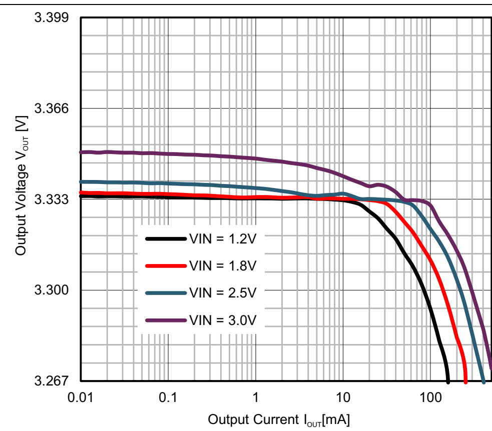
EN/BYP = high L = 3.3µH VSEL = VOUT

Figure 11. Efficiency vs I_{OUT}, V_{OUT} = 3.0V



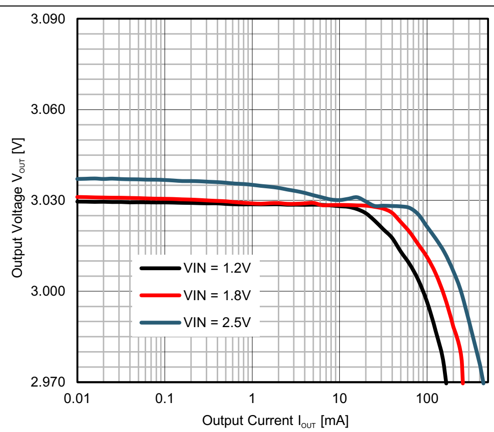
EN/BYP = high L = 3.3µH VSEL = open

Figure 12. Efficiency vs I_{OUT}, V_{OUT} = 2.5V



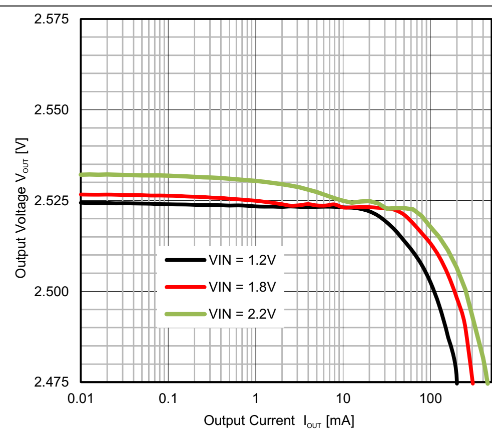
EN/BYP = high L = 3.3µH VSEL = GND

Figure 13. Output Voltage vs Output Current VOUT = 3.3V



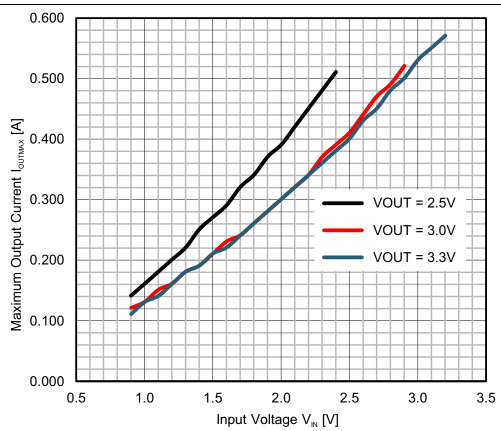
EN/BYP = high L = 3.3µH VSEL = VOUT

Figure 14. Output Voltage vs Output Current VOUT = 3.0V



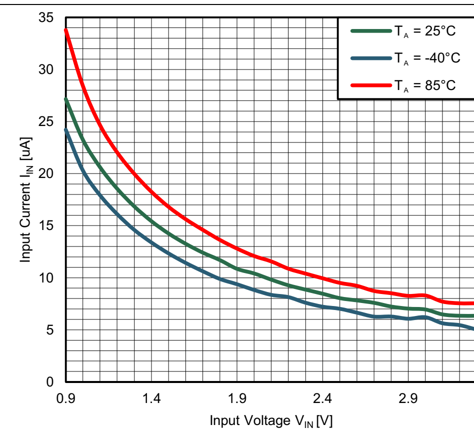
EN/BYP = high L = 3.3µH VSEL = open

Figure 15. Output Voltage vs Output Current VOUT = 2.5V



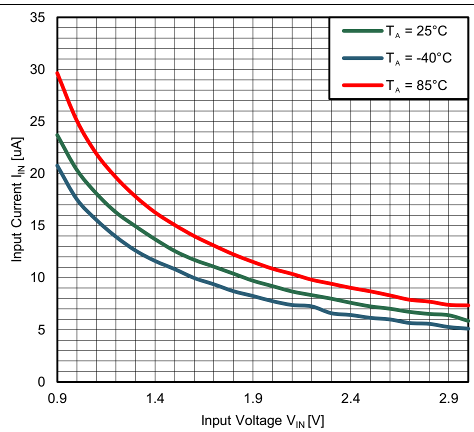
EN/BYP = high
L = 3.3µH
I_{SW} = 1000mA (typical)
Boost mode operation

Figure 16. Maximum Output Current



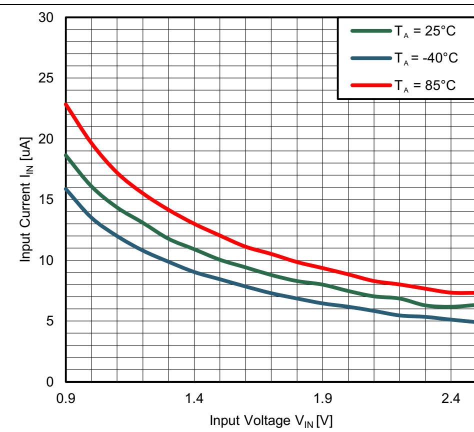
V_{OUT} = 3.3 V
I_{OUT} = 0 mA
L = 3.3 µH
C_{OUT} = 22 µF
Device switching

Figure 17. Supply Current vs. V_{IN}, V_{OUT} = 3.3V, I_{OUT} = 0mA



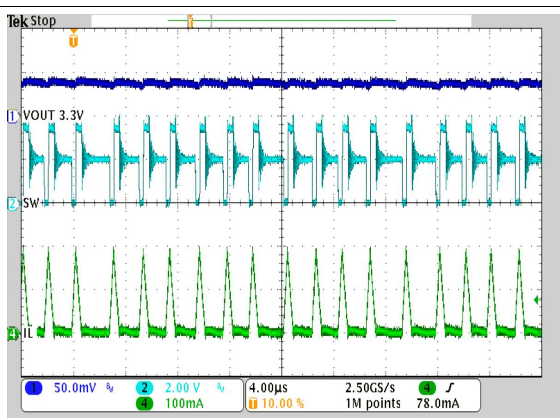
V_{OUT} = 3.0 V
I_{OUT} = 0 mA
L = 3.3 µH
C_{OUT} = 22 µF
Device switching

Figure 18. Supply Current vs. V_{IN}, V_{OUT} = 3.0V, I_{OUT} = 0mA



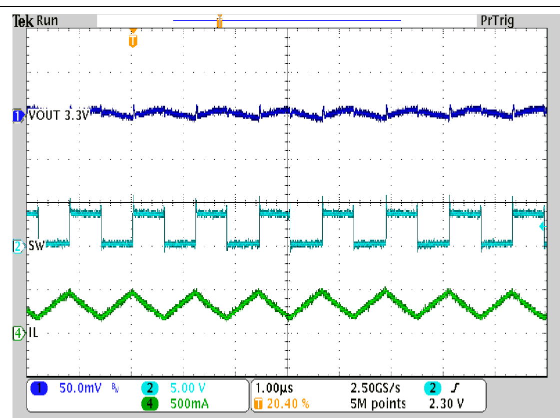
V_{OUT} = 2.5 V
I_{OUT} = 0 mA
L = 3.3 µH
C_{OUT} = 22 µF
Device switching

Figure 19. Supply Current vs. V_{IN}, V_{OUT} = 2.5V, I_{OUT} = 0mA



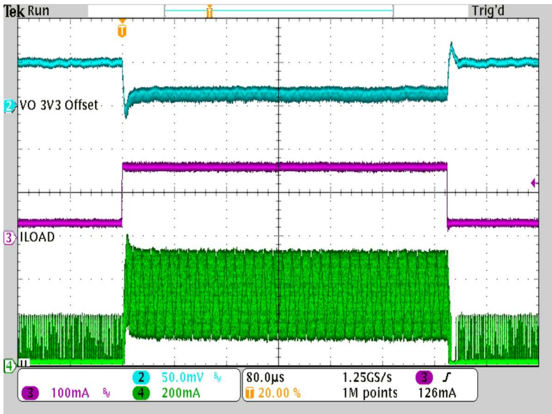
V_{IN} = 2.0 V
V_{OUT} = 3.3 V
L = 3.3 µH
I_{OUT} = 15mA
C_{OUT} = 22 µF
VSEL = GND
EN/BYP = high

Figure 20. Discontinuous Conduction Mode Operation, V_{OUT} = 3.3V



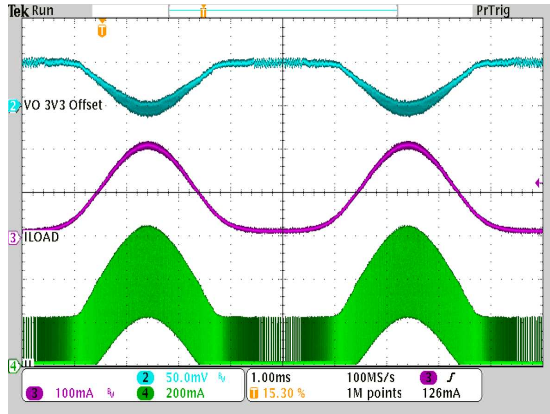
V_{IN} = 1.8 V
V_{OUT} = 3.3 V
VSEL = GND
L = 3.3 µH
C_{OUT} = 22 µF
I_{OUT} = 150 mA
EN/BYP = high

Figure 21. Continuous Conduction Mode Operation, V_{OUT} = 3.3V



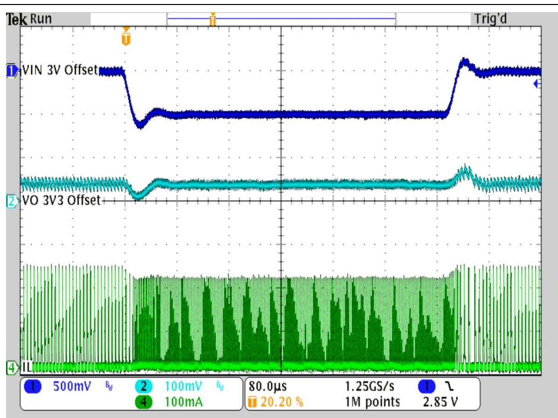
V_{IN} = 1.8V L = 3.3µH C_{OUT} = 22 µF
V_{OUT} = 3.3V VSEL = GND
ILOAD 20mA /150mA

Figure 22. Load Transient Response



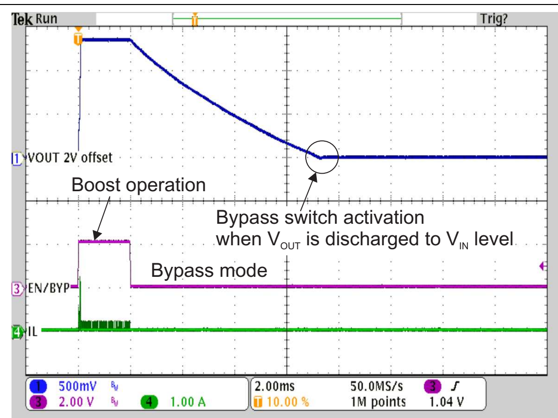
V_{IN} = 1.8V L = 3.3µH C_{OUT} = 22 µF
V_{OUT} = 3.3V VSEL = GND
ILOAD 1mA/200mA

Figure 23. AC Load Sweep



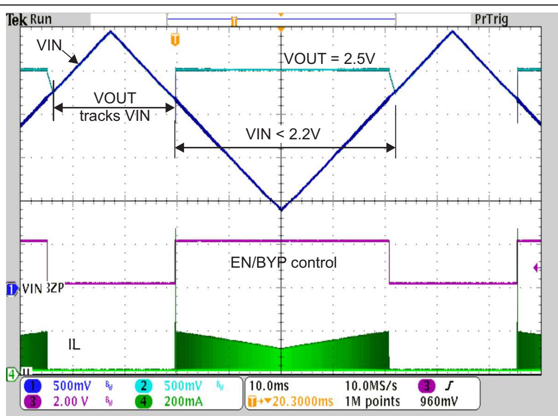
V_{IN} = 2.5V/3V L = 3.3µH C_{OUT} = 22 µF
V_{OUT} = 3.3V VSEL = GND Load =100Ω

Figure 24. Line Transient Response



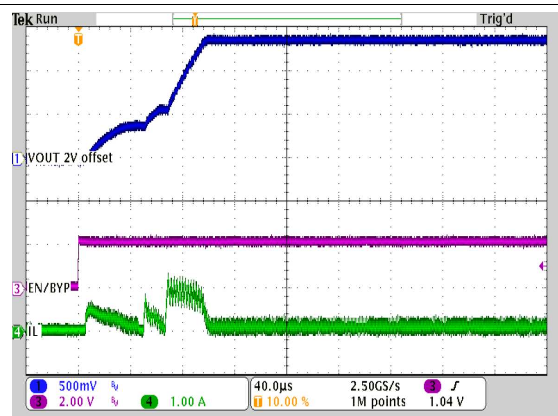
V_{IN} = 2.0V L = 3.3µH C_{OUT} = 22 µF
V_{OUT} = 3.3V VSEL = GND R_{LOAD} = 1kΩ

Figure 25. Boost Mode / Bypass Mode Transition



V_{IN} = 0.9V to 3V VSEL = Open ILOAD = 5mA
V_{OUT} = 2.5V EN/BYP externally controlled
Bypass / Boost mode operation

Figure 26. Bypass / Boost Mode Operation



V_{IN} = 2.0V L = 3.3µH C_{OUT} = 22 µF
V_{OUT} = 3.3V VSEL = GND R_{LOAD} = 100Ω

Figure 27. Startup in Boost Mode

9 Power Supply Recommendations

The input power supply needs to have a current rating according to the supply voltage, output voltage and output current of the TPS61291.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths. In a boost converter, the ripple current on the output is larger than the ripple current on the input. The output capacitor needs to be placed as close as possible between the VOUT and the GND pins. The input capacitor should be placed as close as possible to the VIN and GND pins. Place the inductor close by the IC and connect it with short and thick traces to the IC. Avoid current loops to minimize radiated noise and stray fields. The exposed thermal pad of the package and the GND pin must be connected. See Figure 28 for the recommended PCB layout.

10.2 Layout Example

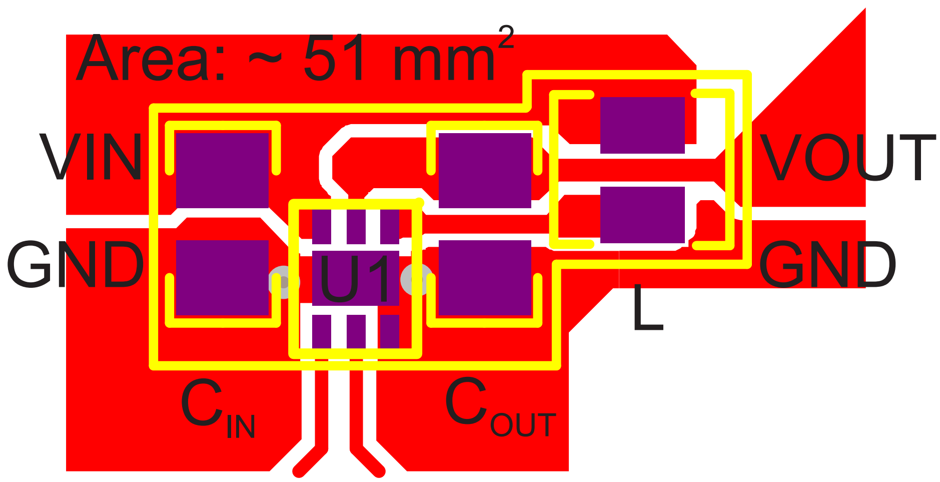


Figure 28. Recommended PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

TPS61291EVM-569 User's Guide, SLVUA29

11.3 Trademarks

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61291DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PC4I	Samples
TPS61291DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PC4I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

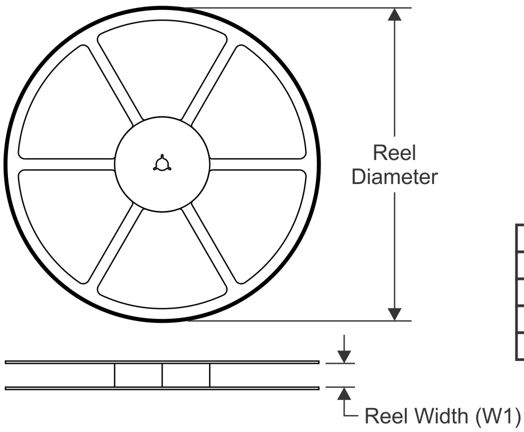
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

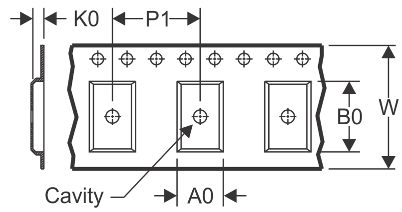
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

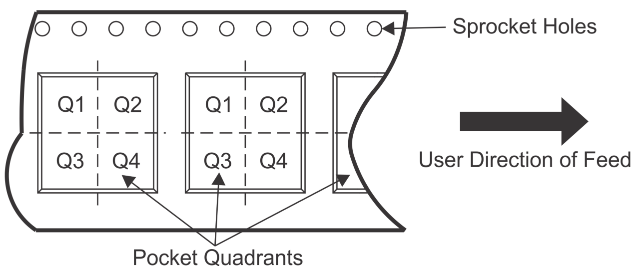


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

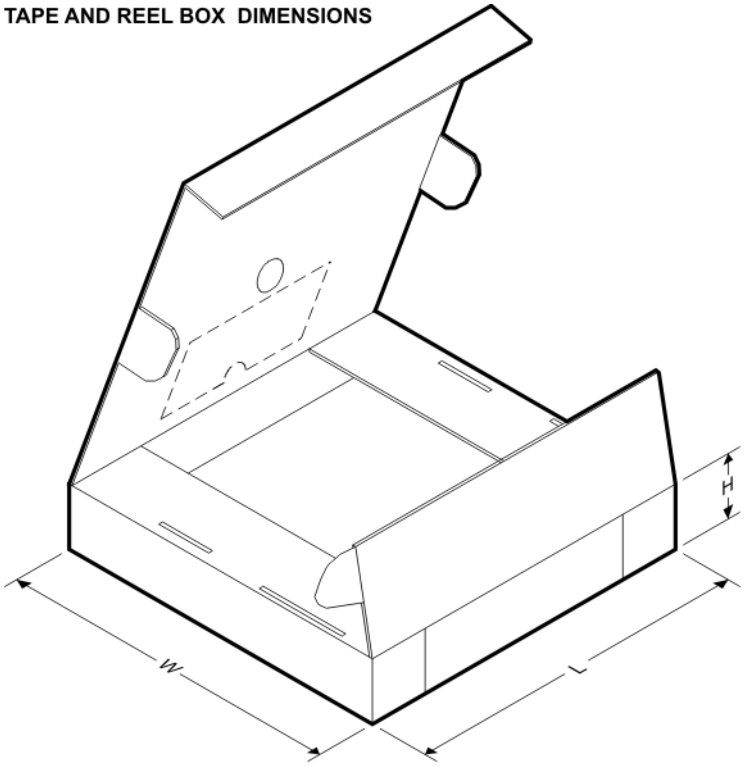
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61291DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61291DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

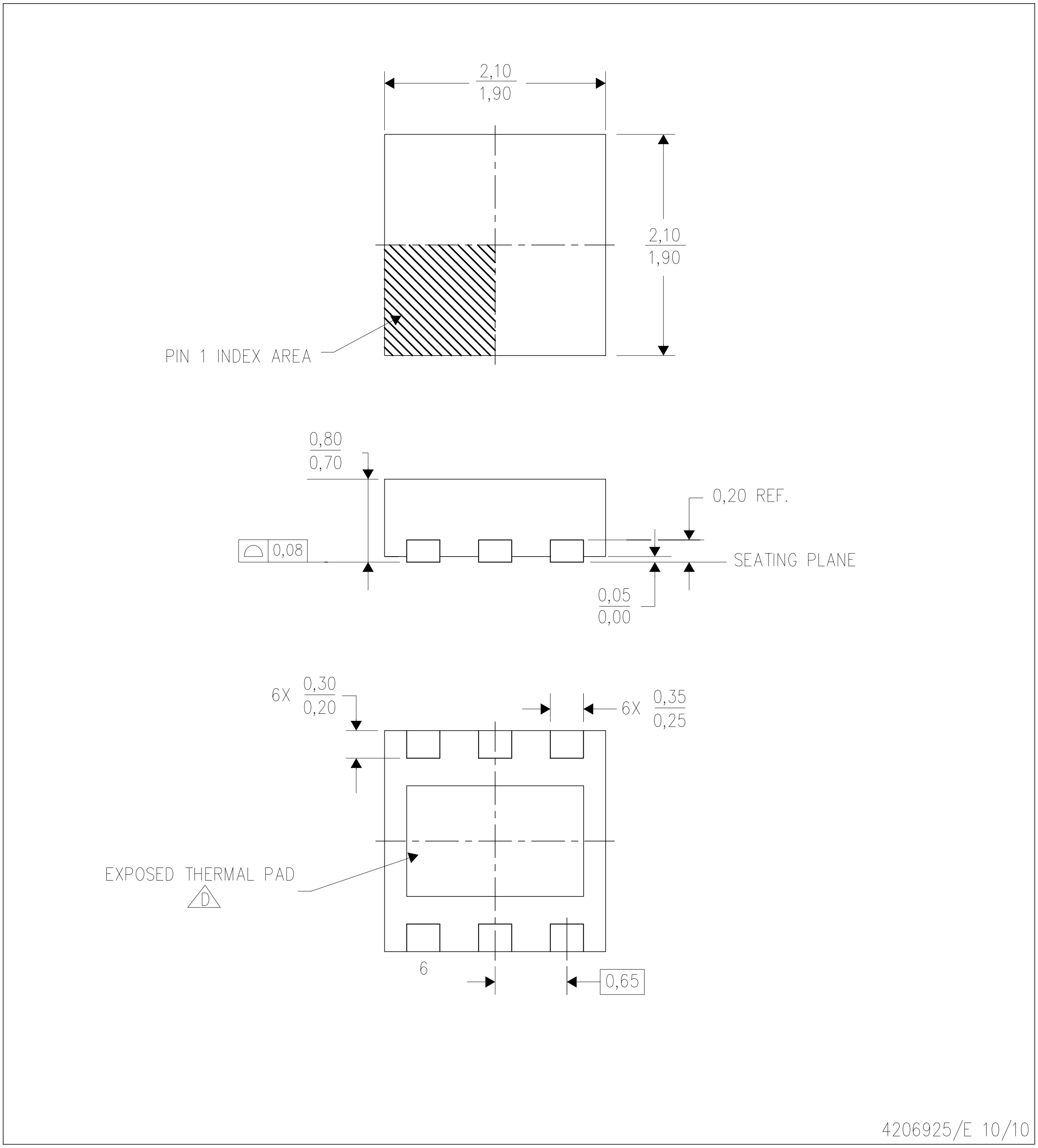
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61291DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61291DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

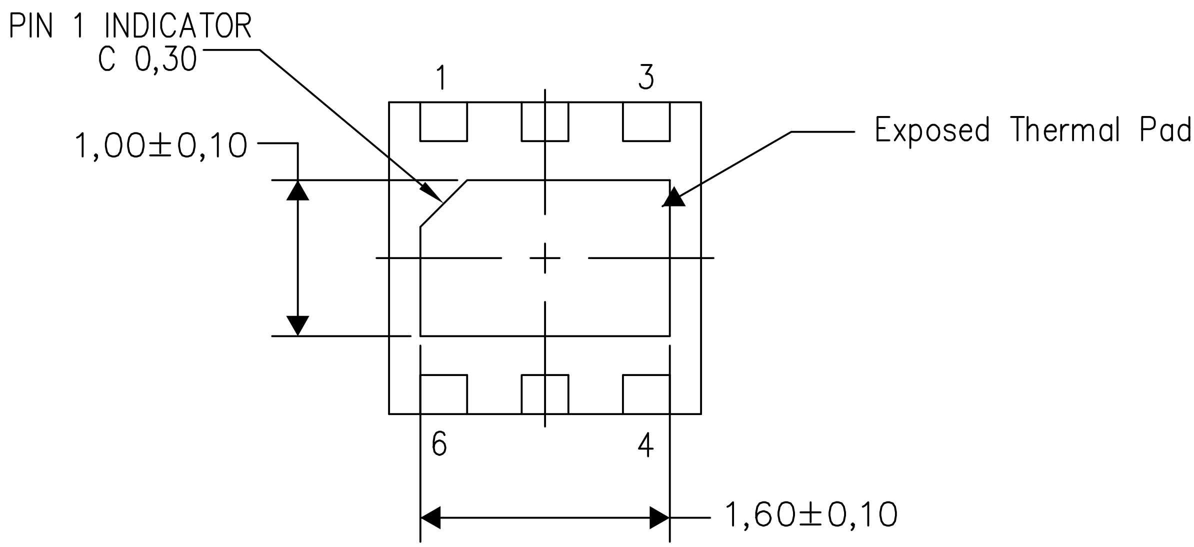
DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



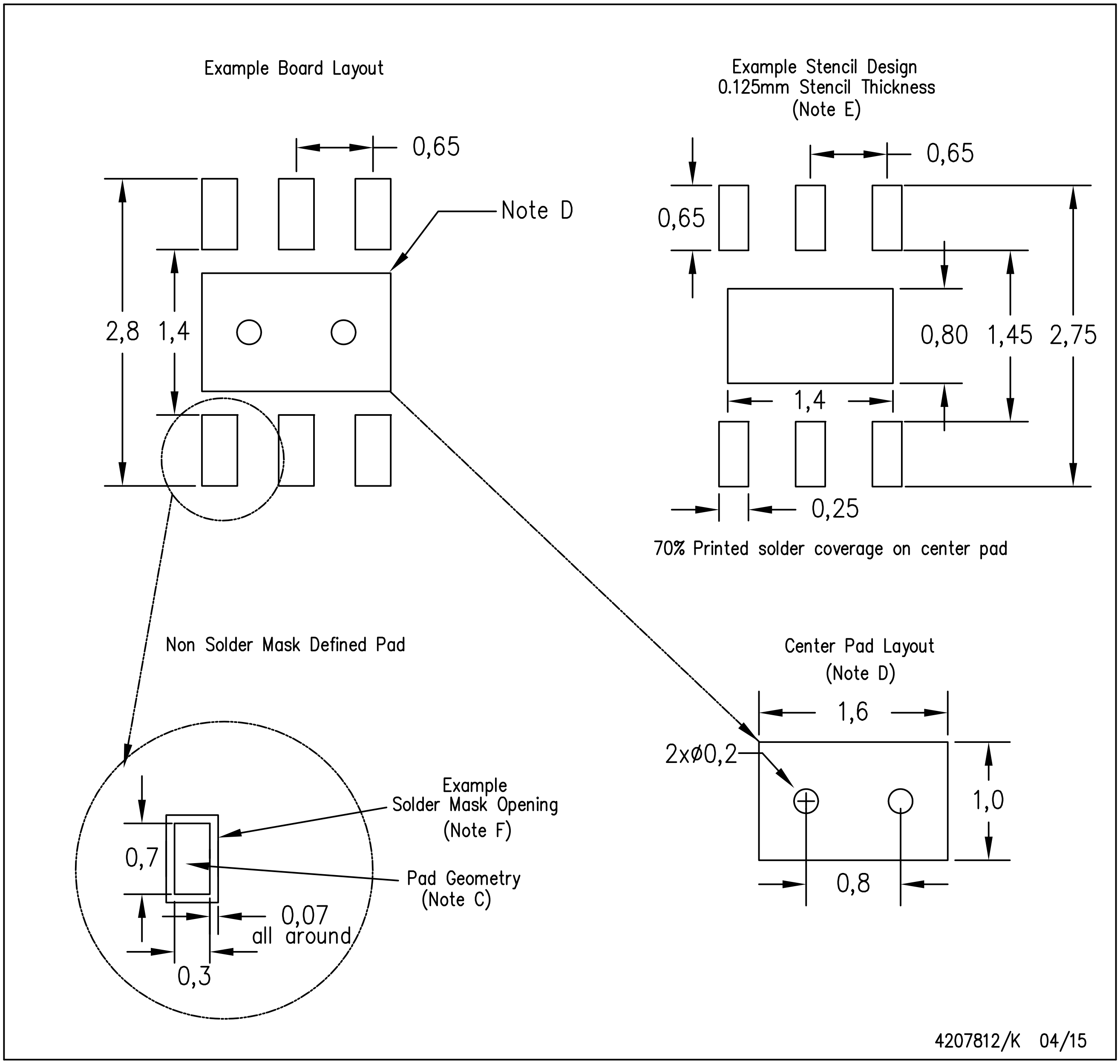
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.