TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade
    - TPS61240IDRVRQ1: Grade 3, –40°C to +85°C Ambient Operating Temperature
    - TPS61240TDRVRQ1: Grade 2, –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Efficiency > 90% at Nominal Operating Conditions
- Total DC Output Voltage Accuracy 5 V ±2%
- Typical 30 μA Quiescent Current
- *Best in Class* Line and Load Transient
- Wide V_{IN} Range From 2.3 V to 5.5 V
- Output current up to 450 mA
- Automatic PFM/PWM Mode transition
- Low Ripple Power Save Mode for Improved Efficiency at Light Loads
- Internal Softstart, 250 μs typical Start-Up time
- 3.5 MHz Typical Operating Frequency
- Load Disconnect During Shutdown
- Current Overload and Thermal Shutdown Protection
- Only Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Total Solution Size < 13 mm^2
- Available in a 2 mm × 2 mm WSON Package

2 Applications

- Advanced Driver Assistance Systems (ADAS)
  - Front Camera
  - Surround View System ECU
  - Radar and LIDAR
- Automotive Infotainment and Cluster
  - Head Unit
  - HMI and Display
- Body Electronics and Lighting
- Factory Automation and Control

3 Description

The TPS61240-Q1 device is a high efficient synchronous step up DC-DC converter optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The TPS61240-Q1 supports output currents up to 450 mA. The TPS61240-Q1 has an input valley current limit of 500 mA.

TPS61240-Q1 device provides fixed output voltage of 5V-typ with an input voltage range of 2.3 V to 5.5 V and the device supports batteries with extended voltage range. During shutdown, the load is completely disconnected from the battery. The TPS61240-Q1 boost converter is based on a quasi-constant on-time valley current mode control scheme.

The TPS61240-Q1 presents a high impedance at the V_{OUT} pin when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS61240-Q1 is shut down.

During light loads the device will automatically pulse skip allowing maximum efficiency at lowest quiescent currents. In the shutdown mode, the current consumption is reduced to less than 1 μA.

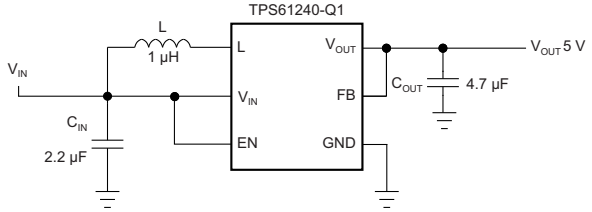
TPS61240-Q1 allows the use of a small inductor and capacitors to achieve a small solution size. The TPS61240-Q1 is available in a 2 mm × 2 mm WSON package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61240-Q1	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2016) to Revision B **Page**

- Added the AEC-Q100 qualified information to the *Features* section ... 1
- Added operating ambient temperature for T version of device (TPS61240TDRVRQ1) in the *Recommended Operating Conditions* table ... 5
- Added shutdown current for T version of device (TPS61240TDRVRQ1) in the *Electrical Characteristics* table ... 6
- Changed the *Electrostatic Discharge Caution* statement ... 18

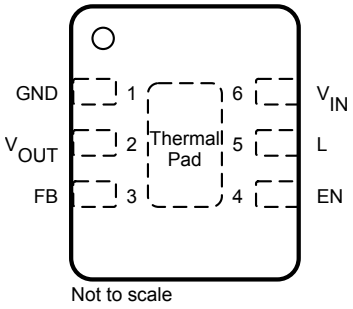
Changes from Original (December 2010) to Revision A **Page**

- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed TPS6124x to TPS61240-Q1 throughout document ... 1
- Changed *Description* section ... 1
- Deleted Ordering Information table ... 1
- Changed *Pin Functions* figure and table ... 4
- Deleted Dissipation Ratings table ... 5
- Added Inductance and Output capacitance values and table note to *Recommended Operating Conditions* ... 5
- Added *Thermal Information* table ... 5
- Changed reference to *Typical Applications* section ... 6
- Changed V_{OUT} test condition to 2.3 V to ≤ V_{IN} ≤ V_{OUT} ... 6
- Added equals before 2.3 V in Output current test condition ... 6
- Removed I_{SW} from all rows except Switch valley current limit ... 6
- Changed Operating quiescent current test condition by adding device not switching ... 6
- Added equals before 600 mVp-p in Line transient response test condition ... 6
- Moved figures 8 through 16 to *Application Curves* section ... 7
- Updated titles of figures 2 through 7 for better clarity Figure 2 ... 7

- Deleted *Parameter Measurement Information* section 9
- Changed Updated *Overview* section for more clarity 9
- Changed Figure 8 Inductor/Rectifier Currents in Current Limit Operation waveform..... 10
- Added Under no load conditions to *Soft Start* section..... 11
- Deleted HDMI / USB-OTG Application title 12
- Updated *Inductor Selection* section..... 13
- Deleted *List of Inductors* table and listed one example inductor in description 13
- Changed 2.7 µF to 2.3 µF in *Output Capacitor* section 14

5 Pin Configuration and Functions

DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	GND	Power ground and IC ground
2	V_{OUT}	O	Output Supply pin. Connected to the load
3	FB	I	Feedback for regulation.
4	EN	I	Positive polarity. Low = IC shutdown.
5	L	I	Inductor connection to FETs
6	V_{IN}	I	Supply from battery
—	PAD	—	For good thermal performance, this pad must be soldered to the land pattern on the PCB

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage, V_I (on V_{IN}, L, and EN)	–0.3	7	V
Voltage on V_{OUT}	–2	7	V
Voltage on FB	–2	14	V
Peak output current	Internally limited		
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage at V_{IN}		2.3		5.5	V
L	Inductance		1		2.2	µH
C_{out}	Output capacitance		1		20	µF
T_A	Operating ambient temperature(1)	TPS61240IDRVRQ1	–40		85	°C
		TPS61240TDRVRQ1	–40		105	°C

(1) In applications where high power dissipation, poor package thermal resistance, or both are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$

6.4 Thermal Information

THERMAL METRIC(1)		TPS61240-Q1 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over full operating ambient temperature range with typical values at T_A = 25°C. Specifications apply for condition V_{IN} = EN = 3.6 V (unless otherwise noted). External components C_{IN} = 2.2 µF, C_{OUT} = 4.7 µF (0603), and L = 1µH (refer to *Typical Applications* section).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE						
V_{IN}	Input voltage range		2.3		5.5	V
V_{OUT}	Fixed output voltage range	2.3 V ≤ V_{IN} ≤ V_{OUT}, 0 mA ≤ I_{OUT} ≤ 200 mA	4.9	5	5.1	V
V_{O_Ripple}	Ripple voltage, PWM mode	I_{LOAD} = 150 mA			20	mVpp
	Output current	VIN = 2.3 V to 5.5 V	200			mA
I_{SW}	Switch valley current limit	V_{OUT} = V_{GS} = 5 V	500	600		mA
	Short circuit current	V_{OUT} = V_{GS} = 5 V	200	350		mApk
	High side MOSFET on-resistance(1)	V_{IN} = V_{GS} = 5 V, T_A = 25°C(1)		290		mΩ
	Low Side MOSFET on-resistance(1)	V_{IN} = V_{GS} = 5 V, T_A = 25°C(1)		250		mΩ
	Operating quiescent current	I_{OUT} = 0 mA, power save mode, device not switching		30	40	µA
	Shutdown current	TPS61240IDRVRQ1, EN = GND			1.5	µA
		TPS61240TDRVRQ1, EN = GND			2.5	
	Reverse leakage current V_{OUT}	EN = 0 V, V_{OUT} = 5 V			2.5	µA
	Leakage current from battery to V_{OUT}	EN = GND			2.5	µA
	Line transient response	V_{IN} = 600 mVp-p AC square wave, 200 Hz, 12.5% DC at 50 mA or 200 mA load		±25	±50	mVpk
	Load transient response	0 mA to 50 mA, 50 mA to 0 mA, V_{IN} = 3.6 V, T_{Rise} = T_{Fall} = 0.1 µs		50		mVpk
		50 mA to 200 mA, 200 mA to 50 mA, V_{IN} = 3.6 V, T_{Rise} = T_{Fall} = 0.1 µs		150		
I_{IN}	Input bias current, EN	EN = GND or V_{IN}		0.01	1.0	µA
V_{UVLO}	Undervoltage lockout threshold	Falling		2.0	2.1	V
		Rising		2.1	2.2	V
CONTROL STAGE						
V_{IH}	High level input voltage, EN	2.3 V ≤ V_{IN} ≤ 5.5 V			1.0	V
V_{IL}	Low level input voltage, EN	2.3 V ≤ V_{IN} ≤ 5.5 V	0.4			V
OVC	Input over-voltage threshold	Falling		5.9		V
		Rising		6		
t_{Start}	Start-up time	Time from active EN to start switching, no-load until V_{OUT} is stable 5 V			300	µs
DC/DC STAGE						
Freq		See Figure 7		3.5		MHz
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

(1) DRV package has an increased R_{DSon} of about 40 mΩ due to bond wire resistance.

6.6 Typical Characteristics

Table 1. Table of Graphs

		Figure
Maximum output current	vs Input voltage	Figure 1
Efficiency	vs Output current, V_{OUT} = 5 V, V_{IN} = [2.3 V, 3 V, 3.6 V, 4.2 V]	Figure 2
	vs Input voltage, V_{OUT} = 5 V, I_{OUT} = [100 µA, 1 mA, 10 mA, 100 mA, 200 mA]	Figure 3
Input current	at No output load (PFM Mode)	Figure 4
Output voltage	vs Output current, V_{OUT} = 5 V, V_{IN} = [2.3 V, 3 V, 3.6 V, 4.2 V]	Figure 5
	vs Input voltage	Figure 6
Frequency	vs Output load, V_{OUT} = 5 V, V_{IN} = [3 V, 4 V, 5 V]	Figure 7

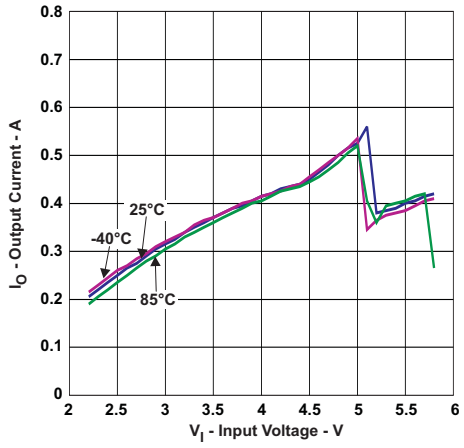


Figure 1. Maximum Output Current vs Input Voltage

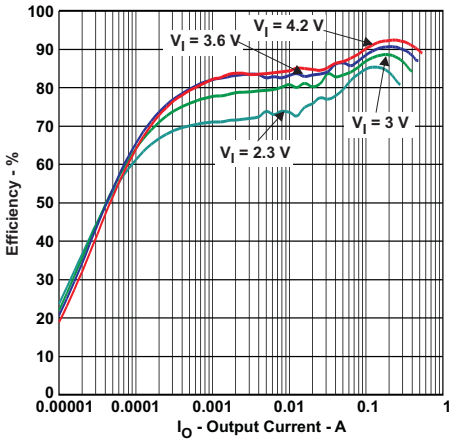


Figure 2. Efficiency vs Output Current for Different V_{IN} (V_I)

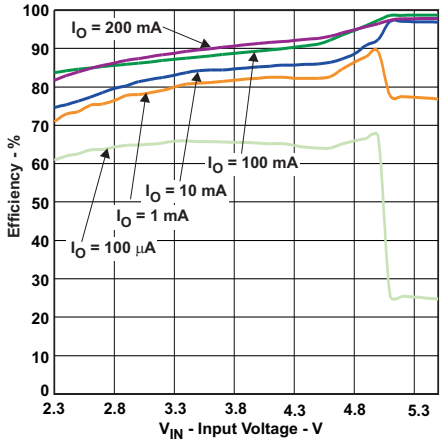


Figure 3. Efficiency vs Input Voltage for Different Output Current (I_O)

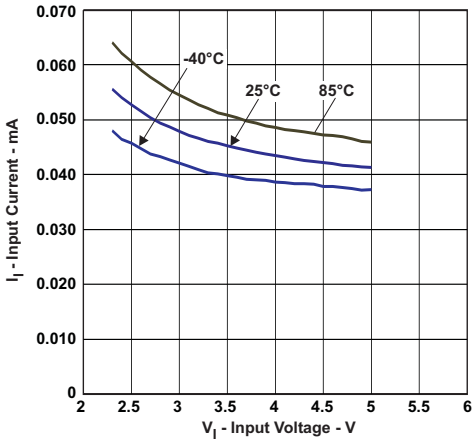


Figure 4. Input Current at No Output Load (PFM Mode) for Different T_A

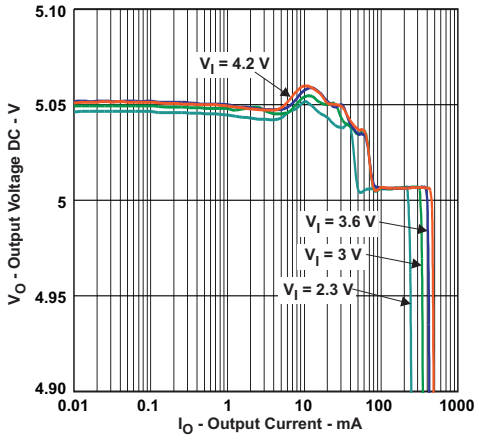


Figure 5. Output Voltage vs Output Current for Different V_{IN} (V_I)

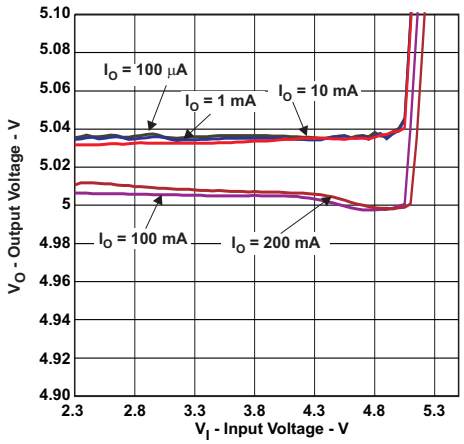


Figure 6. Output Voltage vs Input Voltage for Different Output Current (I_O)

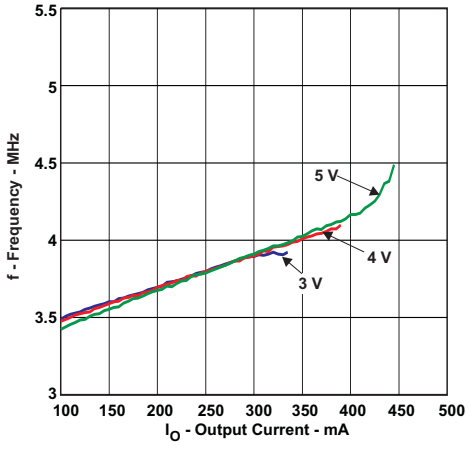


Figure 7. Frequency vs Output Load for Different V_{IN}

7 Detailed Description

7.1 Overview

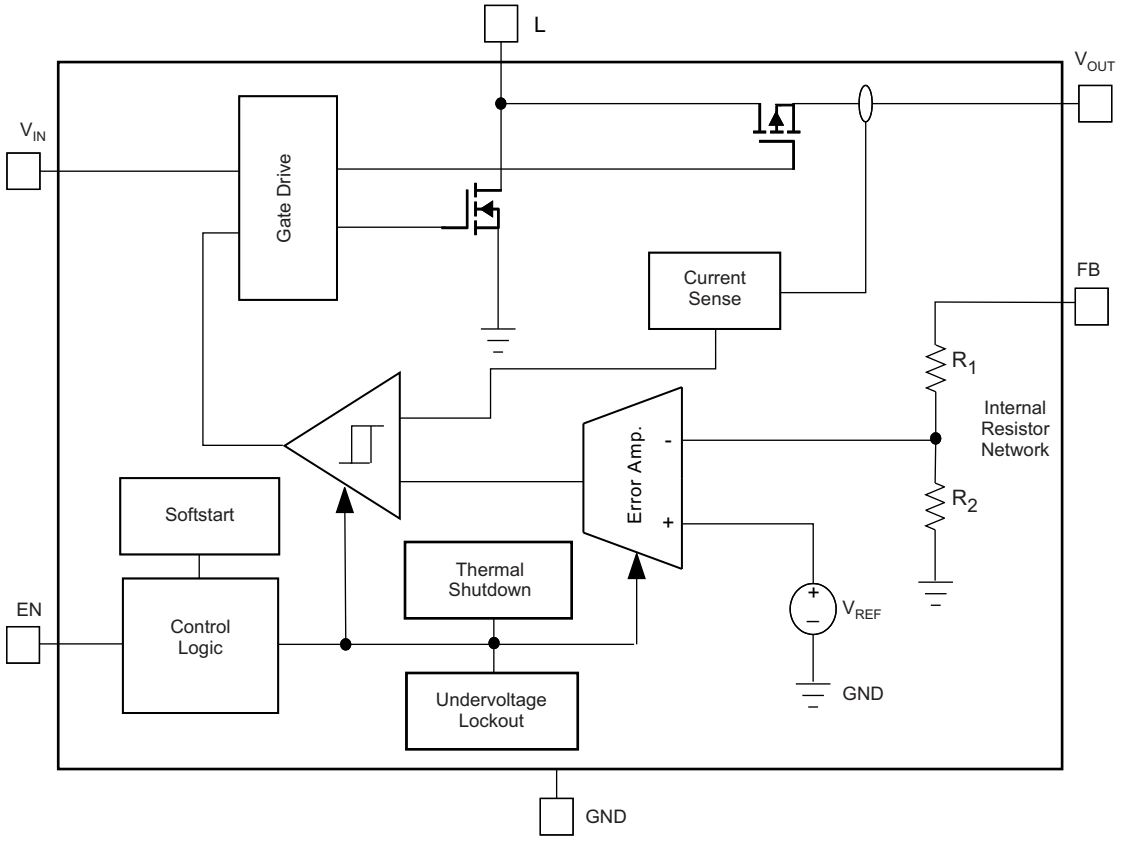
The TPS61240-Q1 boost converter operates with typically a 3.5-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter automatically enters Power Save Mode and then operates in pulse frequency modulation (PFM) mode.

During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme, which allows *best in class* line and load regulation allowing the use of small ceramic input and output capacitors and a small inductor. During shutdown, the load is completely disconnected from the battery.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the peak current is reached, the current comparator trips and the on-timer is reset and this turns off N-MOS switch. Now rectifier switch (P-MOS) is turned on and the inductor current decays to an internally set valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a DC-to-DC step-up converter can only operate in *true* boost mode, that is, the output is *boosted* by a certain amount above the input voltage. The TPS61240-Q1 device operates differently as it can smoothly transition in and out of zero duty-cycle operation. Therefore, the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier.

During the current limit operation, the output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2}\Delta I_L\right) \quad \text{with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

Figure 8 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, I_{OUT}, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

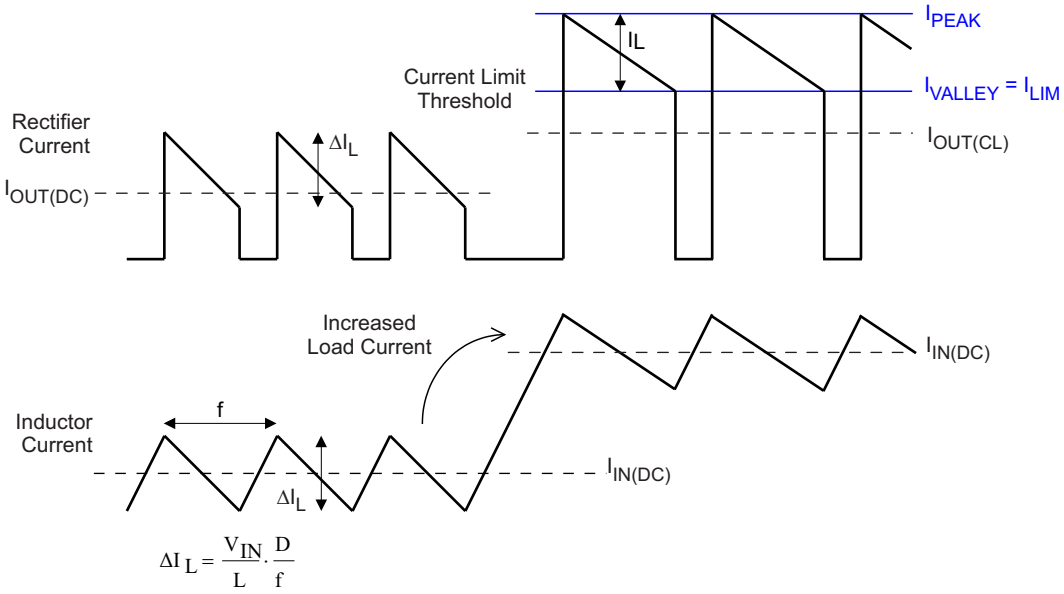


Figure 8. Inductor/Rectifier Currents in Current Limit Operation

7.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is 2 V (typical). The device starts operation once the rising VIN trips undervoltage lockout threshold V_{UVLO} again at 2.1 V (typical).

7.3.3 Input Overvoltage Protection

In the event of an overvoltage condition on the input rail, the output voltage will also experience the overvoltage due to being in dropout condition. An input overvoltage protection feature has been implemented into the TPS61240-Q1, which has an input overvoltage threshold of 6 V. Once this level is triggered, the device will go into shutdown mode to protect itself. If the voltage drops to 5.9 V or below, the device will startup once more into normal operation.

Feature Description (continued)

7.3.4 Enable

Setting EN pin to high, enables the device. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start activates and the output voltage ramps up. The output voltages reach nominal values in typically 250 μs after the device has been enabled.

The EN input can control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

7.3.5 Soft Start

The TPS61240-Q1 has an internal soft start circuit that controls the ramp up of the output voltage. Under no load conditions, the output voltage reaches nominal values within t_{Start} of typically 250 μs after EN pin has been pulled to a high level.

This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches V_{IN}. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF}.

7.3.6 Load Disconnect

Load disconnect electrically removes the output from the input of the power supply when the supply is disabled. This is especially important during shutdown. In shutdown of a boost converter, the load is still connected to the input through the inductor and catch diode. Since the input voltage is still connected to the output, a small current continues to flow, even when the supply is disabled. Even small leakage currents significantly reduce battery life during extended periods of off time.

The benefit of this implemented feature for a system design is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter.

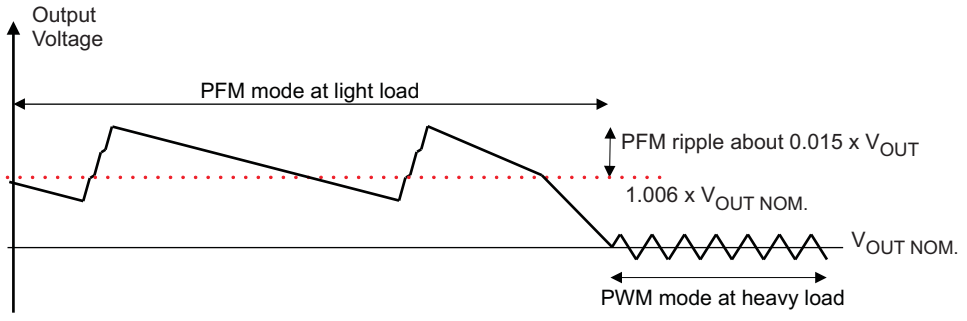
7.3.7 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned off. When the junction temperature falls below the thermal shutdown hysteresis, the device continues operation.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The TPS61240-Q1 family of devices integrates a power save mode to improve efficiency at light load. In power save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.



The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61240-Q1 boost regulator has fixed output voltage of 5 V typical with an input voltage range of 2.3 V to 5.5 V. TPS61240-Q1 allows the use of small inductors and capacitors to achieve a small solution size and supports output currents up to 450 mA. When shut down, the TPS61240-Q1 presents a high impedance at the V_{OUT} pin and the load is disconnected completely from the battery. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS61240-Q1 is shut down.

8.2 Typical Applications

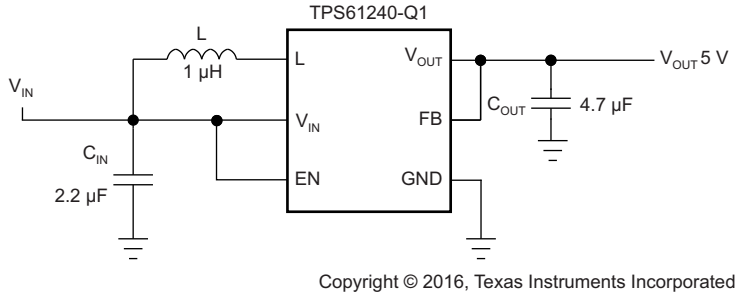


Figure 9. TPS61240-Q1 Fixed 5 V Output from V_{IN} = 3 V to 4.2 V

8.2.1 Design Requirements

Table 2 lists the design parameters for this application example.

Table 2. TPS61240-Q1 5V Output Design Requirements

PARAMETERS	VALUE
Input voltage	3 V to 4.2 V
Output voltage	5 V
Output current	200 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage

The output voltage is set by an internal resistor divider. The FB pin is used to sense the output voltage. To configure the output properly, the FB pin has to be connected directly to the output.

8.2.2.2 Inductor Selection

For correct operation of TPS61240-Q1 device, an inductor must be connected between pin V_{IN} and pin L. A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input (V_{IN}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 2.

$$I_{L\_MAX} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (2)$$

where

- η is the efficiency of the switching regulator

For example, for an output current of 200 mA at 5 V V_{OUT}, with efficiency of 85%, at least 392 mA of average current flows through the inductor at a minimum input voltage of 3 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple (or larger inductor value) reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But with larger inductor, regulation time during load transients rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using Equation 3.

$$L_{MIN} \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}} \quad (3)$$

where

- f is the switching frequency
- ΔI_L is the ripple current in the inductor

With V_{IN} = 4.2 V, V_{OUT} = 5 V, assuming inductor ripple current = 30% of minimum current limit of 0.5 A, the resulting inductor value = 1.28 µH. In typical applications, a 1.0 µH inductance is recommended. The device has been optimized to operate with inductance values between 1.0 µH and 2.2 µH. It is recommended that inductance values of at least 1.0 µH is used, even if Equation 3 yields something lower. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current I.

$$I_{L(peak)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \quad \text{with} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (4)$$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. Inductor with part number, LQM21PN1R0MC0 is one example of an inductor that can be used with this device. Customers need to verify and validate whether it is suitable for their application.

8.2.2.3 Input Capacitor

At least 2.2-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the VIN and GND pins

8.2.2.4 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the V_{OUT} and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (5)$$

where

- ΔV is the maximum allowed ripple

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.3 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using $\Delta V_{ESR} = I_{OUT} \times R_{ESR}$

A capacitor with a value equal to or higher than the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC bias effect, which will have a strong influence on the final effective capacitance. Therefore the correct capacitor value has to be chosen carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. Time between the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times$ ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are very easily interpreted when the device operates in PWM mode. During recovery time, V_O can be monitored for settling time, overshoot or ringing to judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

8.2.3 Application Curves

Table 3. Table of Application Curves

		Figure
Waveforms	Output voltage ripple, PFM mode, I_{OUT} = 10 mA	Figure 10
	Output voltage ripple, PWM mode, I_{OUT} = 150 mA	Figure 11
	Load transient response, V_{IN}, 3.6 V, 0 mA to 50 mA	Figure 12
	Load transient response, V_{IN}, 3.6 V, 50 mA to 200 mA	Figure 13
	Line transient response, V_{IN}, 3.6 V to 4.2 V, I_{OUT} = 50 mA	Figure 14
	Line transient response, V_{IN}, 3.6 V to 4.2 V, I_{OUT} = 200 mA	Figure 15
	Startup after enable, V_{IN}, 3.6 V, V_{OUT} = 5 V, Load = 5 kΩ	Figure 16
	Startup after enable, V_{IN}, 3.6 V, V_{OUT} = 5 V, Load = 16.5 kΩ	Figure 17
	Startup and shutdown, V_{IN}, 3.6 V, V_{OUT} = 5 V, Load = 16.5 kΩ	Figure 18

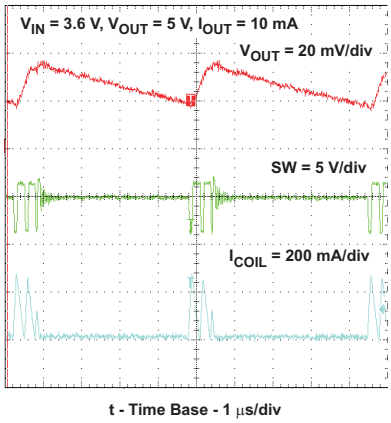


Figure 10. Output Voltage Ripple – PFM Mode

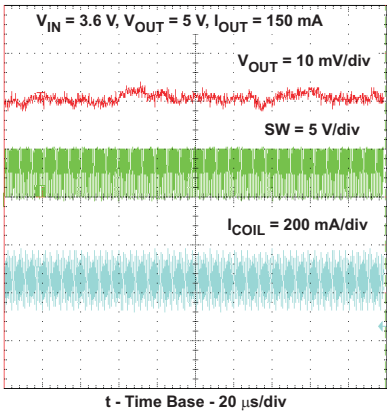


Figure 11. Output Voltage Ripple – PWM Mode

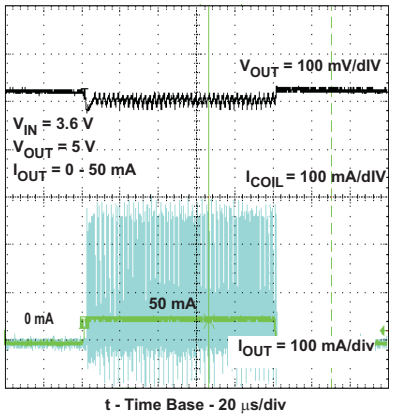


Figure 12. Load Transient Response 0 mA to 50 mA and 50 mA to 0 mA

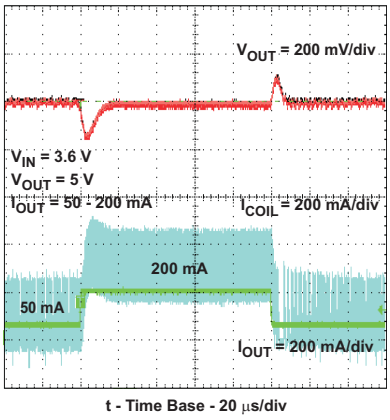


Figure 13. Load Transient Response 0 mA to 200 mA and 200 mA to 0 mA

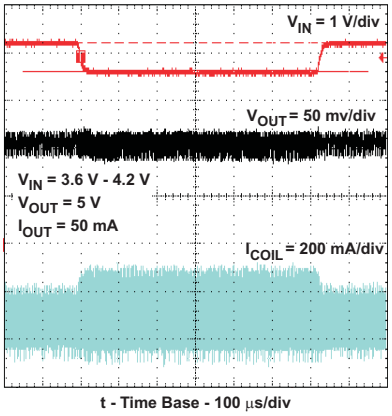


Figure 14. Line Transient Response 3.6 V to 4.2 V at 50 mA Load

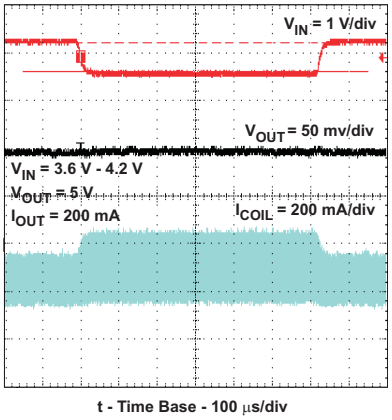


Figure 15. Line Transient Response 3.6 V to 4.2 V at 200 mA Load

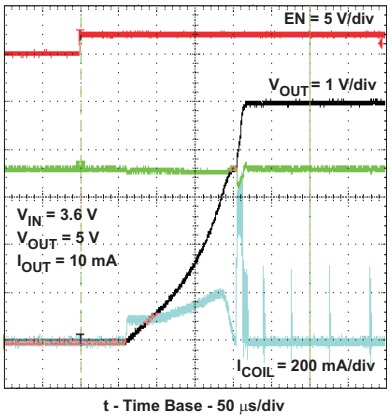


Figure 16. Startup After Enable – No Load

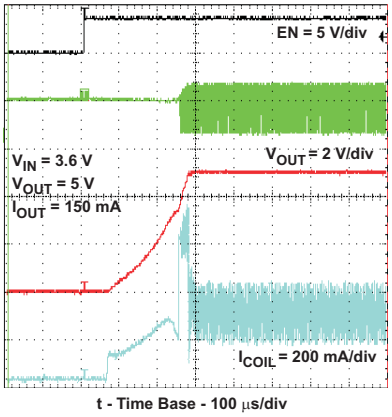


Figure 17. Startup After Enable – With Load

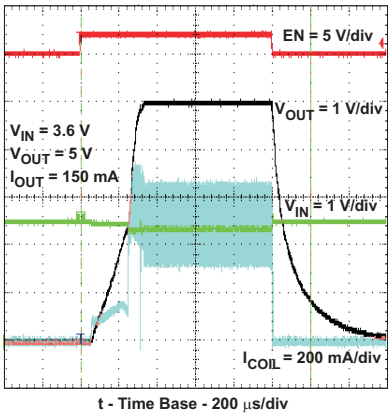


Figure 18. Startup and Shutdown

8.3 System Example

Figure 19 is another example for using the TPS61240-Q1 with fixed 5 V and a Schottky diode for output overvoltage protection.

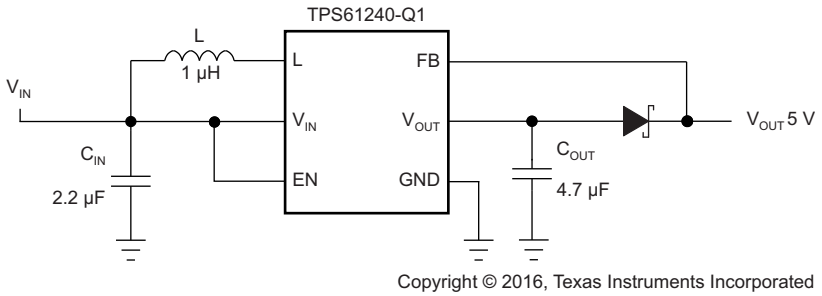


Figure 19. TPS61240-Q1 Fixed 5 V With Schottky Diode for Output Overvoltage Protection

9 Power Supply Recommendations

The input supply should be in the range from 2.3 V to 5.5 V. The input supply can be a regulated supply voltage or a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice for the bulk capacitance.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. The following are some guidelines for good layout design.

Figure 20 provides an example of layout design with the TPS61240-Q1 device. Follow the guidelines for a good layout.

- Use wide and short traces for the main current path and for the power ground tracks.
- The input and output capacitor, as well as the inductor, should be placed as close as possible to the IC.
- Connect the exposed thermal pad to the GND plane and place multiple thermal vias below the thermal pad to enhance the thermal performance.

10.2 Layout Example

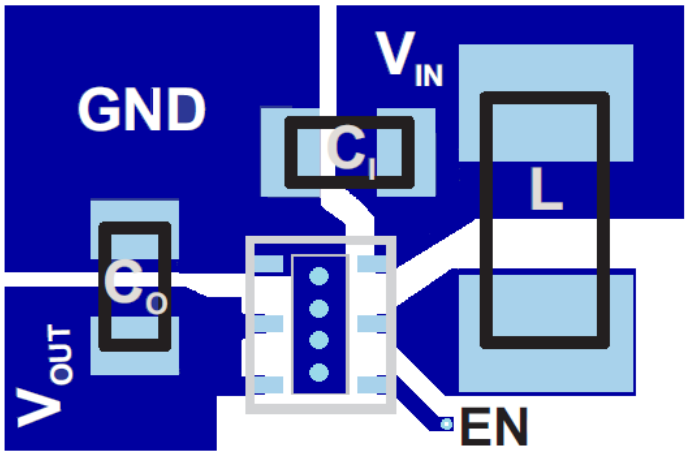


Figure 20. PCB Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *QFN/SON PCB Attachment*
- *Performing Accurate PFM Mode Efficiency Measurements*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61240IDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QVL	Samples
TPS61240TDRVRQ1	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	14T	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61240-Q1 :

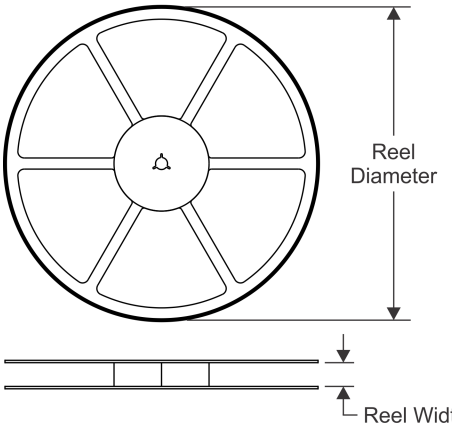
- Catalog: TPS61240

NOTE: Qualified Version Definitions:

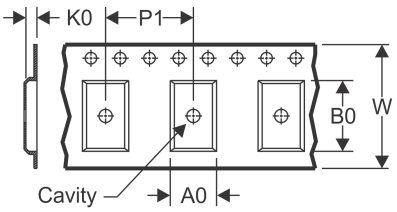
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

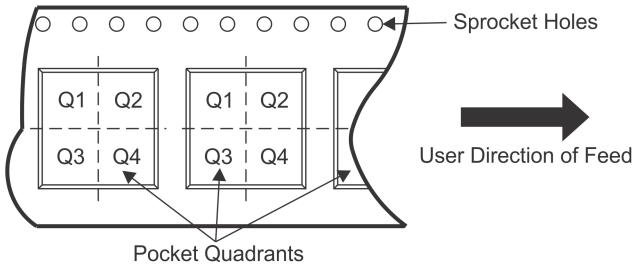


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

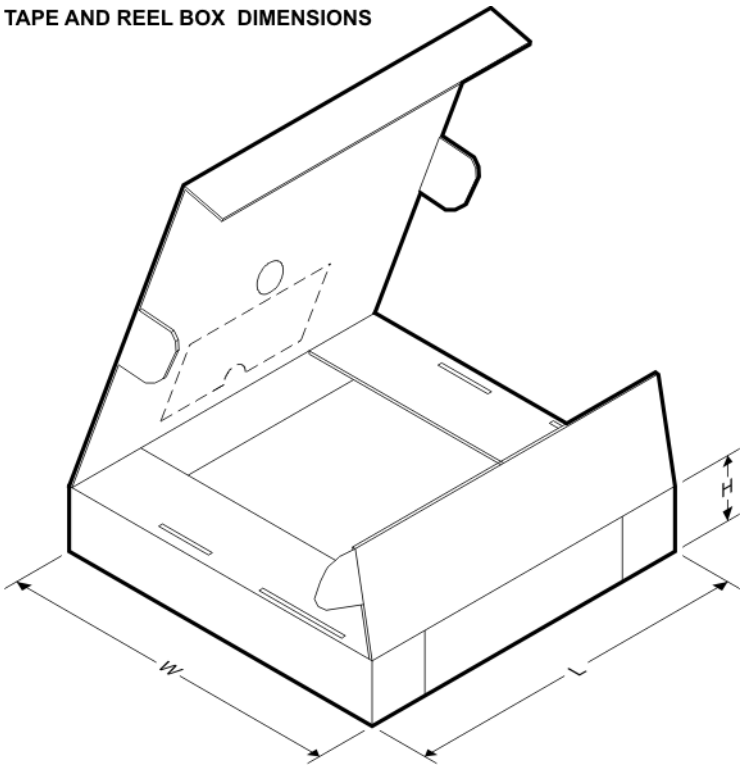
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61240IDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61240TDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

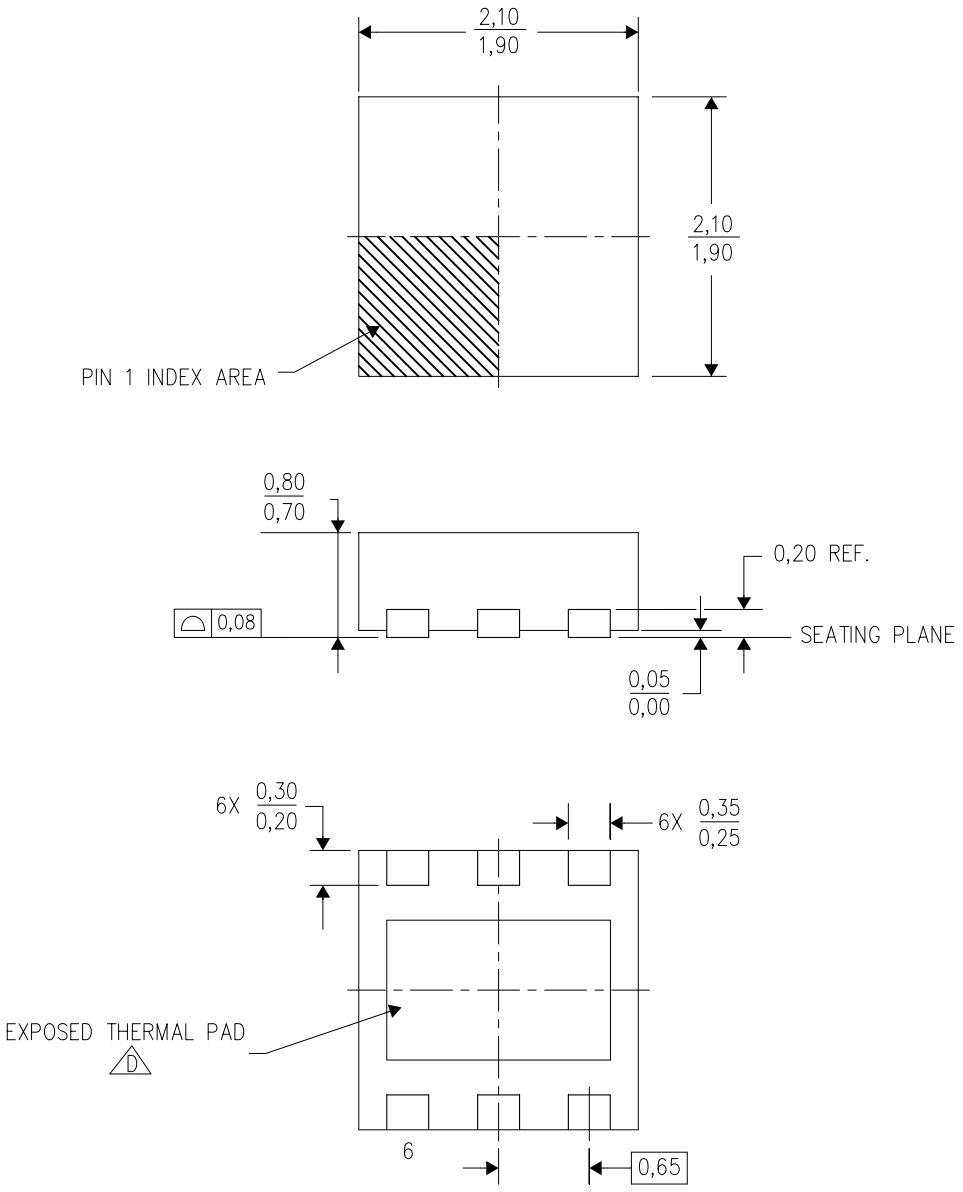
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61240IDRVRQ1	WSON	DRV	6	3000	195.0	200.0	45.0
TPS61240TDRVRQ1	WSON	DRV	6	3000	195.0	200.0	45.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

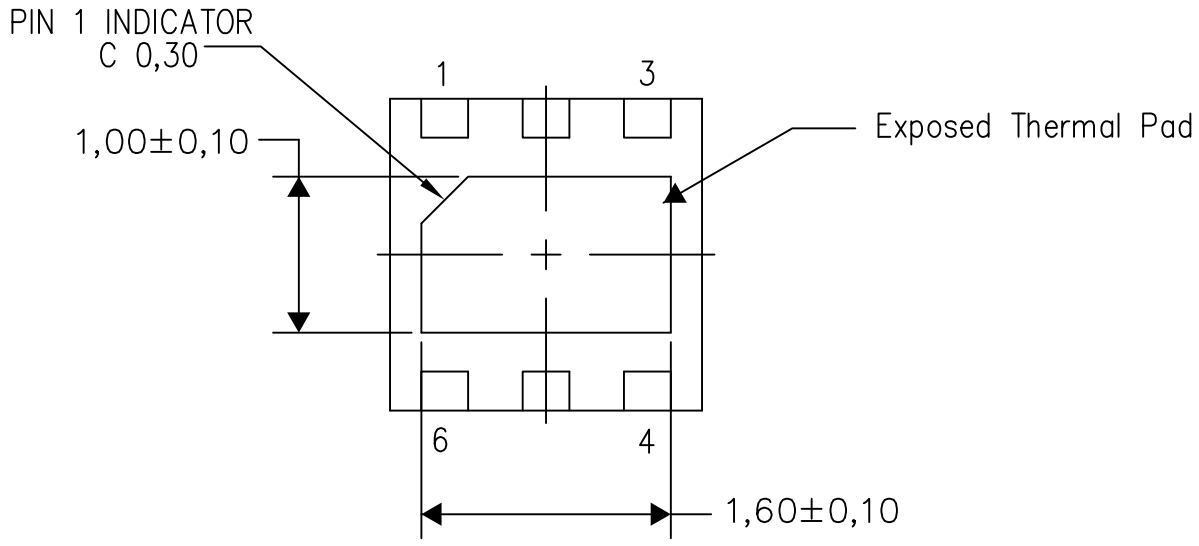
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



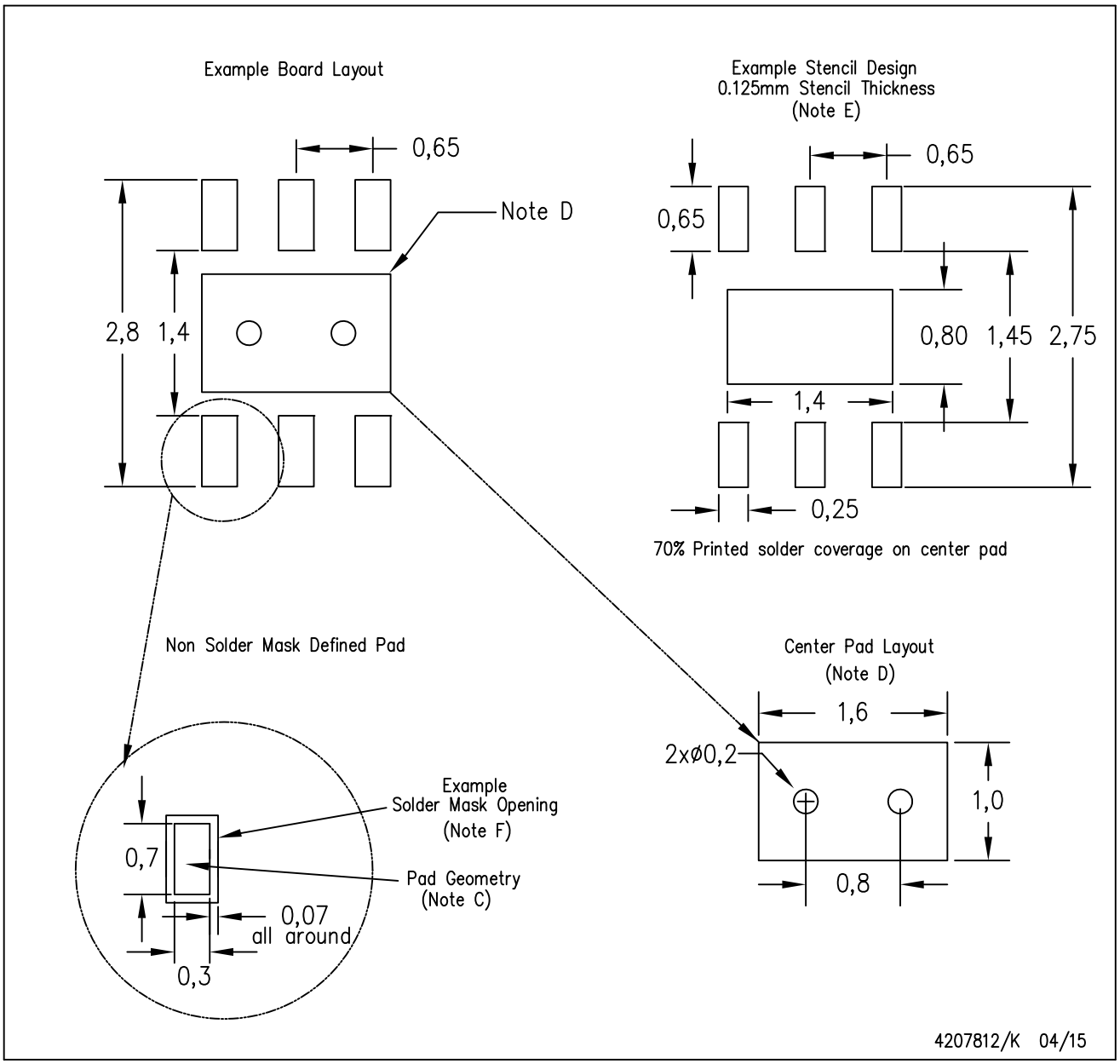
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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