Single-String WLED Driver for LCD TV

Check for Samples: TPS61197

FEATURES

- **8V to 30V Input Voltage**
- **50 kHz to 800 kHz Programmable Switching Frequency**
- **Adaptive Boost Output to White LED Voltage**
- **High Precision PWM Dimming Resolution up to 5000:1**
- **Programmable Over-voltage Protection Threshold at Output**
- **Programmable Under-voltage Threshold at Input with Adjustable Hysteresis**
- **Adjustable Soft Start Time Independent of Dimming Duty Cycle**
- **Built-in LED Open Protection**
- **Built-in Schottky Diode Open/Short Protection**
- **Built-in IFB Short Protection**
- **Thermal Shutdown**
- **16L SOIC Package**

APPLICATIONS

- **LCD TV Backlight**

DESCRIPTION

The TPS61197 provides highly integrated solutions for LCD TV backlight. This device is a current mode boost controller driving one WLED string with multiple LEDs in series. The input voltage range for TPS61197 is from 8V to 30V.The TPS61197 adjusts the boost controller's output voltage automatically to provide only the minimum voltage required by the LED string to generate the setting LED current, thereby optimizing the driver's efficiency. Its switching frequency is programmed by an external resistor from 50 kHz to 800 kHz.

The TPS61197 supports direct PWM brightness dimming method. During the PWM dimming, the white LED current is turned on and off at the duty cycle and frequency which are determined by an external PWM signal. The PWM dimming frequency ranges from 90 Hz to 22 kHz.

The TPS61197 integrates over-current protection, output short circuit protection, Schottky diode open and short protection, LED open protection, LED string short protection and over temperature shutdown circuit. The device also provides programmable input under-voltage lockout threshold and output over-voltage protection threshold.

The TPS61197 has a built-in linear regulator which steps down the input voltage to the VDD voltage for powering the internal circuitry. An internal soft start circuit is implemented to work with an external capacitor to adjust the soft startup time to minimize the in-rush current during boost converter startup. The device is available in 16-pin SOIC package, which is ideal for a single-layer PCB board.

SIMPLIFIED SCHEMATIC CIRCUIT

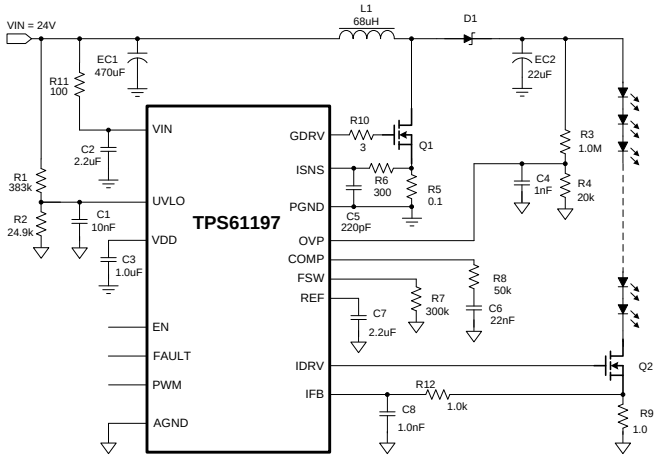


Figure 1. Typical Application of TPS61197

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERING PART NUMBER	TOP MARK
-40°C to 85°C	16-Pin SOIC	TPS61197DR	TPS61197

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	Pin VIN	–0.3	33	V
	Pin FAULT	–0.3	VIN	
	Pin ISNS, IFB	–0.3	3.3	
	Pin EN, PWM, VDD, GDRV, IDRV	–0.3	20	
	Pin GDRV 10ns transient	–2.0	20	
	All other pins	–0.3	7.0	
ESD rating	HBM		2	kV
	MM		200	V
	CDM		1	kV
Continuous power dissipation		See Thermal Information Table		
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61197 SOIC (16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	85.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.5	
θ_{JB}	Junction-to-board thermal resistance	43.3	
ψ_{JT}	Junction-to-top characterization parameter	13.5	
ψ_{JB}	Junction-to-board characterization parameter	42.9	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	8		30	V
V_{OUT}	Output voltage range	V_{IN}		300	V
L_1	Inductor	4.7		470	µH
C_{IN}	Input capacitor	10			µF
C_{OUT}	Output capacitor	1.0		220	µF
f_{SW}	Boost regulator switching frequency	50		800	kHz
f_{DIM}	PWM dimming frequency	0.09		22	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Customers need to verify the component value in their application if the values are different from the recommended values.

ELECTRICAL CHARACTERISTICS

V_{IN}= 24V, T_A = –40°C to 85°C, typical values are at T_A = 25°C, EC1 = 470µF, EC2 = 22µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		8		30	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} falling		6.5	7.0	V
V_{VIN_HYS}	VIN UVLO hysteresis			300		mV
I_{Q_VIN}	Operating quiescent current into VIN	Device enabled, no switching, V_{IN} = 30 V			2.0	mA
I_{SD}	Shutdown current	V_{IN} = 12 V V_{IN} = 30 V			25 50	µA
V_{DD}	Regulation voltage for internal circuit	0 mA < I_{DD} < 15 mA	6.6	7	7.4	V
EN and PWM						
V_H	Logic high input on EN, PWM	V_{IN} = 8 V to 30 V	1.6			V
V_L	Logic low input on EN, PWM	V_{IN} = 8 V to 30 V			0.75	V
R_{PD}	Pull-down resistance on EN, PWM		400	800	1600	kΩ
UVLO						
V_{UVLOTH}	Threshold voltage at UVLO pin		1.204	1.229	1.253	V
I_{UVLO}	UVLO input bias current	V_{UVLO} = V_{UVLOTH} – 50 mV V_{UVLO} = V_{UVLOTH} + 50 mV	–0.1 –4.4	 -3.9	0.1 –3.3	µA
SOFT START						
I_{SS}	Soft start charging current	PWM dimming on, V_{REF}<2.0V		200		µA
CURRENT REGULATION						
V_{IFB_REG}	IFB pin regulation voltage	T_J = 25°C to 85°C	293	300	307	mV
V_{IFB_SCP}	IFB short to ground protection threshold			200		mV
V_{IFB_OVP}	IFB over voltage protection threshold		1.0	1.1	1.2	V
I_{IFB_LEAK}	IFB pin leakage current	V_{IFB} = 300mV	–100		100	nA
BOOST REFERENCE VOLTAGE						
V_{REF}	Reference voltage range for Boost Controller		0		3.5	V
I_{REF_LEAK}	Leakage current at REF	T_J = -40°C to 85°C	–25		25	nA
OSCILLATOR						
f_{SW}	Switching frequency	R = 200 kΩ	187	200	213	kHz
V_{FSW}	FSW pin reference voltage			1.8		V
$D_{(max)}$	Maximum duty cycle	f_{SW} = 200 kHz	90%	94%	98%	
$t_{on(min)}$	Minimum pulse width			300		ns

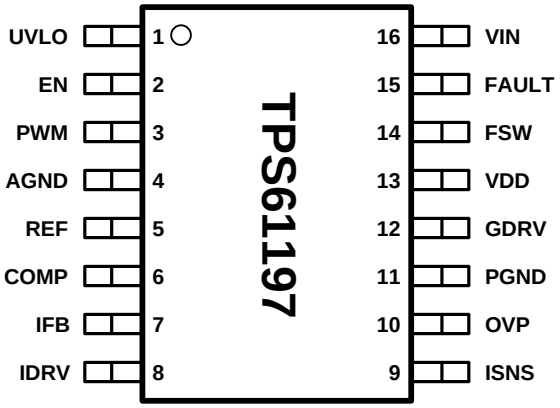
ELECTRICAL CHARACTERISTICS (continued)

V_{IN}= 24V, T_A = –40°C to 85°C, typical values are at T_A = 25°C, EC1 = 470µF, EC2 = 22µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
I_{SINK}	Comp pin sink current	V_{OVP} = V_{REF} + 200mV, V_{COMP} = 1V		20		µA
I_{SOURCE}	Comp pin source current	V_{OVP} = V_{REF} – 200mV, V_{COMP} = 1V		20		µA
Gm_{EA}	Error amplifier transconductance		90	120	150	µS
R_{EA}	Error amplifier output resistance			20		MΩ
f_{EA}	Error amplifier crossover frequency			1000		kHz
GATE DRIVER						
R_{GDRV_SRC}	Gate driver impedance when sourcing	V_{GDRV} = 7 V, I_{GDRV} = –20 mA		5	10	Ω
R_{GDRV_SNK}	Gate driver impedance when sinking	V_{DD} = 7 V, I_{GDRV} = 20 mA		2	5	Ω
I_{GDRV_SRC}	Gate driver source current	V_{DD} = 7 V, V_{GDRV} = 5 V	200			mA
I_{GDRV_SNK}	Gate driver sink current	V_{DD} = 7 V, V_{GDRV} = 2 V	400			mA
V_{PWM_OCP}	Overcurrent detection threshold during PWM	V_{IN} = 8 V to 30 V, T_J = 25°C to 125°C	376	400	424	mV
V_{PFM_OCP}	Overcurrent detection threshold during PFM			180		mV
OVP						
V_{OVPTH}	Over-voltage protection threshold		2.98	3.04	3.10	V
I_{OVP_LEAK}	Leakage current at OVP pin		–100	0	100	nA
FAULT INDICATOR						
I_{FLT_H}	Leakage current at high impedance	V_{FLT} = 24 V		1		nA
I_{FLT_L}	Sink current at low output	V_{FLT} = 1 V	2	5		mA
THERMAL SHUTDOWN						
T_{STDN}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown threshold hysteresis			15		°C

DEVICE INFORMATION

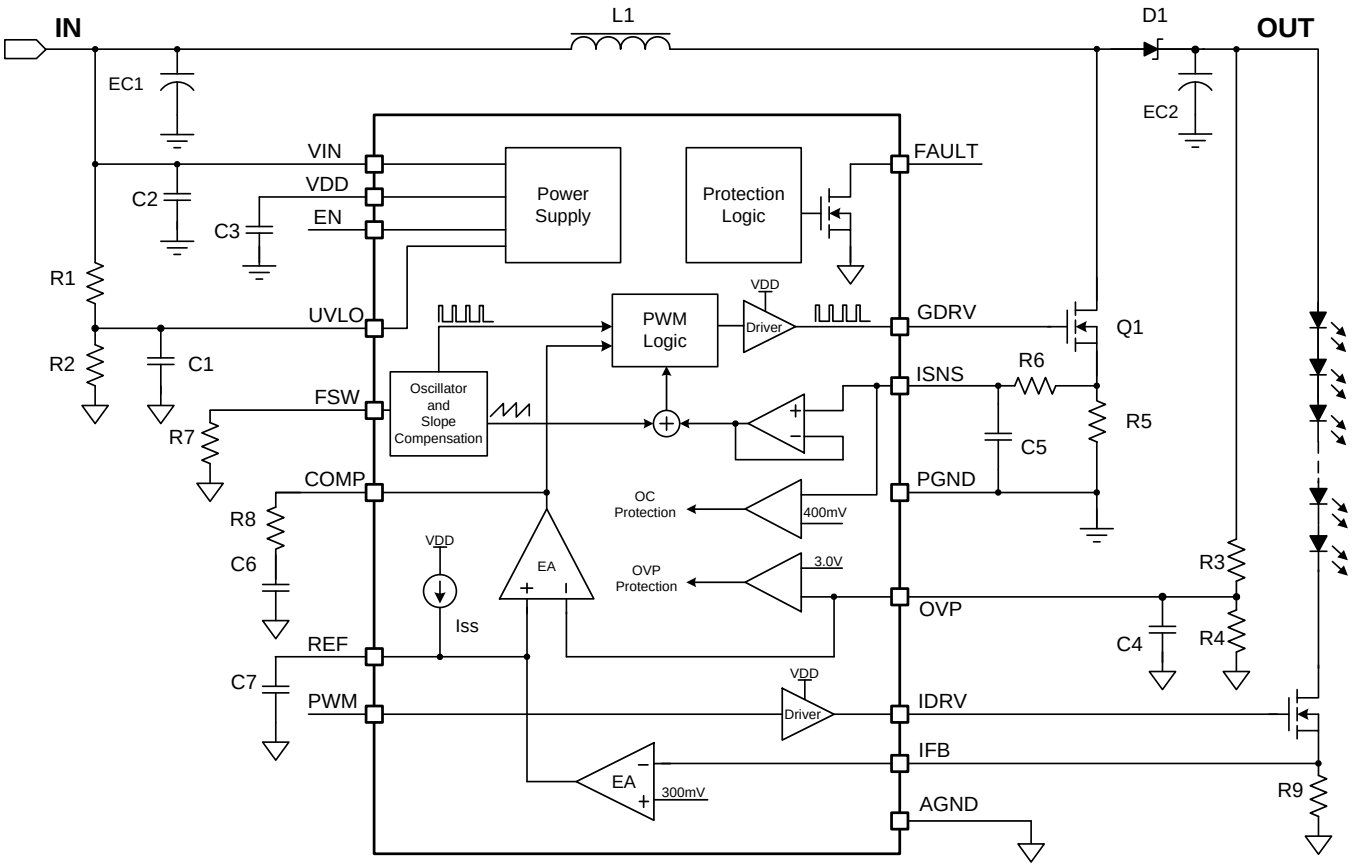
SOIC-16 (D)
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NO. (D)	NAME	
1	UVLO	Low input voltage lockout. Use a resister divider from VIN to this pin to set the UVLO threshold
2	EN	Device enable and disable control input. EN pin high voltage enables the device. EN pin low voltage disables the device.
3	PWM	PWM dimming signal input. The frequency of the PWM signal is in the range of 90Hz to 22 kHz
4	AGND	Analog ground
5	REF	Internal reference voltage for the boost converter. Use a capacitor at this pin to adjust the soft start time.
6	COMP	Loop compensation for the boost converter. Connect a RC network to make loop stable
7	IFB	Connecting a resistor to the pin programs the LED current level for full brightness (i.e., 100% dimming)
8	IDRV	PWM dimming output control pin to drive the external MOSFET or bipolar transistor
9	ISNS	External switch MOSFET current sense positive input
10	OVP	Over-voltage protection detection input. Connect a resistor divider from output to this pin to program the OVP threshold. In addition, this pin is also the feedback of the output voltage of the boost converter.
11	PGND	External MOSFET current sense ground input
12	GDRV	Gate driver output for the external switch MOSFET
13	VDD	Internal regulator output for IC power supply. Connect a ceramic capacitor of more than 1.0µF to this pin.
14	FSW	Boost switching frequency setting pin. Use a resistor to set the frequency between 50 kHz to 800 kHz.
15	FAULT	Fault indicator. Open-drain output. Output high impedance when fault conditions happen
16	VIN	Power supply input pin

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

Figure 1 as test circuit		
TITLE	**TEST CONDITIONS**	**FIGURE**
Dimming Efficiency with 24 LEDs	24 LEDs (V_{OUT} = 80V), I_{OUT} = 300mA, 100Hz Dimming Frequency	Figure 2
Dimming Efficiency with 38 LEDs	38 LEDs (V_{OUT} = 130V), I_{OUT} = 300mA, 100Hz Dimming Frequency	Figure 3
Dimming Linearity	24 LEDs (V_{OUT} = 80V), V_{IN} = 24V	Figure 4
Dimming Linearity at Small Dimming Duty Cycle	24 LEDs (V_{OUT} = 80V), V_{IN} = 24V	Figure 5
DC Load Efficiency	f_{SW} = 130kHz	Figure 6
Switching Frequency Setting	V_{IN} = 24V	Figure 7
Boost Switching Waveform	V_{IN} = 24V, V_{OUT} = 80V, I_{OUT} = 300mA	Figure 8
Dimming Waveform (2% Dimming)	V_{IN} = 24V, V_{OUT} = 80V, I_{OUT} = 300mA, 100Hz Dimming Frequency	Figure 9
Startup Waveform (1% Dimming)	100Hz Dimming Frequency, 1% Dimming Duty Cycle	Figure 10
Startup Waveform (100% Dimming)	100Hz Dimming Frequency, 100% Dimming Duty Cycle	Figure 11
Shutdown Waveform (1% Dimming)	100Hz Dimming Frequency, 1% Dimming Dutyc Cycle	Figure 12
Shutdown Waveform (100% Dimming)	100Hz Dimming Frequency, 100% Dimming Duty Cycle	Figure 13
LED Open Protection (1% Dimming)	100Hz Dimming Frequency, 1% Dimming Duty Cycle	Figure 14
LED Open Protection (100% Dimming)	100Hz Dimming Frequency, 100% Dimming Duty Cycle	Figure 15
LED String Short Protection (1% Dimming)	100Hz Dimming Frequency, 1% Dimming Duty Cycle	Figure 16
LED String Short Protection (100% Dimming)	100Hz Dimming Frequency, 100% Dimming Duty Cycle	Figure 17

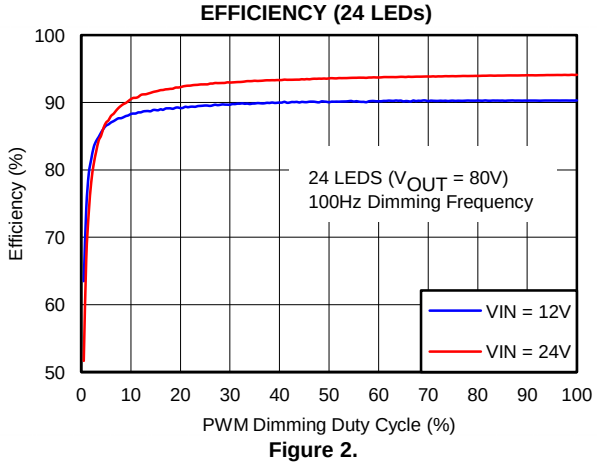


Figure 2.

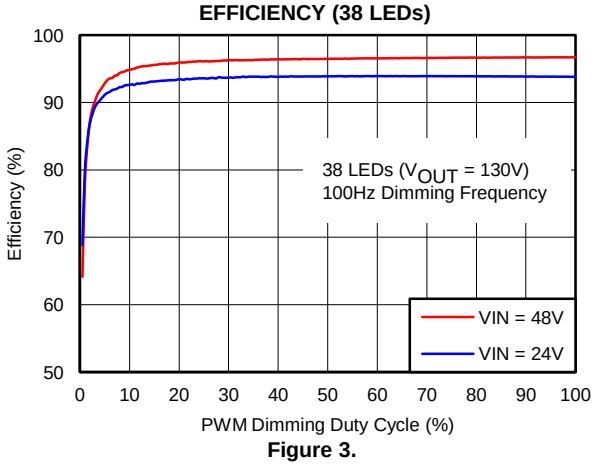


Figure 3.

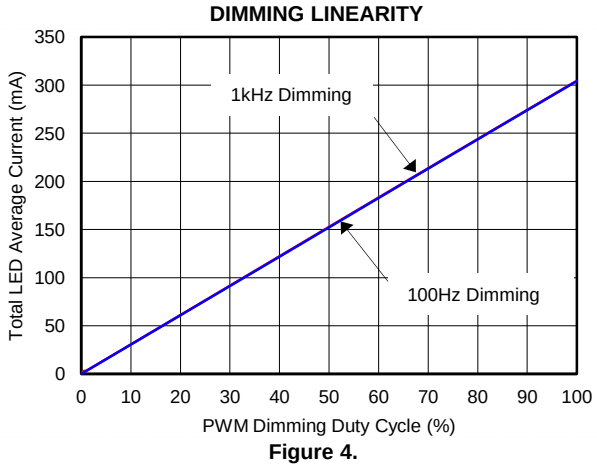


Figure 4.

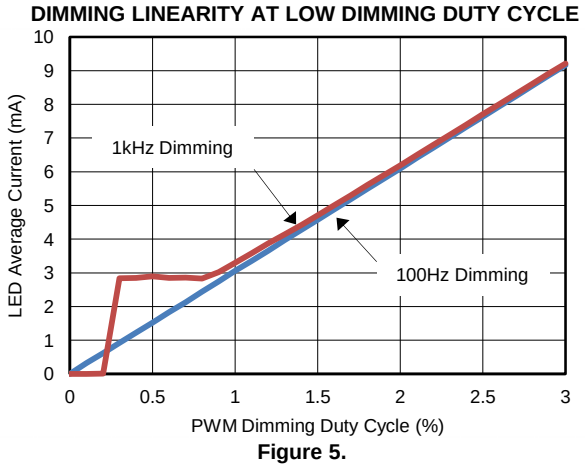


Figure 5.

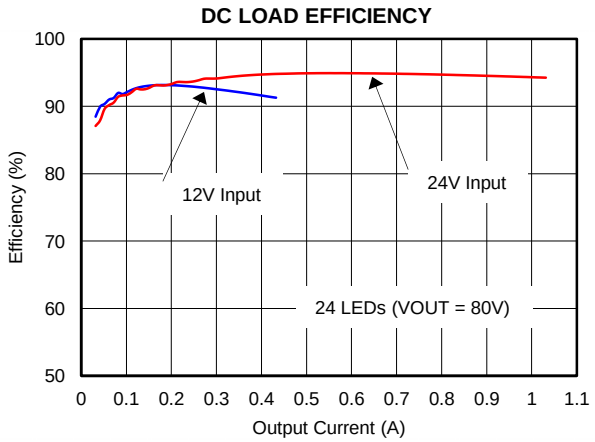


Figure 6.

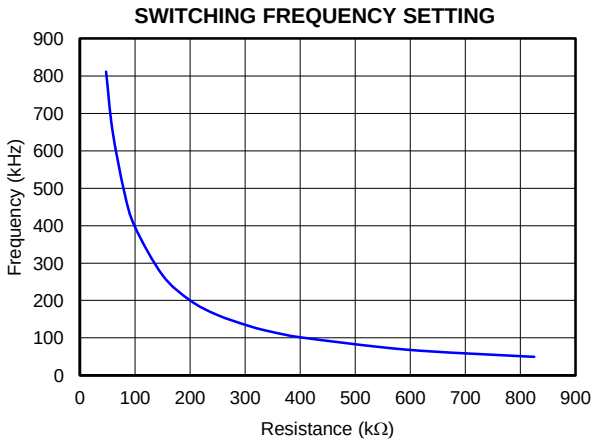


Figure 7.

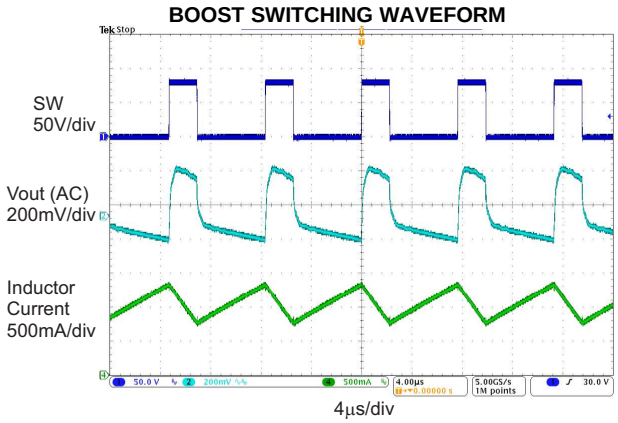


Figure 8.

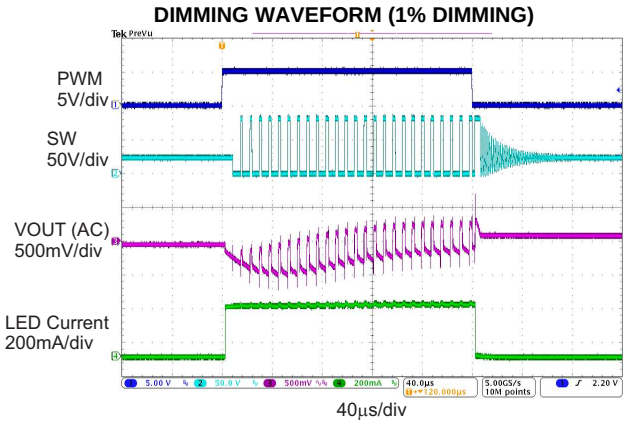


Figure 9.

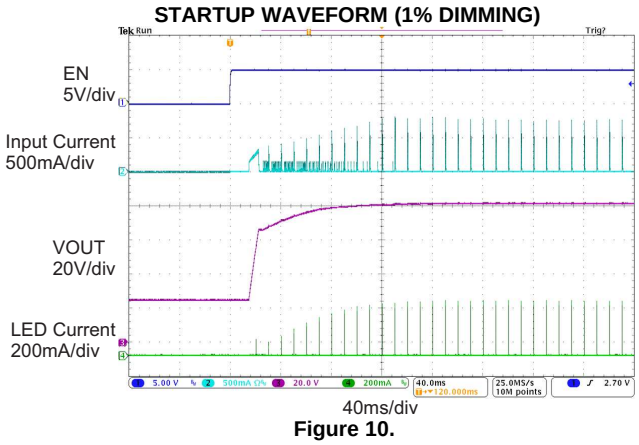


Figure 10.

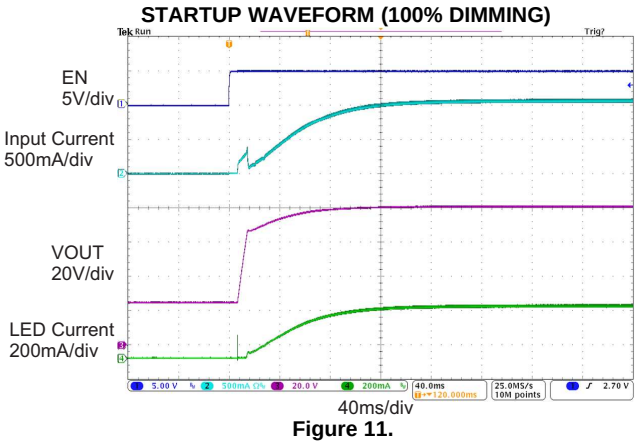


Figure 11.

SHUTDOWN WAVEFORM (1% DIMMING)

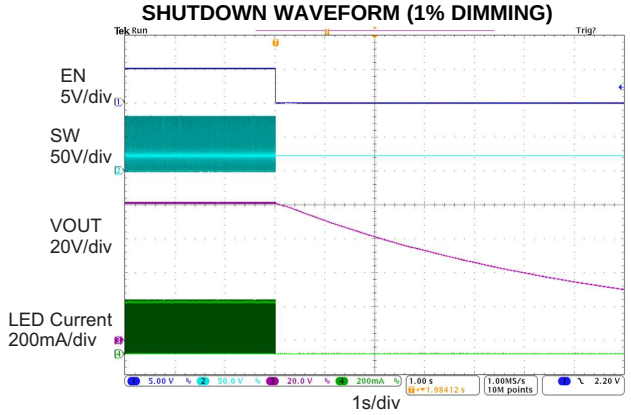


Figure 12.

SHUTDOWN WAVEFORM (100% DIMMING)

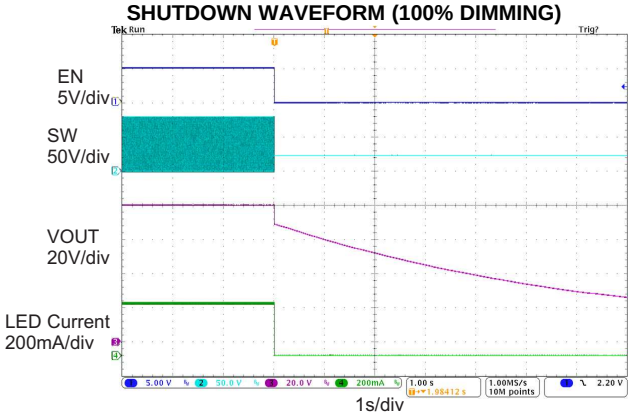


Figure 13.

LED OPEN PROTECTION (1% DIMMING)

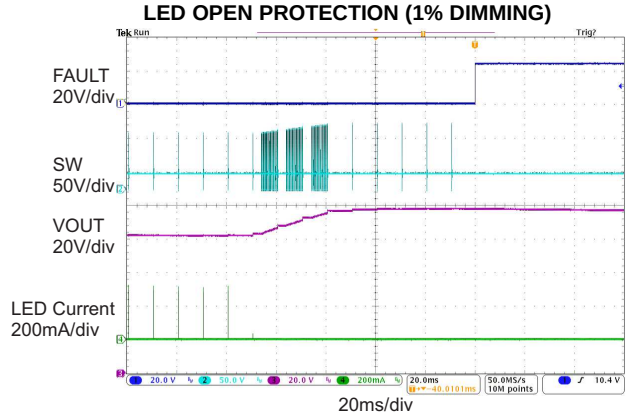


Figure 14.

LED OPEN PROTECTION (100% DIMMING)

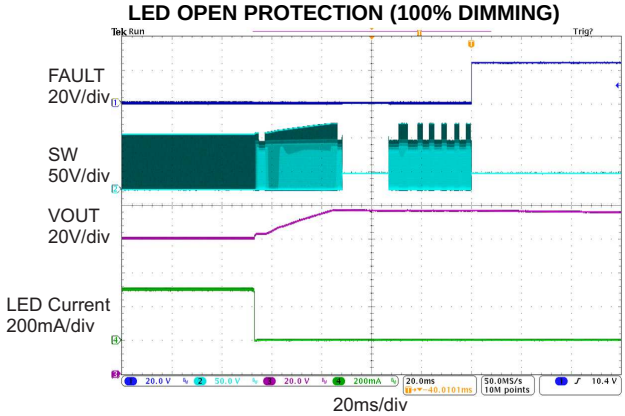


Figure 15.

LED STRING SHORT PROTECTION (1% DIMMING)

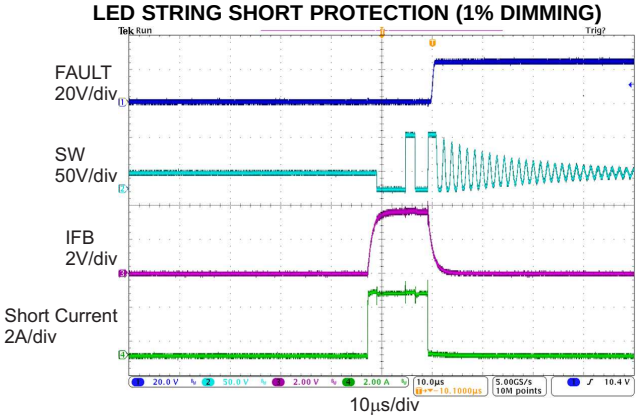


Figure 16.

LED STRING SHORT PROTECTION (100% DIMMING)

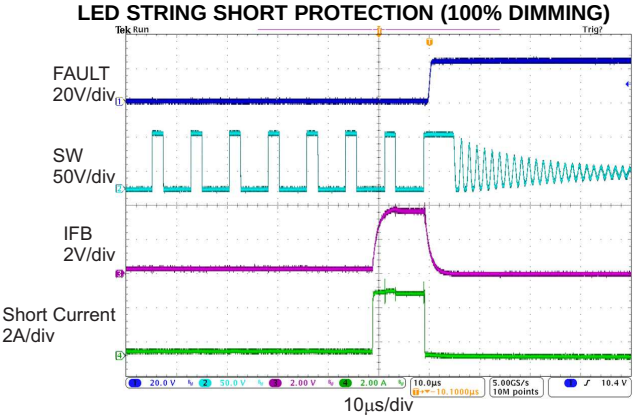


Figure 17.

DETAILED DESCRIPTION

Supply Voltage

The TPS61197 has a built-in linear regulator to supply the IC analog and logic circuitries. The VDD pin, output of the regulator, must be connected to a bypass capacitor with more than 1.0µF capacitance. VDD only has a current sourcing capability of 15mA. VDD voltage is ready after the EN pin is pulled high.

Boost Controller

The TPS61197 regulates the output voltage with peak current mode PWM (pulse width modulation) control. The control circuitry turns on an external switch FET at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the Error Amplifier (EA) output, the switch FET is turned off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. The switching frequency is programmed by an external resistor.

A ramp signal from the oscillator is added to the current ramp to provide slope compensation, shown in the Functional Block Diagram. The duty cycle of the converter is then determined by the PWM logic block which compares the EA output and the slope compensated current ramp. The feedback loop regulates the OVP pin to a reference voltage generated by the current regulation control circuit which senses the LED current at the IFB pin. The output of the EA is connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

The TPS61197 consistently adjusts the boost output voltage to account for any changes in LED forward voltages. In the event that the boost controller is not able to regulate the output voltage due to the minimum pulse width ($t_{on(min)}$, in the ELECTRICAL CHARACTERISTICS table), the TPS61197 enters pulse skip mode. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition or when the input voltage is higher than the output voltage.

Switching Frequency

The switching frequency is programmed between 50kHz to 800kHz by an external resistor (R7 in the SIMPLIFIED SCHEMATIC CIRCUIT). To determine the resistance by a given frequency, use the curve in Figure 7 or calculate the resistance value by Equation 1. Table 1 shows the recommended resistance values for some switching frequencies.

$$f_{SW} = \frac{40000}{R7}(kHz) \quad (1)$$

Table 1. Recommended Resistance Values for Switching Frequencies

R7	f_{SW}
800 k	50 kHz
400 k	100 kHz
200 k	200 kHz
100 k	400 kHz
80 k	500 kHz

Enable and Under Voltage Lockout

The TPS61197 is enabled with soft startup when the EN pin voltage is higher than 1.6V. A voltage of less than 0.75V disables the TPS61197. An under-voltage lockout protection feature is provided in the TPS61197. When the voltage at the VIN pin is less than 6.5V, the TPS61197 is powered off. The TPS61197 resumes the operation once the voltage at the VIN pin recovers above the hysteresis (V_{VIN_HYS}) more than the UVLO falling threshold of input voltage. If a higher under-voltage lockout (UVLO) voltage is required, use the UVLO pin as shown in Figure 18 to adjust the input UVLO threshold by using an external resistor divider. Once the voltage at the UVLO

pin exceeds the 1.229V threshold, the TPS61197 is powered on and a hysteresis current source of 3.9µA is added. When the voltage at the UVLO pin drops lower than 1.229V, the current source is removed and the TPS61197 is powered off. The resistors of R1, R2 can be calculated by Equation 2 from required turn-on voltage (V_{START}) and turn-off voltage (V_{STOP}). To avoid noise coupling, the resistor divider R1 and R2 must be close to the UVLO pin. Placing a filter capacitor of more than 10nF as shown in Figure 18 can eliminate the impact of the switching ripple of the input voltage and improve the noise immunity.

If the UVLO function is not used, pull up the UVLO pin to the VDD pin.

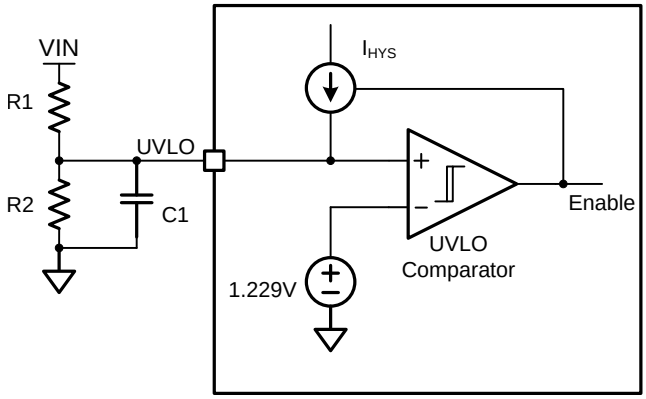


Figure 18. The Under-Voltage Lockout Circuit

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R2 = R1 \frac{1.229V}{V_{START} - 1.229V} \quad (3)$$

Where I_{HYS} is 3.9µA sourcing current from the UVLO pin.

When the UVLO condition happens, the FAULT pin outputs high impedance. As long as the UVLO condition is removed, the FAULT pin outputs low impedance.

Power Up Sequencing and Soft Startup

The input voltage, UVLO pin voltage, EN input signal and the input dimming PWM signal control the power up of the TPS61197. After the input voltage is above the required minimal input voltage of 7.5V, the internal circuit is ready to be powered up. After the UVLO pin voltage is above the threshold of 1.229V and the EN signal is high, the internal LDO and logic circuit are activated. When the PWM dimming signal is high, the soft startup begins.

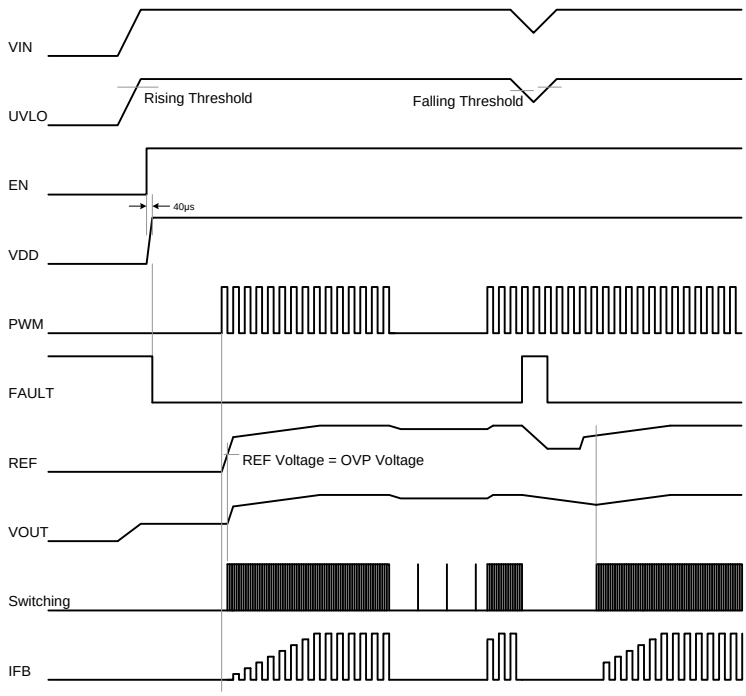


Figure 19. Power up Sequencing

The TPS61197 has integrated the soft-start circuitry working with an external capacitor at the REF pin to avoid inrush current during startup. During the startup period, the capacitor at the REF pin is charged with a soft-start current source. When the REF pin voltage is higher than the output feedback voltage at the OVP pin, the boost controller starts switching and the output voltage starts to ramp up. At the same time, the LED current regulation circuit starts to drive the LED string. At the beginning of the soft start, the charge current is 200µA. Once the voltage of the REF pin exceeds 2.0V, the charge current stops. The output voltage continues to ramp up until the IFB voltage is in regulation of 300mV. The total soft start time is determined by the external capacitance at the REF pin. The capacitance must be within 470nF to 4.7µF for different startup time.

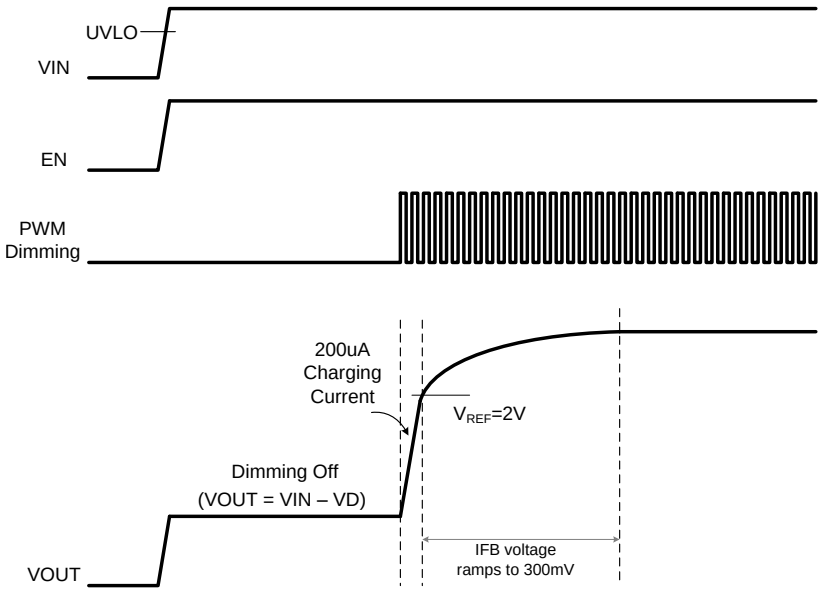


Figure 20. Soft Start Waveforms

Current Regulation

The TPS61197 regulates the IFB voltage to 300mV. Applying a current sense resistor (R9 in the SIMPLIFIED SCHEMATIC CIRCUIT) at the IFB pin to set the required LED current.

$$I_{LED} = \frac{V_{IFB\_REG}}{R9} \quad (4)$$

Where V_{IFB_REG} is the IFB pin regulation voltage of 300mV.

PWM Dimming

LED brightness dimming is set by applying an external PWM signal of 90Hz to 22kHz to the PWM pin. Varying the PWM duty cycle from 0% to 100% adjusts the LED from minimum to maximum brightness respectively. The recommended minimum on time of the LED string is 10µsec. Thus the TPS61197 has a minimum dimming ratio of 500:1 at 200Hz.

When the PWM voltage is pulled low during dimming off, the TPS61197 turns off the LED string and keeps the boost converter running in PFM mode. In PFM mode, the output voltage is kept at a level which is a little bit lower than that when the PWM voltage is high. Thus, the TPS61197 limits the output ripple due to the load transient that occurs during PWM dimming.

When the PWM voltages are pulled low for more than 20ms, to avoid the REF pin voltage dropping due to the leakage current, the voltage of the REF pin is held by an internal reference voltage which is a little bit lower than the REF pin voltage in normal dimming operation. Thus the output voltage will be kept unchanged during the long dimming off time.

Since the output voltage in long time dimming off status is almost the same as the normal voltage for turning the LED on, the TPS61197 turns on the LED very fast without any flicker when recovering from long time dimming off to normal dimming operation.

Protections

The TPS61197 has full set of protections making the system safe to any abnormal conditions. Some protections will latch the TPS61197 in off state until its power supply is recycled or it is disabled and then enabled again. In the latch-off state, the REF pin voltage is discharged to 0V.

1. Switch current limit protection using the ISNS pin

   The TPS61197 monitors the inductor current through the voltage across a sense resistor (R5 in the SIMPLIFIED SCHEMATIC CIRCUIT) in order to provide current limit protection. During the switch FET on period, when the voltage at the ISNS pin rises above the over-current protection threshold (V_{PWM_OCP} or V_{PFM_OCP} in the ELECTRICAL CHARACTERISTICS table), the IC turns off the FET immediately and does not turn it back on until the next switching cycle. The switch current limit is equal to V_{PWM_OCP} / R5 (or V_{PFM_OCP} / R5). The current limit is different for PWM mode and PFM mode. In the PWM mode, the current limit threshold voltage is 400mV typically. In the PFM mode, it is 180mV typically.

2. LED open protection

   When the LED string is open, the IFB pin voltage drops to zero volt during dimming-on time. The TPS61197 keeps increasing the output voltage until it touches the output over-voltage protection threshold. The TPS61197 is then latched off.

3. Schottky diode open protection

   When the TPS61197 is enabled, it checks the topology connection first. The TPS61197 detects the voltage at the OVP pin to check if the Schottky diode is not connected or the boost output is hard-shorted to ground. If the voltage at the OVP pin is lower than 70mV for 80ms, the TPS61197 is locked in off state until the input power is recycled or the TPS61197 is enabled again.

4. Schottky diode short protection

   If the rectifier Schottky diode is shorted, the reverse current from output capacitor to ground is very large when the switch MOSFET is turned on. The TPS61197 uses a secondary current limit threshold of 800mV across the current sense resistor to permanently disable the switching if the threshold is touched.

5. IFB over-voltage protection

When the IFB pin reaches the threshold (V_{IFB_OVP} in the ELECTRICAL CHARACTERISTICS table) of 1.1V during startup or normal operation, the IC stops switching and stays in the latch-off state immediately to protect from damage. This function protects the external dimming MOSFET from damage when the LED string is shorted from the anode (connecting to output of the boost converter) to its cathode.

6. Output over-voltage protection using the OVP pin

Use a resistor divider to program the maximum output voltage of the boost converter. To ensure the LED string can be turned on with setting current, the maximum output voltage must be higher than the forward voltage drop of the LED string. The maximum required voltage can be calculated by multiplying the maximum LED forward voltage ($V_{FWD(max)}$) and number (n) of series LEDs , and adding extra 2V to account for regulation and resistor tolerances and load transients.

The recommended bottom feedback resistor of the resistor divider (R4 in the SIMPLIFIED SCHEMATIC CIRCUIT) is 20kΩ. Calculate the top feedback resistor (R3, in the SIMPLIFIED SCHEMATIC CIRCUIT) using Equation 5, where V_{OUT_OVP} is the output over-voltage protection threshold of the boost converter.

$$R3 = \left(\frac{V_{OUT\_OVP}}{3.04} - 1 \right) \times R4 \quad (5)$$

When the IC detects that the OVP pin voltage exceeds the over-voltage protection threshold of 3.04V, indicating that the output voltage has exceeded the over-voltage proteciton threshold, the TPS61197 clamps the output voltage to prevent it going up any more. If the OVP pin voltage does not drop below the OVP threshold for more than 640ms, the TPS61197 is latched off until the input power or the EN pin is re-cycled.

7. IFB short to ground protection

The TPS61197 monitors the IFB pin voltage when the device is enabled. If the IFB pin voltage is less than 200mV, the TPS61197 keeps increasing the output voltage until the over-voltage protection or the switch over-current protection happens. If the IFB pin voltage is still under 200mV for 60ms in these protection conditions, the TPS61197 is latched off.

8. Thermal Protection

When the internal junction temperature of the TPS61197 is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature falls back to less than 150°C, with approximate 15°C hysteresis.

Table 2. Protection List

PROTECTION ITEM	FAULT CONDITIONS	FAULT	RESULT
Diode Open	V_{OVP} < 70mV for more than 80ms	Y	Latch off
Diode Short	V_{ISNS} > 800mV for three switching cycles	Y	Latch off
Output Over Voltage	V_{OVP} > 3.04V for more than 640ms	Y	Latch off
LED String Open	(V_{IFB} < 200mV and V_{OVP} > 3.04V) for more than 60ms	Y	Latch off
LED String Short	V_{IFB} > 1.1V	Y	Latch off
IFB Short to Ground	(V_{IFB} < 200mV and V_{OVP} > 3.04V) or (V_{IFB} < 200mV and V_{ISNS} > 400mV) for more than 60ms	Y	Latch off
Input Voltage under UVLO Threshold	V_{UVLO} < 1.229V	Y	Retry
Thermal Shutdown	T_J > 150ºC	Y	Retry

Indication for Fault Conditions

The TPS61197 has an open-drain fault indicator pin to indicate abnormal conditions. When the TPS61197 is operating normally, the voltage at the FAULT pin is low. When any fault condition happens, the FAULT pin is in high impedance, which can be pulled up to a high voltage level through an external resistor.

APPLICATION INFORMATION

Inductor Selection

The inductor is the most important component in switching power regulator design because it affects power supply steady state operation, transient behavior, and loop stability. The inductor value, DC resistance and saturation current are important specifications to be considered for better performance. Although the boost power stage can be designed to operate in discontinuous conduction mode (DCM) at maximum load, where the inductor current ramps down to zero during each switching cycle, most applications will be more efficient if the power stage operates in continuous conduction mode (CCM), where a DC current flows through the inductor. Therefore, the Equation 7 and Equation 8 are for CCM operation only. The TPS61197 is designed to work with inductor values between 4.7 µH and 470 µH, depending on the switching frequency. Running the controller at higher switching frequencies allows the use of smaller and/or lower profile inductors in the 4.7µH range. Running the controller at slower switching frequencies requires the use of larger inductors, near 470µH, to maintain the same inductor current ripple but may improve overall efficiency due to smaller switching losses. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value measured at near 0-A, depending on how the inductor vendor defines saturation.

In a boost regulator, the inductor DC current can be calculated with Equation 6.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

Where:

V_{OUT} = boost output voltage
I_{OUT} = boost output current
V_{IN} = boost input voltage
η = power conversion efficiency, use 95% for TPS61197 applications

The inductor peak-to-peak ripple current can be calculated with Equation 7.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (7)$$

Where:

$\Delta I_{L(P-P)}$ = inductor ripple current
L = inductor value
f_{SW} = switching frequency
V_{OUT} = boost output voltage
V_{IN} = boost input voltage

Therefore, the inductor peak current is calculated with Equation 8.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (8)$$

Select an inductor, which saturation current is higher than calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the switch FET and power diode. Besides the external switch FET, the overall efficiency is also affected by the inductor DC resistance (DCR). Usually the lower DC resistance shows higher efficiency. However, there is a tradeoff between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones.

Schottky Diode

The TPS61197 demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the output LED current and inductor peak current. In addition, the diode's reverse breakdown voltage must exceed the application output voltage.

Switch MOSFET and Gate Driver Resistor

The TPS61197 demands a power N-MOSFET (see Q1 in SIMPLIFIED SCHEMATIC CIRCUIT) as a switch. The voltage and current rating of the MOSFET must be higher than the application output voltage and the inductor peak current. The applications benefit from the addition of a resistor (See R10 in SIMPLIFIED SCHEMATIC CIRCUIT) connected between the GDRV pin and the gate of the switch MOSFET. With this resistor, the gate driving current is limited and the EMI performance is improved. A 3-Ω resistor value is recommended. The TPS61197 exhibits lower efficiency when the resistor value is above 3Ω due to the more switching loss of the external MOSFET.

Current Sense and Current Sense Filtering

R5 determines the correct over-current limit protection. To choose the right value of R5, start with the total system power needed P_{OUT}, and calculate the input current I_{IN} by Equation 6. Efficiency can be estimated from Figure 3. The second step is to calculate the inductor peak current based on the inductor value L using Equation 7 and Equation 8. The maximum R5 can now be calculated as R5(max) = V_{ISNS_OC} / $I_{L(P)}$. It is recommended to add 20% or more margins to account for component variations. A small filter placed on the ISNS pin improves performance of the converter (See R6 and C5 in SIMPLIFIED SCHEMATIC CIRCUIT). The time constant of this filter should be approximately 100ns. The range of R6 must be from about 300Ω to 1kΩ for best results. The C5 should be located as close as possible to the ISNS pin to provide noise immunity.

Output Capacitor

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability of the whole system. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$V_{RIPPLE(C)} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}} \quad (9)$$

Where V_{RIPPLE} is the peak to peak output voltage ripple and D_{MAX} is the maximum duty cycle of the boost converter in the application.

D_{MAX} is approximately equal to ($V_{OUT(MAX)}$ – $V_{IN(MIN)}$ / $V_{OUT(MAX)}$) in applications. Care must be taken when evaluating a capacitor's derating under DC voltage. The DC bias voltage can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance.

The ESR impact on the output ripple must be considered as well if tantalum or aluminum electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{RIPPLE} is:

$$V_{RIPPLE(ESR)} = I_{L(P)} \times ESR \quad (10)$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes temperature increase internally to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Therefore, high ripple current type electrolytic capacitor with small ESR is used in the typical application as shown in SIMPLIFIED SCHEMATIC CIRCUIT.

In the typical application, the output requires a capacitor in the range of 1.0µF to 100µF. The output capacitor affects the small signal control loop stability of the boost converter. If the output capacitor is below the range, the boost regulator may potentially become unstable.

Loop Consideration

The COMP pin on the TPS61197 is used for external compensation, allowing the loop response to be optimized for each application. The COMP pin is the output of the internal trans-conductance amplifier. The external resistor R8, along with ceramic capacitors C6 (see in SIMPLIFIED SCHEMATIC CIRCUIT), are connected to the COMP pin to provide poles and zero. The pole and zero, along with the inherent pole and zero in a peak current mode control boost converter, determine the closed loop frequency response. This is important to converter stability and transient response.

The first step is to calculate the pole and the right half plane zero of the peak current mode boost converter by Equation 11 and Equation 12.

$$f_P = \frac{2I_{OUT}}{2\pi V_{OUT} \times C_{OUT}} \quad (11)$$

$$f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi L \times I_{OUT}} \quad (12)$$

To make the loop stable, the loop must have sufficient phase margin at the crossover frequency where the loop gain is 1. To avoid the effect of the right half plane zero on the loop stability, choose the crossover frequency f_{CO} less than 1/5 of the f_{ZRHP}. Then calculate the compensation components by Equation 13 and Equation 14.

$$R8 = \frac{R5 \times 2\pi f_{CO} \times C_{OUT}}{(1-D) \times Gm_{EA}} \times \frac{V_{OUT\_OVP}}{V_{OVPTH}} \quad (13)$$

Where V_{OVPTH} = 3.04V, which is the over-voltage protection threshold at the OVP pin. V_{OUT_OVP} is the setting output over-voltage protection threshold. Gm_{EA} is the trans-conductance of the error amplifier. The typical value of the Gm_{EA} is 120μS. f_{CO} is the crossover frequency, which normally is less than 1/5 of the f_{ZRHP}.

$$C6 = \frac{1}{2\pi f_P \times R8} \quad (14)$$

Where f_P is the pole's frequency of the power stage calculated by Equation 11. If the output capacitor is the electrolytic capacitor which may have large ESR, a capacitor is required at the COMP pin or at the OVP pin to cancel the inherent zero of the output capacitor.

Layout Consideration

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The VDD capacitor, C3 (see in SIMPLIFIED SCHEMATIC CIRCUIT) is the filter and noise decoupling capacitor for the internal linear regulator powering the internal circuitries. It should be placed as close as possible between the VDD and PGND pin to prevent any noise insertion to internal circuitries. The switch node at the drain of Q1 carries high current with fast rising and falling edges. Therefore, the connection between this node to the inductor and the schottky diode should be kept as short and wide as possible. The ground of output capacitor EC2 should be kept close to input power ground or through a large ground plane because of the large ripple current returning to the input ground. When laying out signal grounds, it is recommended to use short traces separate from power ground traces and connect them together at a single point. Resistors R3, R4 and R7 (see in the SIMPLIFIED SCHEMATIC CIRCUIT) are setting resistors for switching frequency and output over-voltage protection. To avoid unexpected noise coupling into the pins and affecting the accuracy, these resistors need to be close to the pins with short and wide traces to AGND pin.

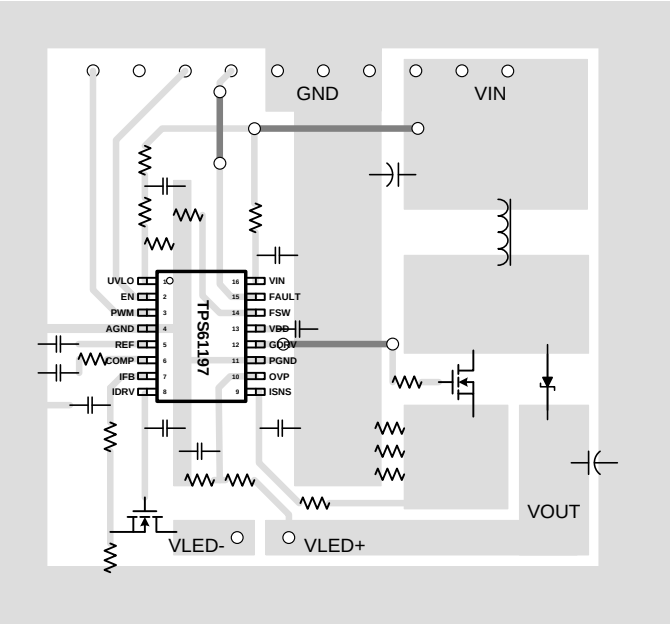


Figure 21. Layout Example

Typical Applications

The TPS61197 can be configured as a simple boost converter to drive the LEDs when the boost ratio of the output voltage to the input voltage is less than 6. When the boost ratio is higher than 6, a transformer is required to replace the inductor to make the switching duty cycle near 50% and lower the voltage rating of the switch FET. Figure 22 shows this application.

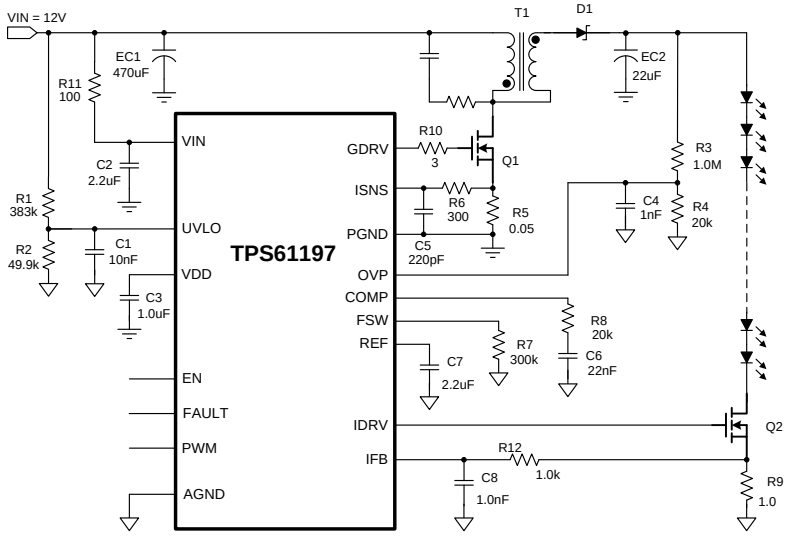


Figure 22. High Boost Ratio Application

The TPS61197 also supports the PWM dimming by turning on and off the boost converter to save cost of the dimming MOSFET. Figure 23 is the application circuit. This application requires small output capacitance so as to discharge the output voltage fast during dimming off period. The minimum dimming on time must be longer than 200µs to ramp up the output voltage to achieve the setting LED current during dimming on period.

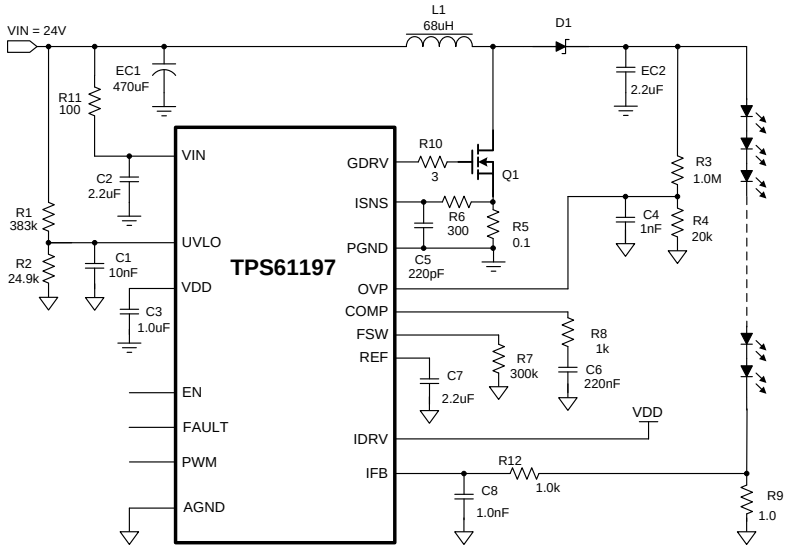


Figure 23. PWM Dimming by Turning on and off the Boost Converter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61197DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	TPS61197	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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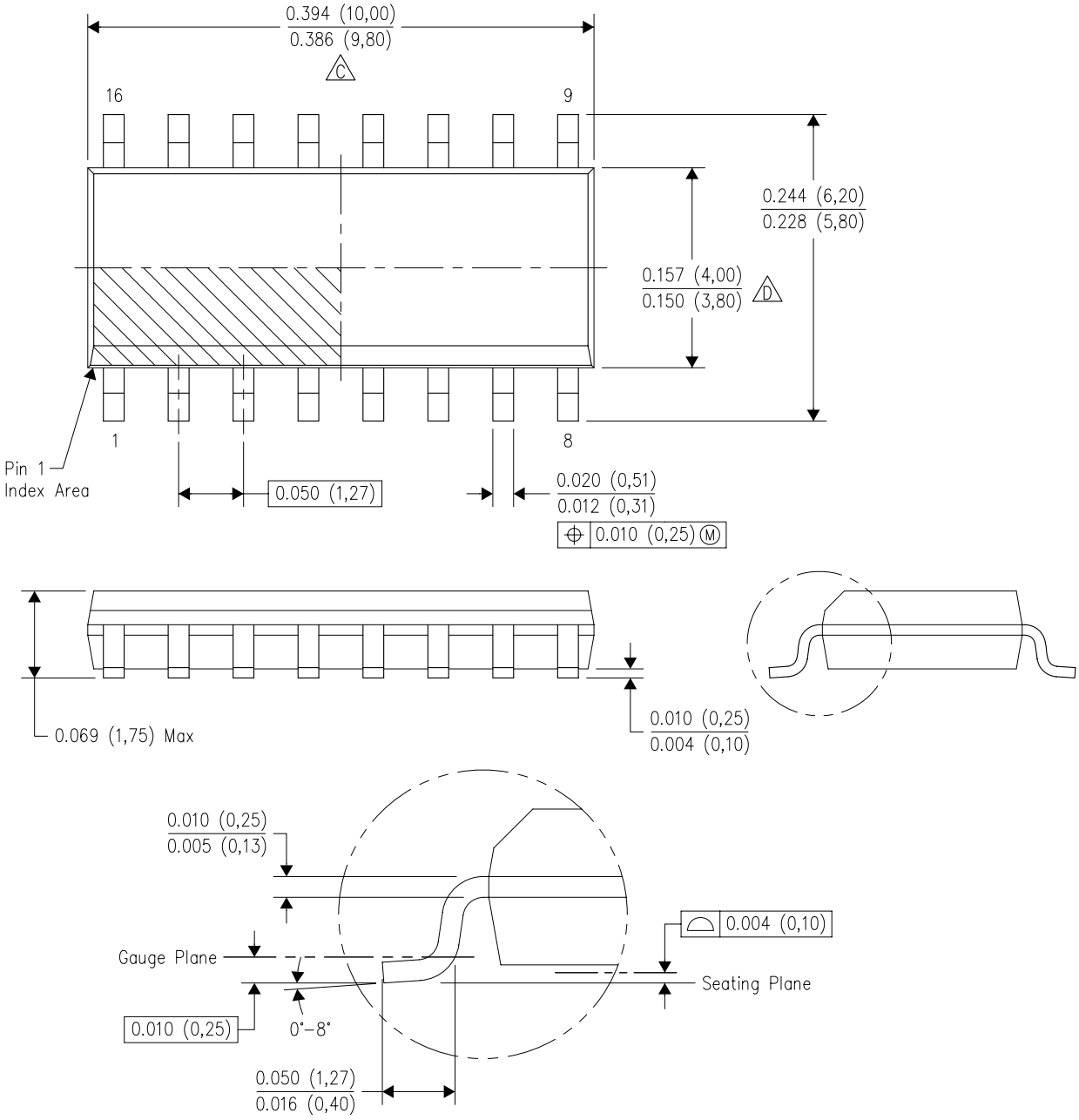
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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