

## High Brightness White LED Driver in SOT-23 Package

Check for Samples: [TPS61165-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- 3-V to 18-V Input Voltage Range
- 38-V Open LED Protection
- 200-mV Reference Voltage With 2% Accuracy
- 1.2-A Switch FET With 1.2-MHz Switching Frequency
- Flexible 1 Wire Digital and PWM Brightness Control
- Built-in Soft Start
- Up to 90% Efficiency
- SOT-23 Package

### APPLICATIONS

- High Brightness LED Lighting
- White LED Backlighting for Media Form Factor Display

### DESCRIPTION

With a 40-V rated integrated switch FET, the TPS61165-Q1 is a boost converter that drives LEDs in series. The boost converter runs at a 1.2-MHz fixed switching frequency with 1.2-A switch current limit, and allows for the use of a high brightness LED in general lighting.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200mV, as shown in the typical application. During the operation, the LED current can be controlled using the 1 wire digital interface (Easyscale™ protocol) through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the TPS61165-Q1 does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS61165-Q1 to prevent the output from exceeding its absolute maximum voltage ratings during open LED conditions.

The TPS61165-Q1 is available in a SOT-23 package.

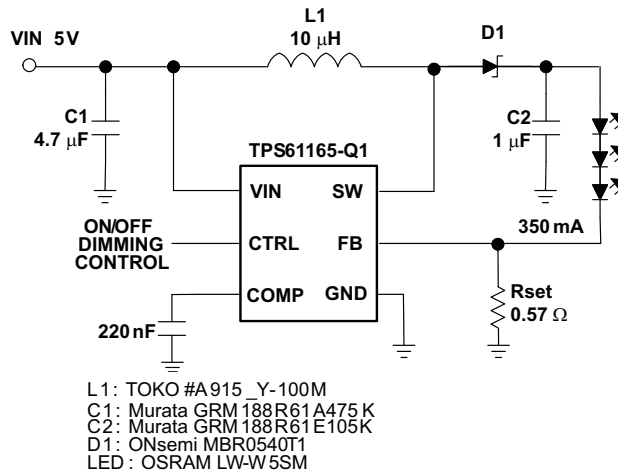


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Easyscale is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	OPEN LED PROTECTION	PACKAGE	PACKAGE MARKING
-40°C to 105°C	38 V (typical)	TPS61165TDBVRQ1	SBM

(1) For the most current package and ordering information, see the TI Web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT
V <sub>I</sub>	Supply Voltages on VIN <sup>(2)</sup>	-0.3 to 20	V
	Voltages on CTRL <sup>(2)</sup>	-0.3 to 20	V
	Voltage on FB and COMP <sup>(2)</sup>	-0.3 to 3	V
	Voltage on SW <sup>(2)</sup>	-0.3 to 40	V
P <sub>D</sub>	Continuous Power Dissipation	See the Thermal Information Table	
T <sub>J</sub>	Operating Junction Temperature Range	-40 to 150	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)(2)</sup>		TPS61165-Q1	UNITS
		DBV	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	210.1	°C/W
θ <sub>JC(top)</sub>	Junction-to-case(top) thermal resistance	46.8	
θ <sub>JB</sub>	Junction-to-board thermal resistance	56.7	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	50.2	
θ <sub>JC(bottom)</sub>	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://SPRA953).

(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
V <sub>I</sub>	Input voltage range, VIN	3		18	V
V <sub>O</sub>	Output voltage range	VIN		38	V
L	Inductor <sup>(1)</sup>	10		22	µH
f <sub>dim</sub>	PWM dimming frequency	5		100	kHz
C <sub>IN</sub>	Input capacitor	1			µF
C <sub>O</sub>	Output capacitor	1		10	µF
T <sub>A</sub>	Operating ambient temperature	-40		105	°C
T <sub>J</sub>	Operating junction temperature	-40		125	°C
	ESD rating, CDM			1.0	kV
	ESD rating, HBM			1.0	kV
	ESD rating, MM			100	V

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

## ELECTRICAL CHARACTERISTICS

VIN = 3.6 V, CTRL = VIN, TA = -40°C to 105°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
VI	Input voltage range, VIN		3		18	V
IQ	Operating quiescent current into VIN	Device PWM switching no load			2.3	mA
ISD	Shutdown current	CTRL=GND, VIN = 4.2 V			2	µA
UVLO	Under-voltage lockout threshold	VIN falling		2.2	2.5	V
Vhys	Under-voltage lockout hysteresis			70		mV
<b>ENABLE AND REFERENCE CONTROL</b>						
V(CTRLh)	CTRL logic high voltage	VIN = 3 V to 18 V	1.2			V
V(CTRLl)	CTRL logic low voltage	VIN = 3 V to 18 V			0.4	V
R(CTRL)	CTRL pull down resistor		400	800	1600	kΩ
t <sub>off</sub>	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
t <sub>es_det</sub>	Easy Scale detection time <sup>(1)</sup>	CTRL pin low	260			µs
t <sub>es_delay</sub>	Easy Scale detection delay		100			µs
t <sub>es_win</sub>	Easy Scale detection window time	Measured from CTRL high	1			ms
<b>VOLTAGE AND CURRENT CONTROL</b>						
VREF	Voltage feedback regulation voltage		196	200	204	mV
V(REF_PWM)	Voltage feedback regulation voltage under brightness control	V <sub>FB</sub> = 50 mV	47	50	53	mV
		V <sub>FB</sub> = 20 mV	17	20	23	
I <sub>FB</sub>	Voltage feedback input bias current	V <sub>FB</sub> = 200 mV			2	µA
f <sub>S</sub>	Oscillator frequency		1.0	1.2	1.5	MHz
D <sub>max</sub>	Maximum duty cycle	V <sub>FB</sub> = 100 mV	90%	93%		
t <sub>min_on</sub>	Minimum on pulse width			40		ns
I <sub>sink</sub>	Comp pin sink current			100		µA
I <sub>source</sub>	Comp pin source current			100		µA
G <sub>ea</sub>	Error amplifier transconductance		240	320	400	umho
R <sub>ea</sub>	Error amplifier output resistance			6		MΩ
f <sub>ea</sub>	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
<b>POWER SWITCH</b>						
R <sub>DS(ON)</sub>	N-channel MOSFET on-resistance	VIN = 3.6 V		0.3	0.6	Ω
		VIN = 3.0 V			0.7	
I <sub>LN_NFET</sub>	N-channel leakage current	V <sub>SW</sub> = 35 V, TA = 25°C			1	µA
<b>OC and OLP</b>						
I <sub>LIM</sub>	N-Channel MOSFET current limit	D = D <sub>max</sub>	0.96	1.2	1.44	A
I <sub>LIM_Start</sub>	Start up current limit	D = D <sub>max</sub>		0.7		A
t <sub>Half_LIM</sub>	Time step for half current limit			5		ms
V <sub>ovp</sub>	Open LED protection threshold	Measured on the SW pin	37	38	39	V
V(FB_OVP)	Open LED protection threshold on FB	Measured on the FB pin, percentage of Vref, Vref = 200 mV and 20 mV		50%		
t <sub>REF</sub>	V <sub>REF</sub> filter time constant			180		µs
t <sub>step</sub>	V <sub>REF</sub> ramp up time	Each step, Measured as number of cycles of the 1.2 MHz clock		213		µs
<b>EasyScale TIMING</b>						
t <sub>start</sub>	Start time of program stream		2			µs
t <sub>EOS</sub>	End time of program stream		2		360	µs
t <sub>H_LB</sub>	High time low bit	Logic 0	2		180	µs
t <sub>L_LB</sub>	Low time low bit	Logic 0	2 × t <sub>H_LB</sub>		360	µs

(1) To select EasyScale™ mode, the CTRL pin has to be low for more than t<sub>es\_det</sub> during t<sub>es\_win</sub>.

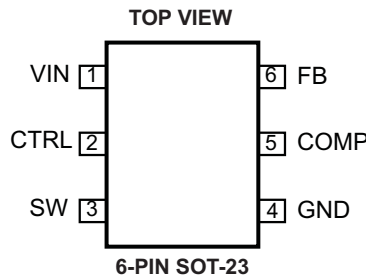
**ELECTRICAL CHARACTERISTICS (continued)**

VIN = 3.6 V, CTRL = VIN, TA = -40°C to 105°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>H_HB</sub>	High time high bit	Logic 1	2 × t <sub>L_HB</sub>		360	µs
t <sub>L_HB</sub>	Low time high bit	Logic 1	2		180	µs
V <sub>ACKNL</sub>	Acknowledge output voltage low	Open drain, R <sub>pullup</sub> =15 kΩ to VIN			0.4	V
t <sub>valACKN</sub>	Acknowledge valid time	See <sup>(2)</sup>			2	µs
t <sub>ACKN</sub>	Duration of acknowledge condition	See <sup>(2)</sup>			512	µs
<b>THERMAL SHUTDOWN</b>						
T <sub>shutdown</sub>	Thermal shutdown threshold				160	°C
T <sub>hysteresis</sub>	Thermal shutdown threshold hysteresis				15	°C

(2) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line must be pulled high by the host with resistor load.

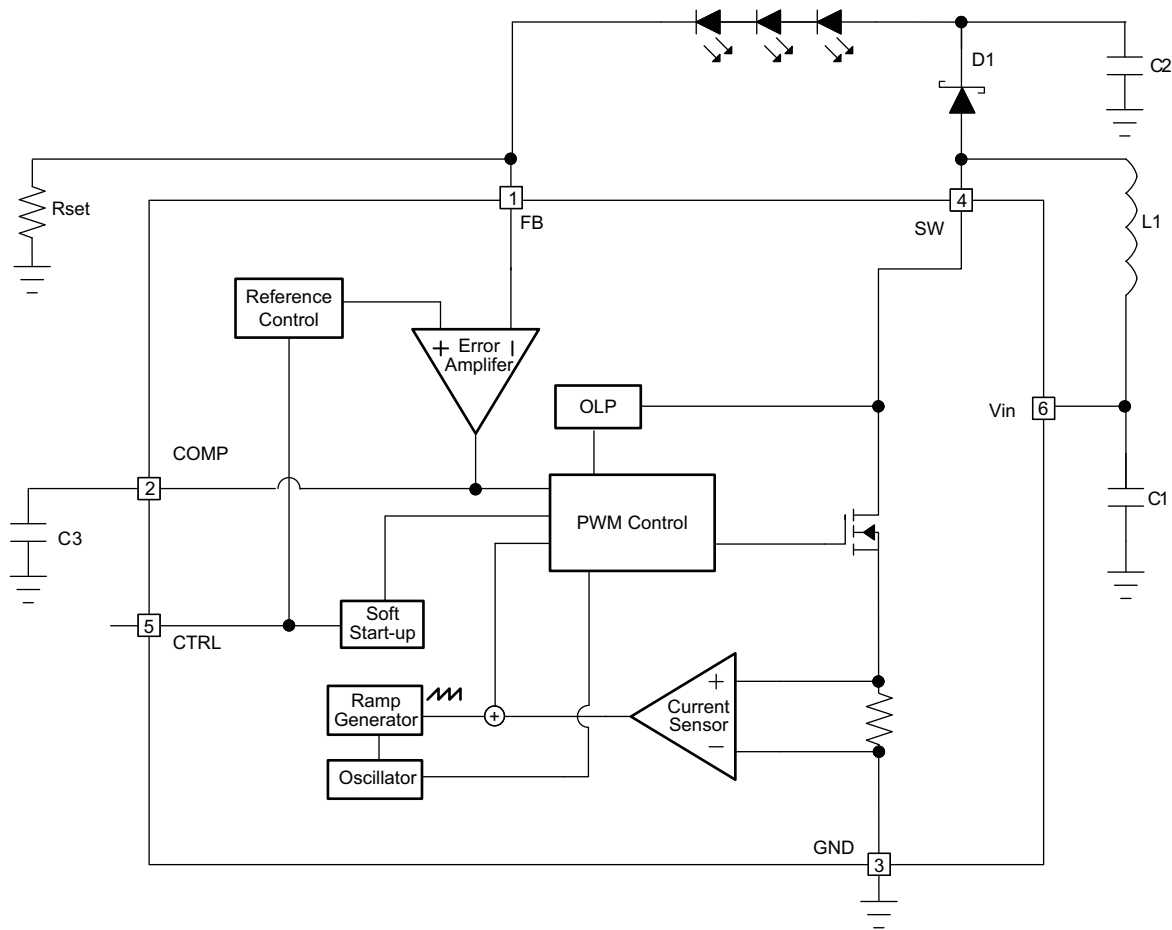
**DEVICE INFORMATION**



**PIN FUNCTIONS**

PIN		I/O	DESCRIPTION
NAME	DBV NO.		
VIN	1	I	The input supply pin for the IC. Connect VIN to a supply voltage between 3V and 18V.
SW	3	I	This is the switching node of the IC. Connect the switched side of the inductor to SW. This pin is also used to sense the output voltage for open LED protection.
GND	4	O	Ground
FB	6	I	Feedback pin for current. Connect the sense resistor from FB to GND.
COMP	5	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the converter.
CTRL	2	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency	3 LEDs (VOUT = 12V); VIN = 3, 5, 8.5V; L = 10 μH	<a href="#">Figure 2</a>
Efficiency	6 LEDs (VOUT = 24V); VIN = 5, 8.5, 12V; L = 10 μH	<a href="#">Figure 3</a>
Current limit	TA = 25°C	<a href="#">Figure 4</a>
Current limit		<a href="#">Figure 5</a>
Easyscale step		<a href="#">Figure 6</a>
PWM dimming linearity	VIN = 3.6 V; PWM Freq = 10 kHz and 32 kHz	<a href="#">Figure 7</a>
Output ripple at PWM dimming	3 LEDs; VIN = 5 V; ILOAD = 350 mA; PWM = 32 kHz	<a href="#">Figure 8</a>
Switching waveform	3 LEDs; VIN = 5 V; ILOAD = 3500 mA; L = 10 μH	<a href="#">Figure 9</a>
Start-up	3 LEDs; VIN = 5 V; ILOAD = 350 mA; L = 10 μH	<a href="#">Figure 10</a>
Open LED protection	8 LEDs; VIN = 3.6 V; ILOAD = 20 mA	<a href="#">Figure 11</a>

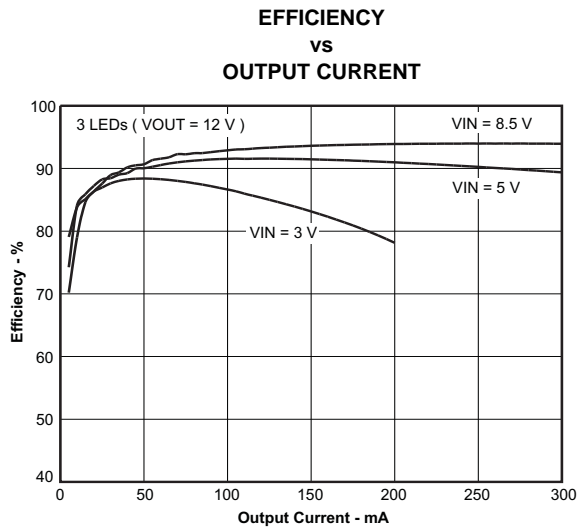


Figure 2.

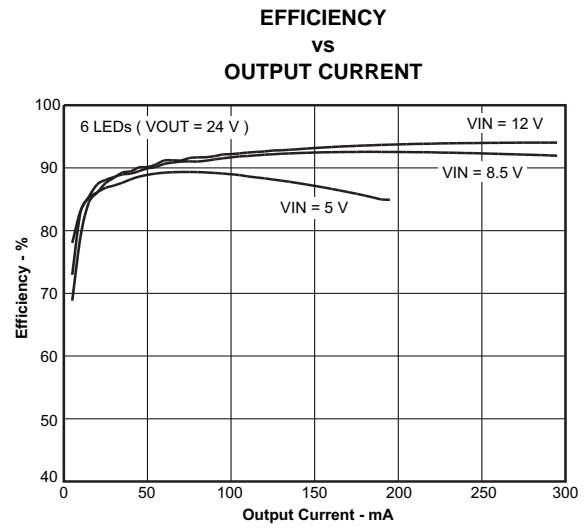


Figure 3.

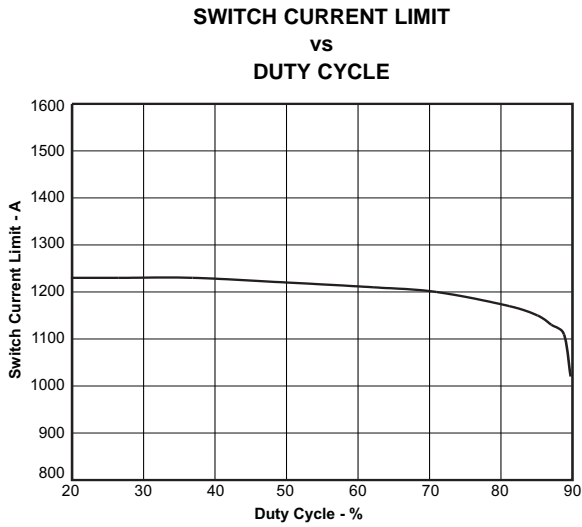


Figure 4.

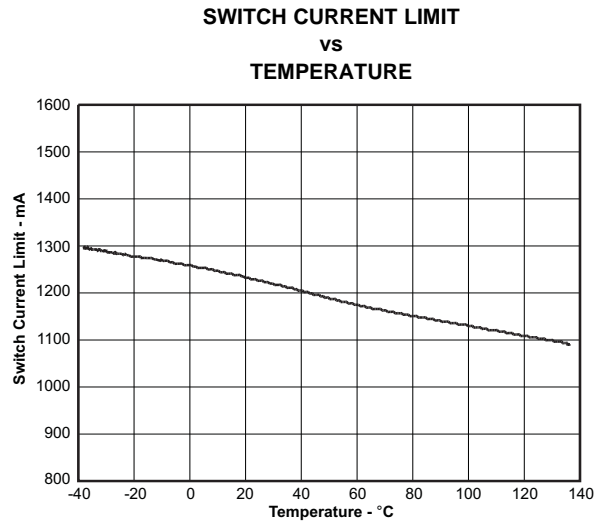


Figure 5.

**FB VOLTAGE  
vs  
EASYSCALE STEP**

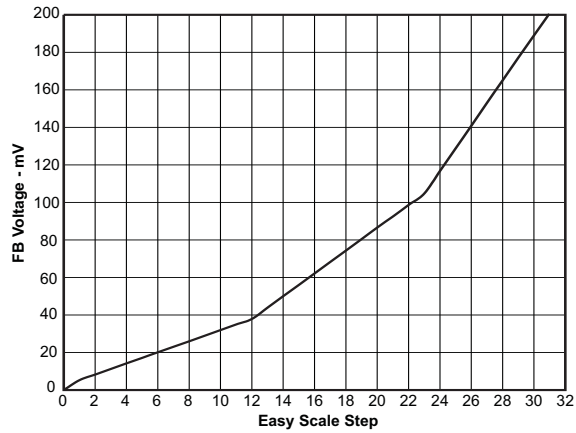


Figure 6.

**FB VOLTAGE  
vs  
PWM DUTY CYCLE**

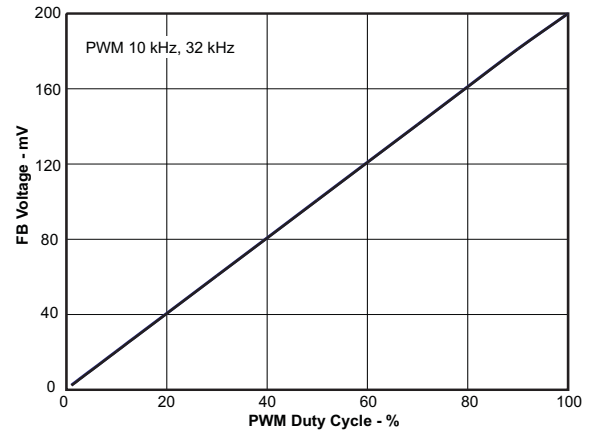


Figure 7.

**OUTPUT RIPPLE at PWM DIMMING**

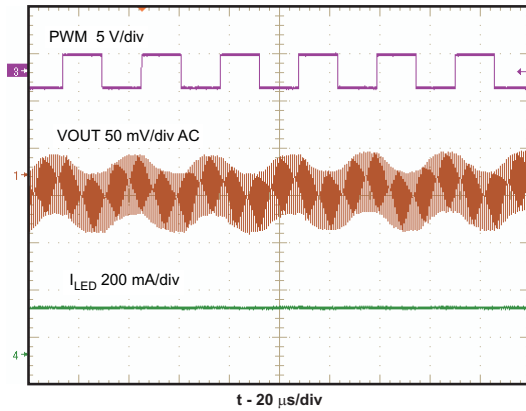


Figure 8.

**SWITCHING WAVEFORM**

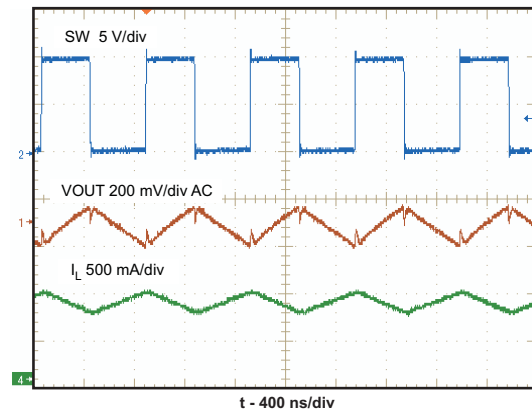


Figure 9.

**START-UP**

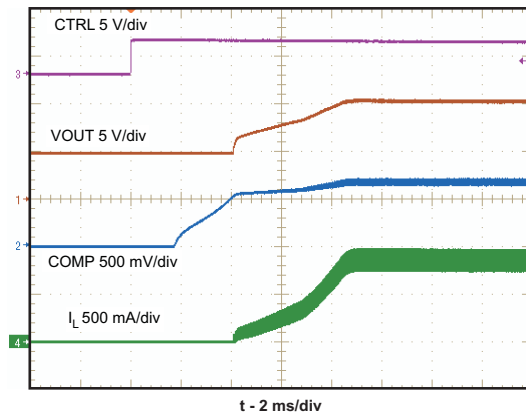


Figure 10.

**OPEN LED PROTECTION**

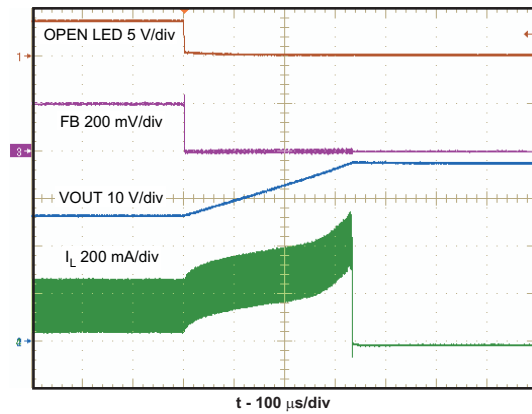


Figure 11.

## DETAILED DESCRIPTION

### OPERATION

The TPS61165-Q1 is a high efficiency, high output voltage boost converter in small package size. The device is ideal for driving white LEDs in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40V/1.2A switch FET and operates in pulse width modulation (PWM) with 1.2MHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, slope compensation is added to the current signal to allow stable operation for duty cycles larger than 40%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

### SOFT START-UP

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps, each step takes 213µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5msec after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 700mA (typical). These two features ensure smooth start-up and minimize the inrush current. See the start-up waveform of a typical example ([Figure 10](#)).

### OPEN LED PROTECTION

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61165-Q1 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions persist for 8 switching clock cycles: (1) the SW voltage exceeds the  $V_{OVP}$  threshold and (2) the FB voltage is less than half of regulation voltage. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin. The product of the number of external series LEDs and each LED's maximum forward voltage plus the 200mV reference voltage does not exceed the 38 V minimum OVP threshold or  $(N_{LEDs} \times V_{LED(MAX)} + 200 \text{ mV} \leq 38 \text{ V})$ .

### SHUTDOWN

The TPS61165-Q1 enters shutdown mode when the CTRL voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is less than 1µA (max). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

### CURRENT PROGRAM

The FB voltage is regulated by a low 0.2V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the  $R_{SET}$  is calculated using [Equation 1](#).

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

Where:

- $I_{LED}$  = output current of LEDs
- $V_{FB}$  = regulated voltage of FB
- $R_{SET}$  = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.



## LED BRIGHTNESS DIMMING MODE SELECTION

The CTRL pin is used for the control input for both dimming modes, PWM dimming and the 1 wire dimming. The dimming mode for the TPS61165-Q1 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter 1 wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61165-Q1, and to start the 1 wire detection window.
2. After the EasyScale detection delay ( $t_{es\_delay}$ , 100 $\mu$ s) expires, drive CTRL low for more than the EasyScale detection time ( $t_{es\_detect}$ , 260 $\mu$ s).
3. The CTRL pin has to be low for more than EasyScale detection time before the EasyScale detection window ( $t_{es\_win}$ , 1msec) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

The IC immediately enters the 1 wire mode once the above 3 conditions are met. the EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start up. This means the IC needs to be shutdown by pulling the CTRL low for 2.5ms and restarts. See the *Dimming Mode Detection and Soft Start* (see Figure 12) for a graphical explanation.

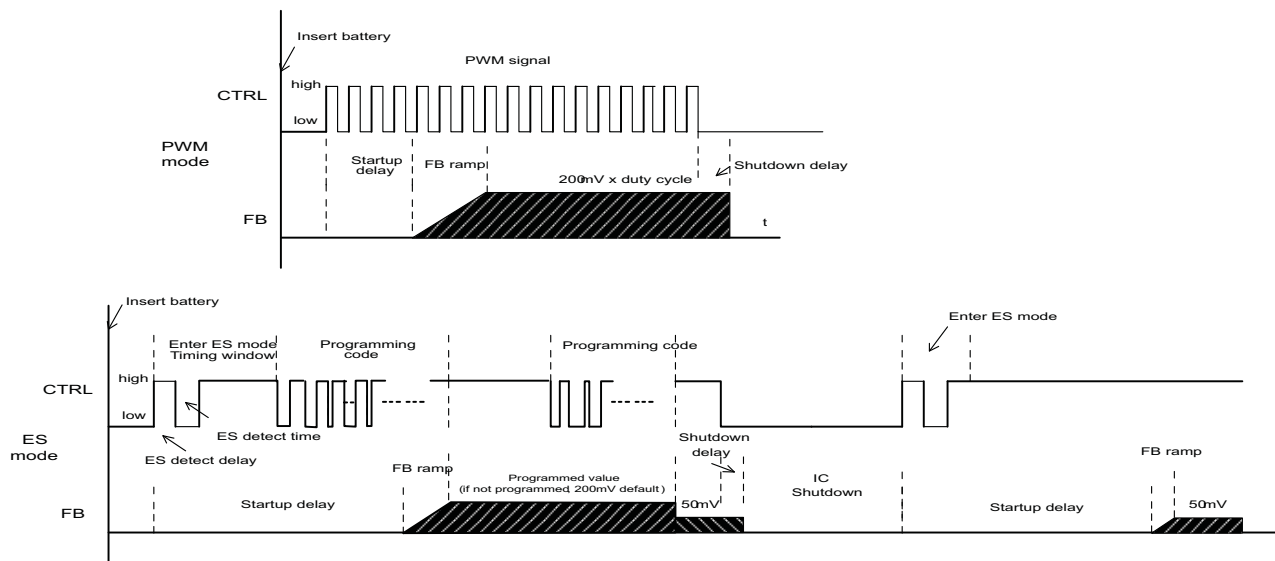


Figure 12. Dimming Mode Detection and Soft Start PWM Brightness Dimming

## PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2:

$$V_{FB} = \text{Duty} \times 200 \text{ mV} \quad (2)$$

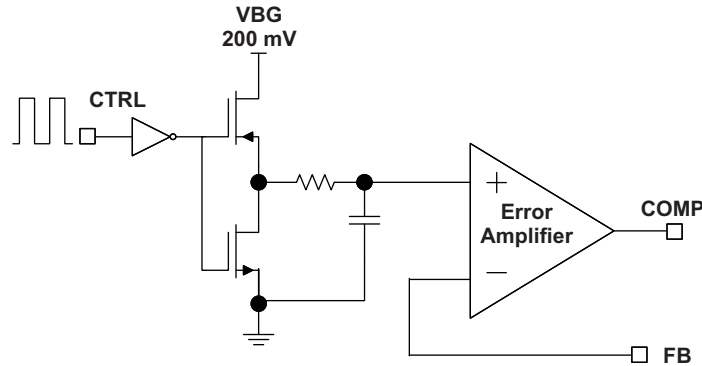
Where:

- Duty = duty cycle of the PWM signal
- 200 mV = internal reference voltage

As shown in Figure 13, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other methods which filters the PWM signal for analog dimming, TPS61165-Q1 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz. The requirement of minimum dimming frequency comes from the EasyScale detection delay and detection time specification in the dimming mode selection. Since the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

To use lower PWM dimming, add external RC network connected to the FB pin as shown in the additional typical application, [Figure 16](#).



**Figure 13. Block Diagram of Programmable FB Voltage Using PWM Signal**

### DIGITAL 1 WIRE BRIGHTNESS DIMMING

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61165-Q1 adopts the EasyScale™ protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See [Table 1](#) for the FB pin voltage steps. The default step is full scale when the device is first enabled ( $V_{FB} = 200\text{ mV}$ ). The programmed reference voltage is stored in an internal register and will not be changed by pulling CTRL low for 2.5ms and then re-enabling the IC by taking CTRL high. A power reset clears the register value and reset it to default.

### EasyScale™: 1 WIRE DIGITAL DIMMING

EasyScale is a simple but flexible one pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. [Figure 14](#) and [Table 2](#) give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other on pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

**Table 1. Selectable FB Voltage**

	FB voltage (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1

Table 1. Selectable FB Voltage (continued)

	FB voltage (mV)	D4	D3	D2	D1	D0
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

DATA IN

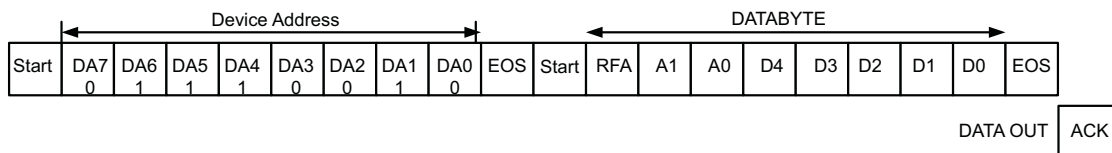


Figure 14. EasyScale™ Protocol Overview

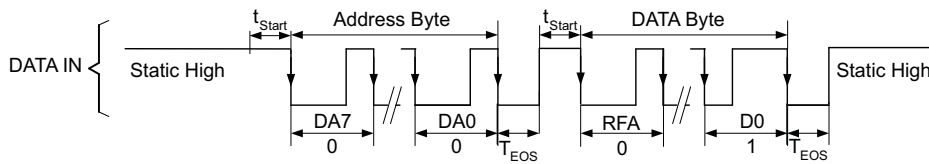
Table 2. EasyScale™ Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address

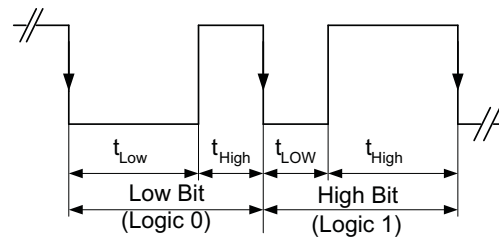
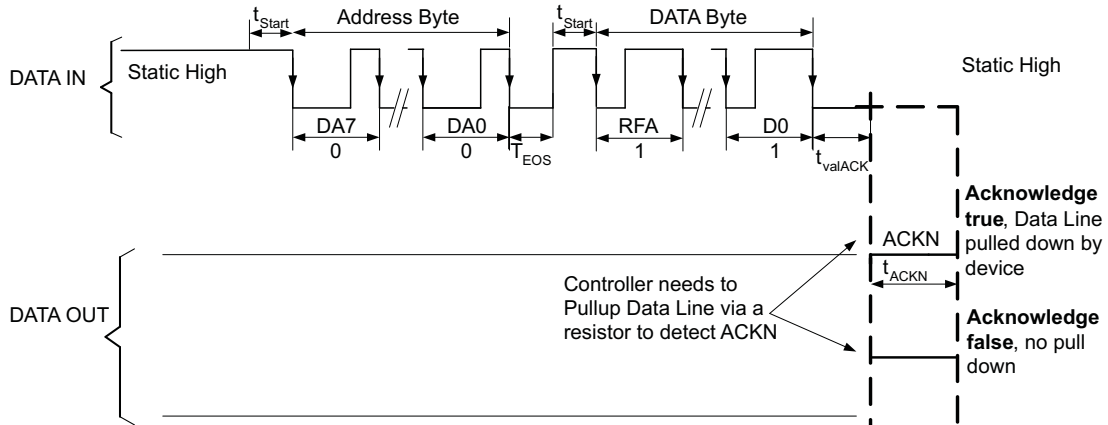
**Table 2. EasyScale™ Bit Description (continued)**

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

**Easy Scale Timing, without acknowledge RFA = 0**



**Easy Scale Timing, with acknowledge RFA = 1**



**Figure 15. EasyScale™— Bit Coding**

All bits are transmitted MSB first and LSB last. [Figure 15](#) shows the protocol without acknowledge request (Bit RFA = 0), [Figure 15](#) with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least  $t_{start}$  (2 $\mu$ s) before the bit transmission starts with the falling edge. If the CTRL pin is already at a high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least  $t_{EOS}$  (2 $\mu$ s).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between  $t_{LOW}$  and  $t_{HIGH}$ . It can be simplified to:

High Bit:  $t_{HIGH} > t_{LOW}$ , but with  $t_{HIGH}$  at least 2x  $t_{LOW}$ , see [Figure 15](#).

Low Bit:  $t_{HIGH} < t_{LOW}$ , but with  $t_{LOW}$  at least 2x  $t_{HIGH}$ , see [Figure 15](#).

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between  $t_{HIGH}$  and  $t_{LOW}$ , the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time  $t_{ACKN}$ , which is 512 $\mu$ s maximum then the Acknowledge condition is valid after an internal delay time  $t_{valACK}$ . This means that the internal ACKN-MOSFET is turned on after  $t_{valACK}$ , when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after  $t_{valACK}$  and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

Note that the acknowledge condition may only be requested if the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CTRL line to limit the current to 500 $\mu$ A is recommended to for such cases as:

- accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

## UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

## THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

## APPLICATION INFORMATION

### MAXIMUM OUTPUT CURRENT

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_p = \frac{1}{\left[ L \times F_s \times \left( \frac{1}{V_{out} + V_f - V_{in}} + \frac{1}{V_{in}} \right) \right]} \quad (3)$$

Where:

$I_p$  = inductor peak to peak ripple

$L$  = inductor value

$V_f$  = Schottky diode forward voltage

$F_s$  = switching frequency

$V_{out}$  = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

$$I_{out\_max} = \frac{V_{in} \times (I_{lim} - I_p/2) \times \eta}{V_{out}} \quad (4)$$

where

$I_{out\_max}$  = Maximum output current of the boost converter

$I_{lim}$  = over current limit

$\eta$  = efficiency

For instance, when  $V_{IN}$  is 3V, 8 LEDs output equivalent to  $V_{OUT}$  of 26V, the inductor is 22 $\mu$ H, the Schottky forward voltage is 0.2V; and then the maximum output current is 110mA in typical condition. When  $V_{IN}$  is 5V, 10 LEDs output equivalent to  $V_{OUT}$  of 32V, the inductor is 22 $\mu$ H, the Schottky forward voltage is 0.2V; and then the maximum output current is 150mA in typical condition.

### INDUCTOR SELECTION

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by [Equation 3](#), pause the inductor DC current given by:

$$I_{in\_DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (5)$$

Inductor values can have  $\pm 20\%$  tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10 $\mu$ H to 22 $\mu$ H inductor value range is recommended. A 22 $\mu$ H inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. [Table 3](#) lists the recommended inductor for the TPS61165-Q1. When recommending inductor value, the factory has considered  $-40\%$  and  $+20\%$  tolerance from its nominal value.

TPS61165-Q1 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10 $\mu$ H, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

**Table 3. Recommended Inductors for TPS61165-Q1**

PART NUMBER	L ( $\mu$ H)	DCR MAX (m $\Omega$ )	SATURATION CURRENT (A)	SIZE (L $\times$ W $\times$ H mm)	VENDOR
A915_Y-100M	10	90	1.3	5.2 $\times$ 5.2 $\times$ 3.0	TOKO
VLCF5020T-100M1R1-1	10	237	1.1	5 $\times$ 5 $\times$ 2.0	TDK
CDRH4D22/HP	10	144	1.2	5 $\times$ 5 $\times$ 2.4	Sumida
LQH43PN100MR0	10	247	0.84	4.5 $\times$ 3.2 $\times$ 2.0	Murata

## SCHOTTKY DIODE SELECTION

The high switching frequency of the TPS61165-Q1 demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. The ONSem MBR0540 and the ZETEX ZHCS400 are recommended for TPS61165-Q1.

## COMPENSATION CAPACITOR SELECTION

The compensation capacitor C3 (see the block diagram), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61165-Q1. A 220nF ceramic capacitor is suitable for most applications.

## INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{out} = \frac{(V_{out} - V_{in}) I_{out}}{V_{out} \times F_s \times V_{ripple}} \quad (6)$$

where,  $V_{ripple}$  = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \quad (7)$$

Due to its low ESR,  $V_{ripple\_ESR}$  can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitors derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1 $\mu$ F to 4.7 $\mu$ F is recommended for input side. The output requires a capacitor in the range of 1 $\mu$ F to 10 $\mu$ F. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

TDK (<http://www.component.tdk.com/components.php>)

Murata (<http://www.murata.com/cap/index.html>)

## LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the IC supply ripple.

## THERMAL CONSIDERATIONS

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61165-Q1. Calculate the maximum allowable dissipation,  $P_{D(max)}$ , and keep the actual dissipation less than or equal to  $P_{D(max)}$ . The maximum-power-dissipation limit is determined using Equation 8:

$$P_{D(max)} = \frac{125^{\circ}\text{C} - T_A}{R_{\theta JA}} \tag{8}$$

where,  $T_A$  is the maximum ambient temperature for the application.  $R_{\theta JA}$  is the thermal resistance junction-to-ambient given in Power Dissipation Table.

## ADDITIONAL TYPICAL APPLICATIONS

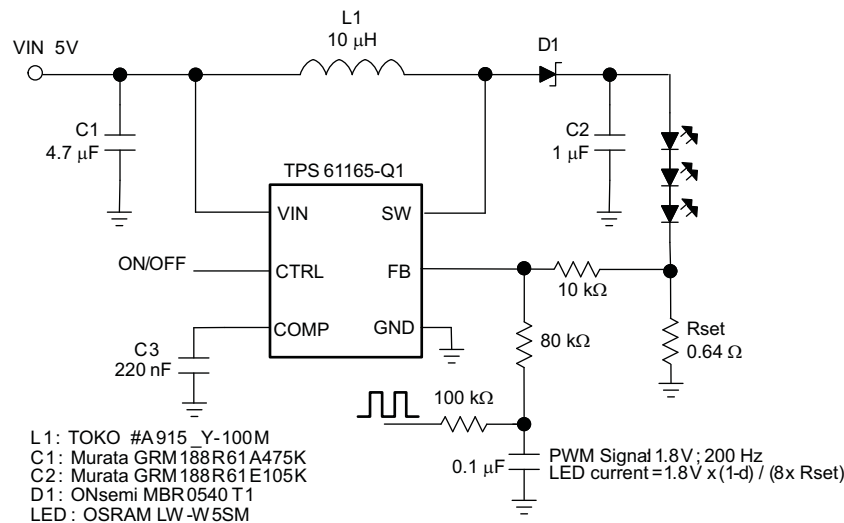


Figure 16. Drive 3 High Brightness LEDs With External PWM Dimming Network

For assistance in selecting the proper values for  $R_{set}$ ,  $R1$ - $R3$ ,  $R_{FLTR}$ ,  $C_{FLTR}$  and  $D2$  for the specific application, see [SLVA471](#) and/or [SLVC366](#).



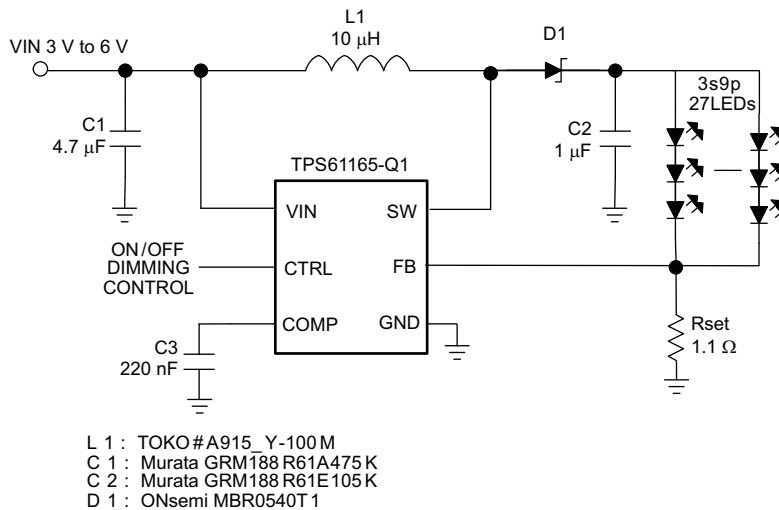


Figure 17. Drive 27 LEDs for Media Form Factor Display

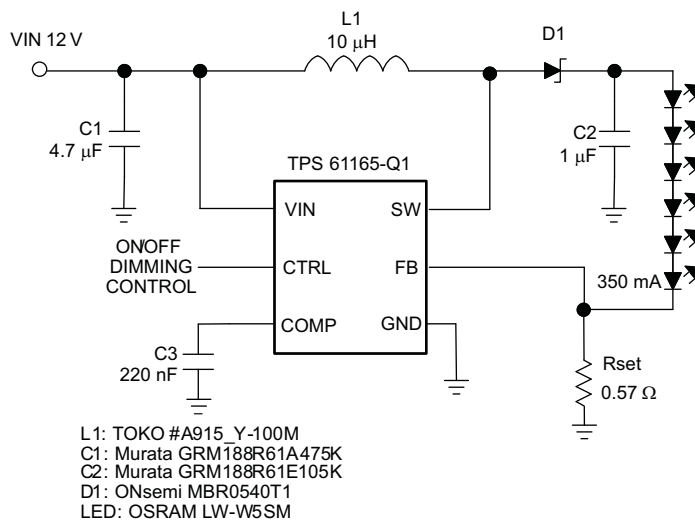
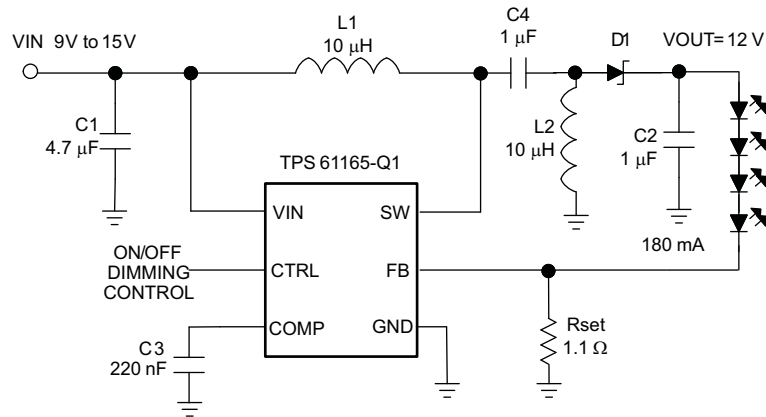


Figure 18. Drive 6 High Brightness LEDs



- L1, L2: TOKO #A915 Y-100M
- C1: Murata GRM188 R61A475K
- C2: Murata GRM188 R61E105K
- C4: Murata GRM188 R61H105K
- D1: ONsemi MBR0540T1
- \*L1, L2 can be replaced by 1:1 transformer

**Figure 19. Drive 4 High Brightness LED With SEPIC Topology**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS61165TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS61165-Q1 :**

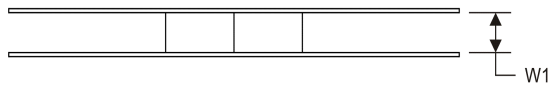
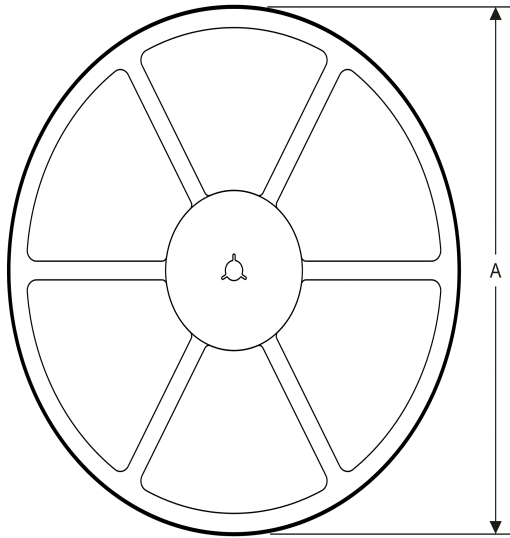
- Catalog: [TPS61165](#)

NOTE: Qualified Version Definitions:

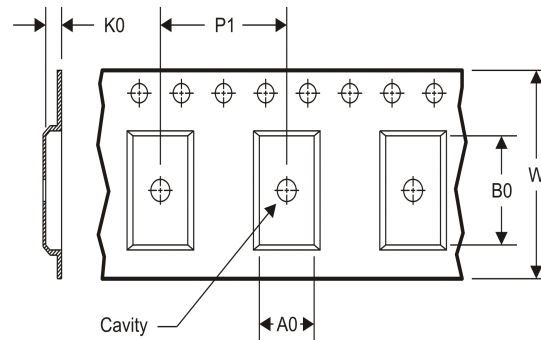
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61165TDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

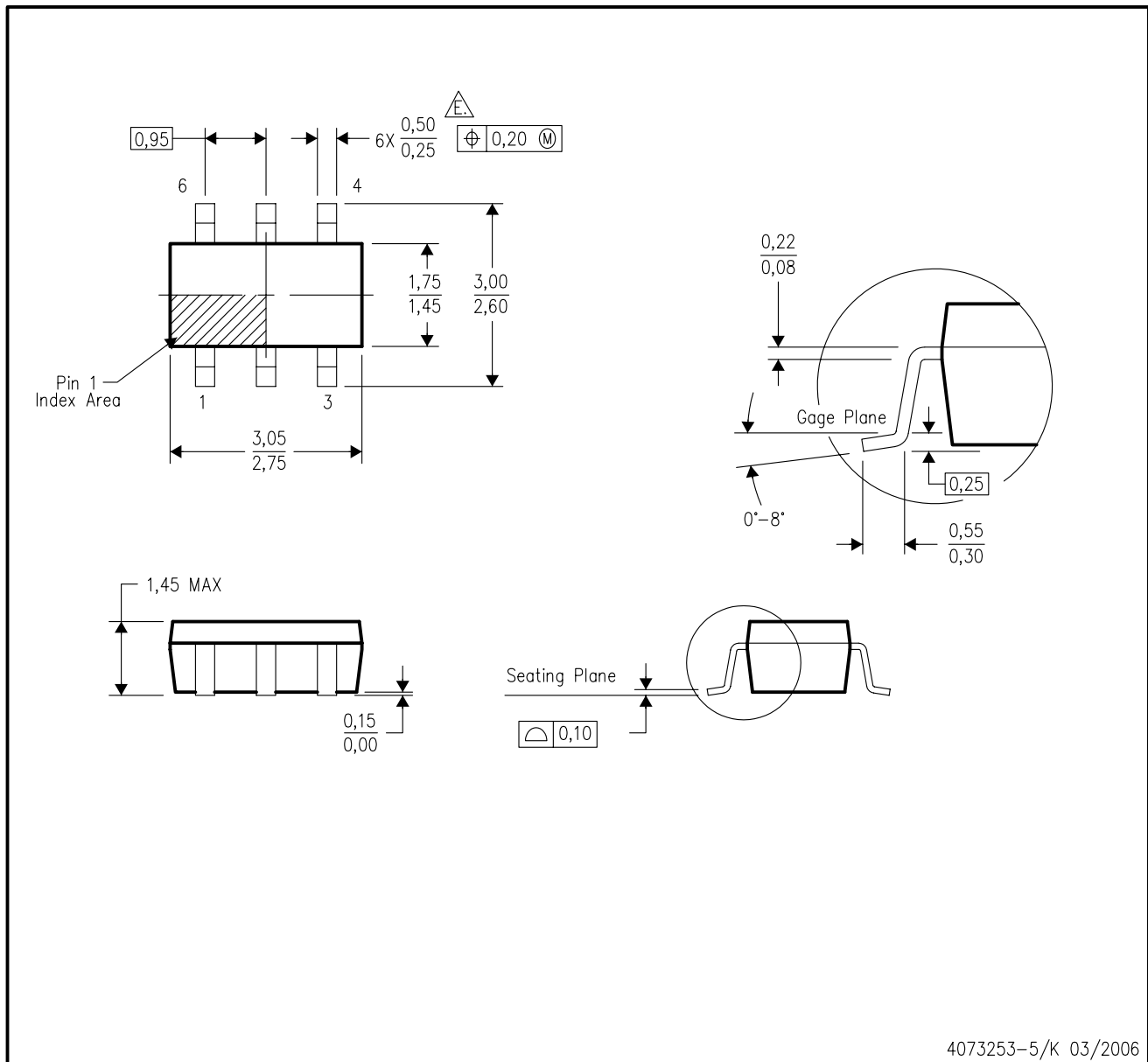


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61165TDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2012, Texas Instruments Incorporated