LOW INPUT BOOST CONVERTER WITH INTEGRATED POWER DIODE AND INPUT/OUTPUT ISOLATION

FEATURES

- **Input Range: 1.6-V to 6-V**
- **Integrated Power Diode and Isolation FET**
- **20-V Internal Switch FET With 1.1-A Current**
- **Fixed 1.2-MHz Switching Frequency**
- **Efficiency at 15-V Output up to 88%**
- **Over Load and Over Voltage Protection**
- **Programmable Soft Start-up**
- **Load Discharge Path After IC Shutdown**
- **2.5 × 2.5 × 0.8 mm SON Package**

APPLICATIONS

- **Glucose Meter**
- **OLED Power Supply**
- **3.3-V to 12-V, 5-V to 12-V Boost Converter**

DESCRIPTION

The TPS61093 is a 1.2-MHz, fixed-frequency boost converter designed for high integration and high reliability. The IC integrates a 20-V power switch, input/output isolation switch, and power diode. When the output current exceeds the over load limit, the IC's isolation switch opens up to disconnect the output from the input. This protects the IC and the input supply. The isolation switch also disconnects the output from the input during shutdown to minimize leakage current. When the IC is shutdown, the output capacitor is discharged to a low voltage level by internal diodes. Other protection features include 1.1-A peak over-current protection (OCP) at each cycle, output over voltage protection (OVP), thermal shutdown, and under voltage lockout (UVLO).

With its 1.6-V minimum input voltage, the IC can be powered by two alkaline batteries, a single Li-ion battery, or 3.3-V and 5-V regulated supply. The output can be boosted up to 17-V. The TPS61093 is available in 2.5 mm × 2.5 mm SON package with thermal pad.

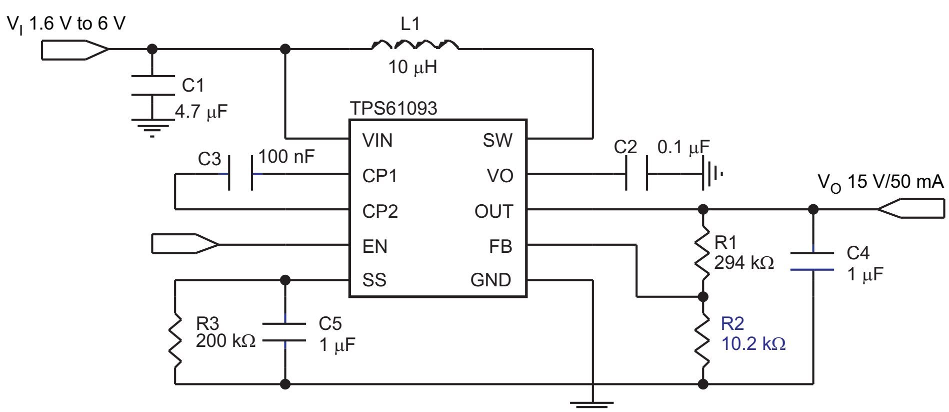


Figure 1. Typical Application

ORDERING INFORMATION(1)

T_A	PART NUMBER(2)	PACKAGE MARKING
–40°C to 85°C	TPS61093DSK	OAP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

(2) The DSK package is available in tape and reel. Add R suffix (TPS61093DSKR) to order quantities of 3000 parts per reel, or add T suffix (TPS61093DSKT) to order 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE / UNITS
Supply voltage on pin VIN (2)	–0.3 V to 7 V
Voltage on pins CP2, EN, and SS (2)	–0.3 V to 7 V
Voltage on pin CP1 and FB (2)	–0.3 V to 3 V
Voltage on pin SW, VO, and OUT (2)	–0.3 V to 20 V
HBM ESD Rating (3)	2 kV
Operating temperature range, T_A	–40°C to 85°C
Maximum operating junction temperature, T_J	150°C
Storage temperature, T_{st}	–55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The Human body model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE θ_{JA} (1)	THERMAL RESISTANCE θ_{JP}	THERMAL RESISTANCE θ_{JC}	POWER RATING $T_A \le 25°C$ (1)	DERATING FACTOR ABOVE $T_A = 25°C$ (1)
DSK	60.6°C/W	6.3°C/W	40°C/W	1650 mW	17 mW/°C

(1) Thermal ratings are determined assuming a high K PCB design according to JEDEC standard JESD51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_i	Input voltage range	1.6		6	V
V_o	Output voltage range at VO pin			17	V
L	Inductor (1)	2.2	4.7	10	µH
C_{in}	Input capacitor	4.7			µF
C_o	Output capacitor at OUT pin (1)	1		10	µF
C_{fly}	Flying capacitor at CP1 and CP2 pins	10			nF
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

ELECTRICAL CHARACTERISTICS

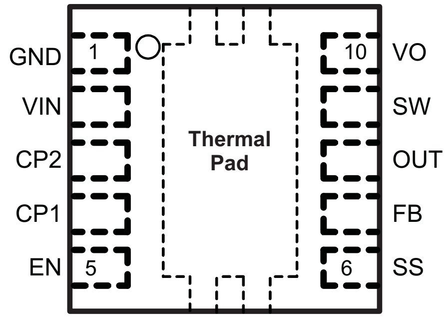
VIN = 3.6 V, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range, VIN		1.6		6	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load		0.9	1.5	mA
I_{SD}	Shutdown current	EN = GND, VIN = 6 V			1	µA
UVLO	Undervoltage lockout threshold	VIN falling		1.5	1.55	V
V_{hys}	Undervoltage lockout hysterisis			50		mV
ENABLE AND PWM CONTROL						
V_{ENH}	EN logic high voltage	VIN = 1.6 V to 6 V	1.2			V
V_{ENL}	EN logic low voltage	VIN = 1.6 V to 6 V			0.3	V
R_{EN}	EN pull down resistor		400	800	1600	kΩ
T_{off}	EN pulse width to shutdown	EN high to low			1	ms
VOLTAGE CONTROL						
V_{REF}	Voltage feedback regulation voltage		0.49	0.5	0.51	V
I_{FB}	Voltage feedback input bias current				100	nA
f_S	Oscillator frequency		1.0	1.2	1.4	MHz
D_{max}	Maximum duty cycle	V_{FB} = 0.1 V, T_A = 85°C	90%	93%		
T_{min_on}	Minimum on pulse width			65		ns
POWER SWITCH, ISOLATION FET						
$R_{DS(ON)N}$	N-channel MOSFET on-resistance	VIN = 3 V		0.25	0.4	Ω
$R_{DS(ON)iso}$	Isolation FET on-resistance	VO = 5 V		2.5	4	Ω
		VO = 3.5 V		4.5		
I_{LN_N}	N-channel leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
I_{LN_iso}	Isolation FET leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
V_F	Power diode forward voltage	Current = 500 mA		0.8		V
OC, ILIM, OVP SC AND SS						
I_{LIM}	N-Channel MOSFET current limit		0.9	1.1	1.5	A
V_{ovp}	Over voltage protection threshold	Measured on the VO pin	18	19		V
V_{ovp_hys}	Over voltage protection hysteresis			0.6		V
I_{OL}	Over load protection		200	300		mA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
$T_{hysteresis}$	Thermal shutdown hysteresis			15		°C

DEVICE INFORMATION

PIN ASSIGNMENTS

TOP VIEW

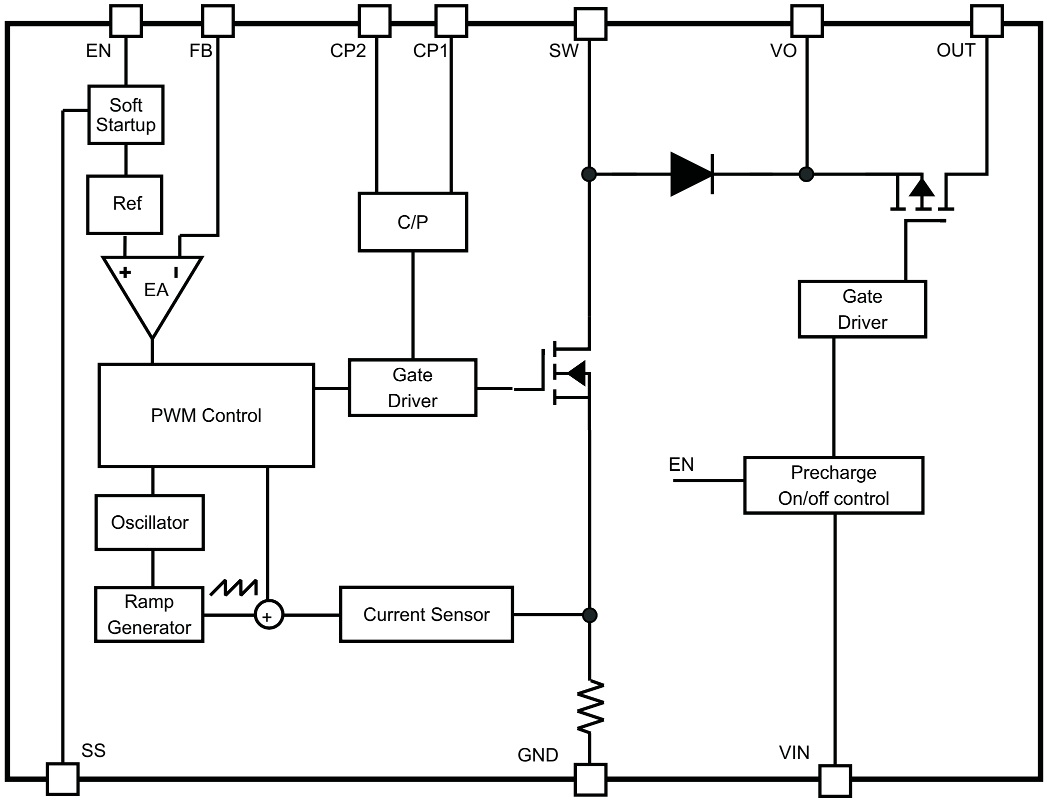


10-PIN 2.5mm x 2.5mm QFN

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	2	I	IC Supply voltage input.
VO	10	O	Output of the boost converter. When the output voltage exceeds the over voltage protection (OVP) threshold, the power switch turns off until VO drops below the over voltage protection hysteresis.
OUT	8	O	Isolation switch is between this pin and VO pin. Connect load to this pin for input/output isolation during IC shutdown. See *WITHOUT ISOLATION FET* for the tradeoff between isolation and efficiency.
GND	1	–	Ground of the IC.
CP1, CP2	3, 4		Connect to flying capacitor for internal charge pump.
EN	5	I	Enable pin (HIGH = enable). When the pin is pulled low for 1 ms, the IC turns off and consumes less than 1-µA current.
SS	6	I	Soft start pin. A RC network connecting to the SS pin programs soft start timing. See *START UP.*
FB	7	I	Voltage feedback pin for output regulation, 0.5-V regulated voltage. An external resistor divider connected to this pin programs the regulated output voltage.
SW	9	I	Switching node of the IC where the internal PWM switch operates.
Thermal Pad	–	–	It should be soldered to the ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

Figure 1, L = TOKO #A915_Y-100M, unless otherwise noted			FIGURE
η	Efficiency	vs Load current at OUT = 15 V	2
η	Efficiency	vs Load current at OUT = 10 V	3
V_{FB}	FB voltage	vs Free-air temperature	4
V_{FB}	FB voltage	vs Input voltage	5
I_{LIM}	Switch current limit	vs Free-air temperature	6
	Line transient response	VIN = 3.3 V to 3.6 V; Load = 50 mA	7
	Load transient response	VIN = 2.5 V; Load = 10 mA to 50 mA; Cff = 100 pF	8
	PWM control in CCM	VIN = 3.6 V; Load = 50 mA	9
	PWM control in DCM	VIN = 3.6 V; Load = 1 mA	10
	Pulse skip mode	VIN = 4.5 V; OUT = 10 V; No load	11
	Soft start-up	VIN = 3.6 V; Load = 50 mA	12

EFFICIENCY
vs
LOAD

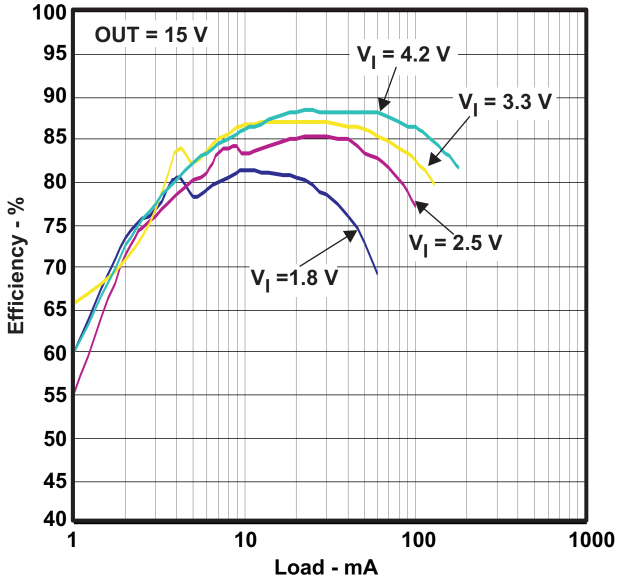


Figure 2.

EFFICIENCY
vs
LOAD

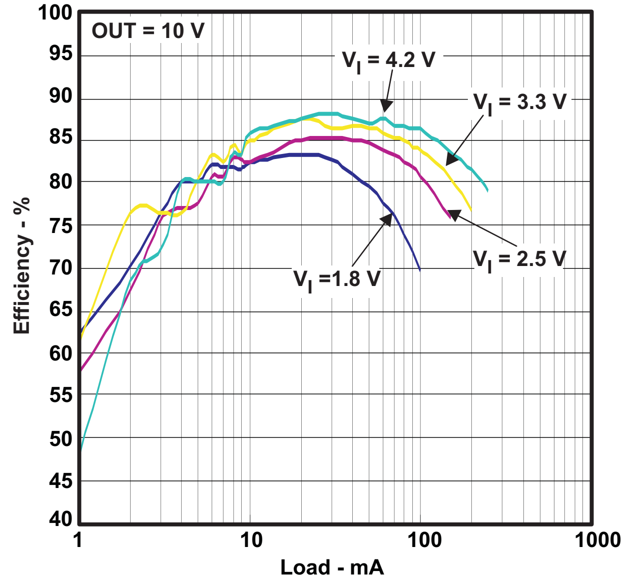


Figure 3.

FB VOLTAGE
vs
FREE-AIR TEMPERATURE

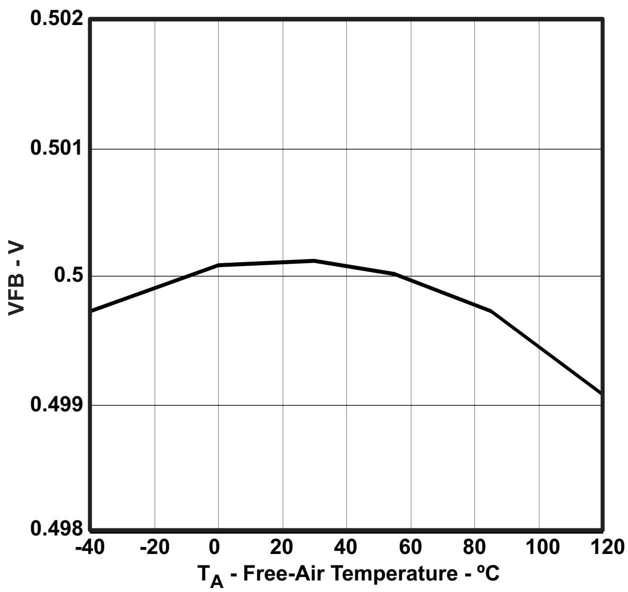


Figure 4.

FB VOLTAGE
vs
INPUT VOLTAGE

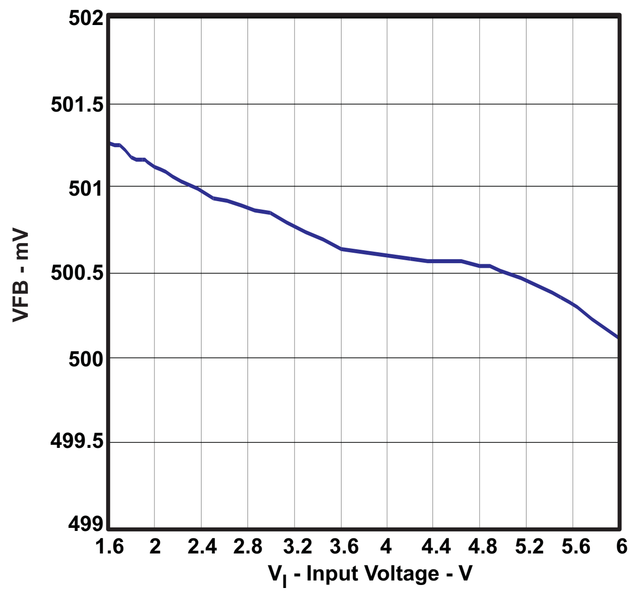


Figure 5.

SWITCH CURRENT LIMIT
vs
FREE-AIR TEMPERATURE

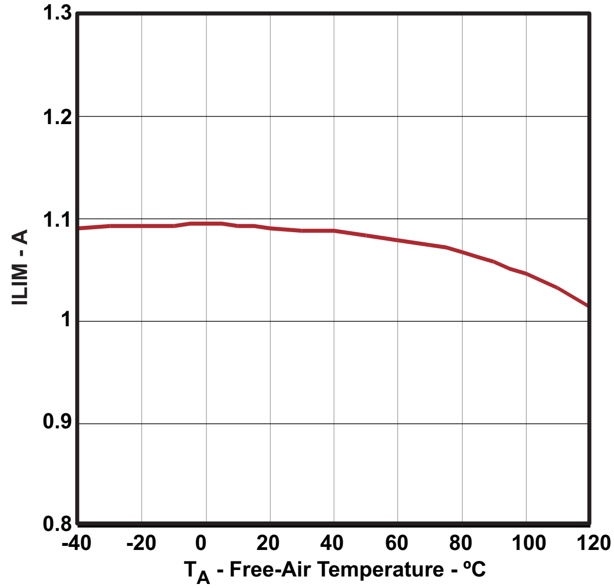


Figure 6.

3.3V to 3.6V LINE TRANSIENT RESPONSE

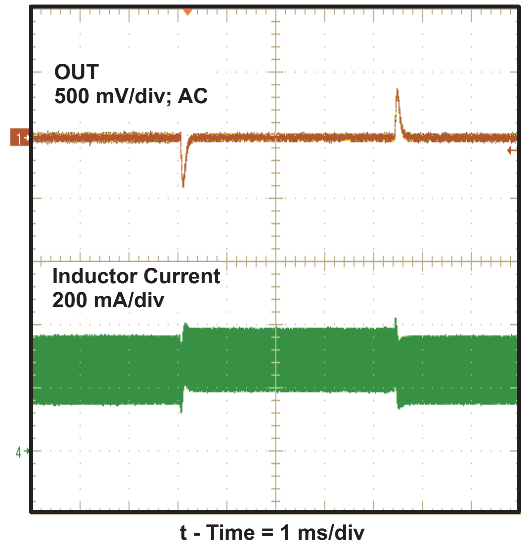


Figure 7.

10mA to 50mA LOAD TRANSIENT RESPONSE

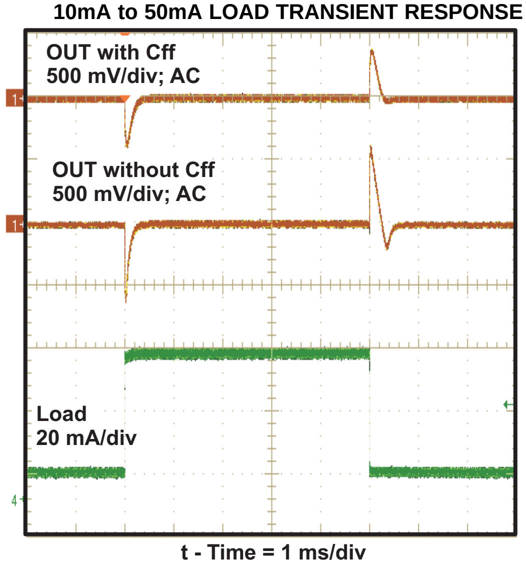


Figure 8.

PWM CONTROL IN CCM

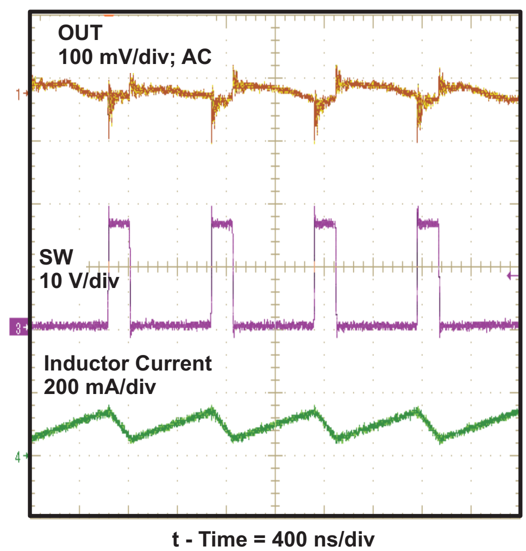


Figure 9.

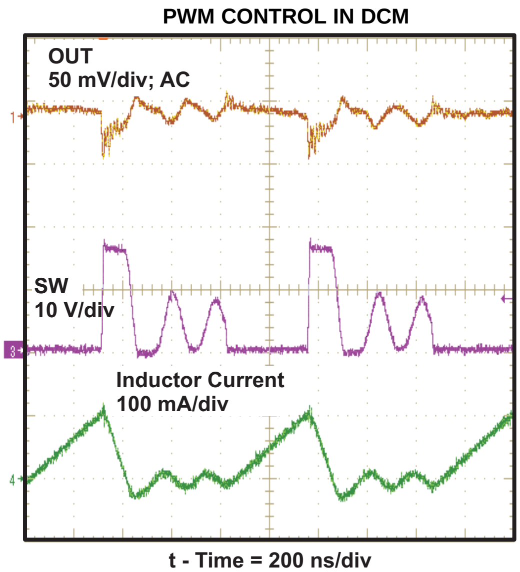


Figure 10.

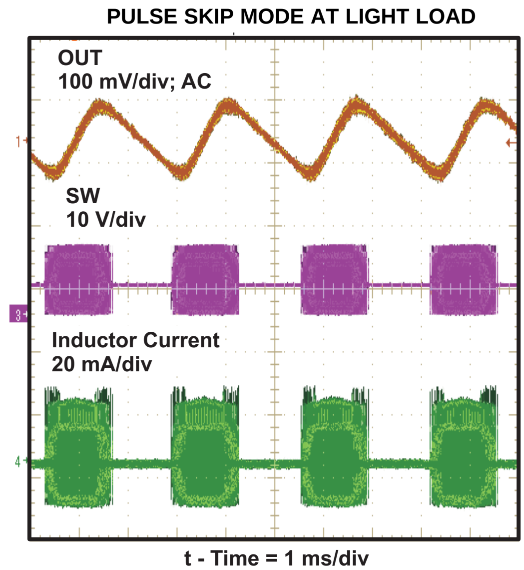


Figure 11.

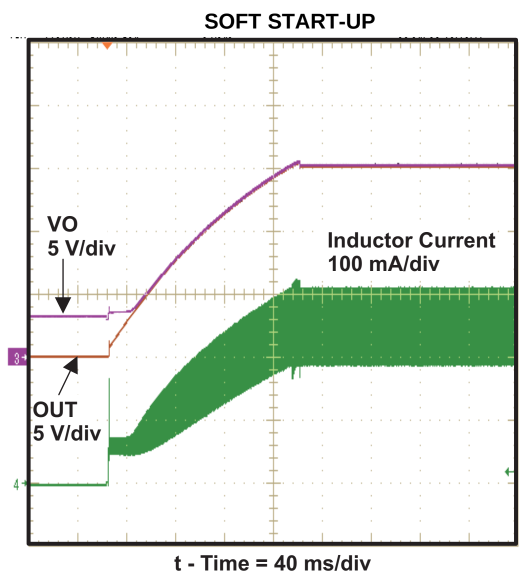


Figure 12.

DETAILED DESCRIPTION

OPERATION

The TPS61093 is a highly integrated boost regulator for up to 17-V output. In addition to the on-chip 1-A PWM switch and power diode, this IC also integrates an output-side isolation switch as shown in the functional block diagram. One common issue with conventional boost regulators is the conduction path from input to output even when the PWM switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown, and excessive over load current. In the TPS61093, the isolation switch turns off under shutdown-mode and over load conditions, thereby opening the current path. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency.

The TPS61093 adopts current-mode control with constant pulse-width-modulation (PWM) frequency. The switching frequency is fixed at 1.2-MHz typical. PWM operation turns on the PWM switch at the beginning of each switching cycle. The input voltage is applied across the inductor and the inductor current ramps up. In this mode, the output capacitor is discharged by the load current. When the inductor current hits the threshold set by the error amplifier output, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor. This operation repeats in the next switching cycle. The error amplifier compares the FB-pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching. This closed-loop system requires frequency compensation for stable operation. The device has a built-in compensation circuit that can accommodate a wide range of input and output voltages. To avoid the sub-harmonic oscillation intrinsic to current-mode control, the IC also integrates slope compensation, which adds an artificial slope to the current ramp.

SHUTDOWN AND LOAD DISCHARGE

When the EN pin is pulled low for 1-ms, the IC stops the PWM switch and turns off the isolation switch, providing isolation between input and output. The internal current path consisting of the isolation switch's body diode and several parasitic diodes quickly discharges the output voltage to less than 3.3-V. Afterwards, the voltage is slowly discharged to zero by the leakage current. This protects the IC and the external components from high voltage in shutdown mode.

In shutdown mode, less than 1-µA of input current is consumed by the IC.

OVER LOAD AND OVER VOLTAGE PROTECTION

If the over load current passing through the isolation switch is above the over load limit (I_{OL}) for 3-µs (typ), the TPS61093 is switched off until the fault is cleared and the EN pin toggles. The function only is triggered 52-ms after the IC is enabled.

To prevent the PWM switch and the output capacitor from exceeding maximum voltage ratings, an over voltage protection circuit turns off the boost switch as soon as the output voltage at the VO pin exceeds the OVP threshold. Simultaneously, the IC opens the isolation switch. The regulator resumes PWM switching after the VO pin voltage falls 0.6-V below the threshold.

UNDER VOLTAGE LOCKOUT (UVLO)

An under voltage lockout prevents improper operation of the device for input voltages below 1.55-V. When the input voltage is below the under voltage threshold, the entire device, including the PWM and isolation switches, remains off.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 150°C is exceeded. The thermal shutdown has a hysteresis of 15°C, typical.

APPLICATION INFORMATION

SWITCH DUTY CYCLE

The maximum switch duty cycle (D) of the TPS61093 is 90% (minimum). The duty cycle of a boost converter under continuous conduction mode (CCM) is given by:

$$D = \frac{Vout + 0.8\ V - Vin}{Vout + 0.8\ V} \quad (1)$$

The duty cycle must be lower than the specification in the application; otherwise the output voltage cannot be regulated.

The TPS61093 has a minimum ON pulse width once the PWM switch is turned on. As the output current drops, the device enters discontinuous conduction mode (DCM). If the output current drops extremely low, causing the ON time to be reduced to the minimum ON time, the TPS61093 enters pulse-skipping mode. In this mode, the device keeps the power switch off for several switching cycles to keep the output voltage in regulation. See Figure 11. The output current when the IC enters skipping mode is calculated with Equation 2.

$$I_{out\_skip} = \frac{Vin^2 \times T_{min\_on}^2 \times f_{SW}}{2 \times (Vout + 0.8V - Vin) \times L} \quad (2)$$

Where

T_{min_on} = Minimum ON pulse width specification (typically 65-ns);
L = Selected inductor value;
f_{SW} = Converter switching frequency (typically 1.2-MHz)

OUTPUT PROGRAM

To program the output voltage, select the values of R1 and R2 (see Figure 13) according to Equation 3.

$$Vout = 1.229\ V \times \left(\frac{R1}{R2} + 1\right)$$

$$R1 = R2 \times \left(\frac{Vout}{1.229V} - 1\right) \quad (3)$$

A recommended value for R2 is approximately 10-kΩ which sets the current in the resistor divider chain to 1.229V/10kΩ = 123-µA. The output voltage tolerance depends on the VFB accuracy and the resistor divider.

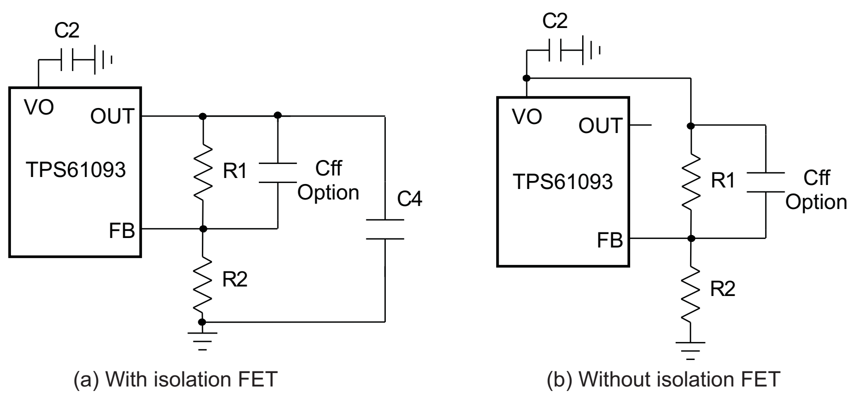


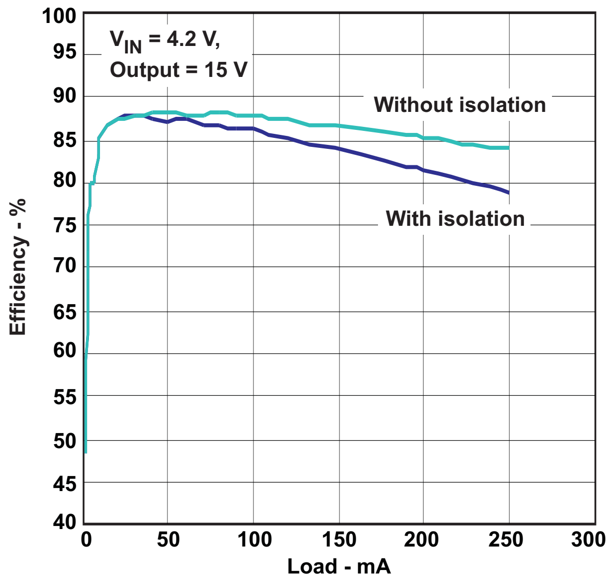
Figure 13. Resistor Divider to Program Output Voltage

WITHOUT ISOLATION FET

The efficiency of the TPS61093 can be improved by connecting the load to the VO pin instead of the OUT pin. The power loss in the isolation FET is then negligible, as shown in Figure 13. The tradeoffs when bypassing the isolation FET are:

- Leakage path between input and output causes the output to be a diode drop below the input voltage when the IC is in shutdown
- No overload circuit protection

When the load is connected to the VO pin, the output capacitor on the VO pin should be above 1-µF.



START UP

The TPS61093 turns on the isolation FET and PWM switch when the EN pin is pulled high. During the soft start period, the R and C network on the SS pin is charged by an internal bias current of 5-µA (typ). The RC network sets the reference voltage ramp up slope. Since the output voltage follows the reference voltage via the FB pin, the output voltage rise time follows the SS pin voltage until the SS pin voltage reaches 0.5-V. The soft start time is given by Equation 4.

$$t_{SS} = \frac{0.5\ V \times C5}{5\ \mu A} \qquad (4)$$

Where C5 is the capacitor connected to the SS pin.

When the EN pin is pulled low to switch the IC off, the SS pin voltage is discharged to zero by the resistor R3. The discharge period depends on the RC time constant. Note that if the SS pin voltage is not discharged to zero before the IC is enabled again, the soft start circuit may not slow the output voltage startup and may not reduce the startup inrush current.

INDUCTOR SELECTION

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance. Considering inductor value alone is not enough.

The saturation current of the inductor should be higher than the peak switch current as calculated in Equation 5.

$$I_{L\_peak} = I_{L\_DC} + \frac{\Delta I_L}{2}$$

$$I_{L\_DC} = \frac{Vout \times Iout}{Vin \times \eta}$$

$$\Delta I_L = \frac{1}{\left[L \times f_{SW} \times \left(\frac{1}{Vout + 0.8\,V - VIN} + \frac{1}{VIN}\right)\right]} \quad (5)$$

Where

I_{L_peak} = Peak switch current
I_{L_DC} = Inductor average current
ΔI_L = Inductor peak to peak current
η = Estimated converter efficiency

Normally, it is advisable to work with an inductor peak-to-peak current of less than 30% of the average inductor current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. Also, the inductor value should not be outside the 2.2-µH to 10-µH range in the recommended operating conditions table. Otherwise, the internal slope compensation and loop compensation components are unable to maintain small signal control loop stability over the entire load range. Table 1 lists the recommended inductor for the TPS61093.

Table 1. Recommended Inductors for the TPS61093

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L×W×H mm)	VENDOR
#A915_Y-4R7M	4.7	45	1.5	5.2x5.2x3.0	Toko
#A915_Y-100M	10	90	1.09	5.2x5.2x3.0	Toko
VLS4012-4R7M	4.7	132	1.1	4.0x4.0x1.2	TDK
VLS4012-100M	10	240	0.82	4.0x4.0x1.2	TDK
CDRH3D23/HP	10	198	1.02	4.0x4.0x2.5	Sumida
LPS5030-103ML	10	127	1.4	5.0x5.0x3.0	Coilcraft

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{out} = \frac{D \times I_{out}}{Fs \times V_{ripple}} \quad (6)$$

Where V_{ripple} = peak to peak output ripple. The ESR impact on the output ripple must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. A ceramic capacitor can lose as much as 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

A 4.7-µF (minimum) input capacitor is recommended. The output requires a capacitor in the range of 1 µF to 10 µF. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

- TDK (http://www.component.tdk.com/components.php)
- Murata (http://www.murata.com/cap/index.html)

SMALL SIGNAL STABILITY

The TPS61093 integrates slope compensation and the RC compensation network for the internal error amplifier. Most applications will be control loop stable if the recommended inductor and input/output capacitors are used. For those few applications that require components outside the recommended values, the internal error amplifier's gain and phase are presented in Figure 14.

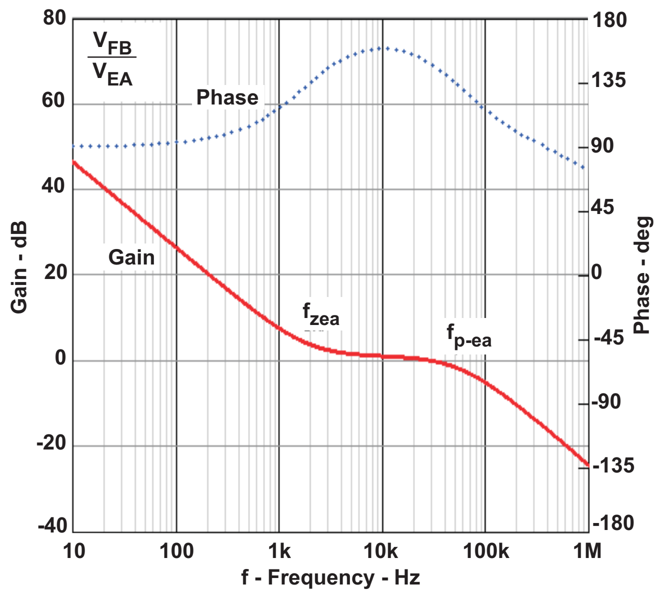


Figure 14. Bode Plot of Error Amplifier Gain and Phase

The RC compensation network generates a pole f_{p-ea} of 57-kHz and a zero f_{z-ea} of 1.9-kHz, shown in Figure 14. Use Equation 7 to calculate the output pole, f_P, of the boost converter. If $f_P << f_{z-ea}$. due to a large capacitor beyond 10 μF, for example, a feed forward capacitor on the resistor divider, as shown in Figure 14, is necessary to generate an additional zero f_{z-f}. to improve the loop phase margin and improve the load transient response. The low frequency pole f_{p-f} and zero f_{z-f} generated by the feed forward capacitor are given by Equation 8 and Equation 9:

$$f_P = \frac{1}{\pi \times R_o \times C_O} \quad \text{(a)} \tag{7}$$

$$f_{p\text{-}f} = \frac{1}{2\pi \times R2 \times C_{ff}} \quad \text{(b)} \tag{8}$$

$$f_{z\text{-}f} = \frac{1}{2\pi \times R1 \times C_{ff}} \quad \text{(c)} \tag{9}$$

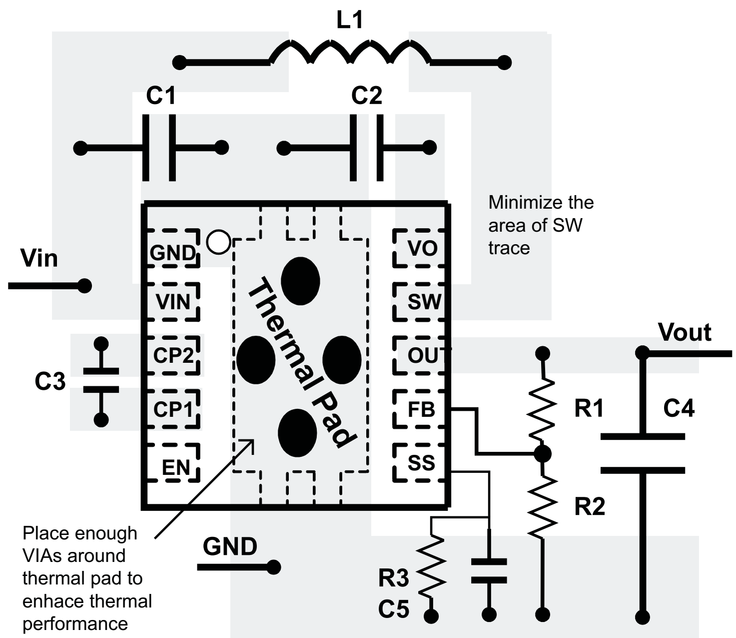
Where C_{ff} = the feed-forward capacitor.

For example, in the typical application circuitry (see Figure 1), the output pole f_P is approximately 1-kHz. When the output capacitor is increased to 100-μF, then the f_P is reduced to 10-Hz. Therefore, a feed-forward capacitor of 10-nF compensates for the low frequency pole.

A feed forward capacitor that sets f_{z-f} near 10-kHz improves the load transient response in most applications, as shown in Figure 8.

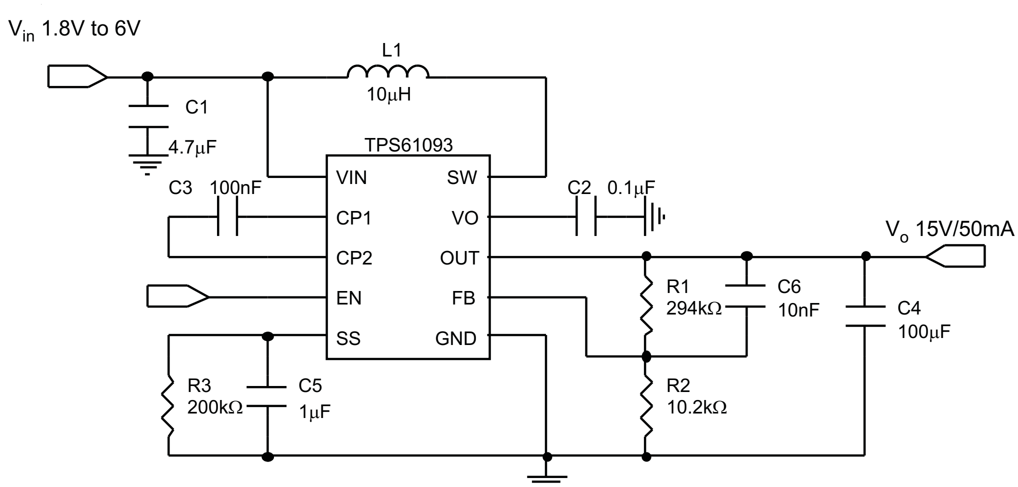
LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high frequency noise (e.g., EMI), proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch and output capacitor contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

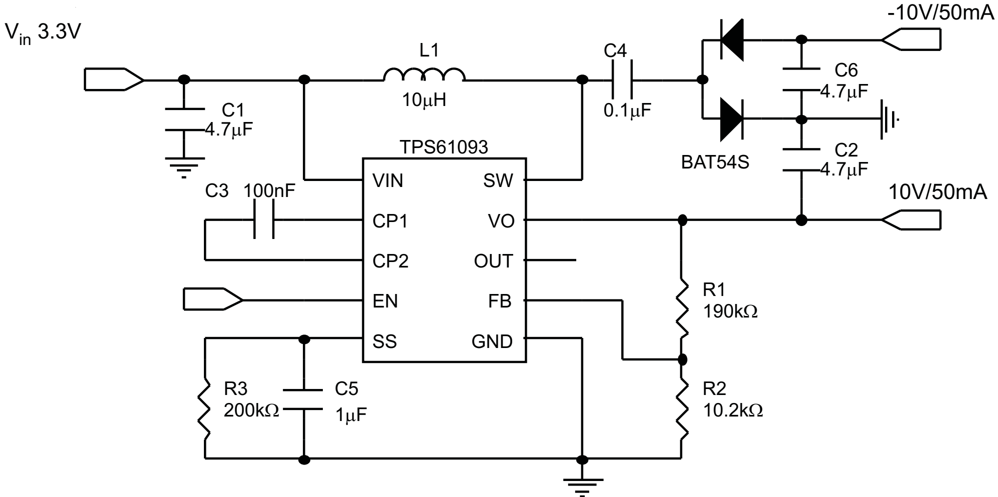


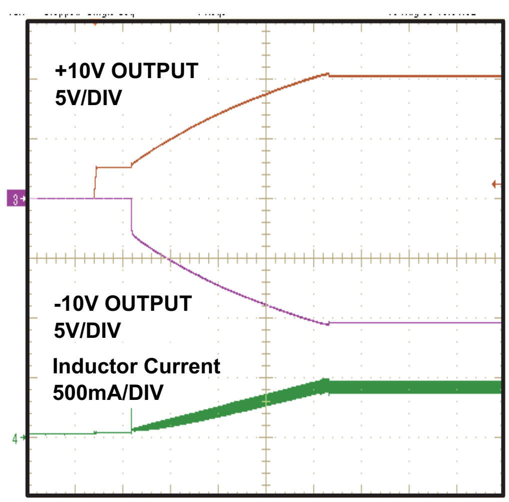
ADDITIONAL APPLICATION

15-V Boost Converter with 100-µF Output Capacitor



10 V, –10 V Dual Output Boost Converter





t - Time = 40 ms/div

Figure 15. Soft Startup Waveform, 10 V, -10 V Dual Output Boost Converter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS61093DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS61093DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

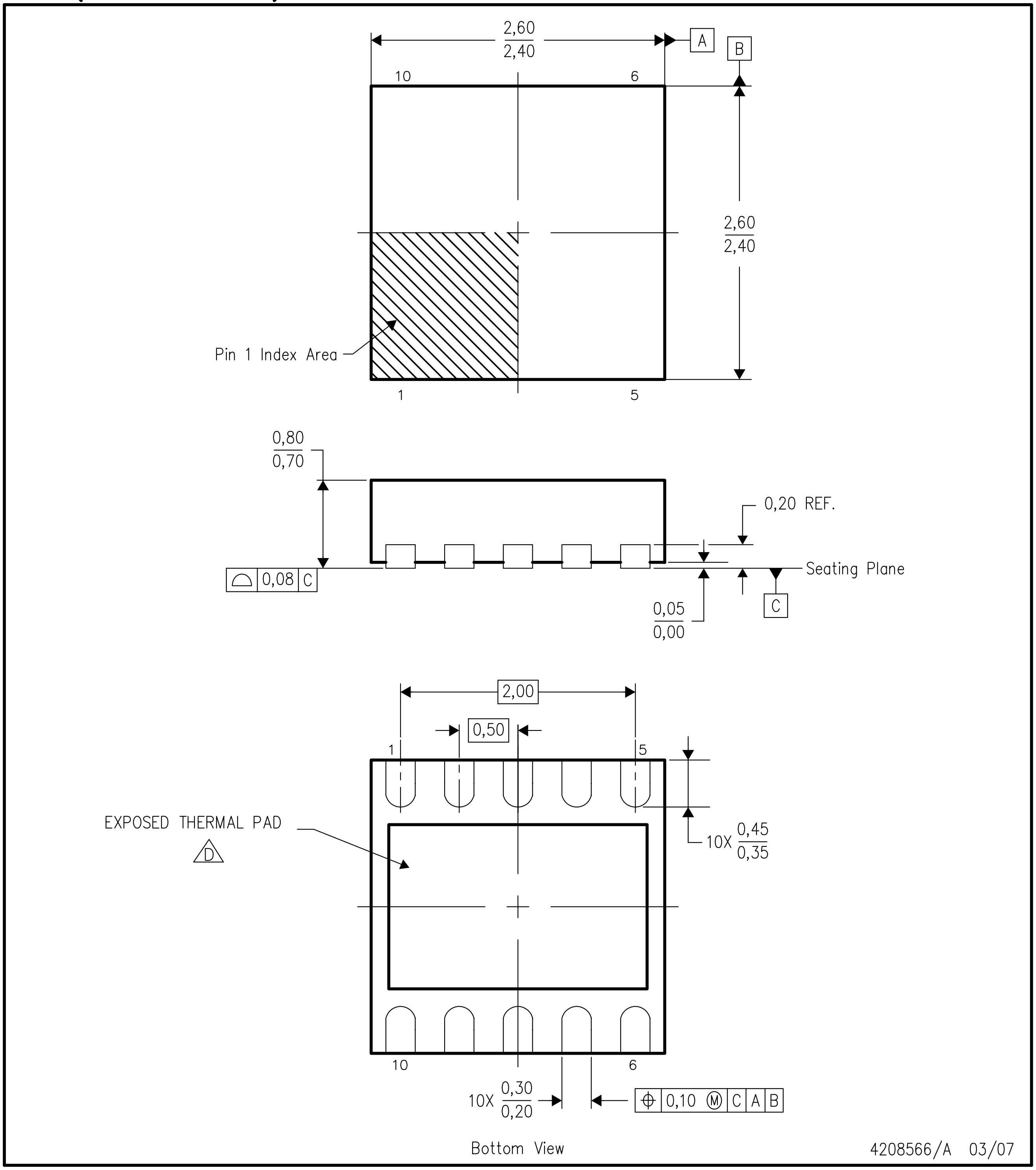
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DSK (S-PDSO-N10) PLASTIC QUAD FLATPACK



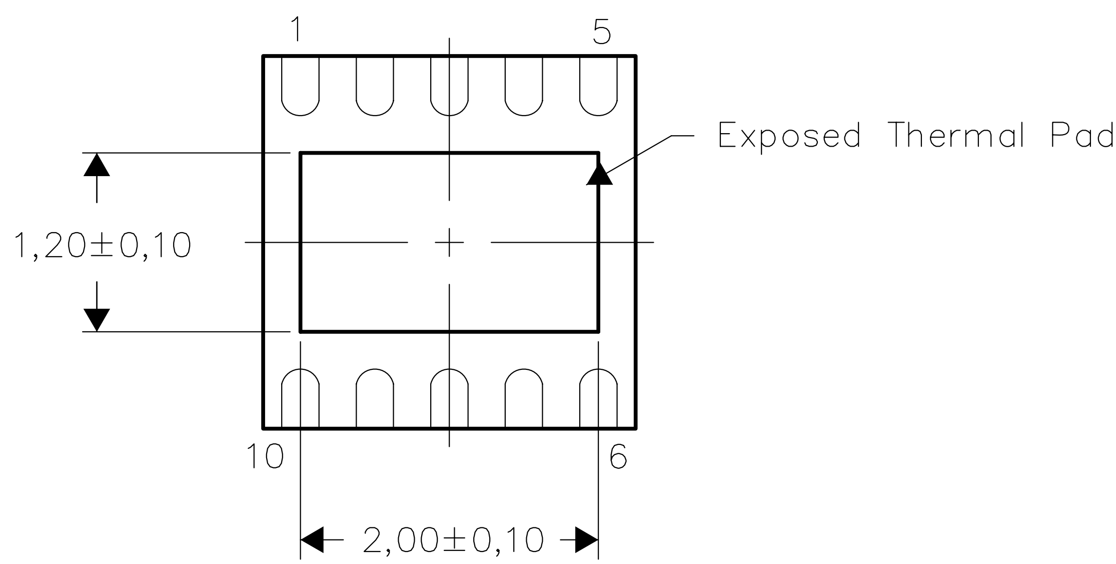
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

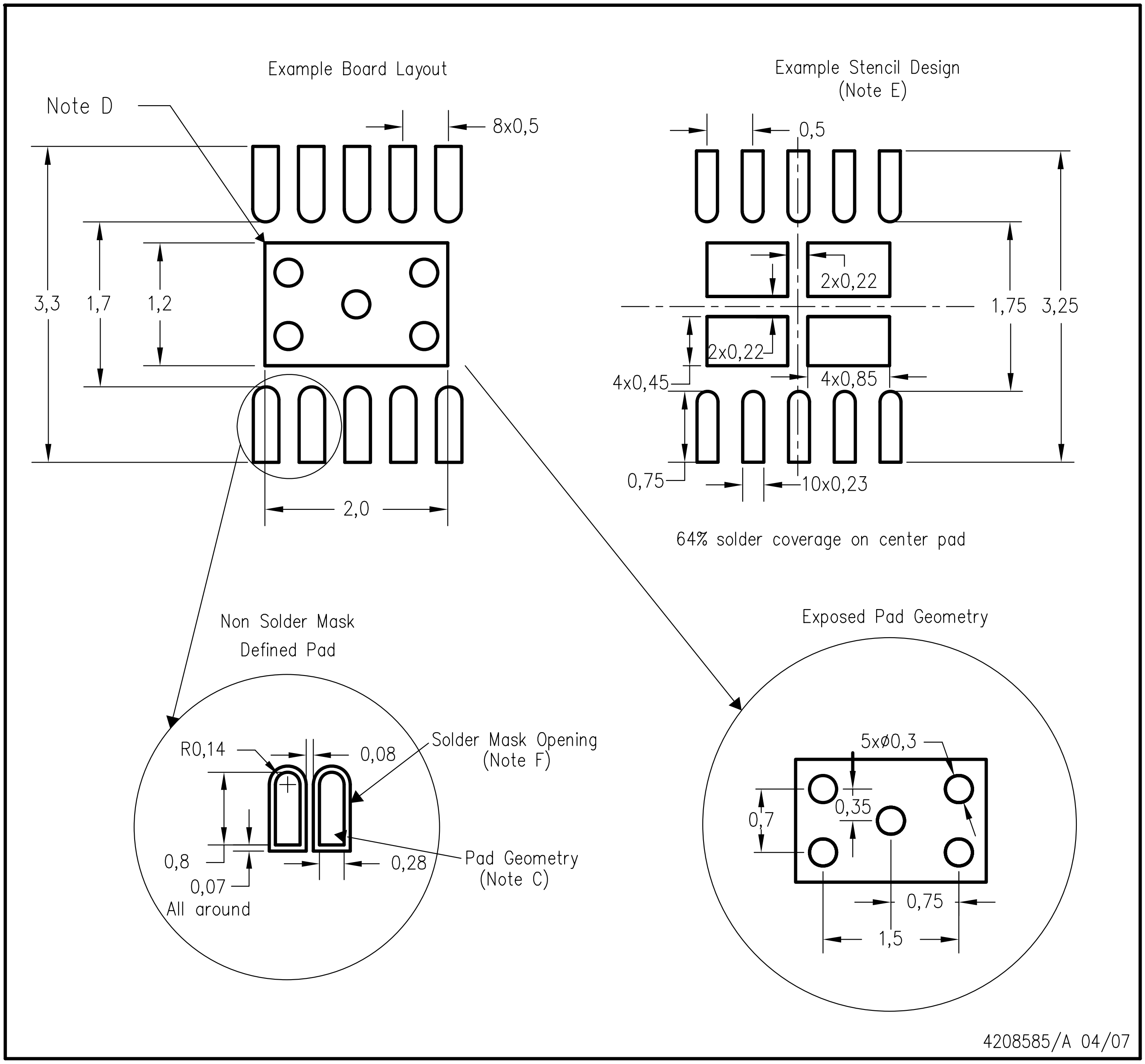


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DSK (S–PDSO–N10)



4208585/A 04/07

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.