

TPS568215 4.5-V to 17-V Input , 8-A Synchronous Step-Down SWIFT™ Converter

1 Features

- Integrated 19-mΩ and 9-mΩ MOSFETs
- Support 8-A Continuous I_{OUT}
- 0.6V +/-1% Reference Voltage across full temperature range
- 0.6 V to 5.5 V Output Voltage Range
- Supports Ceramic Output Capacitors
- D-CAP3™ Control Mode for Fast Transient Response
- Selectable Forced Continuous Conduction Mode (FCCM) for Tight Output Voltage Ripple or Auto-Skipping Eco-mode™ for High Light-Load Efficiency
- Selectable F_{SW} of 400 kHz, 800 kHz and 1.2 MHz
- Monotonic Start Up into Pre-biased Outputs
- Two Adjustable Current Limit Settings with Hiccup Re-start
- Optional External 5V bias for Enhanced Efficiency
- Adjustable Soft Start with a Default 1-ms Soft Start Time
- -40°C to 150°C Operating Junction Temperature
- Small 3.5-mm x 3.5-mm HotRod™ QFN Package
- Supported at the WEBENCH™ Design Center

2 Applications

- Server, Cloud-Computing, Storage
- Telecom & Networking, Point-of-Load (POL)

- IPCs, Factory Automation, Test Measurement
- High-End DTV

3 Description

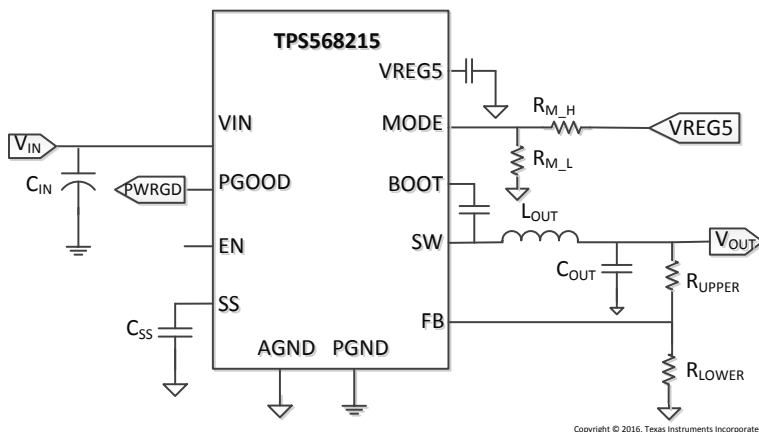
The TPS568215 is TI's smallest monolithic 8-A synchronous buck converter with an adaptive on-time D-CAP3™ control mode. The device integrates low $R_{DS(on)}$ power MOSFETs that enable high efficiency and offers ease-of-use with minimum external component count for space-conscious power systems. Competitive features include a very accurate reference voltage, fast load transient response, auto-skip mode operation for light load efficiency, adjustable current limit and no requirement for external compensation. A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS568215 is available in a thermally enhanced 18-pin HotRod™ QFN package and is designed to operate from -40°C to 150°C junction temperature. TPS568215 is pin to pin compatible with TPS56C215 which gives the user flexibility to pick solutions from 6A to 12A in the same footprint.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS568215	VQFN (18)	3.5 mm x 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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Efficiency vs Output Current

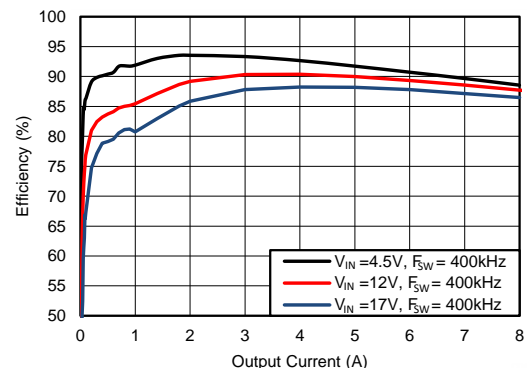


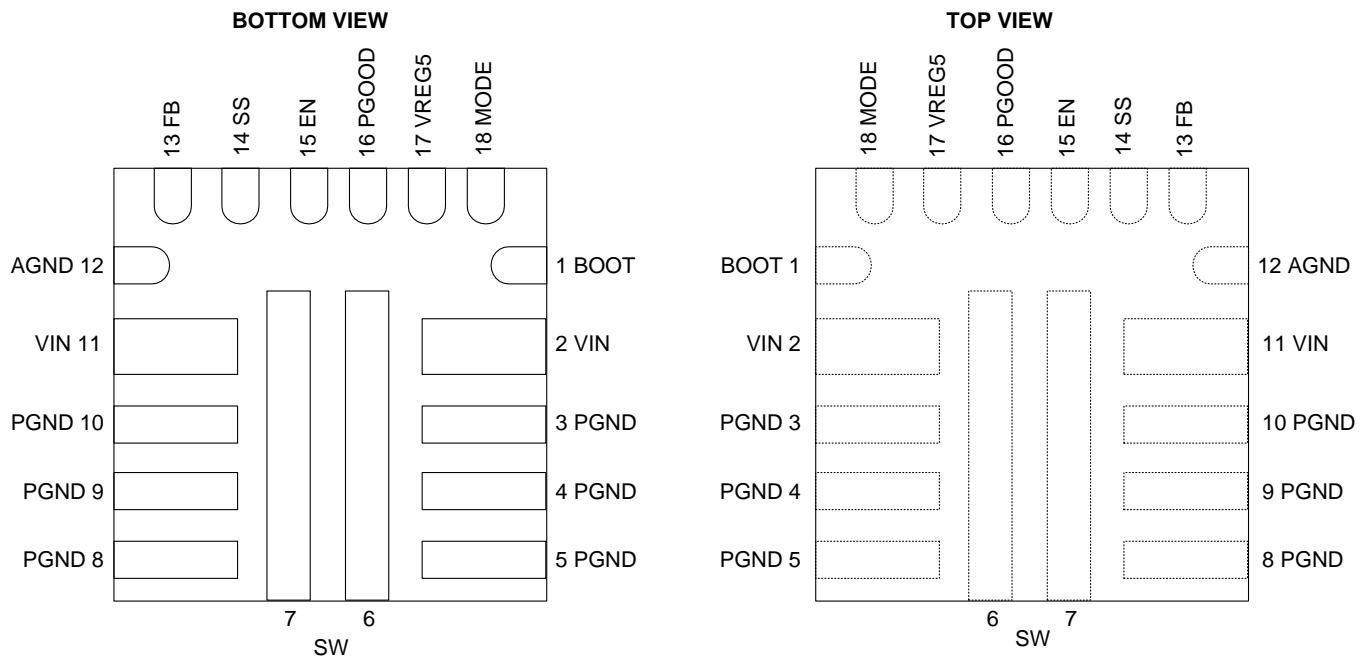
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4 Revision History

DATE	REVISION	NOTES
October 2016	*	Initial release.

5 Pin Configuration and Functions

**RNN Package
18-Pin VQFN**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BOOT	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BOOT and SW.
2,11	VIN	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
3, 4, 5, 8, 9, 10	PGND	G	Power GND terminal for the controller circuit and the internal circuitry. Connect to AGND with a short trace.
6, 7	SW	O	Switch node terminal. Connect the output inductor to this pin.
12	AGND	G	Ground of internal analog circuitry. Connect AGND to PGND plane with a short trace.
13	FB	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and AGND.
14	SS	O	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the converter starts up in 1ms.
15	EN	I	Enable input control, leaving this pin floating enables the converter. It can also be used to adjust the input UVLO by connecting to the center tap of the resistor divider between VIN and EN.
16	PGOOD	O	Open Drain Power Good Indicator, it is asserted low if output voltage is out of PGOOD threshold, Overvoltage or if the device is under thermal shutdown, EN shutdown or during soft start.
17	VREG5	I/O	4.7-V internal LDO output which can also be driven externally with a 5V input. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 4.7- μ F capacitor.
18	MODE	I	Switching Frequency, Current Limit selection and Light load operation mode selection pin. Connect this pin to a resistor divider from VREG5 and AGND for different MODE options shown in table 3.

PRODUCT PREVIEW

6 Device and Documentation Support

6.1 Device Support

6.1.1 Third-Party Products Disclaimer

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6.1.2 Development Support

The evaluation module for system evaluation is shown in .

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

D-CAP3, HotRod, E2E are trademarks of Texas Instruments.

6.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS568215RNNR	PREVIEW	VQFN-HR	RNN	18	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	568215	
TPS568215RNNT	PREVIEW	VQFN-HR	RNN	18	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	568215	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

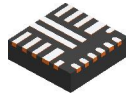
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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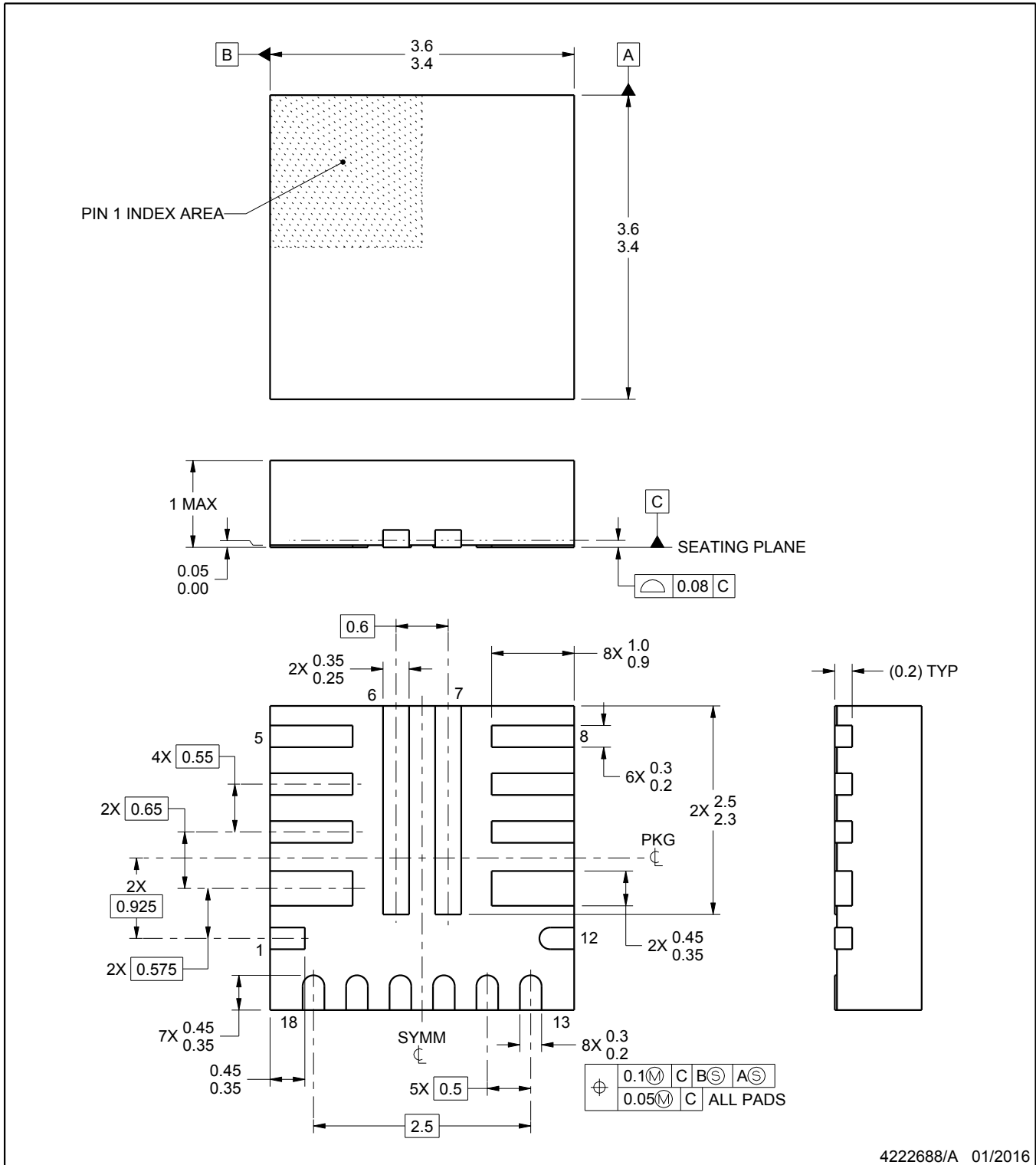
RNN0018A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

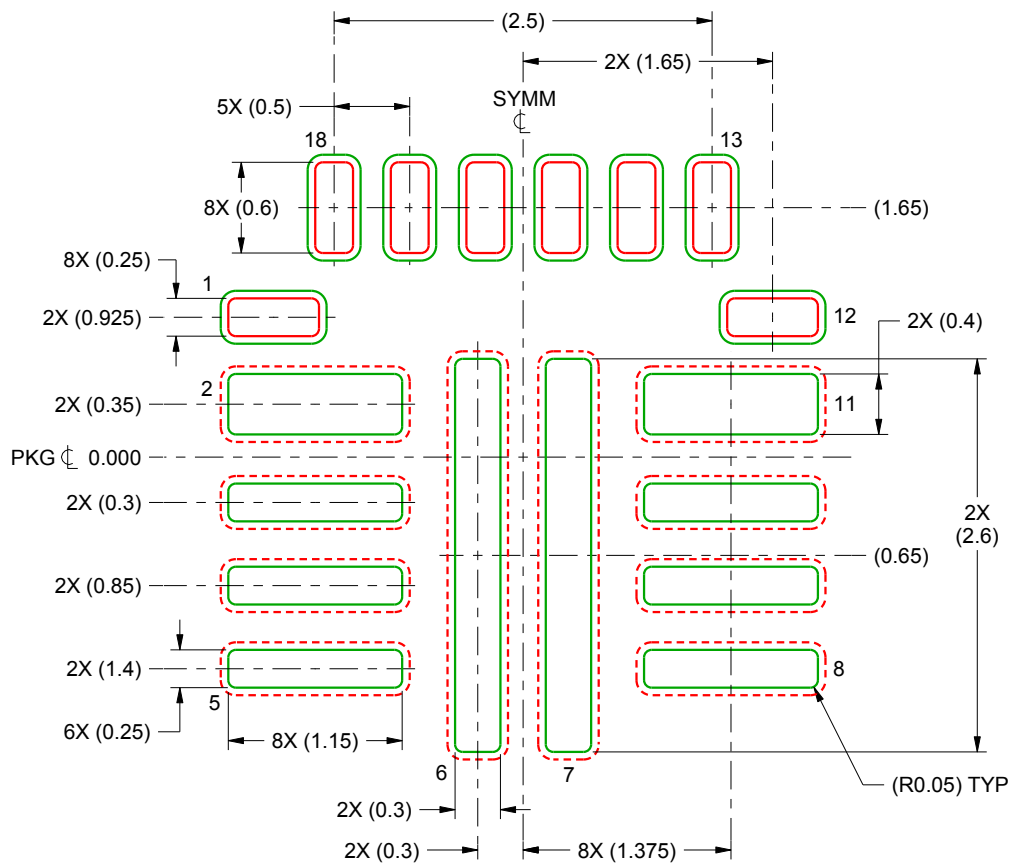
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

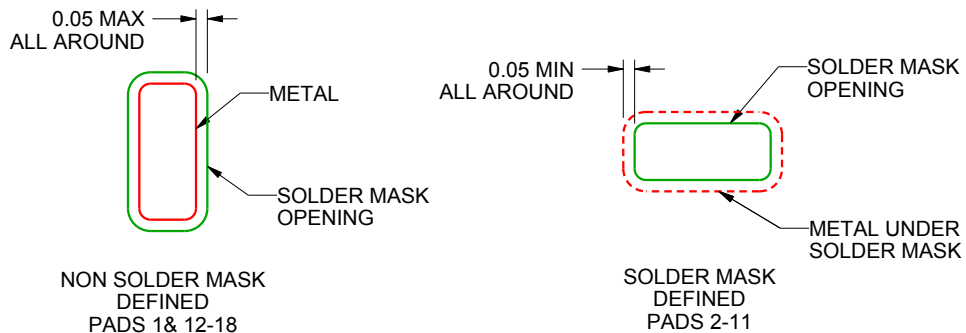
RNN0018A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

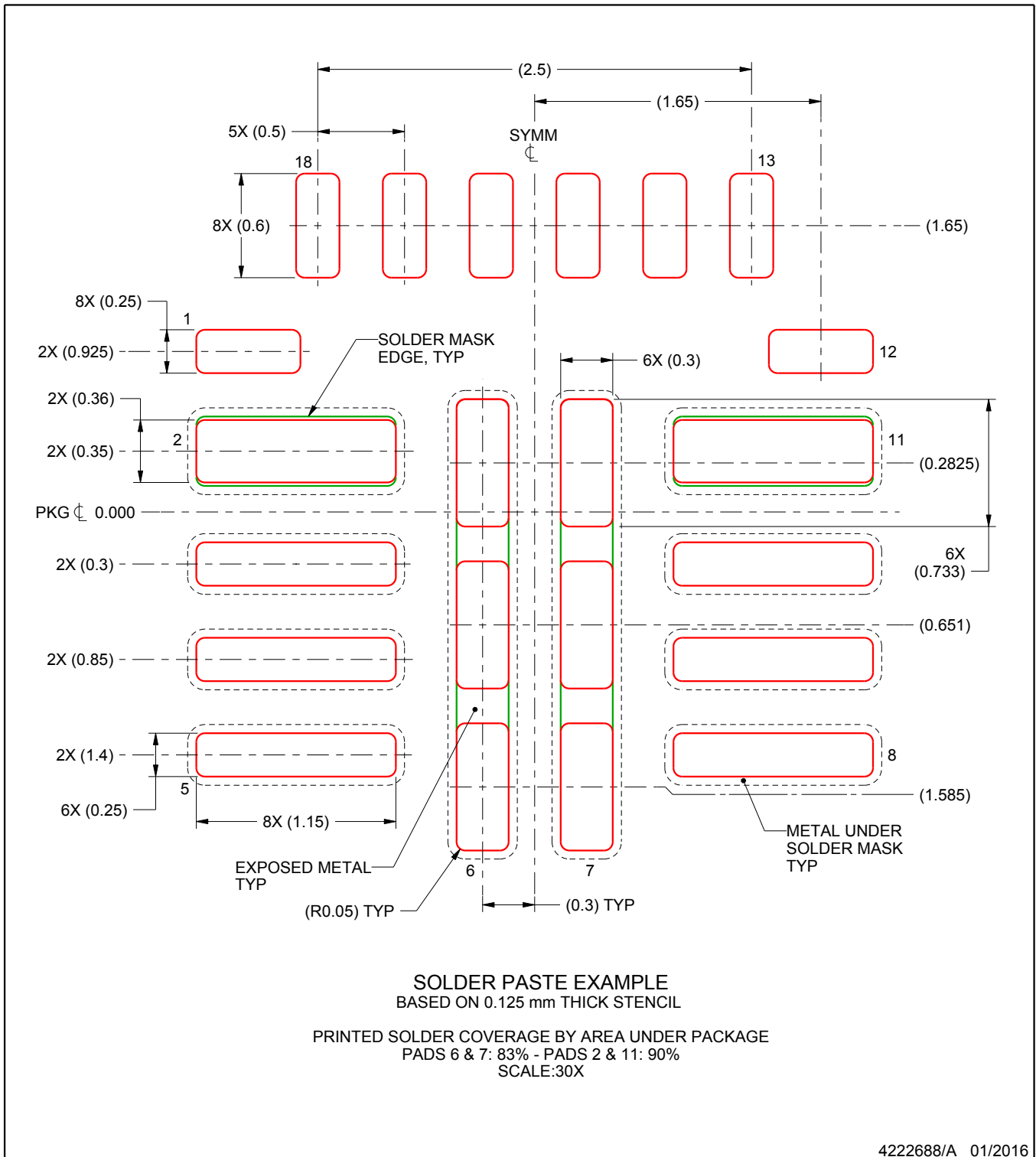
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RNN0018A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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