











TPS548D22

SLUSC70 - MARCH 2016

TPS548D22 1.5-V to 16-V V_{IN}, 4.5-V to 22-V V_{DD}, 40-A SWIFT™ Synchronous Step-Down Converter with Full Differential Sense

Check for Samples: TPS548D22

1 Features

- Conversion Input Voltage Range (PV_{IN}): 1.5 V to 16 V
- Input Bias Voltage (V_{DD}) Range: 4.5 V to 22 V
- Output Voltage Range: 0.6 V to 5.5 V
- Integrated, 2.9-mΩ and 1.2-mΩ Power MOSFETs with 40-A Continuous Output Current
- Voltage Reference 0.6 V to 1.2 V in 50 mV Steps Using VSEL Pin
- ±0.5%, 0.9-V_{REF} Tolerance Range: –40°C to 125°C Junction Temperature
- True Differential Remote Sense Amplifier
- D-CAP3[™] Control Loop to Support Large Bulk Capacitors and/or Small MLCCs Without External Compensation
- Adaptive On-Time Control with 4 Selectable Frequency Settings: 425 kHz, 650 kHz, 875 kHz and 1.05 MHz
- Temperature Compensated and Programmable Current Limit with R_{ILIM} and OC Clamp
- Choice of Hiccup or Latch-Off OVP or UVP
- VDD UVLO External Adjustment by Precision EN Hysteresis
- Prebias Startup Support
- Eco-Mode and FCCM Selectable
- Full Suite of Fault Protection and PGOOD
- 5 mm x 7 mm x 1.5 mm, 40-Pin, Stack Clipped LQFN-CLIP Package

2 Applications

- Enterprise Storage, SSD, NAS
- · Wireless and Wired Communication Infrastructure
- Industrial PCs, Automation, ATE, PLC, Video Surveillance
- Enterprise Server, Switches, Routers
- AISIC, SoC, FPGA, DSP Core and I/O Rails

3 Description

The TPS548D22 device is a compact single buck converter with adaptive on-time, D-CAP3 mode control. It is designed for high accuracy, high efficiency, fast transient response, ease-of-use, low external component count and space-conscious power systems.

This device features full differential sense, TI integrated FETs with a high-side on-resistance of 2.9 m Ω and a low-side on-resistance of 1.2 m Ω . The device also features accurate 0.5%, 0.9-V reference with an ambient temperature range between -40°C and 125°C. Competitive features include: very low external component count, accurate load regulation and line regulation, auto-skip or FCCM mode operation, and internal soft-start control.

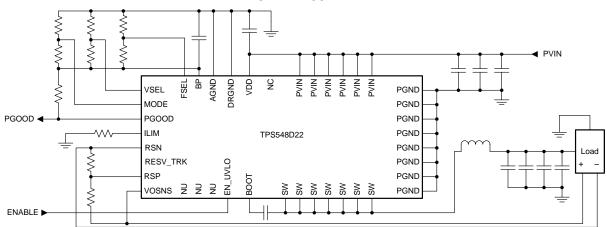
The TPS548D22 device is available in 5 mm x 7 mm, 40-pin, LQFN-CLIP (RVF) package (RoHs exempt).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TPS548D22	QFN (40)	5.00 mm × 7.00 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application





4 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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4.1 Package Option Addendum

4.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking ⁽⁴⁾⁽⁵⁾
TPS548D22	PREVIEW	LQFN-CLIP	RVF	40	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS548D22
TPS548D22	PREVIEW	LQFN-CLIP	RVF	40	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS548D22

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

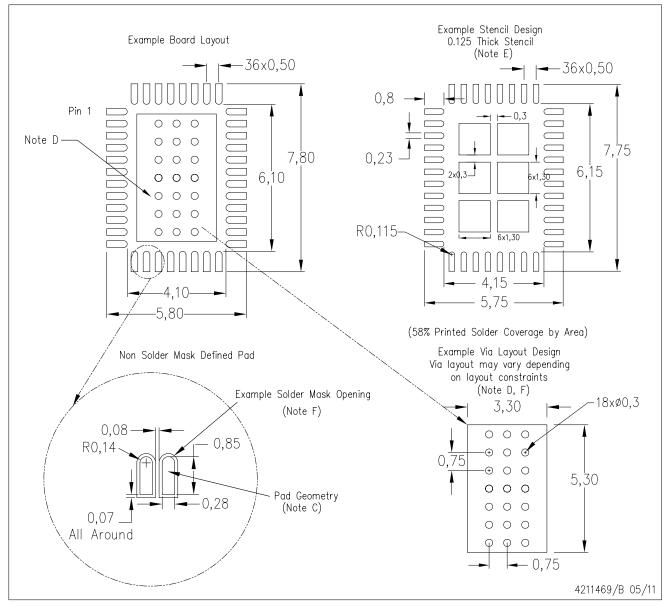
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RVF (R-PLQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



RVF (R-PLQFN-N40)

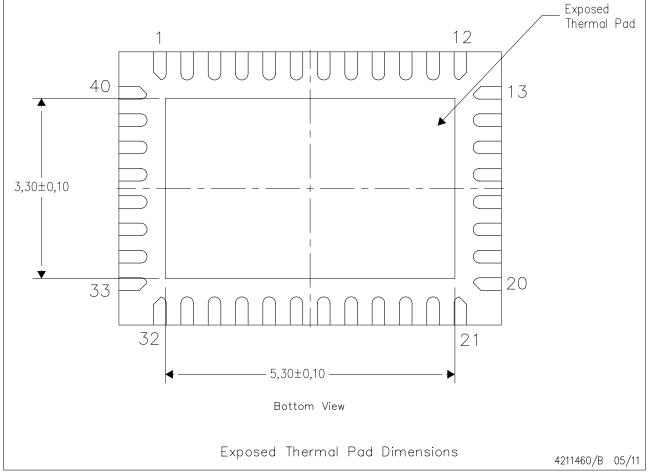
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

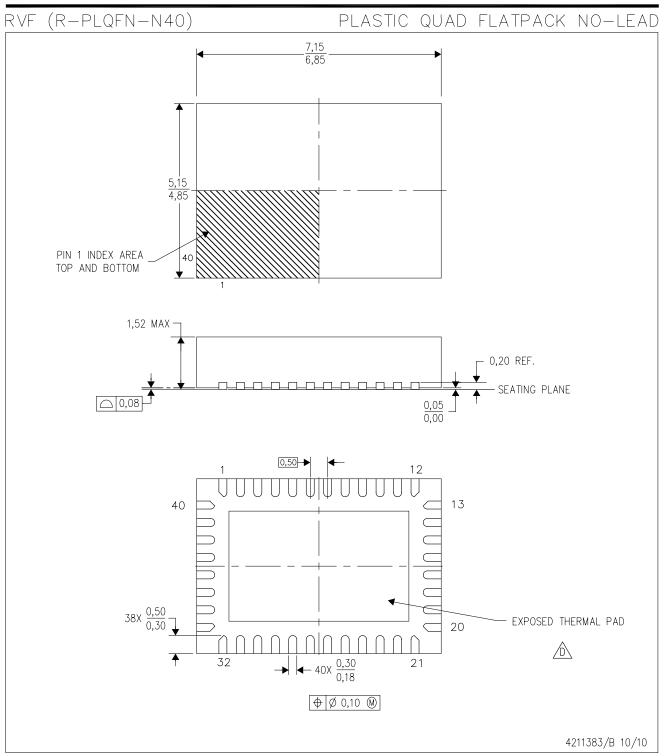
For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters





- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - Ç. Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.





PACKAGE OPTION ADDENDUM

4-Mar-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPS548D22RVFR	PREVIEW	LQFN-CLIP	RVF	40	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS548D22	
TPS548D22RVFT	PREVIEW	LQFN-CLIP	RVF	40	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS548D22	

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- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

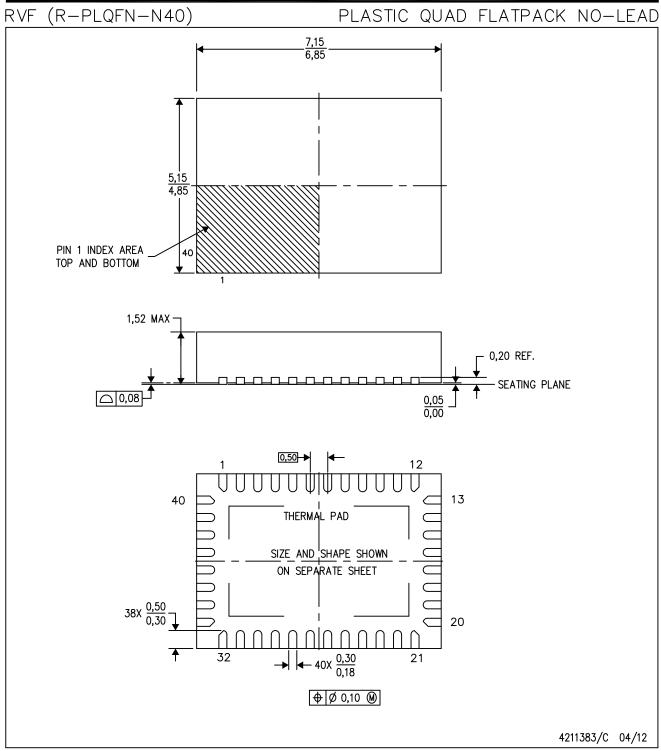
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PACKAGE OPTION ADDENDUM

4-Mar-2016

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- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.



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