TPS54388C-Q1 Automotive 2.95-V to 6-V, 3-A , 2-MHz Synchronous Buck Converter

1 Features

- AEC-Q100-qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Two 12-mΩ (typical) MOSFETs for high efficiency at 3-A loads
- 200-kHz to 2-MHz switching frequency
- 0.8 V ± 1% voltage reference over temperature (–40°C to +150°C)
- Synchronizes to external clock
- Adjustable slow start and sequencing
- UV and OV power-good output
- –40°C to +150°C operating junction temperature range
- Thermally enhanced 3-mm × 3-mm 16-pin WQFN
- Pin compatible to TPS54418

2 Applications

- Low-Voltage, High-Density Power Systems
- Point-of-Load Regulation for High-Performance DSPs, FPGAs, ASICs, and Microprocessors
- Broadband, Networking, and Optical Communications Infrastructure

3 Description

The TPS54388C-Q1 device is a full-featured 6-V, 3-A, synchronous step-down current-mode converter with two integrated MOSFETs.

The TPS54388C-Q1 device enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS54388C-Q1 device provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{ref}) over temperature.

The integrated 12-mΩ MOSFETs and 515-µA typical supply current maximize efficiency. Entering shutdown mode using the enable pin reduces shutdown supply current to 5.5 µA, typical.

The internal undervoltage lockout setting is at 2.45 V, but programming the threshold with a resistor network on the enable pin can increase the setting. The slow-start pin sets the output-voltage start-up ramp. An open-drain power-good signal indicates when the output is within 93% to 107% of its nominal voltage.

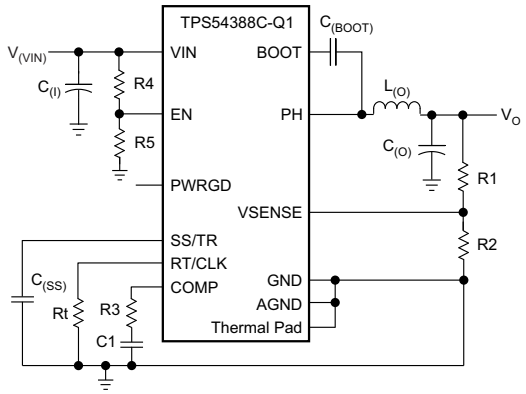
Frequency foldback and thermal shutdown protect the device during an overcurrent condition.

Device Information(1)

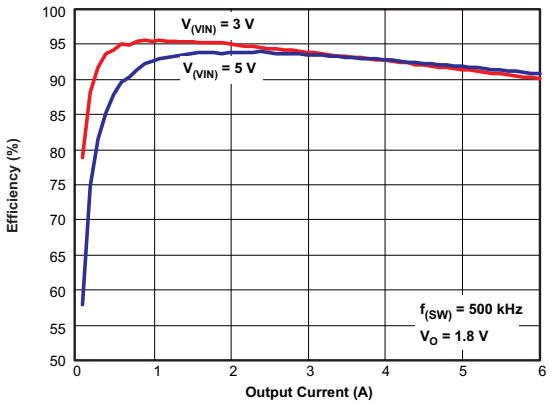
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54388C-Q1	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency Curve



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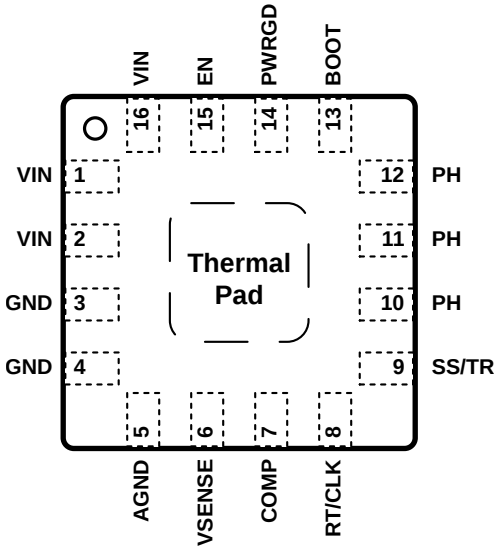
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to Revision A	Page
• First public release	1

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	5	—	Connect analog ground electrically to GND close to the device.
BOOT	13	O	The device requires a bootstrap capacitor between BOOT and PH. A voltage on this capacitor that is below the minimum required by the BOOT UVLO forces the output to switch off until the capacitor recharges.
COMP	7	O	Error amplifier output, and input to the output-switch current comparator. Connect frequency-compensation components to this pin.
EN	15	I	Enable pin, internal pullup-current source. Pull below 1.2 V to disable. Float to enable. One can use this pin to set the on-off threshold (adjust UVLO) with two additional resistors.
GND	3	—	Power ground. Directly connect this pin electrically to the thermal pad under the device.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET
	11		
	12		
PWRGD	14	O	An open-drain output; asserted low if output voltage is low due to thermal shutdown, overcurrent, over- or undervoltage, or EN shutdown.
RT/CLK	8	I	Resistor-timing or external-clock input pin
SS/TR	9	I	Slow start and tracking. An external capacitor connected to this pin sets the output-voltage rise time. Another use of this pin is for tracking.
VIN	1	I	Input supply voltage, 2.95 V to 6 V
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (g_m) error amplifier
Thermal pad		—	Connect the GND pin to the exposed thermal pad for proper operation. Connect this thermal pad to any internal PCB ground planes using multiple vias for good thermal performance.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	EN	–0.3	7	
	BOOT	–0.3	PH + 7	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	7	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	7	
Output voltage	BOOT-PH	–0.3	7	V
	PH	–0.6	7	
	PH 10-ns transient	–2	10	
Source current	EN		100	µA
	RT/CLK		100	
Sink current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Junction temperature, T_J		–40	150	°C
Ambient temperature, T_A		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 16, 4, 5, 8, 9, 12, and 13)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input voltage	2.95		6	V
T_A	Operating ambient temperature	–40		125	ºC

6.4 Thermal Information

THERMAL METRIC[1]		TPS54388C-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

T_J = –40°C to 150°C, $V_{(VIN)}$ = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	VIN UVLO start		2.28	2.5	V
	VIN UVLO stop		2.45	2.6	
Shutdown supply current	$V_{(EN)}$ = 0 V, 25°C, 2.95 V ≤ $V_{(VIN)}$ ≤ 6 V		5.5	15	µA
Quiescent current, $I_{(q)}$	$V_{(SENSE)}$ = 0.9 V, $V_{(VIN)}$ = 5 V, 25°C, Rt = 400 kΩ		515	750	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.25		V
	Falling		1.18		
Input current	Enable threshold + 50 mV		–1.6		µA
	Enable threshold – 50 mV		–1.6		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ $V_{(VIN)}$ ≤ 6 V, –40°C < T_J < 150°C	0.79	0.8	0.811	V
MOSFET					
High-side switch resistance	$V_{(BOOT-PH)}$ = 5 V		12	30	mΩ
	$V_{(BOOT-PH)}$ = 2.95 V		16	30	
Low-side switch resistance	$V_{(VIN)}$ = 5 V		13	30	mΩ
	$V_{(VIN)}$ = 2.95 V		17	30	
ERROR AMPLIFIER					
Input current			2		nA
Error-amplifier transconductance (g_m)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		245		µS
Error-amplifier transconductance (g_m) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		79		µS
Error amplifier source and sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±20		µA
COMP to high-side FET current g_m			25		S

Electrical Characteristics (continued)

T_J = –40°C to 150°C, $V_{(VIN)}$ = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
Current limit threshold		3.7	6.5		A
THERMAL SHUTDOWN					
Thermal shutdown			168		°C
Hysteresis			20		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	Rt = 400 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse duration		75			ns
RT/CLK voltage	Rt = 400 kΩ		0.5		V
RT/CLK high threshold			1.6	2.5	V
RT/CLK low threshold		0.4	0.6		V
Delay from RT/CLK falling edge to PH rising edge	Measure at 500 kHz with RT resistor in series with device pin		90		ns
PLL lock-in time	Measure at 500 kHz		45		µs
PH (PH PIN)					
Minimum on-time	Measured at 50% point on PH, I_O = 3 A		75		ns
	Measured at 50% point on PH, $V_{(VIN)}$ = 6 V, I_O = 0 A		120		
Minimum off-time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_O = 3 A		60		ns
Rise time	$V_{(VIN)}$ = 6 V, 6 A		2.25		V/ns
Fall time	$V_{(VIN)}$ = 6 V, 6 A		2		
BOOT (BOOT PIN)					
BOOT charge resistance	$V_{(VIN)}$ = 5 V		16		Ω
BOOT-PH UVLO	$V_{(VIN)}$ = 2.95 V		2.1		V
SLOW START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ = 0.4 V		2		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		50		mV
SS/TR to reference crossover	98% of normal reference voltage		1.1		V
SS/TR discharge voltage (overload)	$V_{(VSENSE)}$ = 0 V		61		mV
SS/TR discharge current (overload)	$V_{(VSENSE)}$ = 0 V, $V_{(SS/TR)}$ = 0.4 V		350		µA
SS discharge current (UVLO, EN, thermal fault)	$V_{(VIN)}$ = 5 V, $V_{(SS/TR)}$ = 0.5 V		1.9		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% V_{ref}
	VSENSE rising (Good)		93		
	VSENSE rising (Fault)		109		
	VSENSE falling (Good)		107		
Hysteresis	VSENSE falling		2		% V_{ref}
Output-high leakage	$V_{(VSENSE)}$ = V_{ref}, $V_{(PWRGD)}$ = 5.5 V		7		nA
On-resistance			56	100	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.3		V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.65	1.6	V

6.6 Typical Characteristics

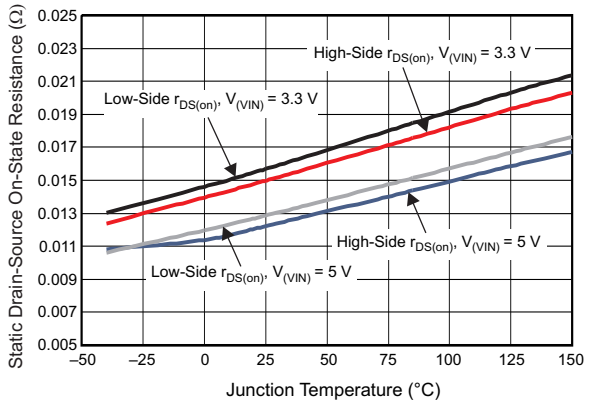


Figure 1. High-Side and Low-Side $r_{DS(on)}$ vs Temperature

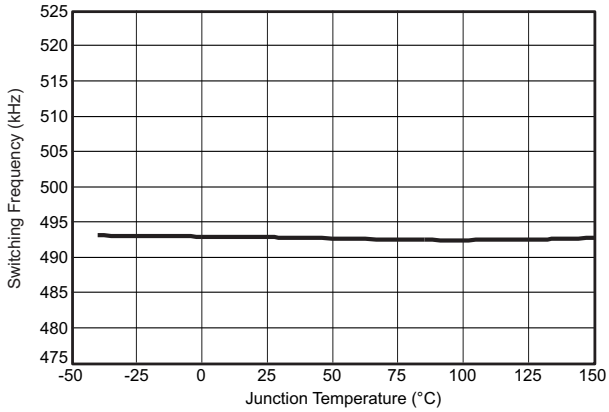


Figure 2. Frequency vs Temperature

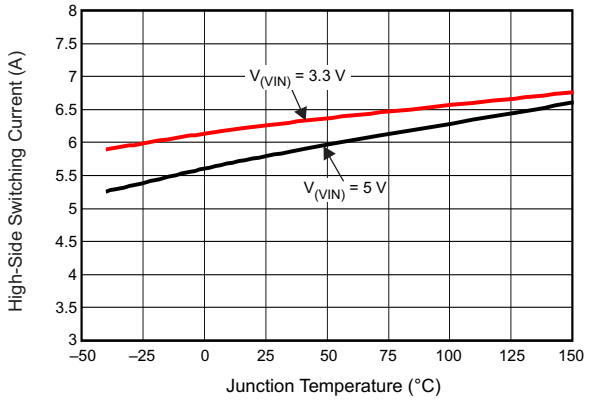


Figure 3. High-Side Current Limit vs Temperature

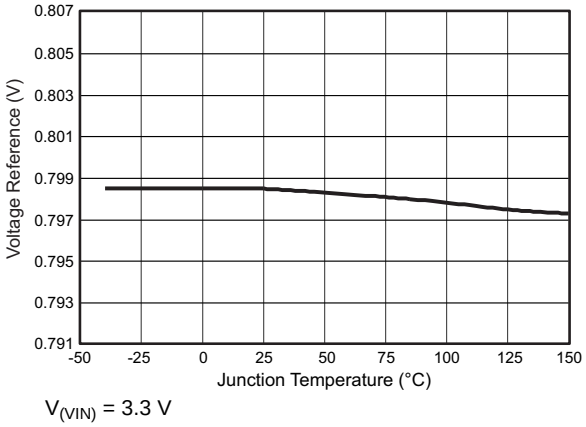


Figure 4. Voltage Reference vs Temperature

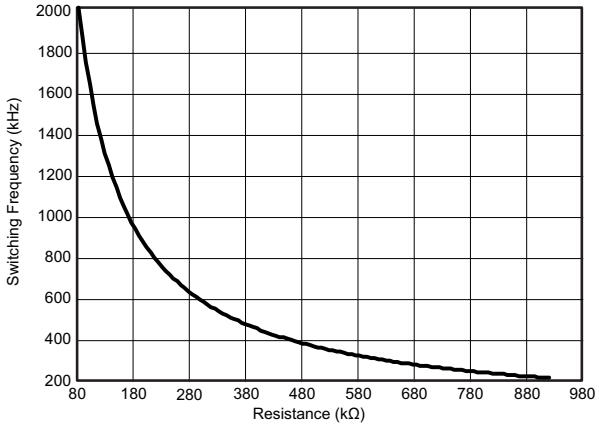


Figure 5. Switching Frequency vs RT Resistance, Low-Frequency Range

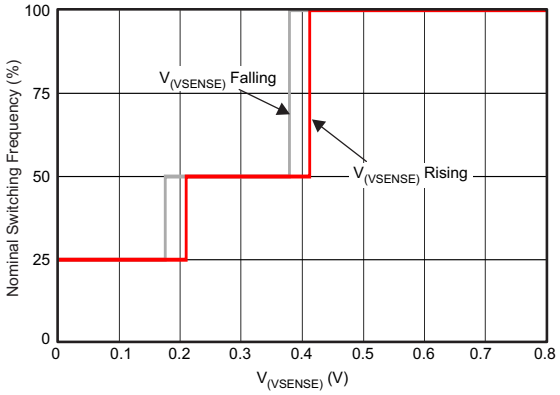
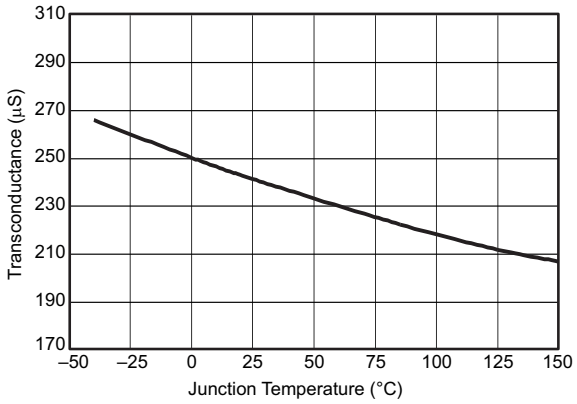


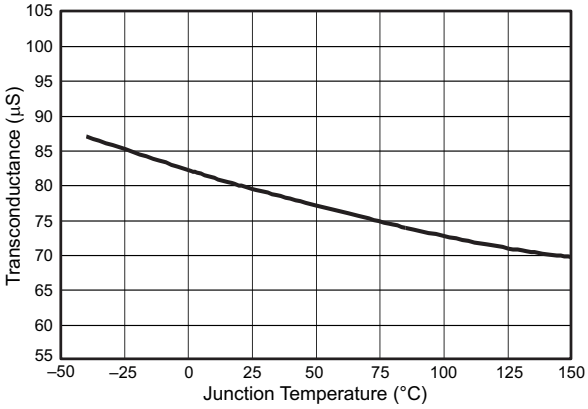
Figure 6. Switching Frequency vs $V_{(VSENSE)}$

Typical Characteristics (continued)



$V_{(VIN)}$ = 3.3 V

Figure 7. Transconductance vs Temperature



$V_{(VIN)}$ = 3.3 V

Figure 8. Transconductance (Slow Start) vs Junction Temperature

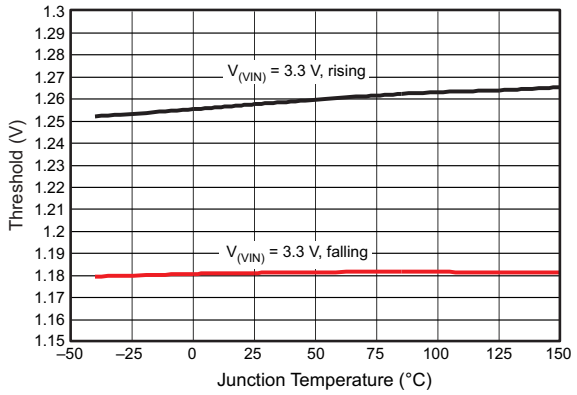
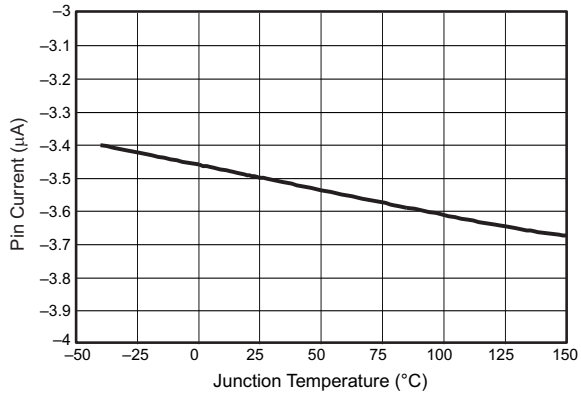


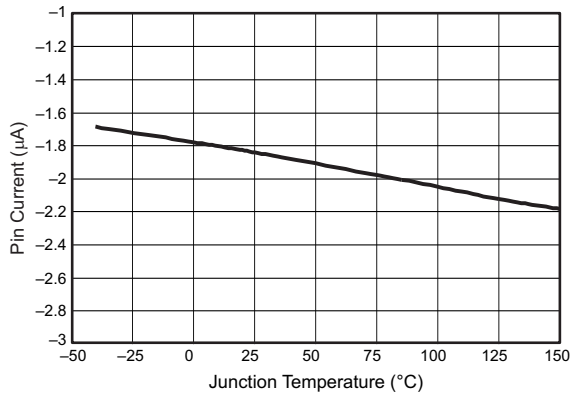
Figure 9. EN Pin Voltage vs Temperature



$V_{(VIN)}$ = 5 V

$V_{(EN)}$ = Threshold + 50 mV

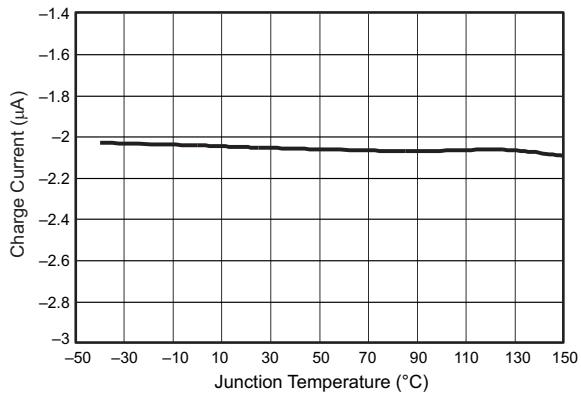
Figure 10. EN Pin Current vs Temperature



$V_{(VIN)}$ = 5 V

$V_{(EN)}$ = Threshold – 50 mV

Figure 11. EN Pin Current vs Temperature



$V_{(VIN)}$ = 5 V

Figure 12. Charge Current vs Temperature

Typical Characteristics (continued)

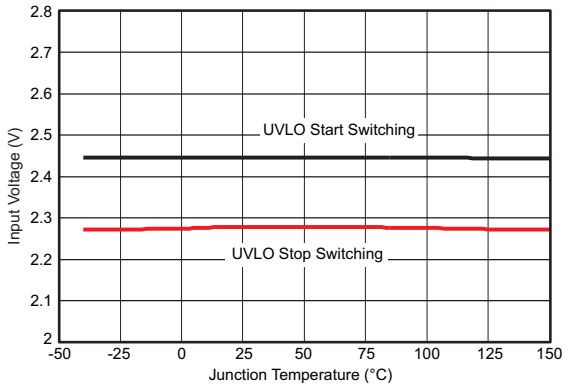
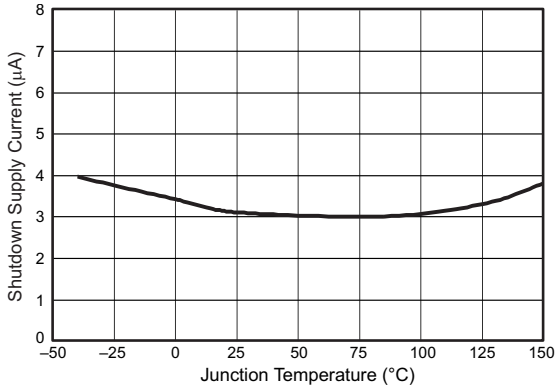
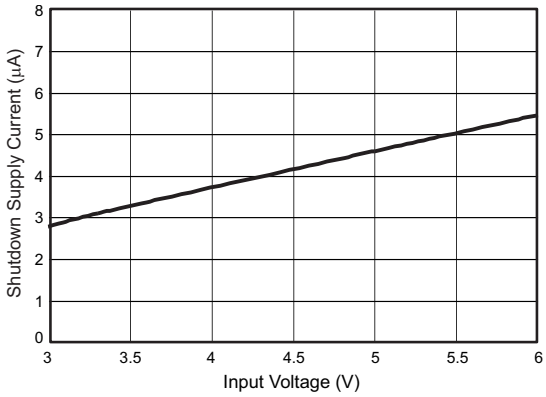


Figure 13. Input Voltage vs Temperature



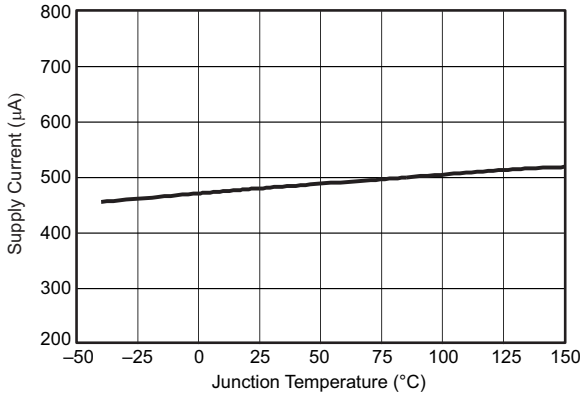
$V_{(VIN)}$ = 3.3 V

Figure 14. Shutdown Supply Current vs Temperature



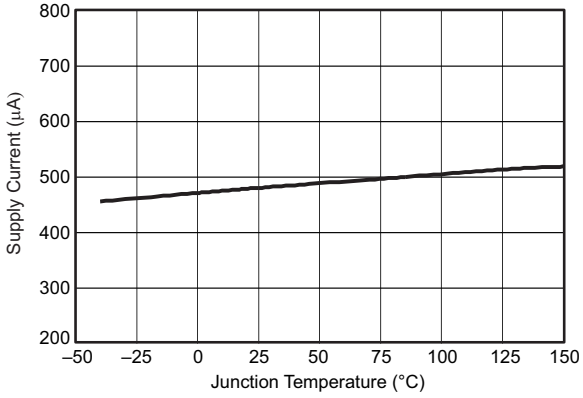
T_J = 25ºC

Figure 15. Shutdown Supply Current vs Input Voltage



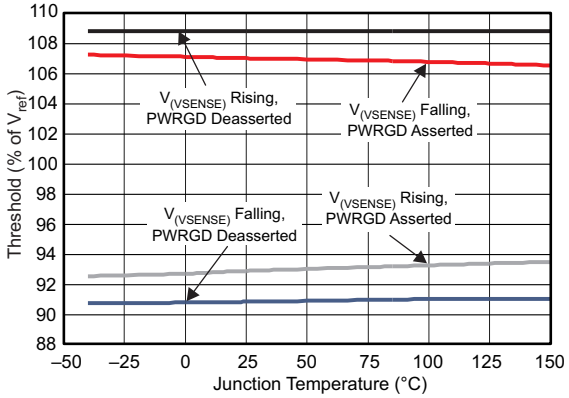
$V_{(VIN)}$ = 3.3 V

Figure 16. VIN Supply Current vs Junction Temperature



T_J = 25ºC

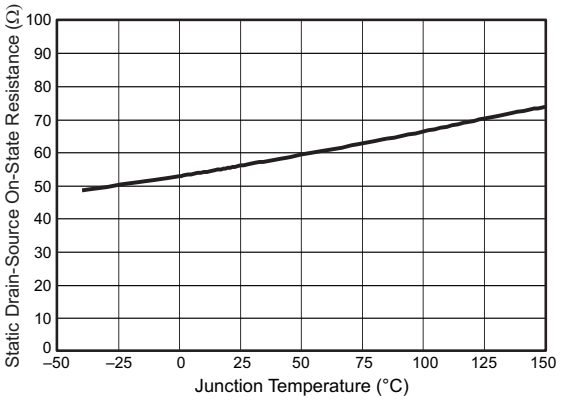
Figure 17. VIN Supply Current vs Input Voltage



$V_{(VIN)}$ = 5 V

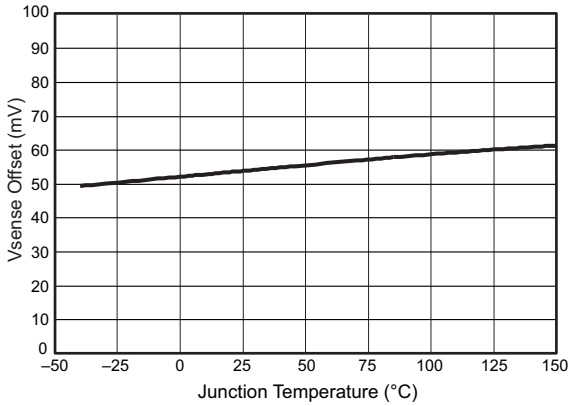
Figure 18. PWRGD Threshold vs Temperature

Typical Characteristics (continued)



$V_{(VIN)}$ = 5 V

Figure 19. PWRGD On-Resistance vs Temperature



$V_{(VIN)}$ = 5 V $V_{(SS/TR)}$ = 0.4 V

Figure 20. SS/TR-to-VSENSE Offset vs Temperature

7 Detailed Description

7.1 Overview

The TPS54388C-Q1 device is a 6-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak-current-mode control, which reduces output capacitance and simplifies external frequency-compensation design. The wide switching-frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output-filter components. A resistor to ground on the RT/CLK pin sets the switching frequency. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power-switch turnon to a falling edge of an external system clock.

The TPS54388C-Q1 device has a typical default start-up voltage of 2.45 V. The EN pin has an internal pullup current source that one can use to adjust the input-voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition, allowing the device to operate when the EN pin is floating. The total operating current for the device is typically 515 μA when not switching and under no load. With the device disabled, the supply current is typically 5.5 μA.

The integrated 12-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 3 A.

The TPS54388C-Q1 device reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit monitors the boot-capacitor voltage and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54388C-Q1 device to operate approaching 100% duty cycle. The lower limit for stepping down the output voltage is the 0.8-V reference.

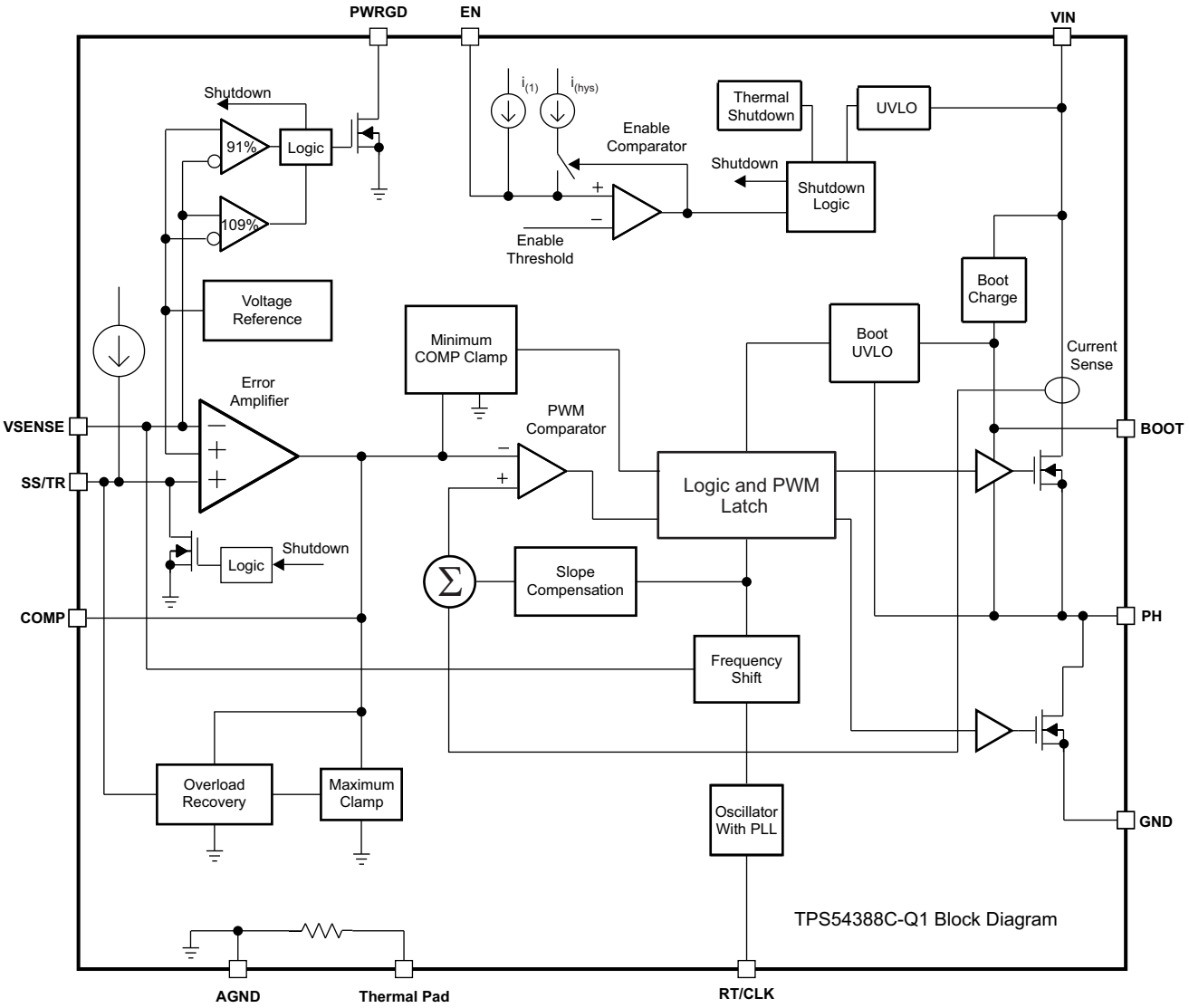
The TPS54388C-Q1 device has a power-good comparator (PWRGD) with 2% hysteresis.

The TPS54388C-Q1 device minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. A regulated output voltage exceeding 109% of the nominal voltage activates the overvoltage comparator, turning off the high-side MOSFET and masking it from turning on until the output voltage is lower than 107% of the nominal voltage.

A use of the SS/TR (slow start pr tracking) pin is to minimize inrush currents or provide power-supply sequencing during power up. Couple a small-value capacitor to the pin for slow start. Discharging the SS/TR pin before the output powers up ensures a repeatable restart after an overtemperature fault, UVLO fault, or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help limit the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The TPS54388C-Q1 device uses an adjustable fixed-frequency, peak-current-mode control. An error amplifier, which drives the COMP pin, compares the output voltage through external resistors on the VSENSE pin to an internal voltage reference. An internal oscillator initiates the turnon of the high-side power switch. The device compares the error-amplifier output to the high-side power-switch current. When the sensed voltage derived from the power-switch current reaches the COMP voltage level, the high-side power switch turns off and the low-side power switch turns on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level, and also implements a minimum clamp for improved transient-response performance.

7.3.2 Slope Compensation and Output Current

The TPS54388C-Q1 device adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

7.3.3 Bootstrap Voltage (BOOT) and Low-Dropout Operation

The TPS54388C-Q1 device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 μF. TI recommends a ceramic capacitor with an X7R- or X5R-grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

The TPS54388C-Q1 design improves dropout by operating at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.2 V. A UVLO circuit turns off the high-side MOSFET, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Thus, the effective duty cycle of the switching regulator is high.

7.3.4 Error Amplifier

The TPS54388C-Q1 device has a transconductance amplifier that it uses as an error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 245 μS during normal operation. When the voltage of VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the g_m is typically greater than 79 μS, but less than 245 μS.

7.3.5 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit. The band-gap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

7.4 Device Functional Modes

7.4.1 Adjusting the Output Voltage

A resistor divider from the output node to the VSENSE pin sets the output voltage. TI recommends using divider resistors with 1% tolerance or better. Start with 100 kΩ for the R1 resistor and use Equation 1 to calculate R2. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \quad (1)$$

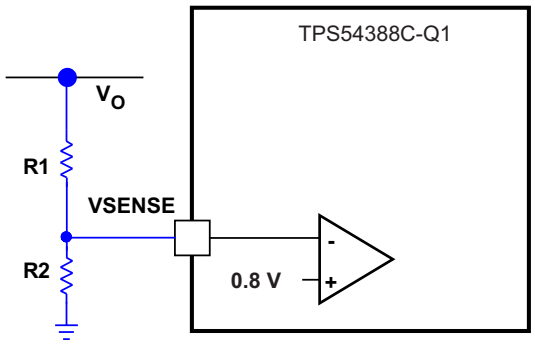


Figure 21. Voltage-Divider Circuit

Device Functional Modes (continued)

7.4.2 Enable Functionality and Adjusting Undervoltage Lockout

The VIN pin voltage on the VIN pin falling below 2.6 V disables the TPS54388C-Q1 device. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 22 to adjust the input voltage UVLO by using two external resistors. TI recommends using the EN resistors to set the UVLO falling threshold ($V_{(STOP)}$) above 2.6 V. Set the rising threshold ($V_{(START)}$) to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of TPS54388C-Q1 operation when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, the circuitry adds an additional 1.6 μA of hysteresis. Pulling the EN pin below 1.18 V removes the 1.6 μA. This additional current facilitates input voltage hysteresis.

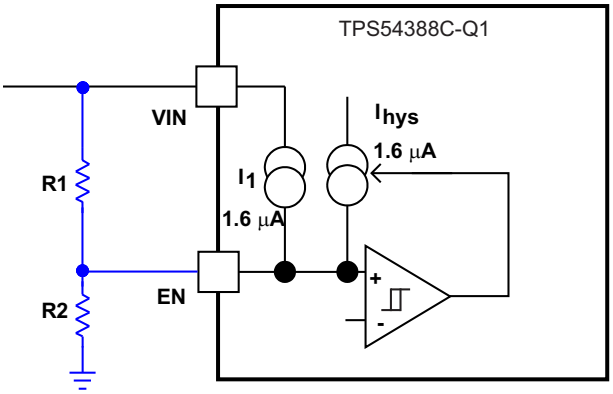


Figure 22. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{(START)}\left(\frac{V_{(ENFALLING)}}{V_{(ENRISING)}}\right) - V_{(STOP)}}{I_{(1)}\left(1 - \frac{V_{(ENFALLING)}}{V_{(ENRISING)}}\right) + I_{(hys)}} \quad (2)$$

where

- $V_{(ENFALLING)}$ = 1.18 V
- $V_{(ENRISING)}$ = 1.25 V
- $I_{(1)}$ = 1.6 μA
- $I_{(hys)}$ = 1.6 μA

$$R2 = \frac{R1 \times V_{(ENFALLING)}}{V_{(STOP)} - V_{(ENFALLING)} + R1 \times (I_{(1)} + I_{(hys)})} \quad (3)$$

7.4.3 Slow-Start or Tracking Pin

The TPS54388C-Q1 device regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS54388C-Q1 device has an internal pullup current source of 2 μA, which charges the external slow-start capacitor. Equation 4 calculates the required slow-start capacitor value, where $t_{(SS/TR)}$ is the desired slow start time in ms, $I_{(SS/TR)}$ is the internal slow start charging current of 2 μA, and V_{ref} is the internal voltage reference of 0.8 V.

$$C_{(SS/TR)}\ (nF) = \frac{t_{(SS/TR)}\ (ms) \times I_{(SS/TR)}\ (\mu A)}{V_{ref}\ (V)} \quad (4)$$

Device Functional Modes (continued)

If during normal operation, VIN goes below UVLO, the EN pin goes below 1.2 V, or a thermal shutdown event occurs, the TPS54388C-Q1 device stops switching. On VIN going above UVLO, the release or pulling high of EN, or exit from a thermal shutdown, SS/TR discharges to below 60 mV before re-initiation of a power-up sequence. The VSENSE voltage follows the SS/TR pin voltage with a 50-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

7.4.4 Sequencing

One can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implementation of the sequential method uses an open-drain or open-collector output of the power-on-reset pin of another device. Figure 23 shows the sequential method. Couple the power-good to the EN pin on the TPS54388C-Q1 device to enable the second power supply once the primary supply reaches regulation.

One can accomplish ratiometric start-up by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, double the pullup current source in Equation 4. Figure 25 shows the ratiometric method.

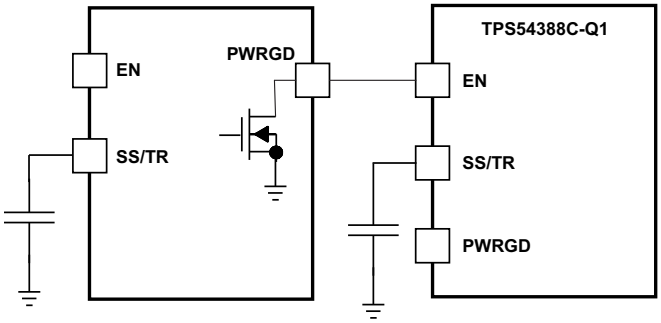


Figure 23. Sequential Start-Up Sequence

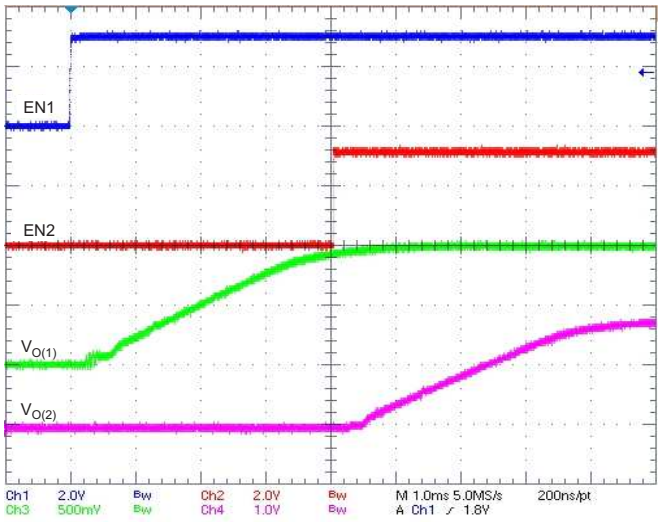


Figure 24. Sequential Start-Up Using EN and PWRGD

Device Functional Modes (continued)

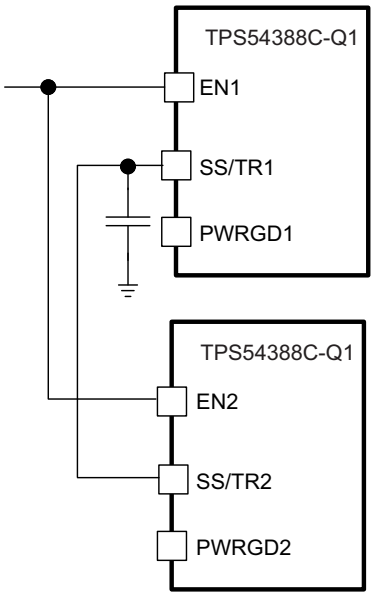


Figure 25. Schematic for Ratiometric Start-Up Sequence

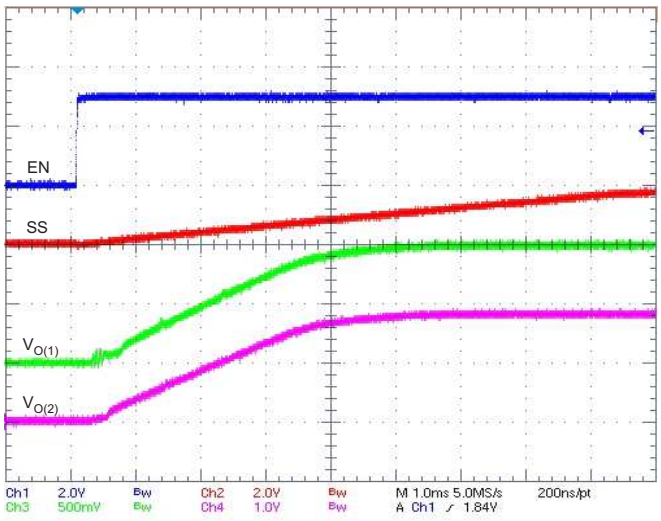


Figure 26. Ratiometric Start-Up With $V_{O(1)}$ Leading $V_{O(2)}$

One can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in Figure 27 to the output of the power supply that requires tracking, or to another voltage reference source. Using Equation 5 and Equation 6, one can calculate the tracking resistors to initiate $V_{O(2)}$ slightly before, after, or at the same time as $V_{O(1)}$. $V_{O(1)} - V_{O(2)}$ is 0 V for simultaneous sequencing. Including $V_{(ssoffset)}$ and $I_{(SS/TR)}$ as variables in the equations minimizes the effect of the inherent SS/TR-to-VSENSE offset ($V_{(ssoffset)}$) in the slow-start circuit and the offset created by the pullup current source ($I_{(ss)}$) and tracking resistors. Because the SS/TR pin requires pulling below 60 mV before starting after an EN, UVLO, or thermal-shutdown fault, select the tracking resistors carefully to ensure the device can restart after a fault. Make sure the calculated R1 value from Equation 5 is greater than the value calculated in Equation 7 to ensure the device can recover from a fault. As the SS/TR voltage becomes more than 85% of the nominal reference voltage, $V_{(ssoffset)}$ becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.1 V for a complete handoff to the internal voltage reference as shown in Figure 26.

$$R1 = \frac{V_{O(1)}}{V_{ref}} \times \frac{V_{(ssoffset)}}{I_{(SS/TR)}} \tag{5}$$

$$R2 = \frac{V_{ref} \times R1}{V_{O(1)} - V_{ref}} \tag{6}$$

$$R1 > 2930 \times V_{O(1)} - 145 \times (V_{O(1)} - V_{O(2)}) \tag{7}$$

Device Functional Modes (continued)

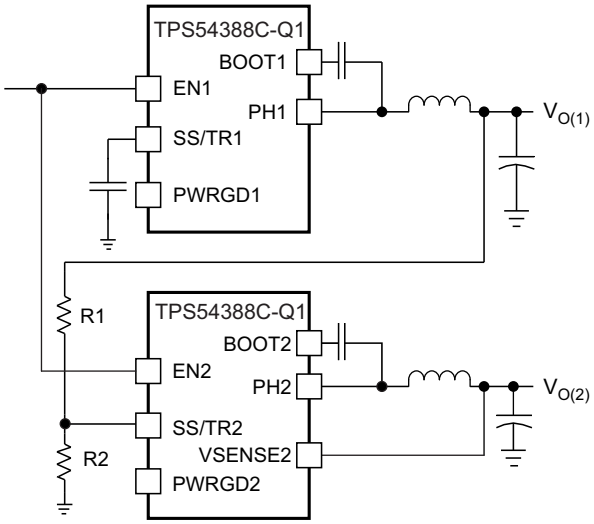


Figure 27. Ratiometric and Simultaneous Start-Up Sequence

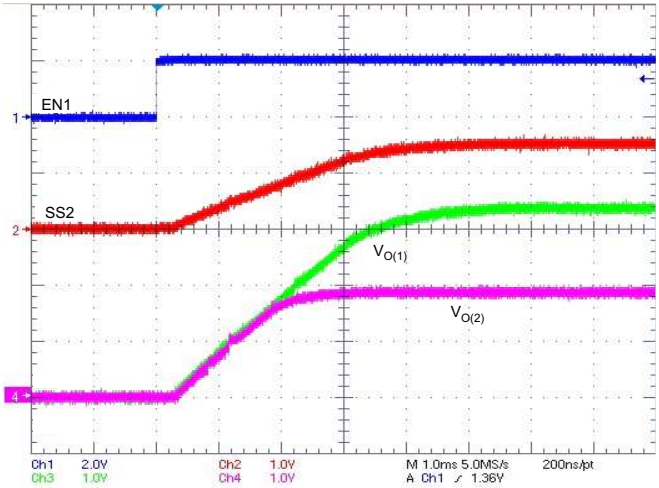


Figure 28. Ratiometric Start-Up Using Coupled SS/TR Pins

7.4.5 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54388C-Q1 device is adjustable over a wide range from 200 kHz to 2000 kHz by placing a resistor on the RT/CLK pin with a value calculated by Equation 8. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The voltage on RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use Equation 8 or the curve in Figure 5.

$$Rt(k\Omega) = \frac{247\,530\ (M\Omega/s)}{f_{(SW)}^{1.0533}(kHz)} \tag{8}$$

$$f_{(SW)}(kHz) = \frac{131\,904\ (M\Omega/s)}{Rt^{0.9492}(k\Omega)} \tag{9}$$

To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the efficiency, maximum input voltage, and minimum controllable on-time.

The minimum controllable on-time is typically 60 ns at full-current load and 120 ns at no load, and limits the maximum operating input voltage or output voltage.

7.4.6 Overcurrent Protection

The TPS54388C-Q1 device implements a cycle-by-cycle current limit. During each switching cycle, the device compares a voltage derived from the high-side switch current to the voltage on the COMP pin. When the instantaneous switch-current voltage intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. An internal clamp on the error-amplifier output functions as a switch-current limit.

7.4.7 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54388C-Q1 device implements a frequency shift. Without this frequency shift, during an overcurrent condition the low-side MOSFET might not turn off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition there is a switching-frequency reduction from 100% to 50%, then 25%, as the voltage decreases from 0.8 V to 0 V on the VSENSE pin. The frequency shift allows the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 V to 0.8 V. See Figure 6 for details.

Device Functional Modes (continued)

7.4.8 Reverse Overcurrent Protection

The TPS54388C-Q1 device implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 4.5 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

7.4.9 Synchronize Using the RT/CLK Pin

The RT/CLK pin synchronizes the converter to an external system clock. See Figure 29. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75 ns. If the square wave pulls the pin above the PLL upper threshold, a mode change occurs, and the pin becomes a synchronization input. The CLK mode disables the internal amplifier, and the pin becomes a high-impedance clock input to the internal PLL. Stopping the clocking edges re-enables the internal amplifier, and the mode returns to the frequency set by the resistor. The square-wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V, typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of PH synchronizes to the falling edge of the RT/CLK pin.

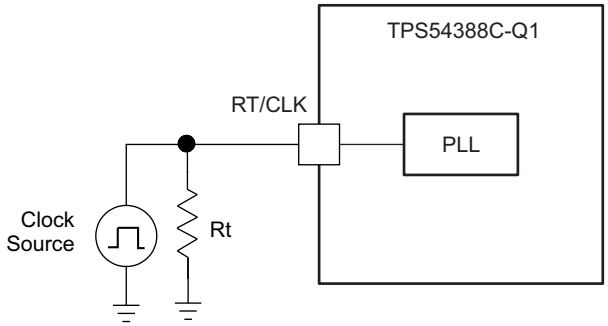


Figure 29. Synchronizing to a System Clock

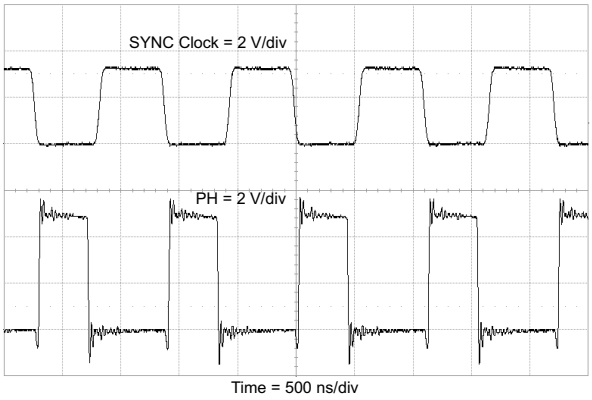


Figure 30. Plot of Synchronizing to a System Clock

7.4.10 Power Good (PWRGD Pin)

The output of the PWRGD pin is an open-drain MOSFET. The output goes low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 109% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 107% of the internal voltage reference, the PWRGD output MOSFET turns off. TI recommends using a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. PWRGD is in a valid state once the VIN input voltage is greater than 1.1 V.

7.4.11 Overvoltage Transient Protection

The TPS54388C-Q1 device incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold, which is 109% of the internal voltage reference. If the VSENSE pin voltage goes higher than the OVTP threshold, the high-side MOSFET turns off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high-side MOSFET turns on in the next clock cycle.

7.4.12 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 168°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 148°C, the device reinitiates the power-up sequence by discharging the SS/TR pin to below 60 mV. The thermal shutdown hysteresis is 20°C.

Device Functional Modes (continued)

7.4.13 Small-Signal Model for Loop Response

Figure 31 shows an equivalent model for the TPS54388C-Q1 control loop, which one can model in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a g_m of 245 µS. One can model the error amplifier using an ideal voltage-controlled current source. The resistor R0 and capacitor C0 model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting a over c vs frequency shows the small-signal response of the frequency compensation. Plotting a over b vs frequency shows the small-signal response of the overall loop. Check the dynamic loop response by replacing $R_{(L)}$ with a current source that has the appropriate load-step amplitude and step rate in a time-domain analysis.

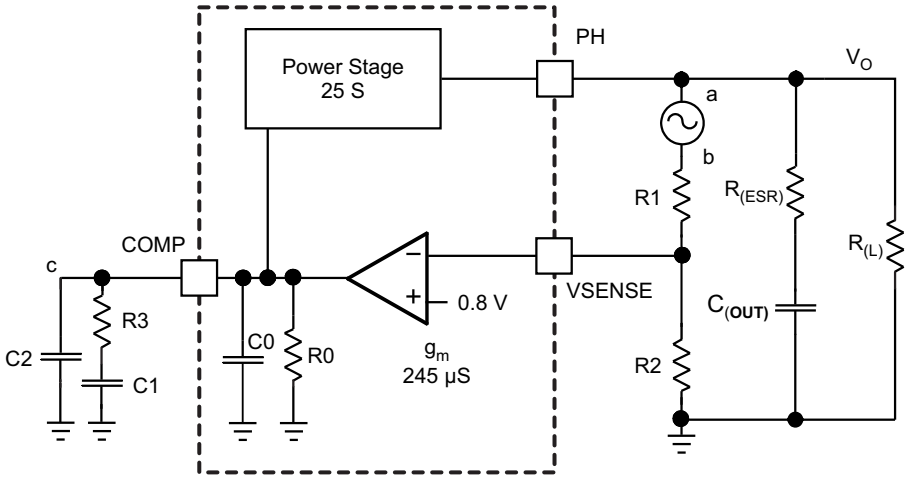


Figure 31. Small-Signal Model for Loop Response

7.4.14 Simple Small-Signal Model for Peak-Current-Mode Control

Figure 31 is a simple small-signal model that one can use to understand how to design the frequency compensation. A voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor approximates the TPS54388C-Q1 power stage. Equation 10 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current divided by the change in COMP pin voltage (node c in Figure 31) is the power-stage transconductance. The g_m for the TPS54388C-Q1 device is 25 S. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance as shown in Equation 11. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current (see Equation 12). The dashed line in the right half of Figure 32 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for varying load conditions, which makes it easier to design the frequency compensation.

Device Functional Modes (continued)

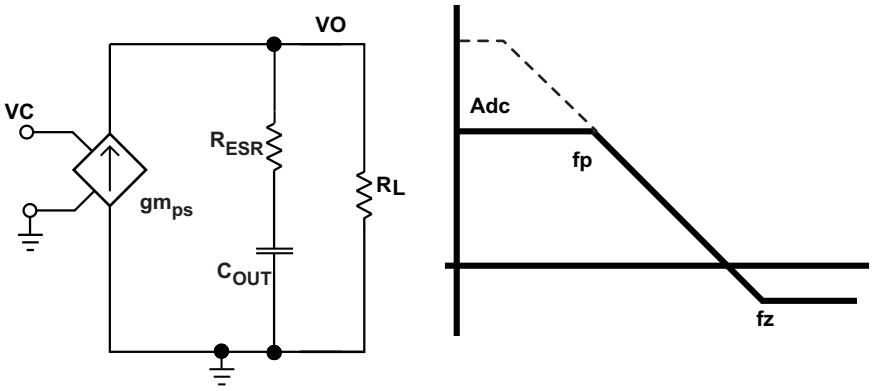


Figure 32. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control

$$\frac{V_O}{V_{(C)}} = A_{(dc)} \times \frac{\left(1+\frac{s}{2\pi \times f_{(z)}}\right)}{\left(1+\frac{s}{2\pi \times f_{(p)}}\right)} \quad (10)$$

$$A_{(dc)} = g_{m(ps)} \times R_{(L)} \quad (11)$$

$$f_{(p)} = \frac{1}{C_{(OUT)} \times R_{(L)} \times 2\pi} \quad (12)$$

$$f_{(z)} = \frac{1}{C_{(OUT)} \times R_{(ESR)} \times 2\pi} \quad (13)$$

7.4.15 Small-Signal Model for Frequency Compensation

The TPS54388C-Q1 device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency-compensation circuits. Figure 33 shows the compensation circuits. The most-likely implementation of Type 2B circuits is in high-bandwidth power-supply designs using low-ESR output capacitors. Type 2A contains one additional high-frequency pole to attenuate high-frequency noise.

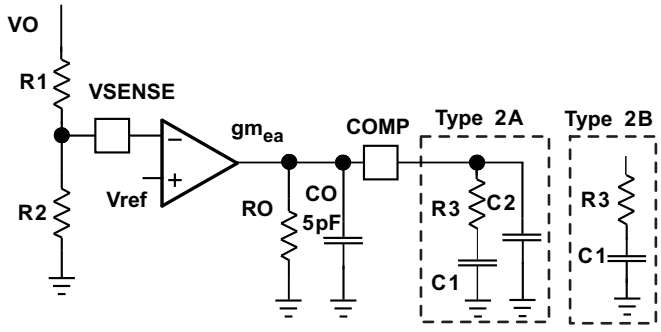


Figure 33. Types of Frequency Compensation

Device Functional Modes (continued)

The design guidelines for TPS54388C-Q1 loop compensation are as follows:

1. Calculate the modulator pole, $f_{(p,mod)}$, and the ESR zero, $f_{(z,mod)}$, using Equation 14 and Equation 15. The output capacitor ($C_{(OUT)}$) may require derating if the output voltage is a high percentage of the capacitor rating. Use the manufacturer information for the capacitor to derate the capacitor value. Use Equation 16 and Equation 17 to estimate a starting point for the crossover frequency, $f_{(c)}$. Equation 16 is the geometric mean of the modulator pole and the ESR zero, and Equation 17 is the mean of the modulator pole and the switching frequency. Use the lower value of Equation 16 or Equation 17 as the maximum crossover frequency.

$$f_{(p,mod)} = \frac{I_{O(max)}}{2\pi \times V_O \times C_{(OUT)}} \quad (14)$$

$$f_{(z,mod)} = \frac{1}{2\pi \times R_{(ESR)} \times C_{(OUT)}} \quad (15)$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times f_{(z,mod)}} \quad (16)$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times \frac{f_{(SW)}}{2}} \quad (17)$$

2. Determine R3 using Equation 18.

$$R3 = \frac{2\pi \times f_{(c)} \times V_O \times C_{(OUT)}}{g_{m(ea)} \times V_{ref} \times g_{m(ps)}} \quad (18)$$

where

- $g_{m(ea)}$ is the amplifier gain (245 µS)
- $g_{m(ps)}$ is the power-stage gain (25 S)

3. Place a compensation zero at the dominant pole:

$$f_{(p)} = \frac{1}{C_{(OUT)} \times R_{(L)} \times 2\pi} \quad (19)$$

4. Determine C1 using Equation 20.

$$C1 = \frac{R_{(L)} \times C_{(OUT)}}{R3} \quad (20)$$

5. C2 is optional. Use it, if necessary, to cancel the zero from the ESR of $C_{(OUT)}$.

$$C2 = \frac{R_{(ESR)} \times C_{(OUT)}}{R3} \quad (21)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Details on how to use this device in automotive applications appear throughout this device specification. The following sections provide the typical application use case with equations and methods on selecting the external components, as well as layout guidelines.

8.2 Typical Application

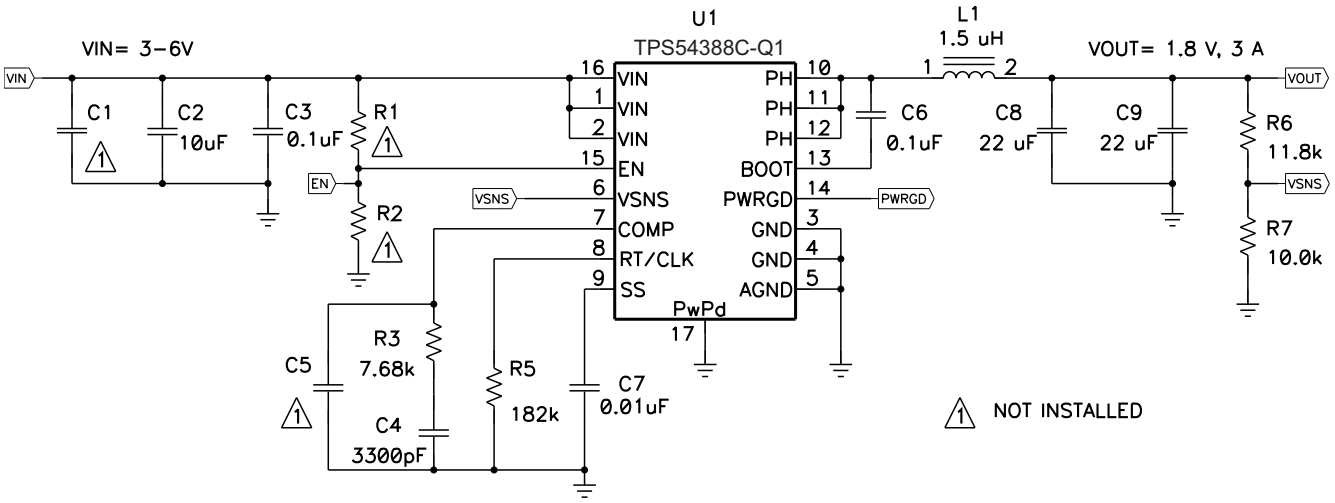


Figure 34. High-Frequency, 1.8-V Output Power-Supply Design With Adjusted UVLO

8.2.1 Design Requirements

This example details the design of a high-frequency switching-regulator design using ceramic output capacitors. To start the design process, it is necessary to know a few parameters. Determination of these parameters is typically at the system level. For this example, start with the following known parameters:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	1.8 V
Transient response, 1-A to 2-A load step	$\Delta V_{(out)}$ = 5%
Maximum output current	3 A
Input voltage	5 V nominal, 3 V to 5 V
Output-voltage ripple	< 30 mV p-p
Switching frequency, $f_{(sw)}$	1000 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, one would choose the highest switching frequency possible to produce the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter performance. The converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is an ultimate goal, select a moderate switching frequency of 1 MHz to achieve both a small solution size and high-efficiency operation. Using Equation 8, calculate R5 to be 180 kΩ. Choose a standard 1% 182-kΩ value for the design.

8.2.2.2 Output Inductor Selection

The inductor selected works for the entire TPS54388C-Q1 input-voltage range. To calculate the value of the output inductor, use Equation 22. The $k_{(IND)}$ coefficient represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, $k_{(IND)}$ is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use $k_{(IND)}$ = 0.3, and the inductor value calculates to be 1.36 µH. For this design, choose the nearest standard value of 1.5 µH. For the output-filter inductor, it is important not to exceed the rms-current and saturation-current ratings. Find the rms and peak inductor current using Equation 24 and Equation 25.

For this design, the rms inductor current is 3.01 A and the peak inductor current is 3.72 A. The chosen inductor is a Coilcraft XLA4020-152ME_ or equivalent. It has a saturation current rating 0f 9.6 A and an RMS current rating of 7.5 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$L1 = \frac{V_{I(max)} - V_O}{I_O \times k_{(IND)}} \times \frac{V_O}{V_{I(max)} \times f_{(SW)}} \quad (22)$$

$$I_{(ripple)} = \frac{V_{I(max)} - V_O}{L1} \times \frac{V_O}{V_{I(max)} \times f_{(SW)}} \quad (23)$$

$$I_{(Lrms)} = \sqrt{I_O^2 + \frac{1}{12} \times \left(\frac{V_O \times (V_{I(max)} - V_O)}{V_{I(max)} \times L1 \times f_{(SW)}} \right)^2} \quad (24)$$

$$I_{(Lpeak)} = I_O + \frac{I_{(ripple)}}{2} \quad (25)$$

8.2.2.3 Output Capacitor

Three primary considerations must be considered for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Base the output-capacitance selection on the most-stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after removal of the input power. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current requirement of the load, such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to see the change in load current and output voltage and then adjust the duty cycle to react to the change. The output capacitor must be large enough to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 26 shows the minimum output capacitance necessary to meet this requirement.

For this example, the specification for transient-load response is a 5% change in V_O for a load step from 0 A (no load) to 1.5 A (50% load). For this example, ΔI_O = 1.5 A – 0 A = 1.5 A and ΔV_O = 0.05 × 1.8 V = 0.09 V. Using these numbers gives a minimum capacitance of 33 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 27 calculates the minimum output capacitance needed to meet the output-voltage ripple specification. In this case, the maximum output-voltage ripple is 30 mV. Under this requirement, Equation 27 yields 2.3 µF.

$$C_{(OUT)} > \frac{2 \times \Delta I_O}{f_{(SW)} \times \Delta V_O}$$

where

- ΔI_O is the change in output current
- $f_{(SW)}$ is the regulator switching frequency
- ΔV_O is the allowable change in the output voltage (26)

$$C_{(OUT)} > \frac{1}{8 \times f_{(SW)}} \times \frac{1}{\frac{V_{O(ripple)}}{I_{(ripple)}}}$$

where

- $f_{(SW)}$ is the switching frequency
- $V_{O(ripple)}$ is the maximum allowable output voltage ripple
- $I_{(ripple)}$ is the inductor ripple current (27)

Use Equation 28 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 28 indicates the ESR should be less than 55 mΩ. In this case, the ESR of the ceramic capacitor is much less than 55 mΩ.

Factoring in additional capacitance deratings for aging, temperature, and dc bias increases this minimum value. For this example, use two 22-µF, 10-V X5R ceramic capacitors with 3 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Select an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Use Equation 29 to calculate the rms ripple current that the output capacitor must support. For this application, Equation 29 yields 333 mA.

$$R_{(ESR)} < \frac{V_{O(ripple)}}{I_{(ripple)}} \tag{28}$$

$$I_{(Co,rms)} = \frac{V_O \times (V_{I(max)} - V_O)}{\sqrt{12} \times V_{I(max)} \times L1 \times f_{(SW)}} \tag{29}$$

8.2.2.4 Input Capacitor

The TPS54388C-Q1 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with at least 4.7 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS54388C-Q1 device. Calculate the input ripple current using Equation 30.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. Minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are the usual selection for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output-capacitor selection must also take dc bias into account. The capacitance value of a capacitor decreases as the dc bias across that capacitor increases.

This example design requires a ceramic capacitor with at least a 10-V voltage rating to support the maximum input voltage. For this example, the selection is one 10-µF 10-V and one 0.1-µF 10-V capacitor in parallel. The input capacitance value determines the input ripple voltage of the regulator. Calculate the input voltage ripple using Equation 31. Using the design example values, $I_{O(max)}$ = 3 A, $C_{(IN)}$ = 10 µF, and $f_{(SW)}$ = 1 MHz, yields an input voltage ripple of 76 mV and an rms input ripple current of 1.47 A.

$$I_{(Ci,rms)} = I_O \times \sqrt{\frac{V_O}{V_{I(min)}} \times \frac{\left(V_{I(min)} - V_O\right)}{V_{I(min)}}} \tag{30}$$

$$\Delta V_I = \frac{I_{O(max)} \times 0.25}{C_{(IN)} \times f_{(SW)}} \tag{31}$$

8.2.2.5 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. Slow start is useful if a load requires a controlled rate of voltage slew. Another use for slow start is if the output capacitance is large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large current necessary to charge the capacitor may make the TPS54388C-Q1 device reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

Calculate the slow-start capacitor value using Equation 32. For the example circuit, the slow-start time is not too critical because the output-capacitor value is 44 µF, which does not require much current to charge to 1.8 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms, which requires a 10-nF capacitor. In the TPS54388C-Q1 device, $I_{(SS/TR)}$ is 2.2 µA and V_{ref} is 0.8 V.

$$C_{(SS)}\ (nF) = \frac{t_{(SS)}\ (ms) \times I_{(SS/TR)}\ (\mu A)}{V_{ref}\ (V)} \tag{32}$$

8.2.2.6 Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

8.2.2.7 Output-Voltage and Feedback-Resistor Selection

For the example design, the R6 selection is 100 kΩ. Using Equation 33, calculate R7 as 80 kΩ. The nearest standard 1% resistor is 80.5 kΩ.

$$R7 = \frac{V_{ref}}{V_O - V_{ref}} \times R6 \tag{33}$$

Because of the internal design of the TPS54388C-Q1 device, there is a minimum output-voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, an output voltage limit may exist due to the minimum controllable on-time. In this case, Equation 34 gives the minimum output voltage:

$$V_{O(min)} = t_{(ONmin)} \times f_{(SWmax)} \times \left(V_{I(max)} - I_{O(min)} \times 2 \times r_{DS(on)}\right) - I_{O(min)} \times \left(R_{(L)} + r_{DS(on)}\right)$$

where

- $V_{O(min)}$ = minimum achievable output voltage
- $t_{(ONmin)}$ = minimum controllable on-time (65 ns typical, 120 ns with no load)
- $f_{(SWmax)}$ = maximum switching frequency, including tolerance
- $V_{I(max)}$ = maximum input voltage
- $I_{O(min)}$ = minimum load current
- $r_{DS(on)}$ = minimum high-side MOSFET on-resistance (15 mΩ–19 mΩ)
- $R_{(L)}$ = series resistance of output inductor

(34)

There is also a maximum achievable output voltage, which is limited by the minimum off-time. Equation 35 gives the maximum output voltage.

$$V_{O(max)} = \left(1 - t_{(OFFmax)} \times f_{(SWmax)}\right) \times \left(V_{I(min)} - I_{O(max)} \times 2 \times r_{DS(on)}\right) - I_{O(max)} \times \left(R_{(L)} + r_{DS(on)}\right)$$

where

- $V_{O(max)}$ = maximum achievable output voltage
- $t_{(OFFmax)}$ = maximum off-time (60 ns, typical)
- $f_{(SWmax)}$ = maximum switching frequency, including tolerance
- $V_{I(min)}$ = minimum input voltage
- $I_{O(max)}$ = maximum load current
- $r_{DS(on)}$ = maximum high-side MOSFET on-resistance (19 mΩ–30 mΩ)
- $R_{(L)}$ = series resistance of output inductor

(35)

8.2.2.8 Compensation

The industry uses several techniques to compensate dc-dc regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54388C-Q1 device. As a result of ignoring the slope compensation, the actual crossover frequency is usually lower than the crossover frequency used in the calculations.

To get started, calculate the modulator pole, $f_{(p,mod)}$, and the ESR zero, $f_{(z,mod)}$, using Equation 36 and Equation 37. For $C_{(OUT)}$, derating the capacitor is not necessary, as the 1.8-V output is a small percentage of the 10-V capacitor rating. If the output is a high percentage of the capacitor rating, use the manufacturer information for the capacitor to derate the capacitor value. Use Equation 38 and Equation 39 to estimate a starting point for the crossover frequency, $f_{(c)}$. For the example design, $f_{(p,mod)}$ is 6.03 kHz and $f_{(z,mod)}$ is 1210 kHz. Equation 38 is the geometric mean of the modulator pole and the ESR zero, and Equation 39 is the mean of the modulator pole and the switching frequency. Equation 38 yields 85.3 kHz and Equation 39 gives 54.9 kHz. Use the lower value of Equation 38 or Equation 39 as the approximate crossover frequency. For this example, $f_{(c)}$ is 56 kHz. Next, calculate the values of the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel with these two components forms the compensating pole (if needed).

$$f_{(p,mod)} = \frac{I_{O(max)}}{2\pi \times V_O \times C_{(OUT)}} \tag{36}$$

$$f_{(z,mod)} = \frac{1}{2\pi \times R_{(ESR)} \times C_{(OUT)}} \tag{37}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times f_{(z,mod)}} \tag{38}$$

$$f_{(c)} = \sqrt{f_{(p,mod)} \times \frac{f_{(SW)}}{2}} \tag{39}$$

The compensation design takes the following steps:

1. Set up the anticipated crossover frequency. Use Equation 40 to calculate the resistor value for the compensation network. In this example, the anticipated crossover frequency ($f_{(c)}$) is 56 kHz. The power-stage gain ($g_{m(ps)}$) is 25 S and the error-amplifier gain ($g_{m(ea)}$) is 245 µS.

$$R3 = \frac{2\pi \times f_{(c)} \times V_O \times C_{(OUT)}}{g_{m(ea)} \times V_{ref} \times g_{m(ps)}} \tag{40}$$

2. Place a compensation zero at the pole formed by the load resistor and the output capacitor. Calculate the capacitor for the compensation network using Equation 41.

$$C3 = \frac{R0 \times C0}{R3} \tag{41}$$

3. One can include an additional pole to attenuate high-frequency noise. In this application, the extra pole is not necessary.

From the procedures above, the compensation network includes a 7.68-kΩ resistor and a 3300-pF capacitor.

8.2.2.9 Power-Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous-conduction mode (CCM) operation. The power dissipation of the IC (P_T) includes conduction loss ($P_{(con)}$), dead-time loss ($P_{(d)}$), switching loss ($P_{(SW)}$), gate-drive loss ($P_{(gd)}$) and supply-current loss ($P_{(q)}$).

$$P_{(con)} = I_O^2 \times r_{DS(on)(Temp)}$$

where

- I_O is the output current (A)
- $r_{DS(on)(Temp)}$ is the on-resistance of the high-side MOSFET at a given temperature (Ω)

(42)

$$P_{(d)} = f_{(SW)} \times I_O \times 0.7 \times 60 \times 10^{-9}$$

where

- $f_{(SW)}$ is the switching frequency (Hz)

(43)

$$P_{(SW)} = 1/2 \times V_I \times I_O \times f_{(SW)} \times 8 \times 10^{-9}$$

where

- V_I is the input voltage (V)

(44)

$$P_{(gd)} = 2 \times V_I \times f_{(SW)} \times 2 \times 10^{-9}$$

(45)

$$P_{(q)} = V_I \times 515 \times 10^{-6}$$

(46)

Therefore:

$$P_T = P_{(con)} + P_{(d)} + P_{(SW)} + P_{(gd)} + P_{(q)}$$

(47)

For a given T_A, use Equation 48 to calculate the junction temperature.

$$T_J = T_A + R_{\theta JA} \times P_T$$

where

- T_J is the junction temperature (°C)
- T_A is the ambient temperature (°C)
- $R_{\theta JA}$ is the thermal resistance of the package (°C/W)
- P_T is the total device power dissipation (W)

(48)

For a given $T_{J(max)}$ = 150°C, use Equation 49 to calculate the maximum ambient temperature.

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} \times P_T$$

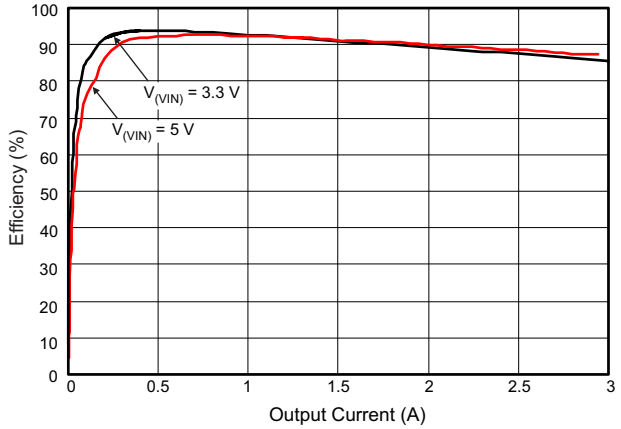
where

- $T_{J(max)}$ is maximum junction temperature (°C)
- $T_{A(max)}$ is maximum ambient temperature (°C)

(49)

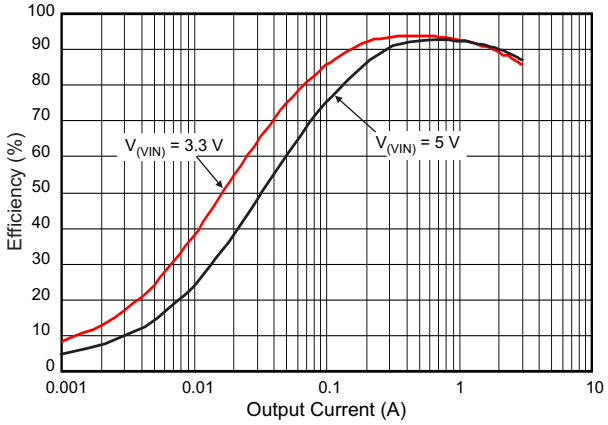
Additional power losses occur in the regulator circuit because of the inductor ac and dc losses and trace resistance that impact the overall efficiency of the regulator.

8.2.3 Application Curves



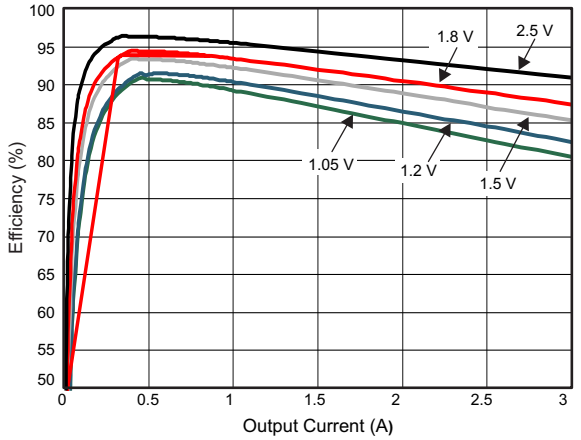
V_O = 1.8 V

Figure 35. Efficiency vs Load Current



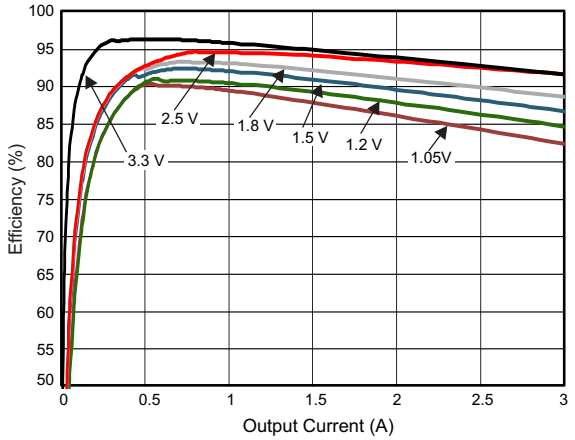
V_O = 1.8 V

Figure 36. Efficiency vs Load Current



$V_{(VIN)}$ = 3.3 V $f_{(SW)}$ = 1 MHz T_A = 25°C

Figure 37. Efficiency vs Load Current



$V_{(VIN)}$ = 5 V $f_{(SW)}$ = 1 MHz T_A = 25°C

Figure 38. Efficiency vs Load Current

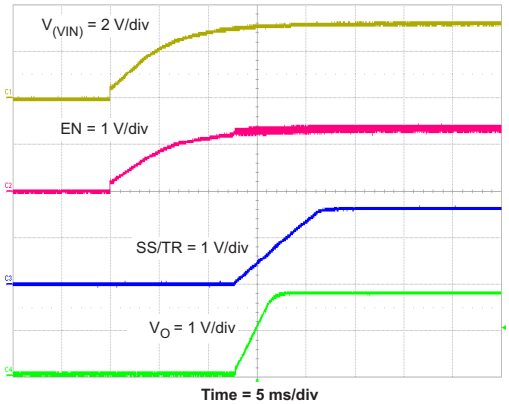


Figure 39. Power Up V_O, $V_{(VIN)}$

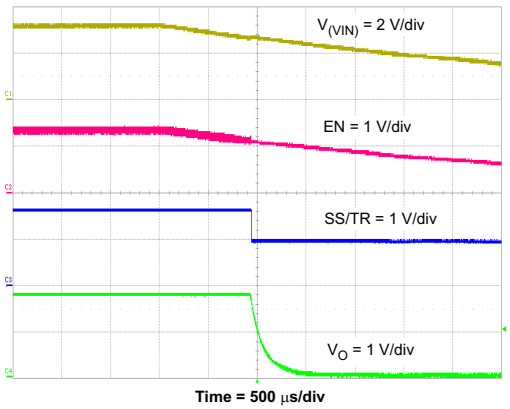


Figure 40. Power Down V_O, $V_{(VIN)}$

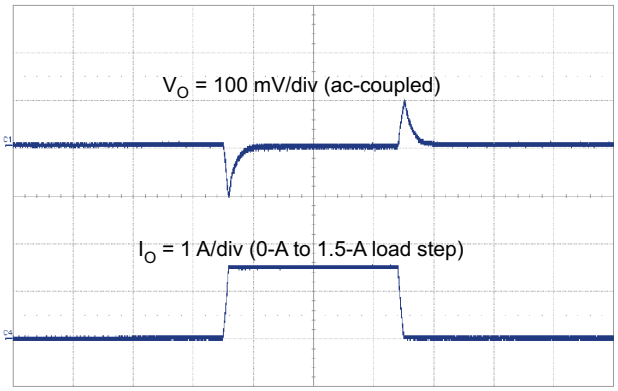


Figure 41. Transient Response, 1.5-A Step

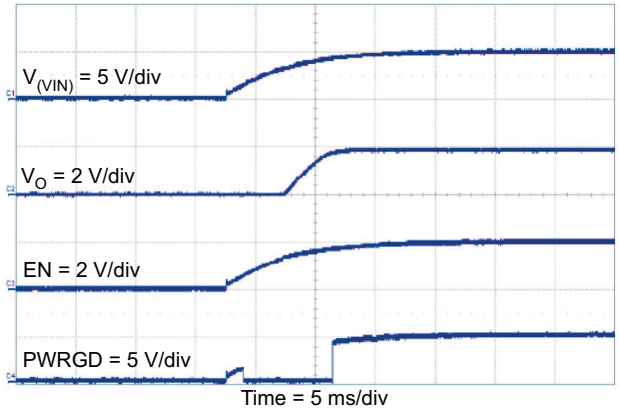


Figure 42. Power Up V_O, $V_{(VIN)}$

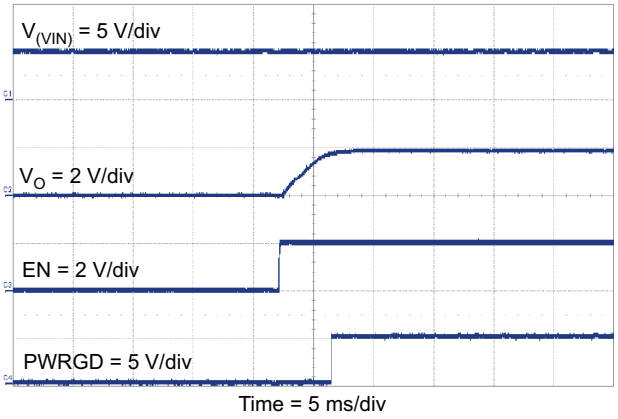


Figure 43. Power Up V_O, EN

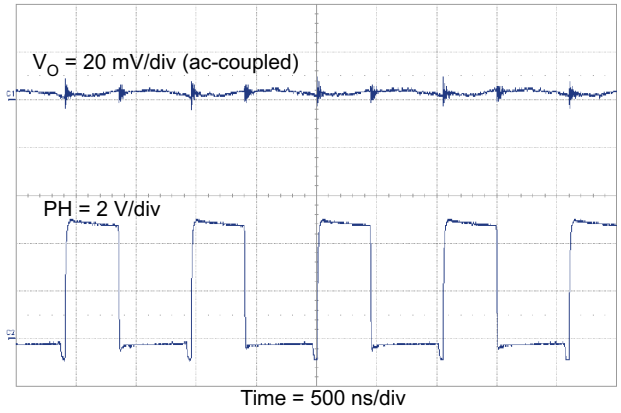


Figure 44. Output Ripple, 3 A

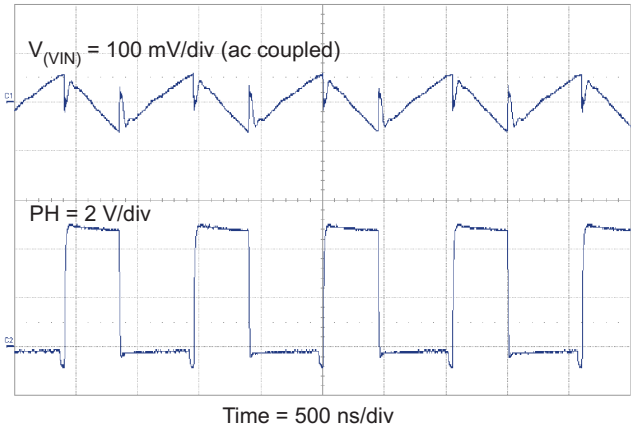


Figure 45. Input Ripple, 3 A

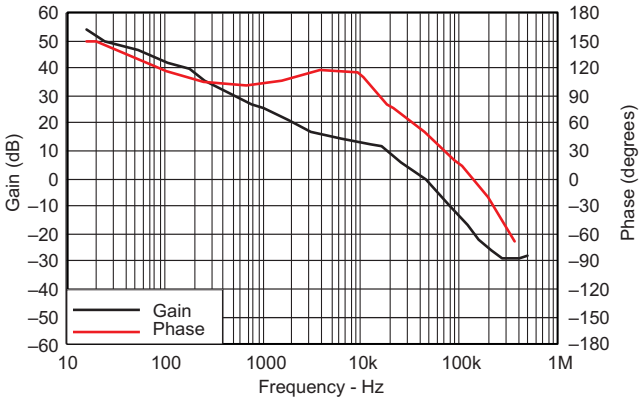


Figure 46. Closed-Loop Response

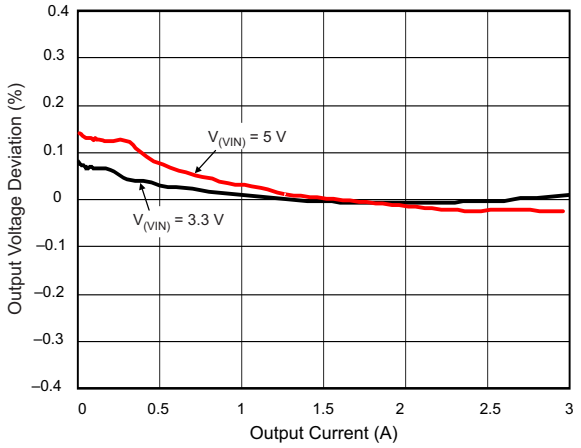


Figure 47. Load Regulation vs Load Current

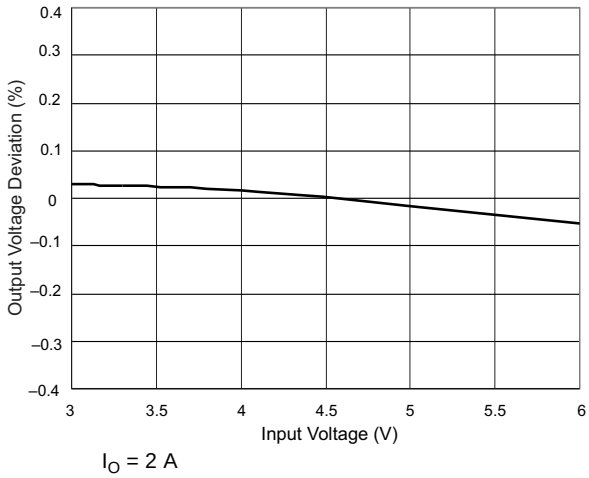


Figure 48. Regulation vs Input Voltage

9 Power Supply Recommendations

By design, the TPS54388C-Q1 device works with an analog supply voltage range of 2.95 V to 6 V. Ensure good regulation for the input supply, and connect the supply to the VIN pins with the appropriate input capacitor as calculated in the *Input Capacitor* section. If the input supply is located more than a few inches from the TPS54388C-Q1 device, the design may require extra capacitance in addition to the recommended value.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power-supply design. The signal paths, which conduct fast-changing currents or voltages, can interact with stray inductance or parasitic capacitance in several ways to generate noise or degrade the power-supply performance. Take care to minimize the loop area formed by the bypass-capacitor connections and the VIN pins. See Figure 49 for a PCB layout example. Tie the GND pins and AGND pin directly to the thermal pad under the IC. Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. Use additional vias to connect the top-side ground area to any internal planes near the input and output capacitors. For operation at full-rated load, the top-side ground area, along with any additional internal ground planes, must provide adequate heat-dissipating area.

Locate the input bypass capacitor as close to the IC as possible. Route the PH pin to the output inductor. Because the PH connection is the switching node, locate the output inductor close to the PH pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. Also. locate the boot capacitor close to the device. Connect the sensitive analog ground connections for the feedback voltage divider, compensation components, slow-start capacitor, and frequency-set resistor to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise, so locate the Rt resistor as close as possible to the IC, and connect it with minimal lengths of trace. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternative PCB layouts. However, this layout, meant as a guideline, produces good results.

10.2 Layout Example

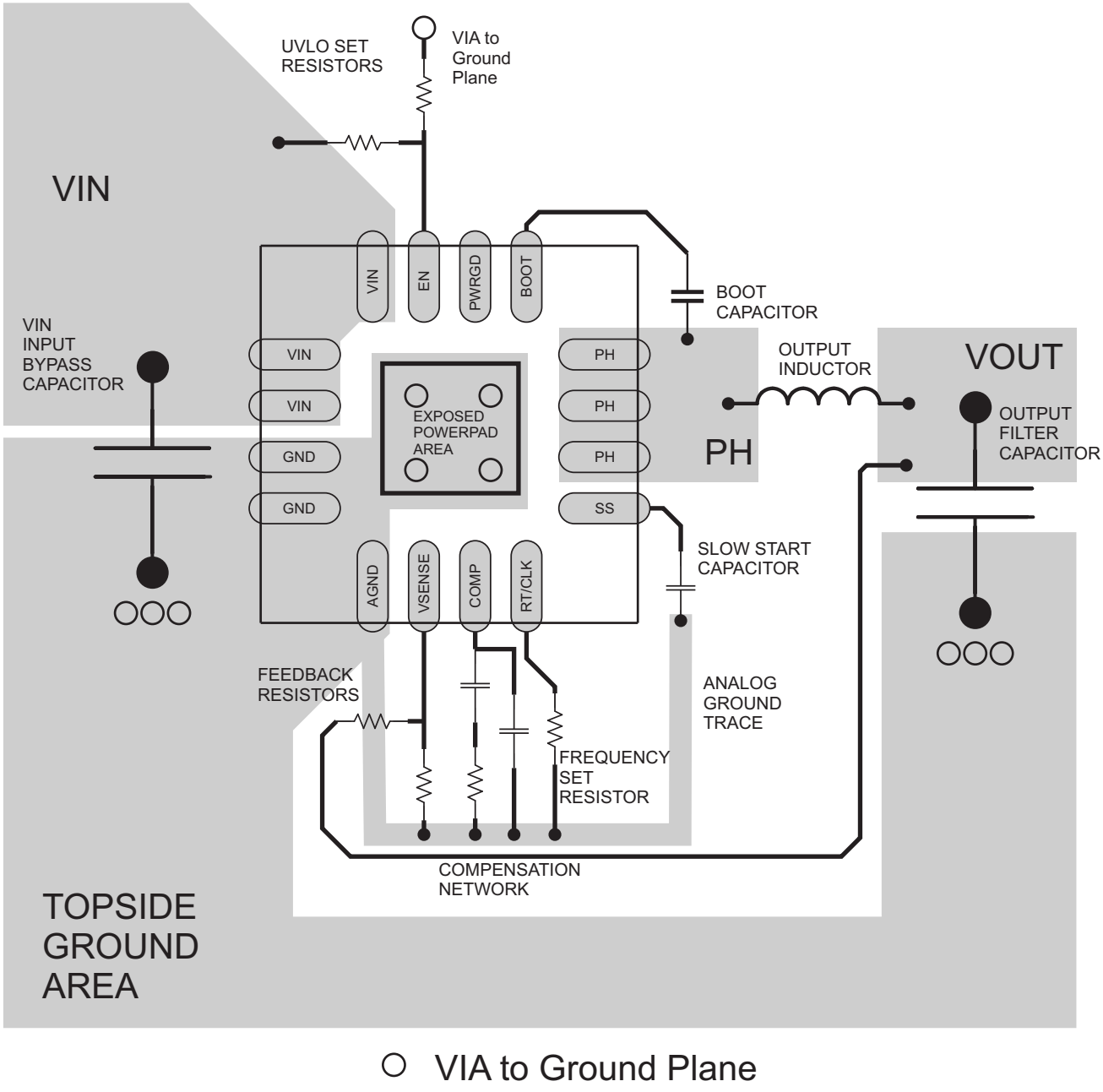


Figure 49. PCB Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

For related documentation, see the following:

- *Enable Functionality and Adjusting Undervoltage Lockout for TPS57112-Q1* (SLVA784)
- *Interfacing TPS57xxx-Q1,TPS65320-Q1 Family, and TPS65321-Q1 Devices With Low Impendence External Clock Drivers* (SLVA755)
- *TPS57112-Q1 High Frequency (2.35 MHz) Operation* (SLVA743)
- *TPS54388EVM User's Guide* (SLVU962)
- *TPS54388-Q1 Pin Open and Short Test Results* (SLVA581)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

E2E is a trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54388CQRTERQ1	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	5438Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

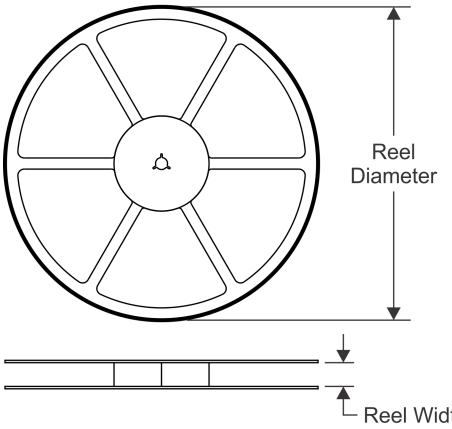
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

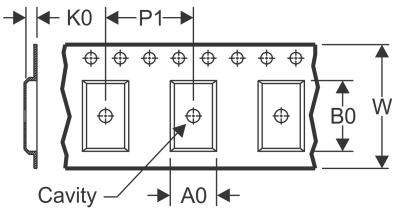
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

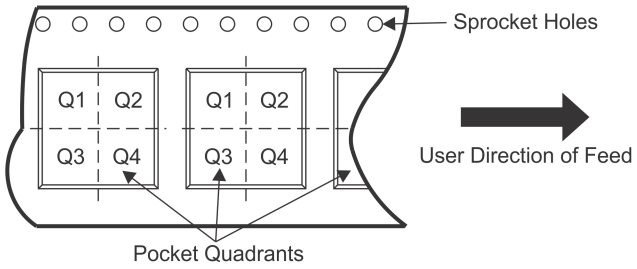


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

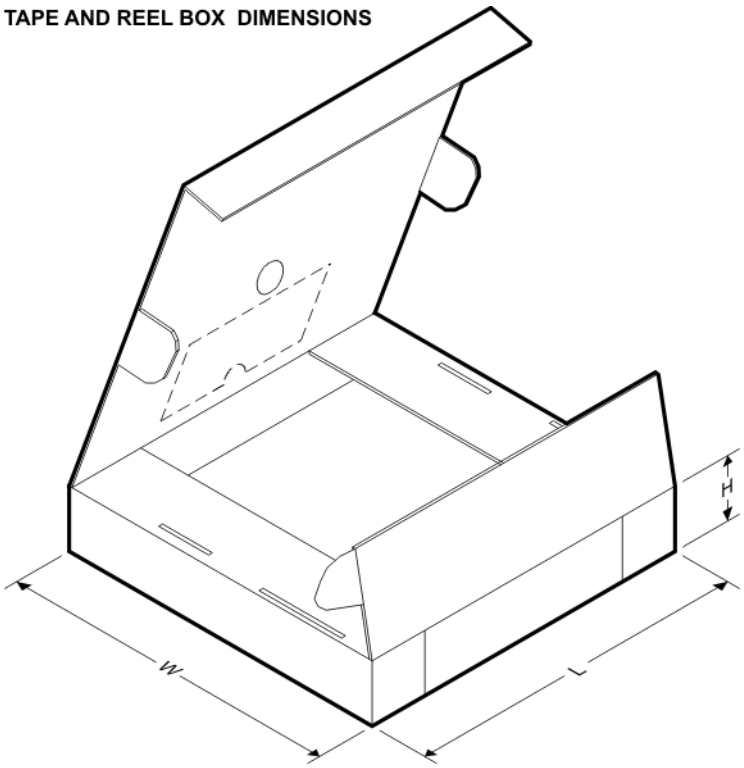
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54388CQRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

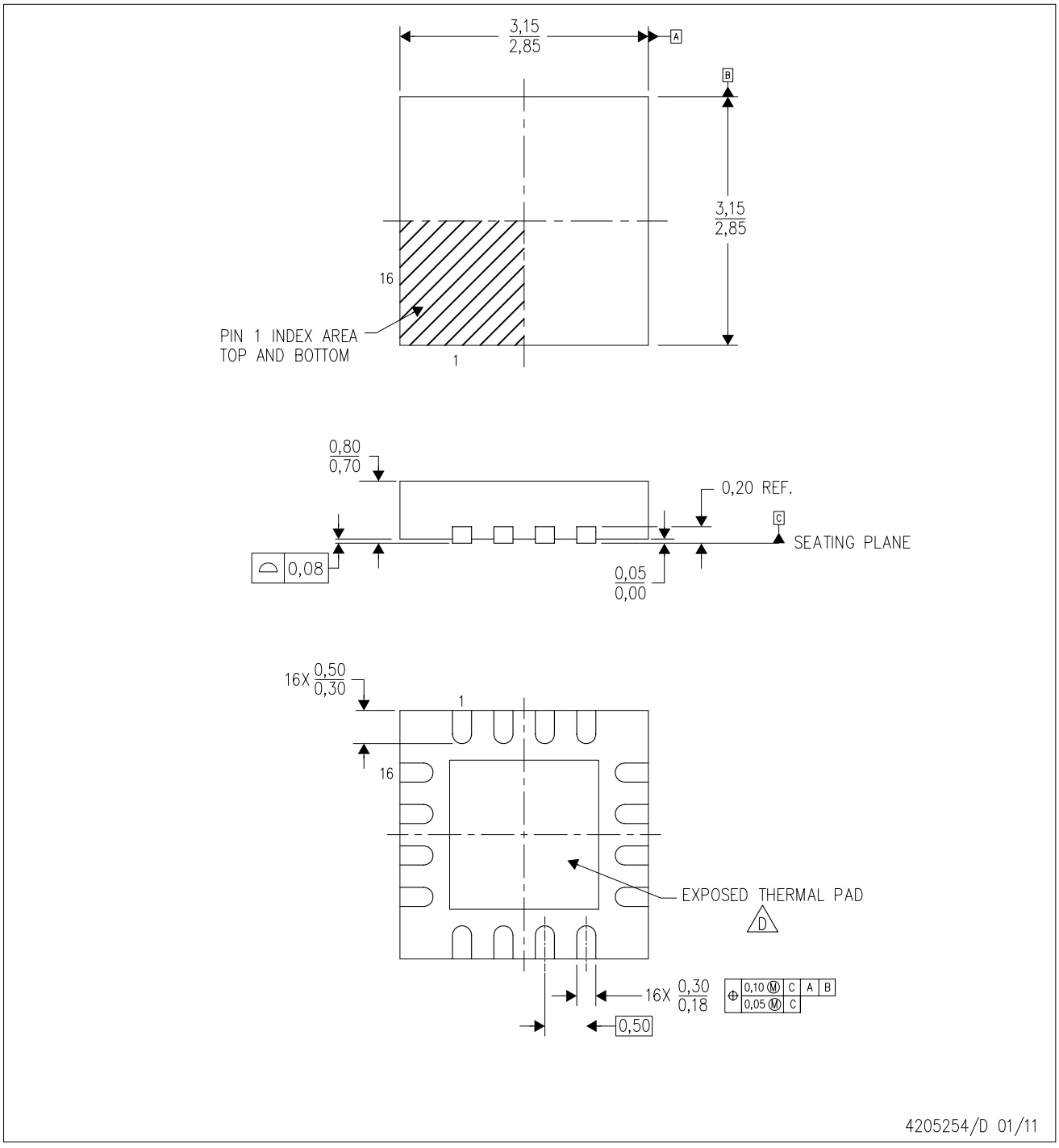
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54388CQRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

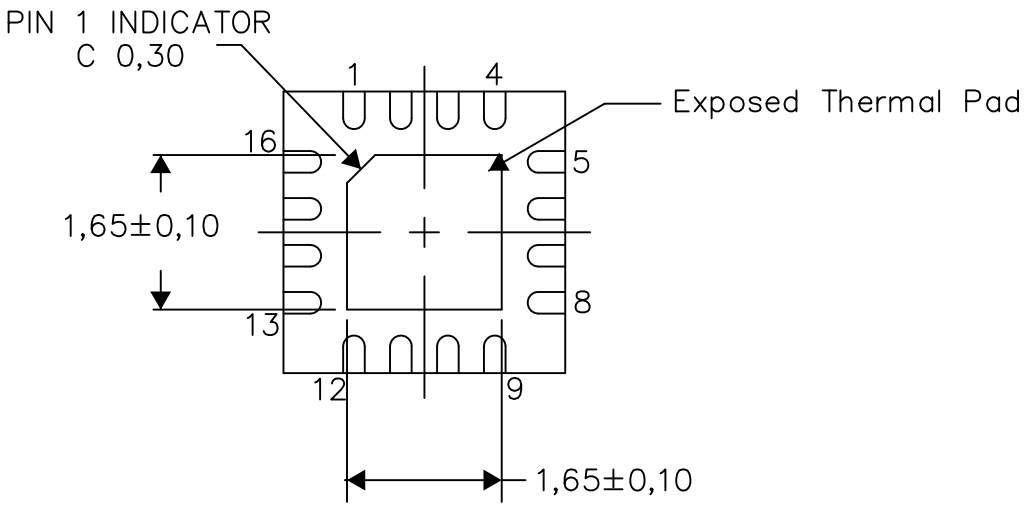
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



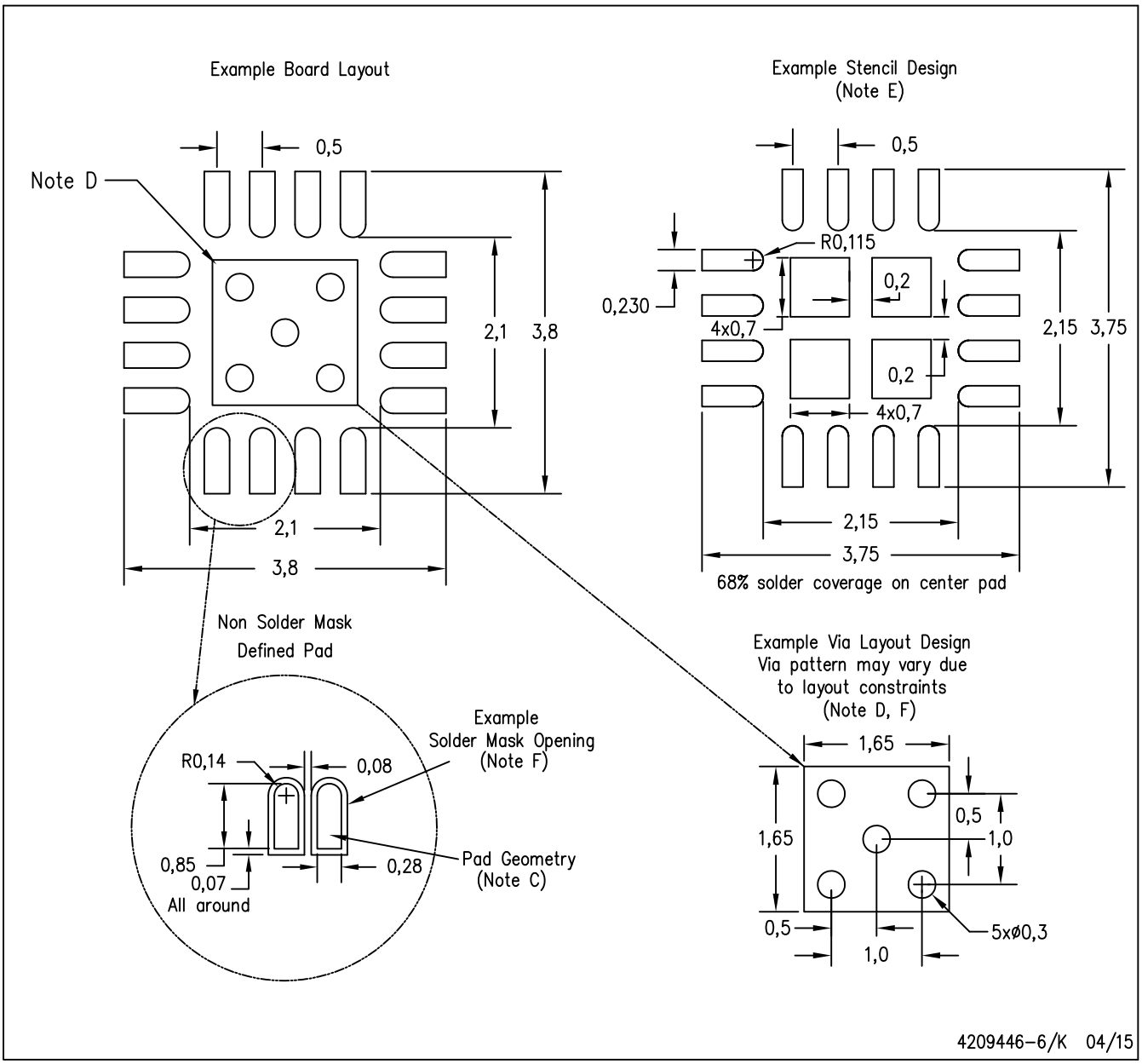
Bottom View

Exposed Thermal Pad Dimensions

4206446–4/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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