2-A 60-V STEP-DOWN DC/DC CONVERTER WITH LOW QUIESCENT CURRENT

Check for Samples: TPS54262-Q1

FEATURES

- **Asynchronous Switch Mode Regulator**
- **3.6 V to 48 V Operating Range, Withstands Transients up to 60 V**
- **2 A Maximum Load Current**
- **50 µA Typical Quiescent Current**
- **200 kHz to 2.2 MHz Switching Frequency**
- **0.8 V ± 1.5% Voltage Reference**
- **High Voltage Tolerant Enable Input**
- **Soft Start on Enable Cycle**
- **Slew Rate Control on Internal Power Switch**
- **Low-Power Mode for Light Load Conditions**
- **Programmable Delay for Power-On Reset**
- **External Compensation for Error Amplifier**
- **Reset Function Filter Time for Fast Negative Transients**
- **Programmable Overvoltage, Undervoltage Output Monitor**
- **Thermal Sensing and Shutdown**
- **Switch Current Limit Protection**
- **Short Circuit and Overcurrent Protection of FET**
- **Junction Temperature Range: –40°C to 150°C**
- **20-Pin HTSSOP PowerPAD™ Package**

APPLICATIONS

- **Qualified for Automotive Applications**
- **Automotive Telematics**
- **Navigation Systems**
- **In-Dash Instrumentation**
- **Battery Powered Applications**

DESCRIPTION

The TPS54262 is a step-down switch-mode power supply with a voltage supervisor and an integrated NMOS switching FET. Integrated input voltage line feed forward topology improves line transient regulation of the voltage mode buck regulator. The regulator has a cycle-by-cycle current limit. The device also features low-power mode operation under light load conditions which reduces the supply current to 50 µA (typical). By pulling the EN pin low, the supply shutdown current is reduced to 1 µA (typical).

An open drain reset signal indicates when the nominal output drops below the reset threshold set by an external resistor divider network. The output voltage start up ramp is controlled by a soft start capacitor. There is an internal undervoltage shut down which is activated when the input supply ramps down to 2.6 V. The device is protected during an overload condition on output by frequency foldback operation, and also has a thermal shutdown protection.

TYPICAL APPLICATION

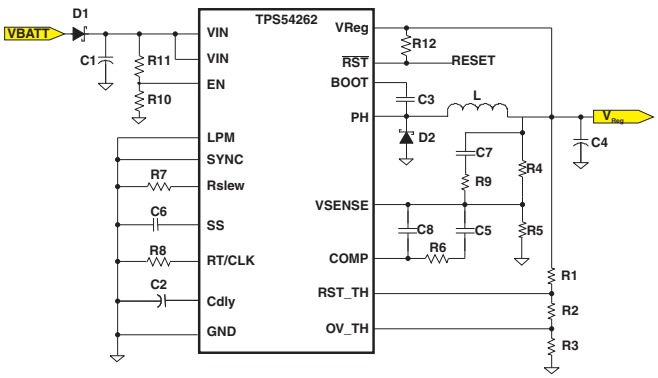


Figure 1.

TYPICAL CONVERTER EFFICIENCY

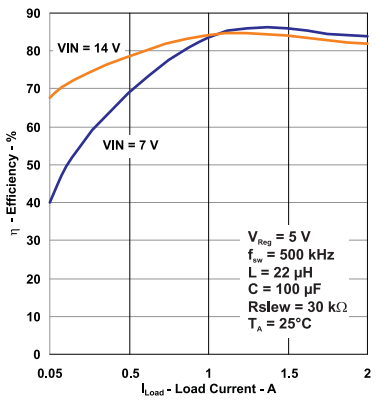


Figure 2.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 150°C	TSSOP – PWP	Reel of 2000	TPS54262QPWPRQ1	54262Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Input voltage	EN	-0.3 to 60	V
	VIN	-0.3 to 60	
	VReg	-0.3 to 20	
	LPM	-0.3 to 5.5	
	OV_TH	-0.3 to 5.5	
	RST_TH	-0.3 to 5.5	
	SYNC	-0.3 to 5.5	
	VSENSE	-0.3 to 5.5	
Output voltage	BOOT	-0.3 to 65	V
	PH	-0.3 to 60	
		-2 for 30ns	
		-1 for 200ns	
		-0.85 at T_J= -40°C	
		-0.5 at T_J= 125°C	
	RT	-0.3 to 5.5	
	$\overline{RST}$	-0.3 to 5.5	
	Cdly	-0.3 to 8	
	SS	-0.3 to 8	
	COMP	-0.3 to 7	
Temperature	Operating virtual junction temperature range, T_J	-40 to 150	°C
	Storage temperature range, T_S	-55 to 165	
Electrostatic discharge (HBM)(2)		2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to ground.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Unregulated buck supply input voltage (VIN, EN)		3.6	48	V
V_{Reg}	Regulated output voltage	In continuous conduction mode (CCM)	0.9	18	V
		Power up in low-power mode (LPM) or discontinuous conduction mode (DCM)	0.9	5.5	V
	Bootstrap capacitor (BOOT)		3.6	56	V
	Switched outputs (PH)		3.6	48	V
	Logic levels ($\overline{RST}$, VSENSE, OV_TH, RST_TH, Rslew, SYNC, RT)		0	5.25	V
	Logic levels (SS, Cdly, COMP)		0	6.5	V
θ_{JA}	Thermal resistance, junction to ambient(1)			35	°C/W
θ_{JC}	Thermal resistance, junction to case(2)			10	°C/W
T_J	Operating junction temperature(3)		–40	150	°C

(1) This assumes a JEDEC JESD 51-5 standard board with thermal vias with High K profile – See PowerPAD section and application note from Texas Instruments (SLMA002) for more information.
(2) This assumes junction to exposed thermal pad.
(3) This assumes $T_A = T_J$ – power dissipation × θ_{JA}.

DC ELECTRICAL CHARACTERISTICS

VIN = 7 V to 48 V, EN = VIN, T_J = –40°C to 150°C (unless otherwise noted)

TEST	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT POWER SUPPLY								
Info	VIN	Supply voltage on VIN	Normal mode: after initial start up		3.6		48	V
			Low-power mode	Falling threshold (LPM disabled)		8		V
				Rising threshold (LPM activated)		8.5		V
				High voltage threshold (LPM disabled)	29	31	34	V
PT	$I_{q\text{-Normal}}$	Quiescent current, normal mode	Open loop test – maximum duty cycle VIN = 7 V to 48 V			5	10	mA
PT	$I_{q\text{-LPM}}$	Quiescent current, low-power mode	I_{Load} < 1 mA, VIN = 12 V	T_A = 25°C		50	70	µA
				–40 < T_J < 150°C			75	µA
			I_{Load} < 1 mA, VIN = 24 V	T_A = 25°C			75	µA
				–40 < T_J < 150°C			75	µA
PT	I_{SD}	Shutdown current	EN = 0 V, device is off	T_A = 25°C, VIN = 12 V		1	4	µA
TRANSITION TIMES (LOW POWER – NORMAL MODES)								
CT	t_{d1}	Transition delay, normal mode to low-power mode	VIN = 12 V, V_{Reg} = 5 V, I_{Load} = 1 A to 1 mA			100		µs
CT	t_{d2}	Transition delay, low-power mode to normal mode	VIN = 12 V, V_{Reg} = 5 V I_{Load} = 1 mA to 1 A			5		µs
SWITCH MODE SUPPLY; V_{Reg}								
Info	V_{Reg}	Regulator output	VSENSE = 0.8 V_{ref}		0.9		18	V
CT	VSENSE	Feedback voltage	V_{Reg} = 0.9 V to 18 V (open loop)		0.788	0.8	0.812	V
PT	$R_{DS(ON)}$	Internal switch resistance	Measured across VIN and PH, I_{Load} = 500 mA				500	mΩ
Info	I_{CL}	Switch current limit, cycle by cycle	VIN = 12 V		2.5	3.2	4.1	A
Info	$t_{ON\text{-Min}}$	Duty cycle pulse width	Bench CHAR only		50	100	150	ns
Info	$t_{OFF\text{-Min}}$		Bench CHAR only		100	200	250	
PT	f_{sw}	Switching frequency	Set using external resistor on RT pin		0.2		2.2	MHz
PT	f_{sw}	Internal oscillator frequency tolerance			–10		10	%
Info	I_{Sink}	Start-up condition	OV_TH = 0 V, V_{Reg} = 10 V				1	mA
Info	I_{Limit}	Prevent overshoot	0 V < OV_TH < 0.8 V, V_{Reg} = 10 V				80	mA

PT: Production tested
CT: Characterization tested only, not production tested
Info: User information only, not production tested

DC ELECTRICAL CHARACTERISTICS

VIN = 7 V to 48 V, EN = VIN, T_J = –40°C to 150°C (unless otherwise noted)

TEST	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE (EN)							
PT	V_{IL}	Low input threshold voltage				0.7	V
PT	V_{IH}	High input threshold voltage		1.7			V
PT	I_{lkg}	Leakage current into EN terminal	EN = 60 V		100	135	µA
			EN = 12 V		8	15	µA
RESET DELAY (Cdly)							
PT	I_O	External capacitor charge current	EN = high	1.4	2	2.6	µA
PT	$V_{Threshold}$	Switching threshold voltage	Output voltage in regulation		2		V
LOW-POWER MODE (LPM)							
PT	V_{IL}	Low input threshold voltage	VIN = 12 V			0.7	V
PT	V_{IH}	High input threshold voltage	VIN = 12 V	1.7			V
PT	I_{lkg}	Leakage current into LPM terminal	LPM = 5 V		65	95	µA
RESET OUTPUT ($\overline{RST}$)							
PT	t_{rdly}	POR delay timer	Based on Cdly capacitor	3.6		7	ms/nF
PT	VReg_RST	Reset threshold voltage for V_{Reg}	Check RST output	0.768		0.832	V
PT	$t_{nRSTdly}$	Filter time	Delay before $\overline{RST}$ is asserted low	10	20	35	µs
SOFT START (SS)							
PT	I_{SS}	Soft-start source current		40	50	60	µA
SYNCHRONIZATION (SYNC)							
PT	V_{IL}	Low input threshold voltage				0.7	V
PT	V_{IH}	High input threshold voltage		1.7			V
PT	I_{lkg}	Leakage current	SYNC = 5 V		65	95	µA
CT	SYNC (f_{ext})	External input clock frequency	VIN = 12 V, V_{Reg} = 5 V, 180 kHz < f_{sw} < f_{ext} < 2 × f_{sw} < 2.2 MHz	180		2200	kHz
Info	$SYNC_{trans}$	External clock to internal clock	No external clock, VIN = 12 V, V_{Reg} = 5 V		32		µs
Info	$SYNC_{trans}$	Internal clock to external clock	External clock = 1 MHz, VIN = 12 V, V_{Reg} = 5 V		2.5		µs
CT	$SYNC_{CLK}$	Minimum duty cycle		30			%
CT	$SYNC_{CLK}$	Maximum duty cycle				70	%
Rslew							
CT	I_{Rslew}	Rslew = 50 kΩ			20		µA
CT	I_{Rslew}	Rslew = 10 kΩ			100		µA
OVERVOLTAGE SUPERVISORS (OV_TH)							
PT	VReg_OV	Threshold voltage for V_{Reg} during overvoltage	Internal switch is turned off	0.768		0.832	V
		V_{Reg} = 5 V	Internal pulldown on V_{Reg}, OV_TH = 1 V		70 (1)		mA
THERMAL SHUTDOWN							
CT	T_{SD}	Thermal shutdown junction temperature			175		°C
CT	T_{HYS}	Hysteresis			30		°C

PT: Production tested

CT: Characterization tested only, not production tested

(1) This is the current flowing into the VReg pin when voltage at OV_TH pin is 1 V.

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)

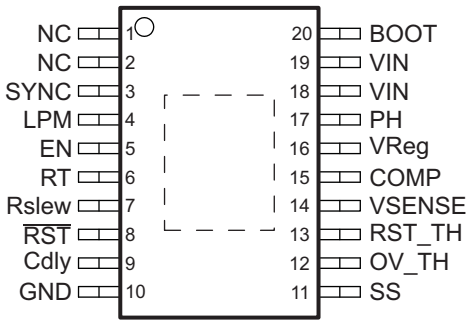


Figure 3.

TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
NC	1	NC	Connect to ground.
NC	2	NC	Connect to ground.
SYNC	3	I	External synchronization clock input to override the internal oscillator clock. An internal pull down resistor of 62kΩ (typical) is connected to ground.
LPM	4	I	Low-power mode control using digital input signal. An internal pull down resistor of 62kΩ (typical) is connected to ground.
EN	5	I	Enable pin, internally pulled up. Must be externally pulled up or down to enable/ disable the device.
RT	6	O	External resistor to ground to program the internal oscillator frequency.
Rslew	7	O	External resistor to ground to control the slew rate of internal switching FET.
$\overline{\text{RST}}$	8	O	Active low, open drain reset output connected to external bias voltage through a resistor, asserted high after the device starts regulating.
Cdly	9	O	External capacitor to ground to program power on reset delay.
GND	10	O	Ground pin, must be electrically connected to the exposed pad on the PCB for proper thermal performance.
SS	11	O	External capacitor to ground to program soft start time.
OV_TH	12	I	Sense input for overvoltage detection on regulated output, an external resistor network is connected between VReg and ground to program the overvoltage threshold.
RST_TH	13	I	Sense input for undervoltage detection on regulated output, an external resistor network is connected between VReg and ground to program the reset and undervoltage threshold.
VSENSE	14	I	Inverting node of error amplifier for voltage mode control.
COMP	15	O	Error amplifier output to connect external compensation components.
VReg	16	I	Internal low-side FET to load output during startup or limit overshoot.
PH	17	O	Source of the internal switching FET.
VIN	18	I	Unregulated input voltage. Pin 18 and pin 19 must be connected externally.
VIN	19	I	Unregulated input voltage. Pin 18 and pin 19 must be connected externally.
BOOT	20	O	External bootstrap capacitor to PH to drive the gate of the internal switching FET.

FUNCTIONAL BLOCK DIAGRAM

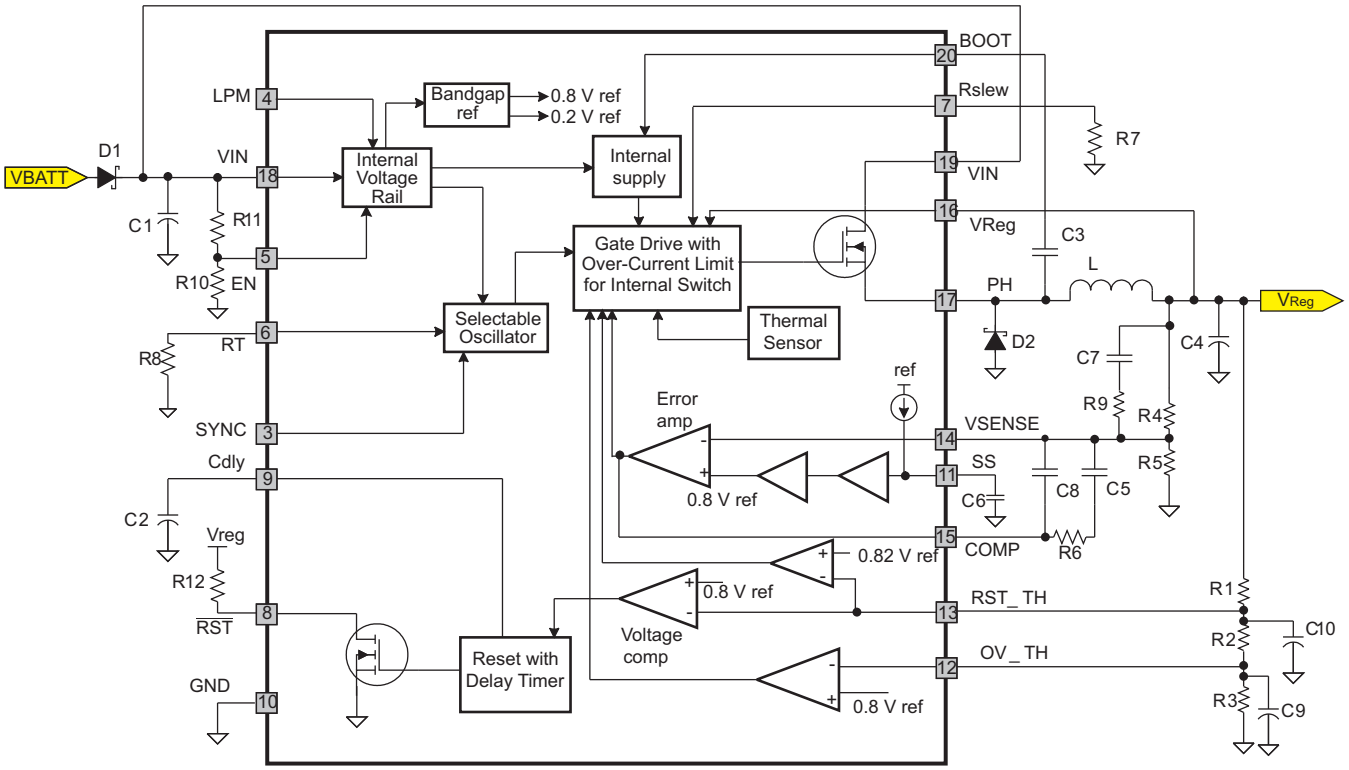


Figure 4.

TYPICAL CHARACTERISTICS

Efficiency Data of Power Supply

FET SWITCHING

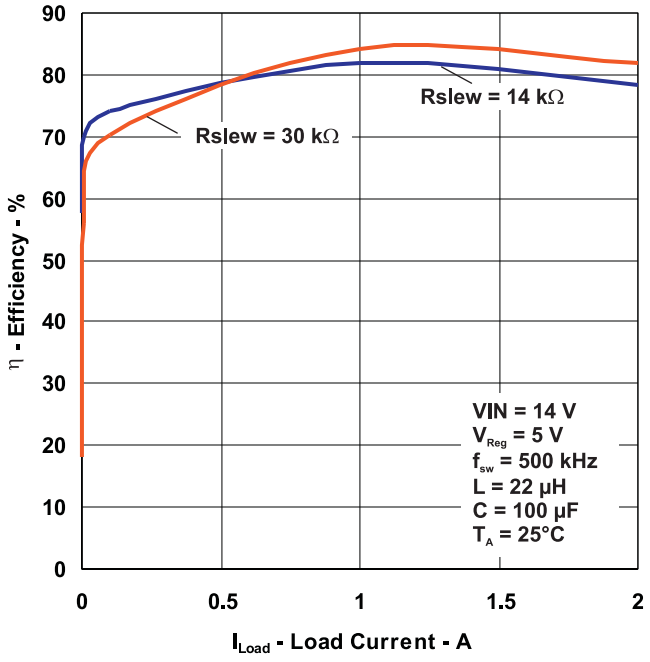


Figure 5.

FAST SLEW RATE ON SWITCHING FET

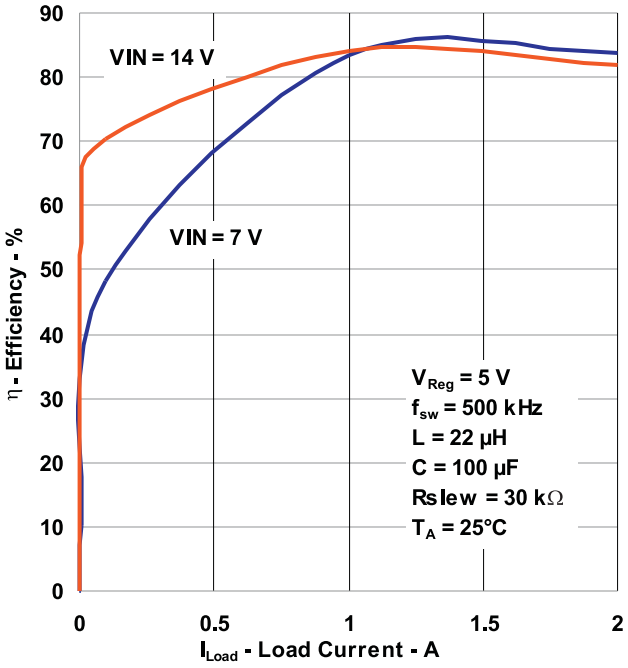


Figure 6.

LPM, QUIESCENT CURRENT VARIATION WITH TEMPERATURE

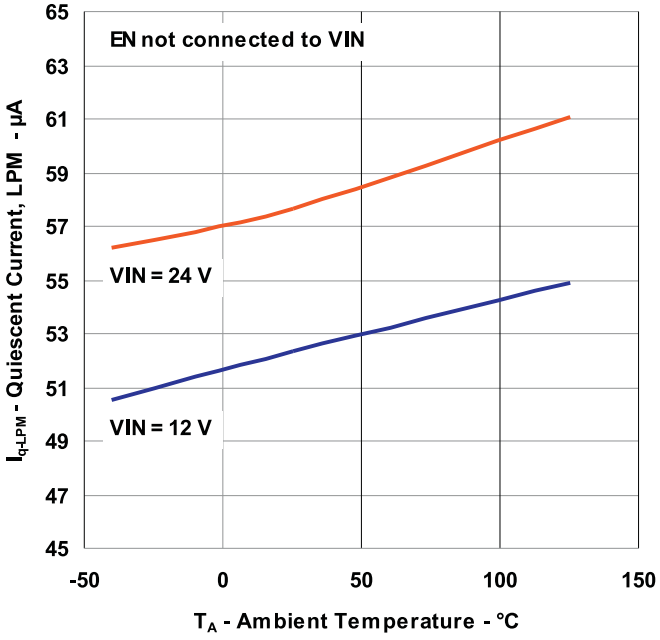


Figure 7.

SHUTDOWN CURRENT VARIATION WITH TEMPERATURE

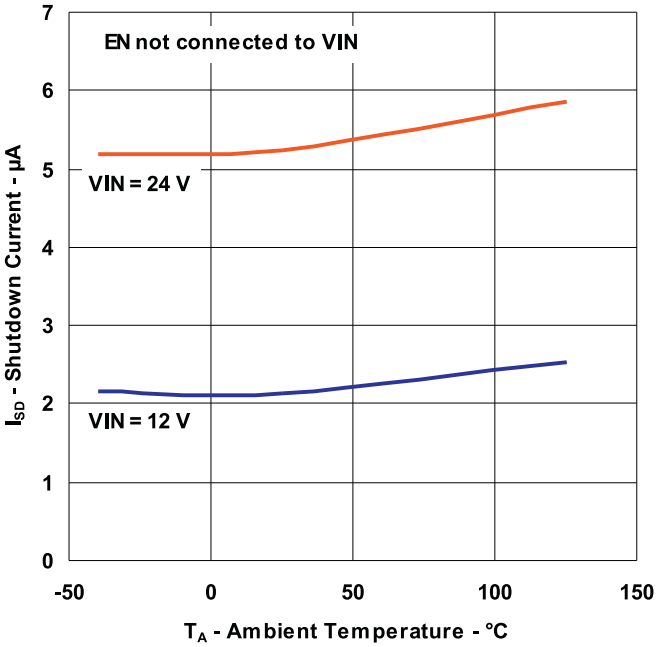


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Output Voltage Drop Out

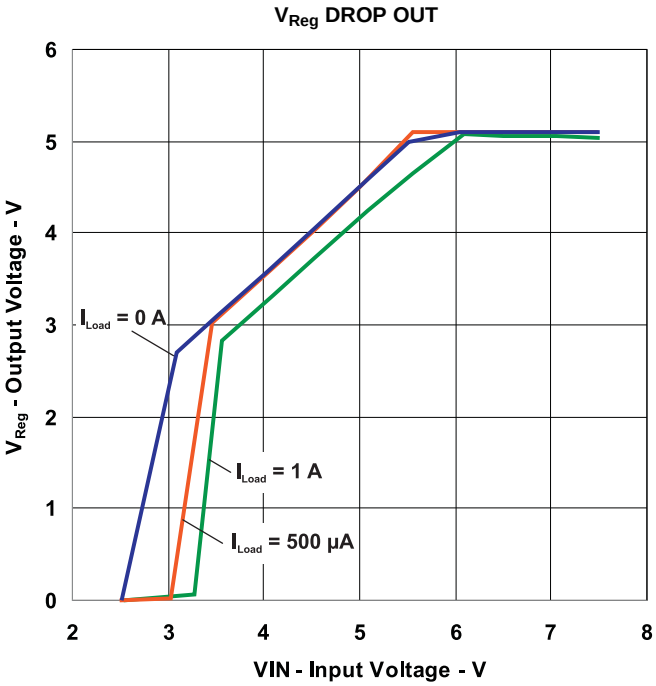


Figure 9.

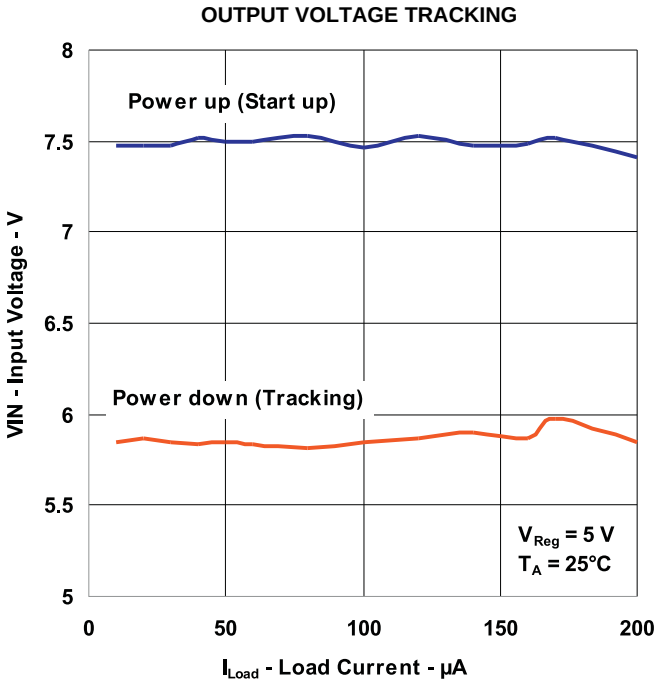


Figure 10.

NOTE

- Power up (Start up): This curve shows the input voltage required to achieve the 5 V regulation during power up over the range of load currents (see Figure 10).
- Power down (Tracking): This curve shows the input voltage at which the output voltage drops approximately by 0.7 V from the programmed 5 V regulated voltage (see Figure 10) or for low input voltages (tracking function) over the range of load currents (see Figure 9).
- In Figure 5 and Figure 6, L and C are output inductor and capacitor respectively.

TYPICAL CHARACTERISTICS (continued)

INTERNAL REFERENCE VOLTAGE

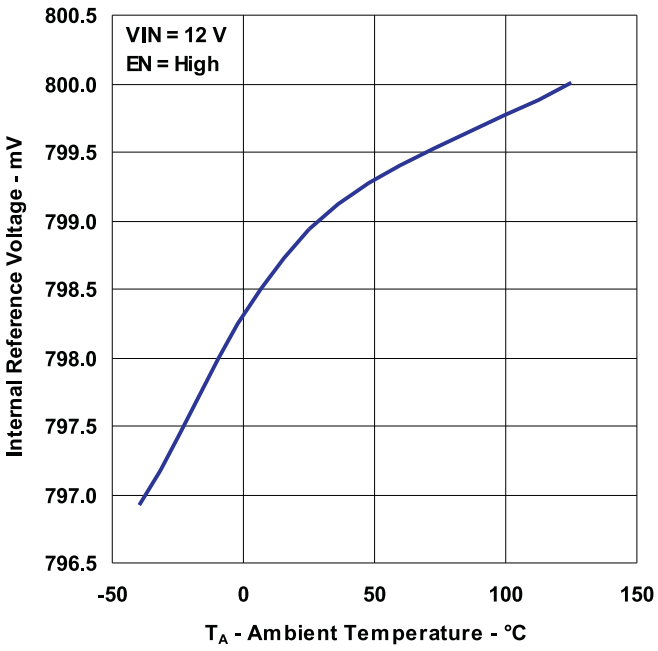


Figure 11.

VOLTAGE DROP ON Rslew FOR CURRENT REFERENCE; (SLEW RATE / Rslew)

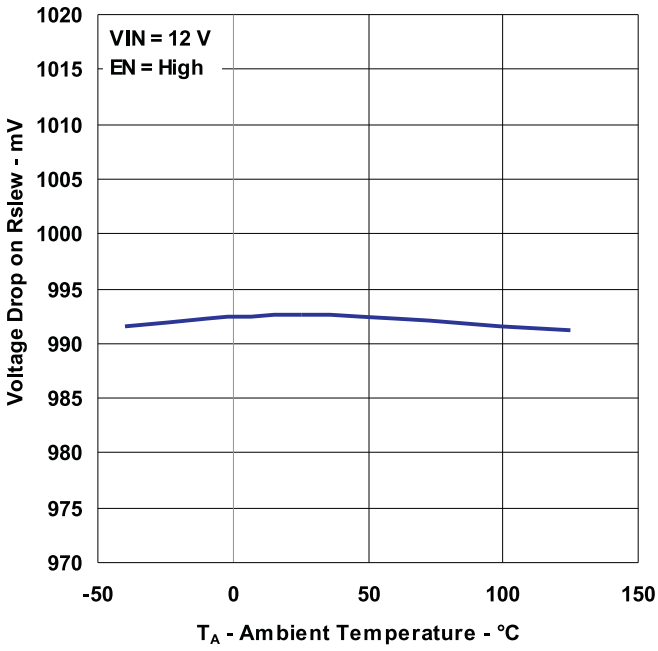


Figure 12.

CURRENT CONSUMPTION WITH TEMPERATURE

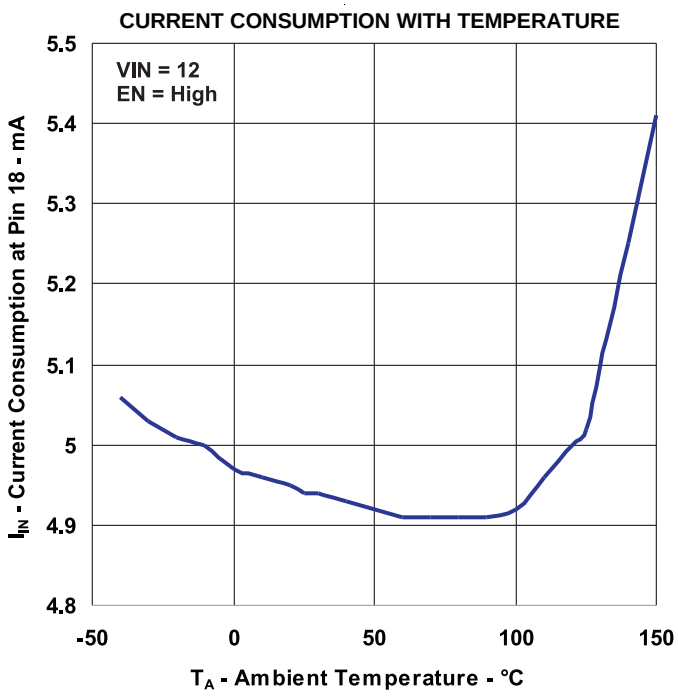


Figure 13.

OVERVIEW

The TPS54262 is a 60 V, 2 A DC/DC step down (buck) converter using voltage-control mode scheme. The device features supervisory function for power-on-reset during system power on. Once the output voltage has exceeded the threshold set by RST_TH pin, a delay of 1 ms/nF (based on capacitor value on Cdly terminal) is invoked before the $\overline{\text{RST}}$ line is released high. Conversely on power down, once the output voltage falls below the same set threshold, the $\overline{\text{RST}}$ line is pulled low only after a de-glitch filter of approximately 20 µs (typical) expires. This is implemented to prevent reset from being triggered due to fast transient line noise on the regulated output supply.

An overvoltage monitor function, is used to limit regulated output voltage to the threshold set by OV_TH pin. Both the RST_TH and OV_TH monitoring voltages are set to be a pre-scale of the output voltage, and thresholds based on the internal bias voltages of the voltage comparators (0.8 V typical).

Detection of undervoltage on the regulated output is based on the RST_TH setting and will invoke $\overline{\text{RST}}$ line to be asserted low. Detection of overvoltage on the output is based on the OV_TH setting and will not invoke the $\overline{\text{RST}}$ line to be asserted low. However, the internal switch is commanded to turn OFF.

In systems where power consumption is critical, low-power mode (LPM) is implemented to reduce the non-switching quiescent current during light load conditions. After the device has been operating in discontinuous conduction mode (DCM) for at least 100 µs (typ), depending upon the load current, it may enter in pulse skip mode (PSM). The operation of when the device enters DCM is dependent on the selection of the external components.

If thermal shutdown is invoked due to excessive power dissipation, the internal switch is disabled and the regulated output voltage starts to decrease. Depending on the load current, the regulated output voltage could decay and the RST_TH threshold may assert the $\overline{\text{RST}}$ output low.

DETAILED DESCRIPTION

The TPS54262 is a DC/DC converter using a voltage-control mode scheme with an input voltage feed-forward technique. The device can be programmed for a range of output voltages with a wide input voltage range. Below are details with regard to setting up the device, detailed functionality and the modes of operation.

Unregulated Input Voltage

The input voltage is supplied through VIN pins (pin 18 and 19) which must be externally protected against voltage levels greater than 60 V and reverse input polarity. An external diode is connected to protect these pins from reverse input polarity. The input current drawn from this pin is pulsed, with fast rise and fall times. Therefore, this input line requires a filter capacitor to minimize noise. Additionally, for EMI considerations, an input filter inductor may also be required.

NOTE

For design considerations, VIN/V_{Reg} ratios should always be set such that the minimum required duty cycle pulse ($t_{ON\text{-}Min}$) is greater than 150 ns. The minimum off time ($t_{OFF\text{-}Min}$) is 250 ns for all conditions.

Regulated Output Voltage

The regulated output voltage (V_{Reg}) is fed back to the device through VReg pin (pin 16). Typically, an output capacitor of value within range of 10 µF to 400 µF is connected at this pin. It is also recommended to use a filter capacitor with low ESR characteristics to minimize ripple in regulated output voltage. The VReg pin is also internally connected to a load of ~100 Ω, which is turned ON in the following conditions:

- During startup condition, when the device is powered up with no-load, or whenever EN is toggled, the internal load connected to VReg pin is turned ON to charge the bootstrap capacitor to provide gate drive voltage to the switching transistor.
- During normal operating conditions, when the regulated output voltage (V_{Reg}) exceeds the overvoltage threshold (VReg_OV, preset by external resistors R1, R2, and R3), the internal load is turned ON, and this pin is pulled down to bring the regulated output voltage down.

- When VIN is less than typical VIN falling threshold level while LPM is disabled. From device specifications, VIN typical falling threshold (LPM disabled) = 8 V (see *DC Electrical Characteristics*).
- When $\overline{RST}$ is low.

Regulation/Feedback Voltage

The regulated output voltage (V_{Reg}) can be programmed by connecting external resistor network at VSENSE pin (pin 14). The output voltage is selectable between 0.9 V to 18 V according to the following relationship:

$$V_{Reg} = V_{ref}\left(1 + \frac{R4}{R5}\right) \quad (1)$$

Where,

R4, R5 = feedback resistors (see Figure 4)

V_{ref} = 0.8 V (typical)

The overall tolerance of the regulated output voltage is given by Equation 2.

$$tol_{VReg} = tol_{Vref} + \frac{R4}{R4 + R5} \times (tol_{R4} + tol_{R5}) \quad (2)$$

Where,

tol_{Vref} = tolerance of internal reference voltage (tol_{Vref} = ± 1.5%)

tol_{R4},tol_{R5} = tolerance of feedback resistors R4, R5

For a tighter tolerance on V_{Reg}, lower-value feedback resistors can be selected. However, for proper operation in low-power mode (see *Modes of Operation*), it is recommended to keep R4 + R5 around 250 kΩ (typical).

The output tracking depends upon the loading conditions and is explained in Table 1 and is shown in Figure 10.

Table 1. Load Conditions

LOAD CONDITION	OUTPUT TRACKING
Nominal load in CCM	V_{Reg} tracks VIN approximately as: V_{Reg} = 95% (VIN – I_{Load} × 0.5)
No load/light load in LPM	To enable the tracking feature, following conditions should be met: 1) f_{SW} < 600 kHz 2) V_{Reg} < 8 V, typical (related to VIN falling threshold when LPM is disabled)

Modes of Operation

TPS54262 operates in the following modes based on the output loading conditions, input voltage and LPM pin configuration. These operating conditions and modes of operations are shown in Figure 14.

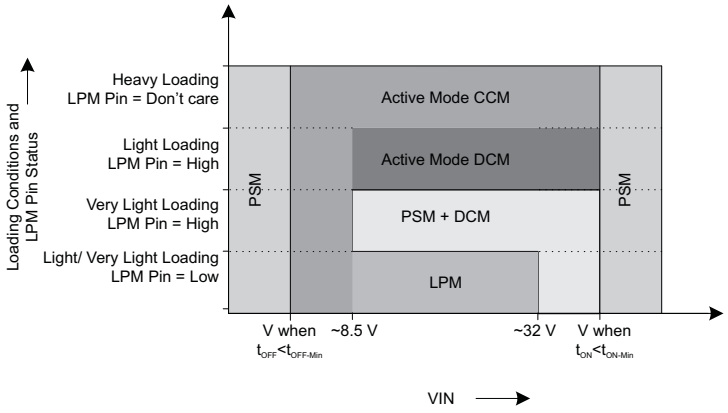


Figure 14. Modes of Operation

1) Active Mode Continuous Conduction Mode (CCM)

In this mode of operation the switcher operates in continuous conduction mode, and the inductor current is always non-zero if the total load current (internal and external) is greater than $I_{L\_DISCONT}$ shown in Equation 3.

$$I_{L\_DISCONT} = I_{L\_LPM} = \frac{(1-D)\cdot V_{Reg}}{2\cdot f_{sw}\cdot L} \quad (3)$$

Where,

D = duty cycle
L = output inductor
V_{Reg} = output voltage
f_{sw} = switching frequency

For VIN < 8.5 V, the device enables an internal ~100 Ω load. This, combined with the external load, can cause the device to enter into CCM even under light external loading conditions (see Figure 14). This mode of operation is shown in Figure 15 is also called the Normal mode of operation.

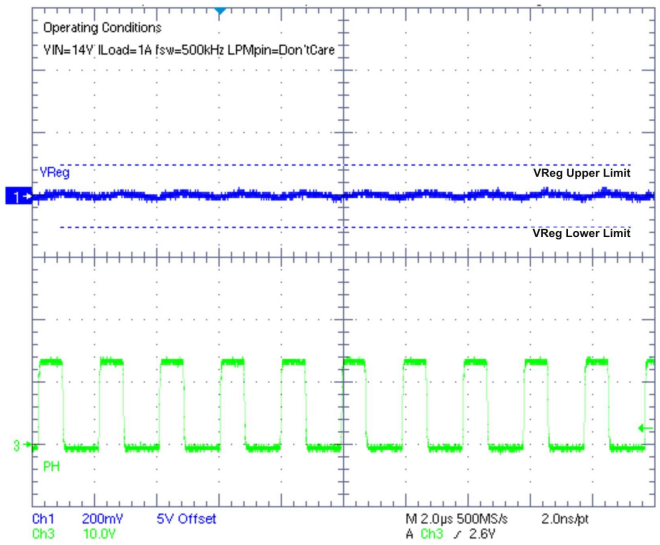


Figure 15. Active Mode CCM

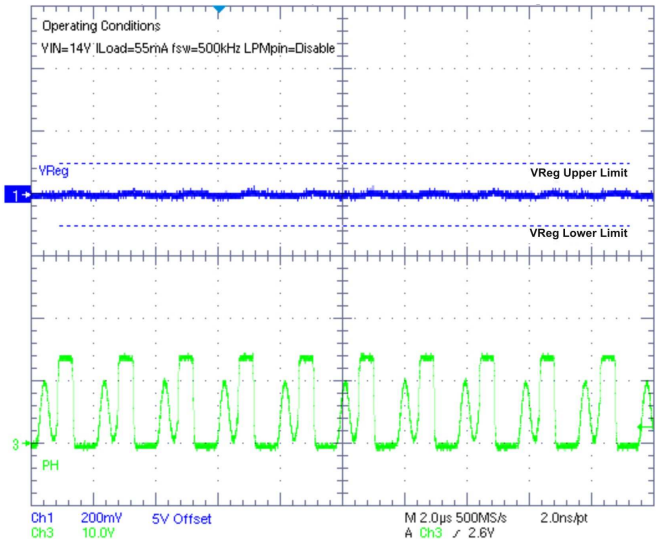


Figure 16. Active Mode DCM

2) Active Mode Discontinuous Conduction Mode (DCM)

In this mode of operation the switcher operates in discontinuous conduction mode, and the inductor current becomes zero if the total load current (internal and external) is less than $I_{L\_DISCONT}$ shown in Equation 4.

$$I_{L\_DISCONT} = I_{L\_LPM} = \frac{(1-D)\cdot V_{Reg}}{2\cdot f_{sw}\cdot L} \quad (4)$$

The device enters in this mode of operation when LPM pin is set high (i.e disabled) and output loading is less than $I_{L\_DISCONT}$. This mode of operation is shown in Figure 16.

3) Pulse Skip Mode (PSM)

In this mode of operation the switcher operates in discontinuous conduction mode, and the inductor current becomes zero. The device enters in this mode of operation in the following conditions:

- At low input voltages when V_{Reg} starts losing regulation and the OFF time (t_{OFF}) of the switching FET tends to be close to or slightly less than the minimum OFF time ($t_{OFF\text{-}Min}$). If OFF time is much smaller than $t_{OFF\text{-}Min}$, there is a risk that the part stops switching and regulation is lost until power is re-cycled with OFF time greater than $t_{OFF\text{-}Min}$. This mode of operation is shown in Figure 18. Comparing Figure 17 and Figure 18, pulse skipping occurs in Figure 18 but not in Figure 17 under similar output loading conditions.

$$VIN - I_{Load}\times R_{DS(ON)} < \sim V_{Reg} \quad \text{and} \quad \left(1 - \frac{V_{Reg}}{VIN}\right) \times \frac{1}{f_{sw}} > t_{OFF\text{-}Min} \quad (5)$$

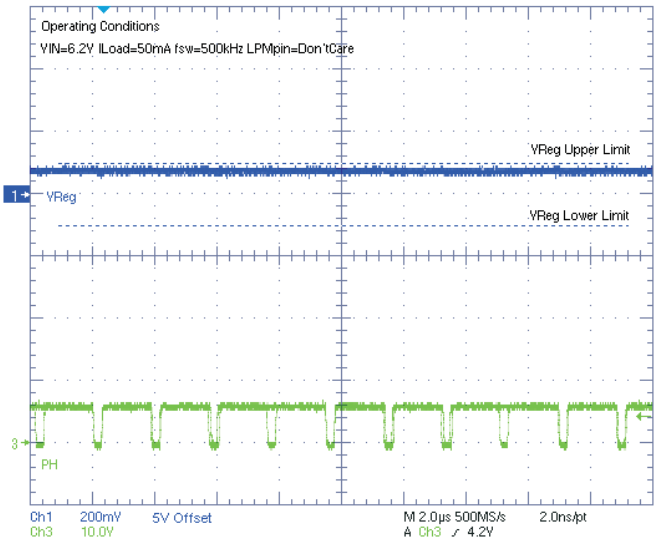


Figure 17. Active Mode CCM

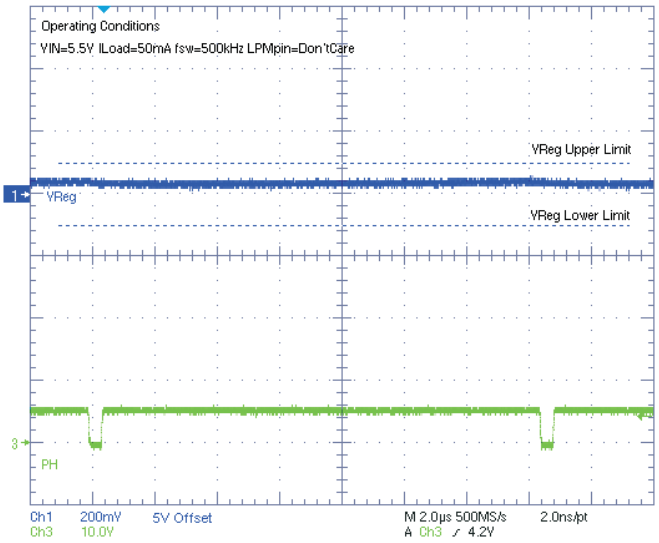


Figure 18. PSM at Low VIN

- Likewise, at higher input voltages when the ON time (t_{ON}) of the switching FET becomes close to or slightly less than the minimum ON time (t_{ON-Min}) and the V_{Reg} start losing regulation, the device enters in PSM. If ON time is much smaller than t_{ON-Min}, there is a risk that the part stops switching and regulation is lost until power is re-cycled with ON time greater than t_{ON-Min}.
- At nominal input voltages during very light output loading. This mode of operation is shown in Figure 19. Comparing Figure 16 and Figure 19, in both cases the device is operating in discontinuous conduction mode; however, pulse skipping happens in Figure 19 because of very light output loading for similar input voltage. LPM pin must be set high (i.e., disabled) for this to happen.

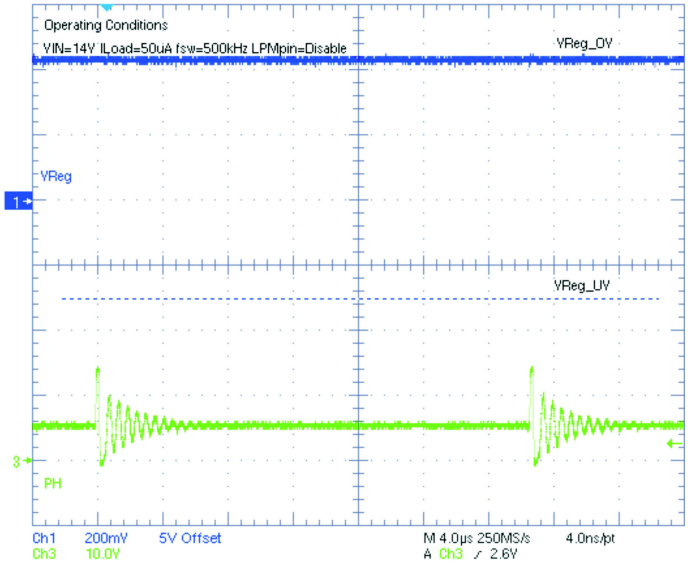


Figure 19. PSM at Nominal VIN

4) Low Power Mode (LPM)

In this mode of operation the device briefly operates in discontinuous conduction mode and then turns off until V_{Reg} < VReg_UV threshold and this cycle is repeated. The LPM pin must be enabled to enable LPM mode of operation. When total load is less than $I_{L\_DISCONT}$, the device operates in LPM for VIN ~8.5 V to ~32 V. This mode of operation is shown in Figure 20 and Figure 21 (zoomed out).

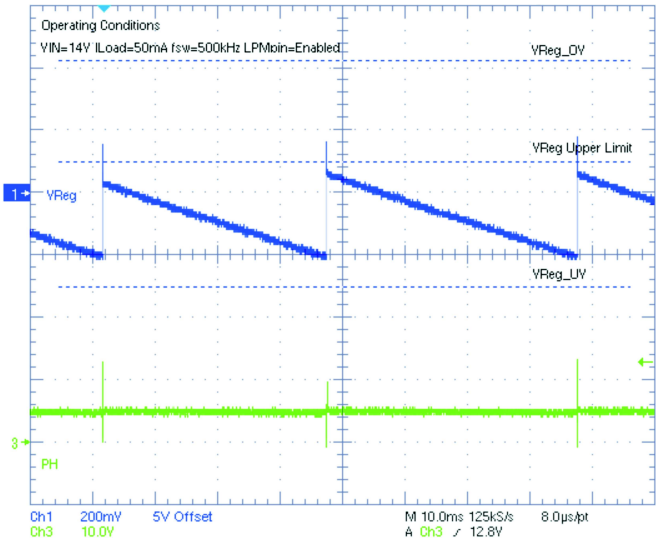


Figure 20. Low Power Mode

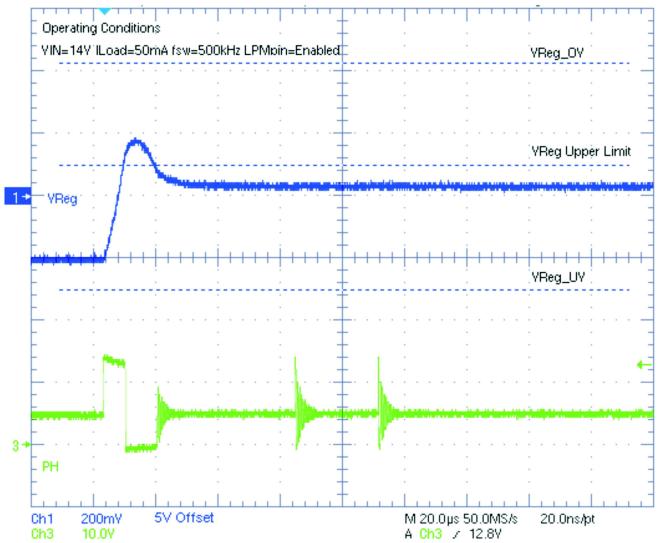


Figure 21. Low Power Mode (Zoom In)

Any transition from low-power mode to active mode CCM occurs within 5 µs (typical). In low-power mode, the converter operates as a hysteretic controller with the threshold limits set by VReg_UV (see Equation 10, Figure 4 and Figure 22), for the lower limit and ~V_{Reg} for the upper limit. To ensure tight regulation in the low-power mode, R2 and R3 values are set accordingly (see discussion on *Noise Filter on RST_TH and OV_TH Terminals*). The device operates in both automatic (LPM pin is connected to ground) and digitally controlled (status of LPM pin is controlled by an external device, for example by a microcontroller) low-power mode. The digital low-power mode can over-ride the automatic low-power mode function by applying the appropriate signal on the LPM terminal. The part goes into active mode CCM for at least 100 µs, whenever RST_TH or VReg_UV is tripped.

Table 2. LPM Pin Status

LPM PIN STATUS	MODES OF OPERATION
High	Device is forced in normal mode.
	At light loads, the device operates in DCM with a switching frequency determined by the external resistor connected to RT pin.
	At very light loads, the device operates in PSM with a reduced switching frequency (see Figure 14).
Low or open	Device automatically changes between normal mode and low-power mode depending on the load current.

Table 3. Modes of Operation

MODES OF OPERATION	DESCRIPTION
Normal mode (active mode)	All circuits including overvoltage threshold circuit (OV_TH) are enabled.
	At heavy loads, the device operates in continuous conduction mode irrespective of the status of LPM pin. OR At light loads, the device operates in discontinuous conduction mode (DCM) only if LPM pin is externally set high.
Low-power mode	OV_TH circuit is disabled. The device is in DCM, and LPM pin should be forced low.

When the device is operating in low-power mode, and if the output is shorted to ground, a reset is asserted. The thermal shutdown and current limiting circuitry is activated to protect the device. The LPM pin is active low and is internally pulled down; therefore, the low-power mode is automatically enabled unless this pin is driven high externally (for example, by a microcontroller) and the device is in continuous conduction mode. However, the low-power mode operation is initiated only when the device enters discontinuous mode of operation at light loads, and the LPM pin is low (or connected to ground).

5) Hysteretic Mode

The device enters in this mode of operation when the main loop fails to respond during line/ load transients and regulate within specified tolerances. The device exits this mode of operation when the main control loop responds, after the error amplifier stabilizes, and controls the output voltage within tighter tolerance.

The power up conditions in different modes of operations are explained in Table 4.

Table 4. Power-Up Conditions

MODE OF OPERATION	POWER-UP CONDITIONS
CCM	VIN > 3.6 V (minimum)
LPM/DCM	V_{Reg} < 5.5 V and (VIN - V_{Reg}) > 2.5 V (applicable only for f_{sw} > 600 kHz)

Output Tolerances in Different Modes of Operation

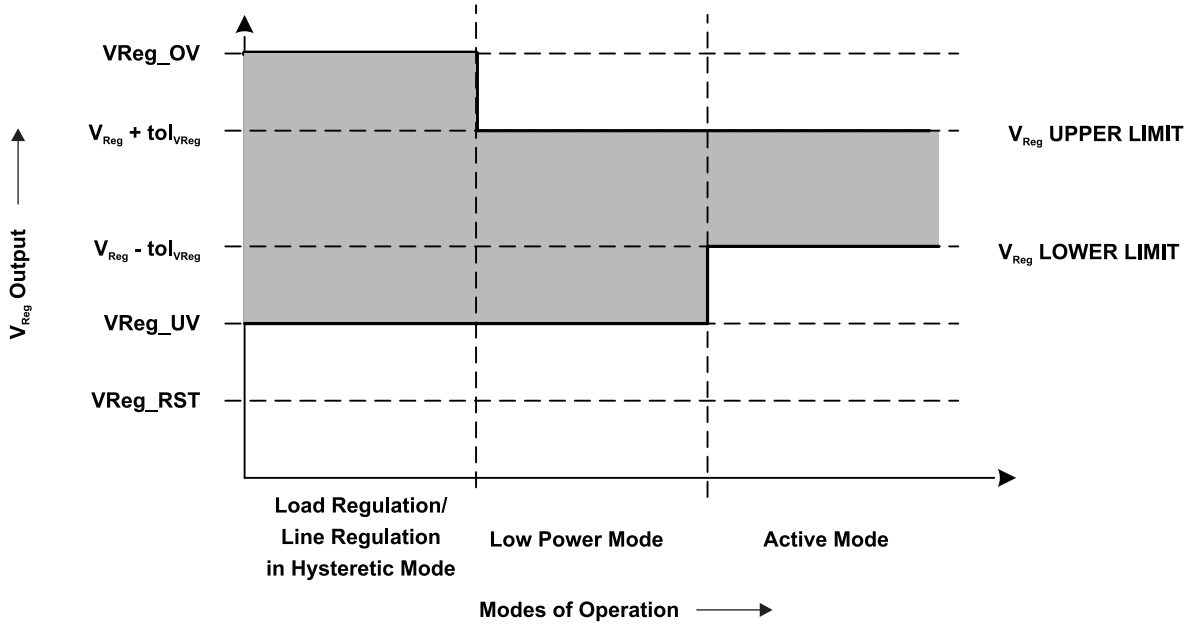


Figure 22.

Table 5.

MODE OF OPERATION	V_{Reg} LOWER LIMIT	V_{Reg} UPPER LIMIT	COMMENTS
Hysteretic mode	VReg_UV	VReg_OV	Minimum to maximum ripple on output
Low-power mode	VReg_UV	V_{Reg} + tol_{VReg}	Minimum to maximum ripple on output
Active mode (Normal)	V_{Reg} – tol_{VReg}	V_{Reg} + tol_{VReg}	Minimum to maximum ripple on output

Table 6.

SUPERVISOR THRESHOLDS	V_{Reg} TYPICAL VALUE	TOLERANCE	COMMENTS
VReg_OV	$\frac{R1+R2+R3}{R3} \times 0.8\ V$	$\pm (tol_{Vref} + (\frac{R1+R2}{R1+R2+R3}) \times (tol_{R1} + tol_{R2} + tol_{R3})$	Overvoltage threshold setting
VReg_RST	$\frac{R1+R2+R3}{R2+R3} \times 0.8\ V$	$\pm (tol_{Vref} + (\frac{R1}{R1+R2+R3}) \times (tol_{R1} + tol_{R2} + tol_{R3})$	Reset threshold setting

Enable and Shutdown

The EN pin (pin 5) provides electrical ON/OFF control of the regulator. Once the EN pin voltage exceeds the upper threshold voltage (V_{IH}), the regulator starts operating and the internal soft start begins to ramp. If the EN pin voltage is pulled below the lower threshold voltage (V_{IL}), the regulator stops switching and the internal soft start resets. Connecting this pin to ground or to any voltage less than V_{IL} disables the regulator and causes the device to shut down. This pin must have an external pullup or pulldown to change the state of the device.

Soft Start

An external soft start capacitor is connected to SS pin (pin 11) to set the minimum time to reach the desired regulated output voltage (V_{Reg}) during power up cycle. This prevents the output voltage from overshooting when the device is powered up. This is also useful when the load requires a controlled voltage slew rate, and also helps to limit the current drawn from the input voltage supply line.

For proper operation, the following conditions must be satisfied during power-up and after a short circuit event:

- VIN – V_{Reg} > 2.5 V
- Load current < 1 A, until $\overline{RST}$goes high

The current limit foldback is released after the feedback voltage (at VSENSE pin) is high enough such that $\overline{RST}$ is asserted high. The recommended value of soft start capacitor is 100 nF (typical) for startup load current of 1 A (maximum).

Oscillator Frequency

The oscillator frequency can be set by connecting an external resistor (R8 in Figure 4) to RT pin (pin 6) . Figure 23 shows the relation between the resistor value (RT) and switching frequency (f_{sw}). The switching frequency can be set in the range 200 kHz to 2200 kHz. In addition, the switching frequency can be imposed externally by a clock signal (f_{ext}) at the SYNC pin.

Selecting the Switching Frequency

A power supply switching at a higher switching frequency allows use of lower value inductor and smaller output capacitor compared to a power supply that switches at a lower frequency. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The switching frequency that can be selected is limited by the following factors:

- The input voltage
- The minimum target regulated voltage
- Minimum on-time of the internal switching transistor
- Frequency shift limitation

Selecting lower switching frequency results in using an inductor and capacitor of a larger value, where as selecting higher switching frequency results in higher switching and gate drive power losses. Therefore, a tradeoff has to be made between physical size of the power supply and the power dissipation at the system/ application level.

The minimum and maximum duty cycles can be expressed in terms of input and output voltage as shown in Equation 6.

$$D_{Min} = \frac{V_{Reg\text{-}Min}}{VIN_{Max}} \quad \text{and} \quad D_{Max} = \frac{V_{Reg\text{-}Min}}{VIN_{Min}} \tag{6}$$

Where,

D_{Min} = minimum duty cycle
D_{Max} = maximum duty cycle
VIN_{Min} = minimum input voltage
VIN_{Max} = maximum input voltage
$V_{Reg\text{-}Min}$ = minimum regulated output voltage
$V_{Reg\text{-}Max}$ = maximum regulated output voltage

From Equation 6, maximum switching frequency can be calculated in Equation 7.

$$f_{sw\text{-}Max} = \frac{V_{Reg\text{-}Min} / VIN_{Max}}{t_{ON\text{-}Min}} \quad (7)$$

Where,

$f_{sw\text{-}Max}$ = maximum switching frequency

$t_{ON\text{-}Min}$ = minimum on-time of the NMOS switching transistor

Knowing the switching frequency, the value of resistor to be connected at RT pin can be calculated using the graph shown in Figure 23.

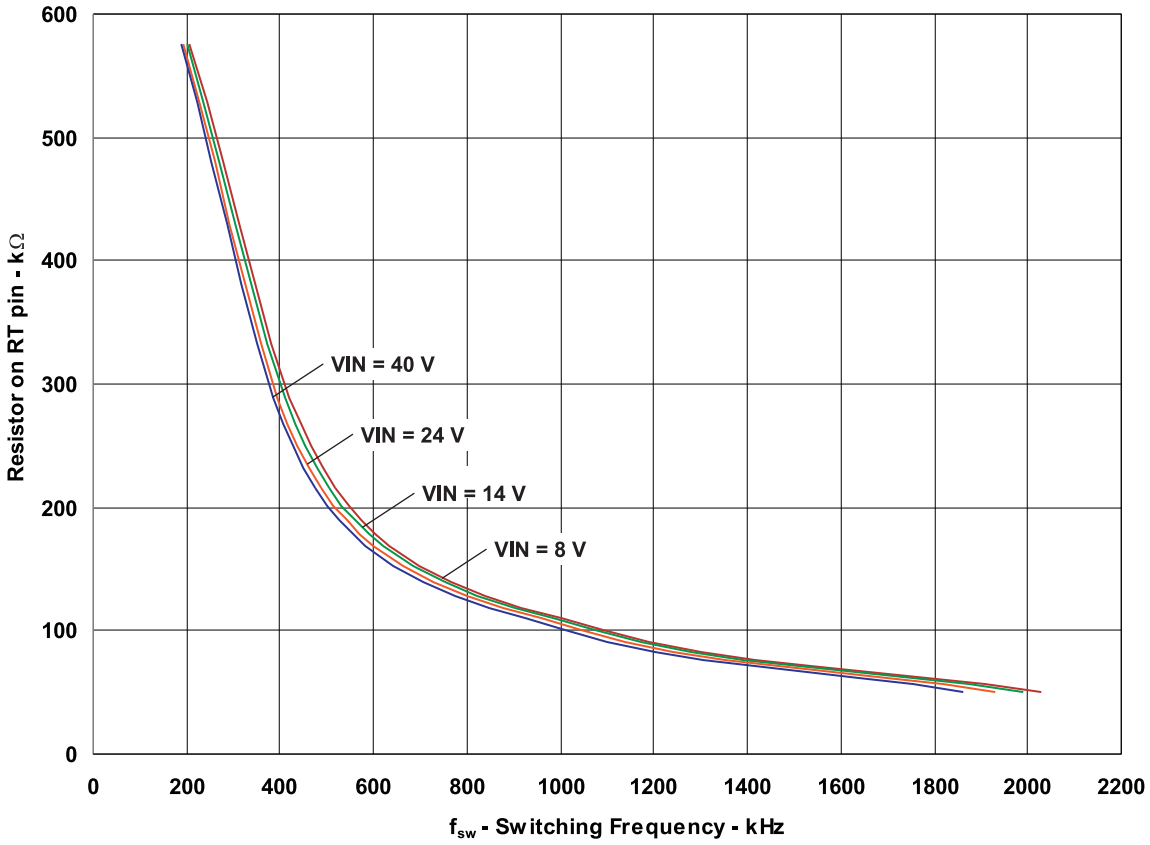


Figure 23. Switching Frequency vs Resistor Value

Synchronization With External Clock

An external clock signal can be supplied to the device through SYNC pin (pin 3) to synchronize the internal oscillator frequency with an external clock frequency. The synchronization input overrides the internal fixed oscillator signal. The synchronization signal has to be valid for approximately two clock cycles before the transition is made for synchronization with the external frequency input. If the external clock input does not transition low or high for 32 µs (typical), the system defaults to the internal clock set by the resistor connected to the RT pin. The SYNC input can have a frequency according to Equation 8.

$$180\ \text{kHz} < f_{sw} < f_{ext} < 2 \times f_{sw} < 2.2\ \text{MHz} \quad (8)$$

Where,

f_{sw} = oscillator frequency determined by resistor connected to the RT pin

f_{ext} = frequency of the external clock fed through SYNC pin

For example, if the resistor connected at RT pin is selected such that the switching frequency (f_{sw}) is 500 kHz, then the external clock can have a frequency (f_{ext}) between 500 kHz and 1000 kHz. But, if the resistor connected at RT pin is selected such that the switching frequency (f_{sw}) is 1500 kHz, then the external clock can have a frequency (f_{ext}) between 1500 kHz and 2200 kHz only.

If the external clock gets struck for less than 32 µs, the NMOS switching FET is turned off and the output voltage starts decreasing. Depending upon the load conditions, the output voltage may hit the under voltage threshold and reset threshold before the external clock appears. The NMOS switching FET stays OFF until the external clock appears again. If the output voltage hits the reset threshold, the $\overline{\text{RST}}$ pin is asserted low after a deglitch time of 20 µs (typical).

If the external clock gets struck for more than 32 µs, the NMOS switching FET is turned off and the output voltage starts decreasing. Under this condition the default internal oscillator clock set by RT pin overrides the external after 32 µs and the NMOS switching FET resumes switching. When the external clock appears again (such that 180 kHz < f_{sw} < f_{ext} < 2 × f_{sw} < 2.2 MHz), the NMOS switching FET starts switching at the frequency determined by the external clock.

Slew Rate Control

The slew rate of the NMOS switching FET can be set by using an external resistor (R7 in Figure 4). The range of rise times and fall times for different values of slew resistor are shown in Figure 24 and Figure 25.

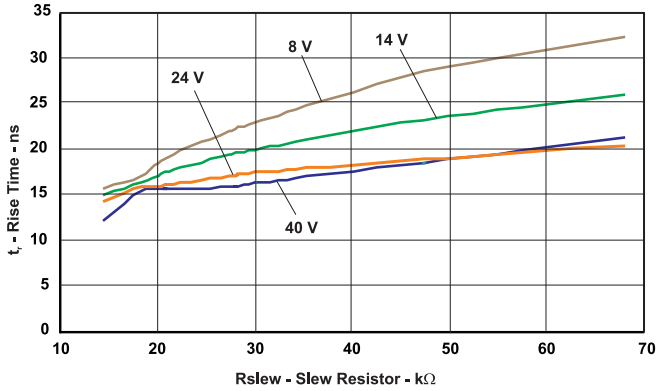


Figure 24. FET Rise Time

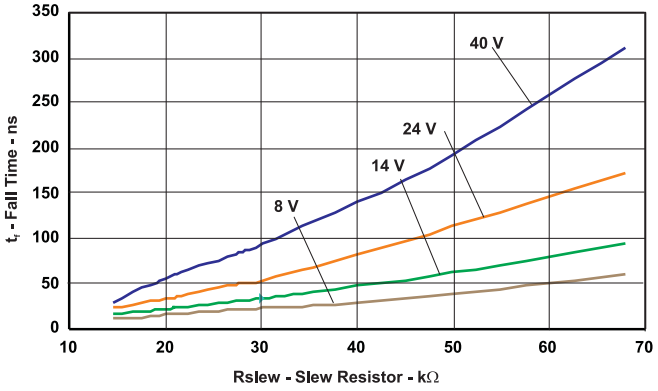


Figure 25. FET Fall Time

Reset

The $\overline{\text{RST}}$ pin (pin 8) is an open drain output pin used to indicate external digital devices/ loads if the device has powered up to a programmed regulated output voltage properly. This pin is asserted low until the regulated output voltage (V_{Reg}) exceeds the programed reset threshold (VREG_RST, see Equation 11) and the reset delay timer (set by Cdly pin) has expired. Additionally, whenever the EN pin is low or open, $\overline{\text{RST}}$ is immediately asserted low regardless of the output voltage. There is a reset filter timer to prevent reset being invoked due to short negative transients on the output line. If thermal shut down occurs due to excessive thermal conditions, this pin is asserted low when the switching FET is commanded OFF and the output falls below the reset threshold.

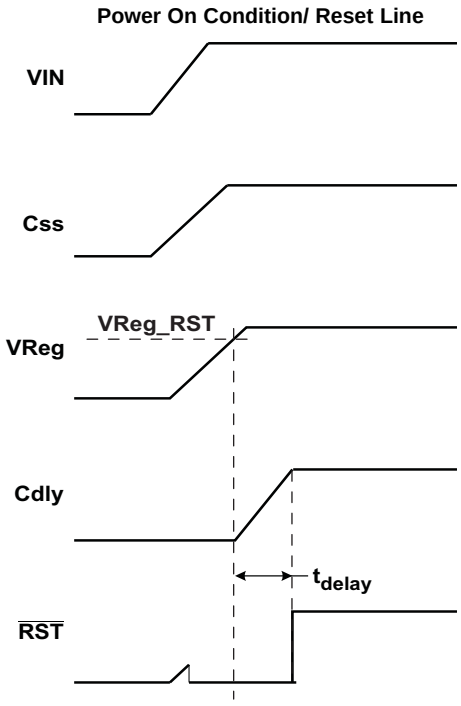


Figure 26.

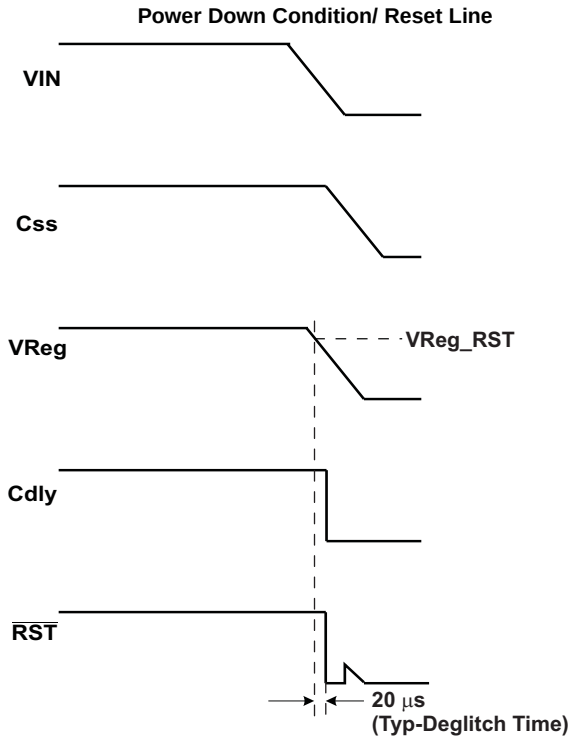


Figure 27.

Reset Delay

The delay time to assert the $\overline{RST}$ pin high after the supply has exceeded the programmed VReg_RST voltage (see Equation 11 to calculate VReg_RST) can be set by external capacitor (C2 in Figure 4) connected to the Cdly pin (pin 9). The delay may be programmed in the range of 2.2 ms to 200 ms using a capacitor in the range of 2.2 nF to 200 nF. The delay time is calculated using Equation 9:

$$PORdly = \frac{1ms}{nF} \times C \quad (9)$$

Where,

C = capacitor on Cdly pin

Reset Threshold and Undervoltage Threshold

The undervoltage threshold (VReg_UV) level for proper regulation in low-power mode and the reset threshold level (VReg_RST) to initiate a reset output signal can be programmed by connecting an external resistor string to the RST_TH pin (pin 13). The resistor combination of R1, R2, and R3 is used to program the threshold for detection of undervoltage. Voltage bias on R2 + R3 sets the reset threshold.

Undervoltage threshold for transient and low-power mode operation is given by the Equation 10. The recommended range for VReg_UV is 73% to 95% of V_{Reg}.

$$VReg\_UV = \frac{R1 + R2 + R3}{R2 + R3} \times 0.82\ V \quad (10)$$

Reset threshold is given by Equation 11. The recommended range for VReg_RST is 70% to 92% of V_{Reg}.

$$VReg\_RST = \frac{R1 + R2 + R3}{R2 + R3} \times 0.8\ V \quad (11)$$

Overvoltage Supervisor

The overvoltage monitoring of the regulated output voltage, V_{Reg} can be achieved by connecting an external resistor string to the OV_TH pin (pin 12). The resistor combination of R1, R2, and R3 is used to program the threshold for detection of overvoltage. The bias voltage of R3 sets the overvoltage threshold and the accuracy of regulated output voltage in hysteretic mode during transient events.

$$VReg\_OV = \frac{R1 + R2 + R3}{R3} \times 0.8\ V \quad (12)$$

Recommended range for VReg_OV is 106% to 110% of V_{Reg}.

Noise Filter on RST_TH and OV_TH Terminals

External capacitors may be required to filter the noise added to RST_TH and OV_TH terminals. The noise is more pronounced with fast falling edges on the PH pin. Therefore, selecting a smaller Rslew resistor (R7 in Figure 4) for a higher slew rate will require more external capacitance to filter the noise.

The RC time constant depends on external components (R2, R3, C9 and C10 in Figure 4) connected to RST_TH and OV_TH pins. For proper noise filtering, improved loop transient response and better short circuit protection, Equation 13 must be satisfied.

$$(R2 + R3) \times (C9 + C10) < 2\ \mu s \quad (13)$$ (13)

To meet this requirement, it is recommended to use lower values of external capacitors and resistors. The value of the time constant is also affected by the PCB capacitance and the application setup. Therefore, in some cases the external capacitors (C9, C10) on RST_TH and OV_TH terminals may not be required. Users can place a footprint on the application PCB and only populate it if necessary. Also, the external resistors (R1, R2, R3) should be sized appropriately to minimize any significant effect of board leakage.

For most cases, it is recommended to keep the external capacitors (either from board capacitance or by connecting external capacitors) between 10 pF to 100 pF; therefore, to meet time constant requirement in Equation 13, the total external resistance (R1 + R2 + R3) should be less than 200 kΩ.

Boost Capacitor

An external boot strap capacitor (C3 in Figure 4) is connected to pin 20 to provide the gate drive voltage for the internal NMOS switching FET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature. The capacitor value may need to be adjusted higher for high V_{Reg} and/or low frequencies applications (e.g., 100 nF for 500 kHz/5 V and 220 nF for 500 kHz/8 V).

Loop Control Frequency Compensation

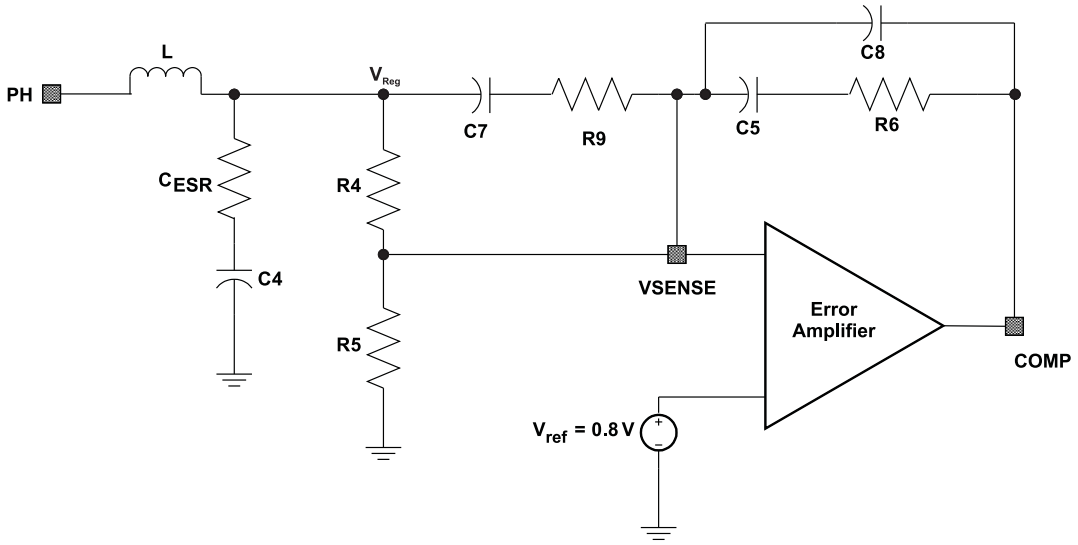


Figure 28. Type 3 Compensation

Type 3 Compensation

Type 3 compensation has been used in the feedback loop to improve the stability of the convertor and regulation in the output in response to the changes in input voltage or load conditions. This becomes important because the ceramic capacitors used to filter the output have a low Equivalent Series Resistance (ESR). Type 3 compensation is implemented by connecting external resistors and capacitors to the COMP pin (output of the error amplifier, pin 15) of the device as shown in Figure 28.

The crossover frequency should be less than 1/5th to 1/10th of the switching frequency, and should be greater than five times the double pole frequency of the LC filter.

$$f_c < f_{sw} \times (0.1 \text{ to } 0.2) \quad (14)$$ (14)

Where,

f_{sw} = switching frequency

The modulator break frequencies as a function of the output LC filter are derived from Equation 15 and Equation 16. The LC output filter gives a double pole that has a –180° phase shift.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (15)$$

Where,

L = output inductor

C = output capacitor (C4 in functional block diagram)

The ESR of the output capacitor C gives a "ZERO" that has a 90° phase shift.

$$f_{ESR} = \frac{1}{2\pi C \times ESR} \quad (16)$$

Where,

ESR = Equivalent series resistance of a capacitor at a specified frequency

The regulated output voltage, V_{Reg} is given by Equation 17.

$$V_{Reg} = V_{ref}\left(1 + \frac{R4}{R5}\right) \quad (17)$$

$$\frac{V_{Reg}}{0.8} = \frac{R4 + R5}{R5} \quad (18)$$

For VIN = 8 V to 50 V, the VIN/V_{ramp} modulator gain is approximately 10 and has a tolerance of about 20%.

$$\text{Gain} = A_{mod} = \frac{VIN}{V_{ramp}} = 10 \tag{19}$$

Therefore,

$$\text{Gain (dB)} = 20 \times \log\left(\frac{VIN}{V_{ramp}}\right) = 20 \times \log(10) = 20 \text{ dB} \tag{20}$$

Also, V_{ramp} is fixed for the following range of VIN. V_{ramp} = 1 V for VIN < 8 V, and V_{ramp} = 5 V for VIN > 48 V.

The frequencies for poles and zeros are given by following equations.

$$fp1 = \frac{(C5 + C8)}{2\pi \times R6 \times (C5 \times C8)} \tag{21}$$

$$fp2 = \frac{1}{2\pi \times R9 \times C7} \tag{22}$$

$$fz1 = \frac{1}{2\pi \times R6 \times C5} \tag{23}$$

$$fz2 = \frac{1}{2\pi \times (R4 + R9) \times C7} \tag{24}$$

Guidelines for selecting compensation components selection are provided in the *Application Information* section of this document.

Bode Plot of Converter Gain

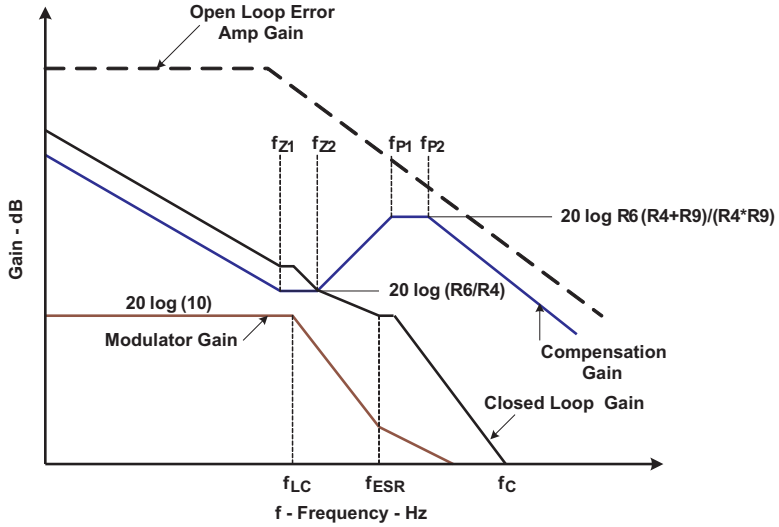


Figure 29.

Short-Circuit Protection

The TPS54262 features an output short-circuit protection. Short-circuit conditions are detected by monitoring the RST_TH pin, and when the voltage on this node drops below 0.2 V, the switching frequency is decreased and current limit is folded back to protect the device. The switching frequency is folded back to approximately 25 kHz and the current limit is reduced to 30% of the typical current limit value.

Thermal Shutdown (TSD)

The TPS54262 protects itself from overheating with an internal thermal shutdown (TSD) circuit. If the junction temperature exceeds the thermal shutdown trip point, the NMOS switching FET is turned off. The device is automatically restarted under the control of soft-start circuit when the junction temperature drops below the thermal shutdown hysteretic trip point. During low-power mode operation, the thermal shutdown sensing circuitry is disabled for reduced current consumption. If V_{Reg} drops below VReg_UV, thermal shutdown monitoring is activated.

Overcurrent Protection

The device features overcurrent protection to protect it from load currents greater than 2 A. Overcurrent protection is implemented by sensing the current through the NMOS switching FET. The sensed current is compared to a current reference level representing the overcurrent threshold limit (I_{CL}). If the sensed current exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent protection is triggered. The NMOS switching FET is turned off for the rest of the cycle after a propagation delay. The overcurrent protection scheme is called cycle-by-cycle current limiting. If the sensed current continues to increase during cycle-by-cycle current limiting, the temperature of the part will start rising, the TSD will kick in and shut down switching until the part cools down.

Internal Undervoltage Lockout (UVLO)

This device is enabled on power up once the internal bandgap and bias currents are stable; this happens typically at VIN = 3.4 V (minimum). On power down, the internal circuitry is disabled at VIN = 2.6 V (maximum).

Power Dissipation and Temperature Considerations

The power dissipation losses are applicable for continuous conduction mode operation (CCM). The total power dissipated by the device is the sum of the following power losses.

Conduction losses, P_{CON}

$$P_{CON} = I_{Load}^2 \times R_{DS(ON)} \times \frac{V_{Reg}}{VIN} \quad (25)$$

Switching losses, P_{SW}

$$P_{SW} = \frac{1}{2} VIN \times I_{Load} \times (t_r + t_f) \times f_{sw} \quad (26)$$

Gate drive losses, P_{Gate}

$$P_{Gate} = V_{drive} \times Q_g \times f_{sw} \quad (27)$$

Power supply losses, P_{IC}

$$P_{IC} = VIN \times I_{q\text{-}Normal} \quad (28)$$

Therefore, the total power dissipated by the device is given by Equation 29.

$$P_{Total} = P_{CON} + P_{SW} + P_{Gate} + P_{IC} \quad (29)$$

Where,

- VIN = unregulated input voltage
- I_{Load} = output load current
- t_r = FET switching rise time (t_r= 40 ns (maximum))
- t_f = FET switching fall time
- f_{sw} = switching frequency
- V_{drive} = FET gate drive voltage (V_{drive} = 6 V (typical), V_{drive} = 8 V (maximum))
- Q_g = 1×10^{-9} C
- $I_{q\text{-}Normal}$ = quiescent current in normal mode (Active Mode CCM)

For device under operation at a given ambient temperature (T_A), the junction temperature (T_J) can be calculated using Equation 30.

$$T_J = T_A + (R_{th} \times P_{Total}) \quad (30)$$ (30)

Therefore, the rise in junction temperature due to power dissipation is shown in Equation 31.

$$\Delta T = T_J - T_A = (R_{th} \times P_{Total}) \quad (31)$$ (31)

For a given maximum junction temperature ($T_{J\text{-}Max}$), the maximum ambient temperature ($T_{A\text{-}Max}$) in which the device can operate is calculated using Equation 32.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (R_{th} \times P_{Total}) \quad (32)$$ (32)

Where,

T_J = junction temperature in °C
T_A = ambient temperature in °C
R_{th} = thermal resistance of package in W/°C
$T_{J\text{-}Max}$ = maximum junction temperature in °C
$T_{A\text{-}Max}$ = maximum ambient temperature in °C

There are several other factors that also affect the overall efficiency and power losses. Examples of such factors are AC and DC losses in the inductor, voltage drop across the copper traces on PCB, power losses in the flyback catch diode etc. Above discussion does not include such factors.

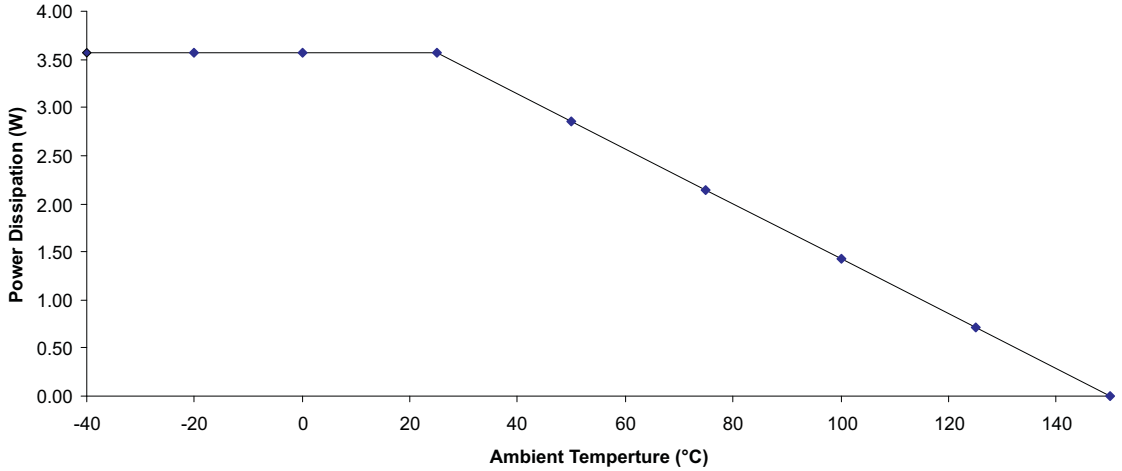


Figure 30. Power Dissipation vs Ambient Temperature

NOTE

The output current rating for the regulator may have to be derated for ambient temperatures above 85°C. The derated value will depend on calculated worst-case power dissipation and the thermal management implementation in the application.

APPLICATION INFORMATION

These guidelines address the following topics in detail for TPS54262-Q1.

1. Component selection
2. Design example
3. PCB layout guidelines

Component Selection

This section explains considerations for the external components selection. The following schematic shows the interconnection between external components and the device for a typical DC/DC step down application.

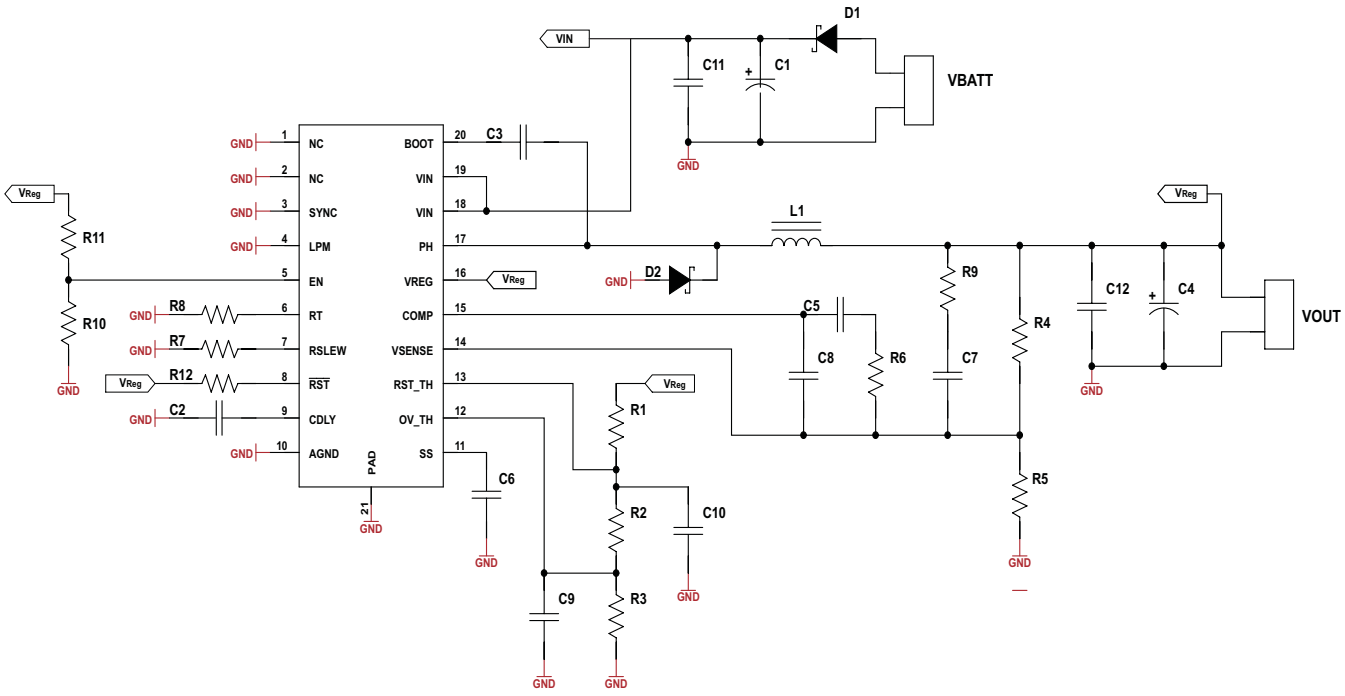


Figure 31. Typical Application Schematic

1) Input Capacitors (C1, C11)

Input filter capacitor (C11) is used to filter out high frequency noise in the input line. Typical values of C11 are 0.1µF to 0.01µF. For higher frequency noise, low capacitor values are recommended.

To minimize the ripple voltage, input ceramic de-coupling capacitor (C1) of type X5R or X7R should be used. The DC voltage rating for the input decoupling capacitor must be greater than the maximum input voltage. This capacitor must have an input ripple current rating higher than the maximum input ripple current of the converter for the application; and is determined by Equation 33.

$$I_{RMS} = I_{Load} \sqrt{\frac{V_{Reg}(VIN_{Min} - V_{Reg})}{VIN_{Min}^{2}}} \quad (33)$$

The input capacitors for power regulators are chosen to have a reasonable capacitance-to-volume ratio and fairly stable over temperature. The value of the input capacitance also determines the input ripple voltage of the regulator, shown by Equation 34.

$$\Delta VIN = \frac{0.25 \times I_{Load\text{-}Max}}{C1 \times f_{sw}} \quad (34)$$

Input ceramic filter capacitors should be located in close proximity to the VIN terminal. Surface mount capacitors are recommended to minimize lead length and reduce noise coupling.

2) Output Capacitor (C4, C12)

The selection of the output capacitor will determine several parameters in the operation of the converter, for example voltage drop on the output capacitor and the output ripple. The capacitor value also determines the modulator pole and the roll-off frequency due to the LC output filter double pole. This is expressed in Equation 15.

The minimum capacitance needed to maintain desired output voltage during high to low load transition and prevent over shoot is given by Equation 35.

$$C4 = \frac{L \times (I_{Load\text{-}Max}^{2} - I_{Load\text{-}Min}^{2})}{V_{Reg\text{-}Max}^{2} - V_{Reg\text{-}Min}^{2}} \quad (35)$$

Where,

L = output inductor

$I_{Load\text{-}Max}$ = maximum load current

$I_{Load\text{-}Min}$ = minimum load current

$V_{Reg\text{-}Max}$ = maximum tolerance of regulated output voltage

$V_{Reg\text{-}Min}$ = minimum tolerance of regulated output voltage

During a load step from no load to full load or changes in the input voltage, the output capacitor must hold up the output voltage above a certain level for a specified time and not issue a reset, until the main regulator control loop responds to the change. The minimum output capacitance required to allow sufficient drop on the output voltage without issuing a reset is determined by Equation 36.

$$C4 > \frac{2 \times \Delta I_{Load}}{f_{sw} \times \Delta V_{Reg}} \quad (36)$$

Where,

ΔV_{Reg} = transient response during load stepping

The minimum capacitance needed for output voltage ripple specification is given by Equation 37.

$$C4 > \frac{1}{8 \times f_{sw} \times \frac{V_{Reg\text{-}Ripple}}{I_{Ripple}}} \quad (37)$$

Additional capacitance de-ratings for temperature, aging, and DC bias have to be factored in, and so a value of 100 µF with ESR calculated using Equation 38 of less than 100 mΩ should be used on the output stage.

Maximum ESR of the output capacitor is based on output ripple voltage specification in Equation 38 . The output ripple voltage is a product of the output capacitor ESR and ripple current.

$$R_{ESR} < \frac{V_{Reg\text{-}Ripple}}{I_{Ripple}} \quad (38)$$

Output capacitor root mean square (RMS) ripple current is given by Equation 39. This is to prevent excess heating or failure due to high ripple currents. This parameter is sometimes specified by the manufacturers.

$$I_{Load\text{-}RMS} = \frac{V_{Reg} (VIN_{Max} - V_{Reg})}{\sqrt{12} \times VIN_{Max} \times f_{sw} \times L1} \quad (39)$$

Filter capacitor (C12) of value 0.1 µF (typical) is used to filter out the noise in the output line.

3) Soft-Start Capacitor (C6)

The soft start capacitor determines the minimum time to reach the desired output voltage during a power up cycle. This is useful when a load requires a controlled voltage slew rate, and helps to limit the current draw from the input voltage supply line. A 100 nF capacitor is recommended for startup loads of 1A (max.).

4) Bootstrap Capacitor (C3)

A 0.1µF ceramic capacitor must be connected between the PH and BOOT terminals for the converter to operate and regulate to the desired output voltage. It is recommended to use a capacitor with X5R or better grade dielectric material, and the voltage rating on this capacitor of at least 25V to allow for derating.

5) Power-On Reset Delay (PORdly) Capacitor (C2)

The value of this capacitor can be calculated using Equation 9.

6) Output Inductor (L1)

Use a low EMI inductor with a ferrite type shielded core. Other types of inductors may be used; however, they must have low EMI characteristics and should be located away from the low-power traces and components in the circuit.

To calculate the minimum value of the inductor, the ripple current should be first calculated using Equation 40.

$$I_{Ripple} = K_{IND} \times I_{Load} \quad (40)$$ (40)

Where,

I_{Load} = maximum output load current

I_{Ripple} = allowable peak to peak inductor ripple current, typ. 20% of maximum I_{Load}

K_{IND} = coefficient that represents the amount of inductor ripple current relative to the maximum output current. Since, the inductor ripple current is filtered by the output capacitor; therefore K_{IND} is typically in the range of 0.2 to 0.3, depending on the ESR and the ripple current rating of the output capacitor (C4).

The minimum value of output inductor can be calculated using Equation 41.

$$L_{Min} = \frac{(VIN_{Max} - V_{Reg}) \times V_{Reg}}{f_{sw} \times I_{Ripple} \times VIN_{Max}} \quad (41)$$

Where,

VIN_{Max} = maximum input voltage

V_{Reg} = regulated output voltage

f_{sw} = switching frequency

The RMS and peak currents flowing in the inductor are given by Equation 42 and Equation 43.

$$I_{L,RMS} = \sqrt{I_{Load}^2 + \frac{I_{Ripple}^2}{12}} \quad (42)$$

$$I_{L,pk} = I_{Load} + \frac{I_{Ripple}}{2} \quad (43)$$

7) Flyback Schottky Diode (D2)

The TPS54262 requires an external Schottky diode connected between the PH and power ground termination. The absolute voltage at PH pin should not go beyond the values in *Absolute Maximum Ratings*. The Schottky diode conducts the output current during the off state of the internal power switch. This Schottky diode must have a reverse breakdown voltage higher than the maximum input voltage of the application. A Schottky diode is selected for its lower forward voltage. The Schottky diode is selected based on the appropriate power rating, which factors in the DC conduction losses and the AC losses due to the high switching frequencies; this is determined by Equation 44.

$$P_{diode} = \frac{(VIN_{Max} - V_{Reg}) \times I_{Load} \times V_{fd}}{VIN_{Max}} + \frac{(VIN - V_{fd}) \times f_{sw} \times C_J}{2} \quad (44)$$

Where,

P_{diode} = power rating

V_{fd} = forward conducting voltage of Schottky diode

C_J = junction capacitance of the Schottky diode

Recommended part numbers are PDS 360 and SBR8U60P5.

8) Resistor to Set Slew Rate (R7)

The slew rate setting is asymmetrical; i.e., for a selected value of R7, the rise time and fall time are different. R7 can be approximately determined from Figure 24 and Figure 25. The minimum recommended value is 10 kΩ.

9) Resistor to Select Switching Frequency (R8)

Please refer to the section *Selecting Switching Frequency*, Figure 23 and Equation 7.

10) Resistors to Select Output Voltage (R4, R5)

To minimize the effect of leakage current on the VSENSE terminal, the current flowing through the feedback network should be greater than 5 mA to maintain output accuracy. Higher resistor values help improve the converter efficiency at low output currents, but may introduce noise immunity problems. Please refer to Equation 1. It is recommended to fix R4 to a standard value (say 187 kΩ) and calculate R5.

11) Resistors to Set Undervoltage, Overvoltage, and Reset Thresholds (R1, R2, R3)

Overvoltage resistor selection

Using Equation 12, the value of R3 can be determined to set the overvoltage threshold at up to 106% to 110% of V_{Reg}. The sum of R1, R2, and R3 resistor network to ground should be is approximately 100 kΩ .

Reset threshold resistor selection

Using Equation 11 the value of R2 + R3 can be calculated, and knowing R3 from the OV_TH setting, R2 can be determined. Suggested value of reset threshold is 92% of V_{Reg}.

Undervoltage threshold for low-power mode and load transient operation

This threshold is set above the reset threshold to ensure the regulator operates within the specified tolerances during output load transient of low load to high load and during discontinuous conduction mode. The typical voltage threshold can be determined using Equation 10. Suggested value of undervoltage threshold is 95% of V_{Reg}.

Low-Power Mode (LPM) Threshold

An approximation of the output load current at which the converter is operating in discontinuous mode can be obtained from Equation 4 with ± 30% hysteresis. The values used in Equation 6 for minimum and maximum input voltage will affect the duty cycle and the overall discontinuous mode load current. These are the nominal values, and other factors are not taken into consideration like external component variations with temperature and aging.

12) Pullup Resistor for Enable (R12)

An external pull resistor of 30.1 kΩ is recommended to enable the device for operation.

13) Type 3 Compensation Components (R5, R6, R9, C5, C7, C8)

First, make the 'ZEROs' close to double pole frequency, using Equation 15, Equation 16, and Equation 14.

fz1 = (50% to 70%) f_{LC}

fz2 = f_{LC}

Second, make the 'POLEs' above the crossover frequency, using Equation 21 and Equation 22.

fp1 = f_{ESR}

fp2 = ½f_{sw}

Resistors

From Equation 1, knowing V_{Reg} and R4 (fix to a standard value), R5 can be calculated as shown in Equation 45:

$$R5 = \frac{R4}{\frac{V_{Reg}}{V_{ref}} - 1} \tag{45}$$

Using Equation 14 and Equation 18, R6 can be calculated as shown in Equation 46:

$$R6 = \frac{f_c \times V_{Ramp} \times R4}{VIN \times f_{LC}} \tag{46}$$

R9 can be calculated as shown in Equation 47:

$$R9 = \frac{R4}{\left(\frac{f_{SW}}{2f_{LC}} - 1\right)} \quad (47)$$

Capacitors

Using Equation 23, C5 can be calculated as shown in Equation 48:

$$C5 = \frac{1}{\pi \times R6 \times f_{LC}} \quad (48)$$

C7 can be calculated as shown in Equation 49:

$$C7 = \frac{1}{\pi \times R9 \times f_{SW}} \quad (49)$$

C8 can be calculated as shown in Equation 50:

$$C8 = \frac{C5}{2\pi \times R6 \times C5 \times f_{ESR} - 1} \quad (50)$$

14) Noise Filter on RST_TH and OV_TH Terminals (C9, C10)

These capacitors may be required in some applications to filter the noise on RST_TH and OV_TH pins. Typical capacitor values for RST_TH and OV_TH pins are between 10 pF to 100 pF for total resistance on RST_TH/OV_TH divider of less than 200 kΩ. See discussion on *Noise Filter on RST_TH and OV_TH Terminals*.

DESIGN EXAMPLE

The following examples demonstrate the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level.

Example 1

For this example, we will start with the following known and target parameters:

Table 7.

Known	Input voltage, VIN	Minimum = 8 V, Maximum = 28 V, Typical = 14 V
Target	Output voltage, V_{Reg}	5 V ± 2%
	Maximum output current, $I_{Load-Max}$	1.8 A
	Ripple/ transient occurring in input voltage, ΔVIN	1% of VIN (minimum)
	Reset threshold, VReg_RST	92% of V_{Reg}
	Overvoltage threshold, VReg_OV	106% of V_{Reg}
	Undervoltage threshold, VReg_UV	95% of V_{Reg}
	Transient response 0.25 A to 2 A load step, ΔV_{Reg}	5% of V_{Reg}
	Power on reset delay, PORdly	2.2 ms

Step 1. Calculate the Switching Frequency (f_{sw})

To reduce the size of output inductor and capacitor, higher switching frequency can be selected. It is important to understand that higher switching frequency will result in higher switching losses, causing the device to heat up. This may result in degraded thermal performance. To prevent this, proper PCB layout guidelines must be followed (explained in the later section of this document).

Based upon the discussion in section *Selecting the Switching Frequency*, calculate the maximum and minimum duty cycle.

Knowing V_{Reg} and tolerance on V_{Reg}, the $V_{Reg-Max}$ and $V_{Reg-Min}$ are calculated to be:

$V_{Reg-Max}$ = 102% of V_{Reg} = 5.1 V and $V_{Reg-Min}$ = 98% of V_{Reg} = 4.9 V.

Using Equation 6, the minimum duty cycle is calculated to be, D_{Min} = 17.5%

Knowing t_{ON-Min} = 150 ns from the device specifications, and using Equation 7, maximum switching frequency is calculated to be, f_{sw-Max} = 1166 kHz.

Since the oscillator can also vary by ±10%, the switching frequency can be further reduced by 10% to add margin. Also, to improve efficiency and reduce power losses due to switching, the switching frequency can be further reduced by about 550 kHz. Therefore f_{sw} = 500 kHz.

From Figure 23, R8 can be approximately determined to be, R8 = 205 kΩ.

Step 2. Calculate the Ripple Current (I_{Ripple})

Using Equation 40, for K_{IND} = 0.2 (typical), inductor ripple current is calculated to be: I_{Ripple} = 0.36 A.

The ripple current is chosen such that the converter enters discontinuous mode (DCM) at 20% of max load. The 20% is a typical value, it could go higher to a maximum of up to 40%.

Step 3. Calculate the Inductor Value (L1)

Using Equation 41, the inductor value is calculated to be, L_{Min} = 22.8 µH. A closest standard inductor value can be used.

Step 4. Calculate the Output Capacitor and ESR (C4)

Calculate capacitance

To calculate the capacitance of the output capacitor, minimum load current must be first determined. Typically, in standby mode the load current is 100 µA, however this really depends on the application. With this value of minimum load current and using Equation 35, Equation 36, and Equation 37, C4 is calculated to be, C4 > 34 µF .

To allow wider operating conditions and improved performance in low-power mode it is recommended to use a 100 µF capacitor. Higher value of output capacitor allows improved transient response during load stepping.

Calculate ESR

Using Equation 38, ESR is calculated to be, R_{ESR} < 555 mΩ.

Capacitors with lowest ESR values should be selected. To meet both the requirements, capacitance and low ESR, several low ESR capacitors may be connected in parallel. In this example, we will select a capacitor with ESR value as 30 mΩ.

Filter capacitor (C12) of value 0.1µF can be added to filter out the noise in the output line.

Step 5. Calculate the Feedback Resistors (R4, R5)

To keep the quiescent current low and avoid instability problems, it is recommended to select R4 and R5 such that, R4 + R5 ~ 250 kΩ.

Using Equation 1 and using a fixed standard value of R4 = 187 kΩ, R5 is calculated to be, R5 = 35.7 kΩ .

Step 6. Calculate Type 3 Compensation Components

Resistances (R6, R9)

Using Equation 19, for VIN_{Typ} = 14 V, V_{Ramp} is calculated to be, V_{Ramp} = 1.4 V.

Using Equation 15, f_{LC} is calculated to be, f_{LC} = 3.33 kHz.

Using V_{Ramp}, f_{LC} from above, assuming f_c as 1/10th of f_{sw} and Equation 46, R6 is calculated to be, R6 = 280.65 kΩ.

Using Equation 47, R9 is calculated to be, R9 = 2.53 kΩ.

Capacitors (C5, C8, C7)

Using Equation 48, C5 is calculated to be, C5 = 340.45 pF.

Using Equation 16, f_{ESR} is calculated to be, f_{ESR} = 53.06 kHz.

Using Equation 50, C8 is calculated to be, C8 = 11.04 pF.

Using Equation 49, C7 is calculated to be, C7 = 250.07 pF.

Step 7. Calculate Soft-Start Capacitor (C6)

The recommended value of soft-start capacitor is 100nF (typical).

Step 8. Calculate Bootstrap Capacitor (C3)

The recommended value of bootstrap capacitor is 0.1 µF (typical).

Step 9. Calculate Power-On Reset Delay Capacitor (C2)

To achieve 2.2-ms delay, the reset delay capacitor can be calculated using Equation 9 to be C2 = 2.2 nF.

Step 10. Calculate Input Capacitor (C1, C11)

Typical values for C11 are 0.1 µF and 0.01 µF.

Input capacitor (C1) should be rated more than the maximum input voltage (VIN_{Max}). The input capacitor should be big enough to maintain supply in case of transients in the input line. Using Equation 34, C1 is calculated to be, C1 = 1.2 µF. For improved transient response, a higher value of C1 such as 220 µF is recommended.

Step 11. Calculate Resistors to Control Slew Rate (R7)

The value of slew rate resistor (R7) can be approximately determined from Figure 24 and Figure 25 at different typical input voltages. The minimum recommended value is 10 kΩ. To achieve rise time, t_r = 20 ns and fall time, t_f = 35 ns, the slew rate resistor is approximately of value 30 kΩ.

Step 12. Resistors to Select Undervoltage, Overvoltage and Reset Threshold Values (R1, R2, R3)

The sum of these three resistors should be approximately equal to 100 kΩ. In this example,

VReg_OV = 106% of V_{Reg} = 5.3 V
VReg_RST = 92% of V_{Reg} = 4.6 V
VReg_UV = 95% of V_{Reg} = 4.75 V

Using Equation 12, R3 = 15 kΩ.

Using Equation 11, R2 = 2.29 kΩ.

Using Equation 10, R1 = 82.6 kΩ

Step 13. Diode D1 and D2 Selection

Diode D1 is used to protect the IC from the reverse input polarity connection. The diode should be rated at maximum load current. Only Schottky diode should be connected at the PH pin. The recommended part numbers are PDS360 and SBR8U60P5.

Step 14. Noise Filter on RST_TH and OV_TH Terminals (C9 and C10)

Typical capacitor values for RST_TH and OV_TH pins are between 10 pF to 100 pF for total resistance on RST_TH/ OV_TH divider of less than 200 kΩ.

Step 15. Power Budget and Temperature Estimation

Using Equation 25, conduction losses for typical input voltage are calculated to be, P_{CON} = 0.289 W.

Assuming slew resistance R7 = 30 kΩ, from Figure 24 and Figure 25, rise time, t_r = 20 ns and fall time, t_f = 35 ns. Using Equation 26, switching losses for typical input voltage are calculated to be, P_{SW} = 0.693 W.

Using Equation 27, gate drive losses are calculated to be, P_{Gate} = 3 mW.

Using Equation 28, power supply losses are calculated to be, P_{IC} = 1.8 mW.

Using Equation 29, the total power dissipated by the device is calculated to be, P_{Total} = 987 mW.

Using Equation 31, and knowing the thermal resistance of package = 35°C/W, the rise in junction temperature due to power dissipation is calculated to be, ΔT = 34.5°C.

Using Equation 32, for a given maximum junction temperature 150°C, the maximum ambient temperature at which the device can be operated is calculated to be, $T_{A\text{-}Max}$ = 115°C (approximately).

Example 2

For this example, we will start with the following known and target parameters:

Table 8.

Known	Input voltage, VIN	minimum=8 V, maximum= 28 V, typical=14 V
Target	Output voltage, V_{Reg}	3.3 V ± 2%
	Maximum output current, $I_{Load-Max}$	2 A
	Ripple/ transient occurring in input voltage, ΔVIN	1% of VIN (minimum)
	Reset threshold, VReg_RST	92% of V_{Reg}
	Overvoltage threshold, VReg_OV	106% of V_{Reg}
	Undervoltage threshold, VReg_UV	95% of V_{Reg}
	Transient response 0.25 A to 2 A load step, ΔV_{Reg}	5% of V_{Reg}
	Power on Reset delay, PORdly	2.2 ms

Step 1. Calculate the Switching Frequency (f_{sw})

To reduce the size of output inductor and capacitor, higher switching frequency can be selected. It is important to understand that higher switching frequency will result in higher switching losses, causing the device to heat up. This may result in degraded thermal performance. To prevent this, proper PCB layout guidelines must be followed (explained in the later section of this document).

Based upon the discussion in section *Selecting the Switching Frequency*, calculate the maximum and minimum duty cycle.

Knowing V_{Reg} and tolerance on V_{Reg}, the $V_{Reg-Max}$ and $V_{Reg-Min}$ are calculated to be:

$V_{Reg-Max}$ = 102% of V_{Reg} = 3.366 V and $V_{Reg-Min}$ = 98% of V_{Reg} = 3.234 V.

Using Equation 6, the minimum duty cycle is calculated to be, D_{Min} = 11.55%

Knowing t_{ON-Min} = 150 ns from the device specifications, and using Equation 7, maximum switching frequency is calculated to be, f_{sw-Max} = 770 kHz.

Since the oscillator can also vary by ±10%, the switching frequency can be further reduced by 10% to add margin. Also, to improve efficiency and reduce power losses due to switching, the switching frequency can be further reduced by about 100 kHz. Therefore f_{sw} = 593 kHz.

From Figure 23, R8 can be approximately determined to be, R8 = 170 kΩ.

Step 2. Calculate the Ripple Current (I_{Ripple})

Using Equation 40, for K_{IND} = 0.2 (typical), inductor ripple current is calculated to be: I_{Ripple} = 0.4 A.

The ripple current is chosen such that the converter enters discontinuous mode (DCM) at 20% of max load. The 20% is a typical value, it could go higher to a maximum of up to 40%.

Step 3. Calculate the Inductor Value (L1)

Using Equation 41, the inductor value is calculated to be, L_{Min} = 12.3 µH. A closest standard inductor value can be used.

Step 4. Calculate the Output Capacitor and ESR (C4, C12)

Calculate capacitance

To calculate the capacitance of the output capacitor, minimum load current must be first determined. Typically, in standby mode the load current is 100 µA, however this really depends on the application. With this value of minimum load current and using Equation 35, Equation 36, and Equation 37, C4 is calculated to be, C4 > 56 µF .

To allow wider operating conditions and improved performance in low-power mode, it is recommended to use a 100 µF capacitor. Higher value of output capacitor allows improved transient response during load stepping.

Calculate ESR

Using Equation 38, ESR is calculated to be, R_{ESR} < 330 mΩ.

Capacitors with lowest ESR values should be selected. To meet both the requirements, capacitance and low ESR, several low ESR capacitors may be connected in parallel. In this example, we will select a capacitor with ESR value as 30 mΩ.

Filter capacitor (C12) of value 0.1µF can be added to filter out the noise in the output line.

Step 5. Calculate the Feedback Resistors (R4, R5)

To keep the quiescent current low and avoid instability problems, it is recommended to select R4 and R5 such that, R4 + R5 ~ 250 kΩ.

Using Equation 1 and using a fixed standard value of R4 = 187 kΩ, R5 is calculated to be, R5 = 59.8 kΩ .

Step 6. Calculate Type 3 Compensation Components

Resistances (R6, R9)

Using Equation 19, for VIN_{Typ} = 14 V, V_{Ramp} is calculated to be, V_{Ramp} = 1.4 V.

Using Equation 15, f_{LC} is calculated to be, f_{LC} = 4.54 kHz.

Using V_{Ramp}, f_{LC} from above, assuming f_c as 1/10th of f_{sw} and Equation 46, R6 is calculated to be, R6 = 244 kΩ.

Using Equation 47, R9 is calculated to be, R9 = 2.9 kΩ.

Capacitors (C5, C8, C7)

Using Equation 48, C5 is calculated to be, C5 = 287.04 pF.

Using Equation 16, f_{ESR} is calculated to be, f_{ESR} = 53.06 kHz.

Using Equation 50, C8 is calculated to be, C8 = 12.84 pF.

Using Equation 49, C7 is calculated to be, C7 = 184.4 pF.

Step 7. Calculate Soft-Start Capacitor (C6)

The recommended value of soft-start capacitor is 100nF (typical).

Step 8. Calculate Bootstrap Capacitor (C3)

The recommended value of bootstrap capacitor is 0.1 µF (typical).

Step 9. Calculate Power-On Reset Delay Capacitor (C2)

To achieve 2.2-ms delay, the reset delay capacitor can be calculated using Equation 9 to be C2 = 2.2 nF.

Step 10. Calculate Input Capacitor (C1, C11)

Typical values for C11 are 0.1 µF and 0.01 µF.

Input capacitor (C1) should be rated more than the maximum input voltage (VIN_{Max}). The input capacitor should be big enough to maintain supply in case of transients in the input line. Using Equation 34, C1 is calculated to be, C1 = 10.53 µF. For improved transient response, a higher value of C1 such as 220 µF is recommended.

Step 11. Calculate Resistors to Control Slew Rate (R7)

The value of slew rate resistor (R7) can be approximately determined from Figure 24 and Figure 25 at different typical input voltages. The minimum recommended value is 10 kΩ. To achieve rise time, t_r = 20 ns and fall time, t_f = 35 ns, the slew rate resistor is approximately of value 30 kΩ.

Step 12. Resistors to Select Undervoltage, Overvoltage and Reset Threshold Values (R1, R2, R3)

The sum of these three resistors should be approximately equal to 100 kΩ. In this example,

VReg_OV = 106% of V_{Reg} = 3.498 V
VReg_RST = 92% of V_{Reg} = 3.036 V
VReg_UV = 95% of V_{Reg} = 3.135 V

Using Equation 12, R3 = 22.87 kΩ.

Using Equation 11, R2 = 3.48 kΩ.

Using Equation 10, R1 = 73.65 kΩ

Step 13. Diode D1 and D2 Selection

Diode D1 is used to protect the IC from the reverse input polarity connection. The diode should be rated at maximum load current. Only Schottky diode should be connected at the PH pin. The recommended part numbers are PDS360 and SBR8U60P5.

Step 14. Noise Filter on RST_TH and OV_TH Terminals (C9 and C10)

Typical capacitor values for RST_TH and OV_TH pins are between 10 pF to 100 pF for total resistance on RST_TH/ OV_TH divider of less than 200 kΩ.

Step 15. Power Budget and Temperature Estimation

Using Equation 25, conduction losses for typical input voltage are calculated to be, P_{CON} = 0.235 W.

Assuming slew resistance R7 = 30 kΩ, from Figure 14 and Figure 15, rise time, t_r = 20 ns and fall time, t_f = 35 ns. Using Equation 22, switching losses for typical input voltage are calculated to be, P_{SW} = 0.913 W.

Using Equation 26, gate drive losses are calculated to be, P_{Gate} = 3.5 mW.

Using Equation 28, power supply losses are calculated to be, P_{IC} = 1.8 mW.

Using Equation 29, the total power dissipated by the device is calculated to be, P_{Total} = 1.15 W.

Using Equation 31, and knowing the thermal resistance of package = 35°C/W, the rise in junction temperature due to power dissipation is calculated to be, ΔT = 40.4°C.

Using Equation 32, for a given maximum junction temperature 150°C, the maximum ambient temperature at which the device can be operated is calculated to be, $T_{A\text{-}Max}$ ~105°C (approximately).

PCB LAYOUT GUIDELINES

The following guidelines are recommended for PCB layout of the TPS54262 device.

Traces and Ground Place Routing

All power (high current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This will reduce EMI radiated by the power traces due to high switching currents. In a two sided PCB, it is recommended to have ground planes on both sides of the PCB to help reduce noise and ground loop errors. The ground connection for the input and output capacitors and IC ground should be connected to this ground plane.

In a multilayer PCB, the ground plane is used to separate the power plane (high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also, it is recommended to arrange the components such that the switching current loops curl in the same direction. This can be done by placing the high current components such that during conduction, the current paths are in the same direction. This will prevent magnetic field reversal caused by the traces between the two half cycles, helping to reduce radiated EMI.

Component Routing for the Feedback Loop

It is recommended to route the feedback traces such that there is minimum interaction with any noise sources associated with the switching components. Recommended practice is to ensure the inductor is placed away from the feedback trace to prevent EMI noise source.

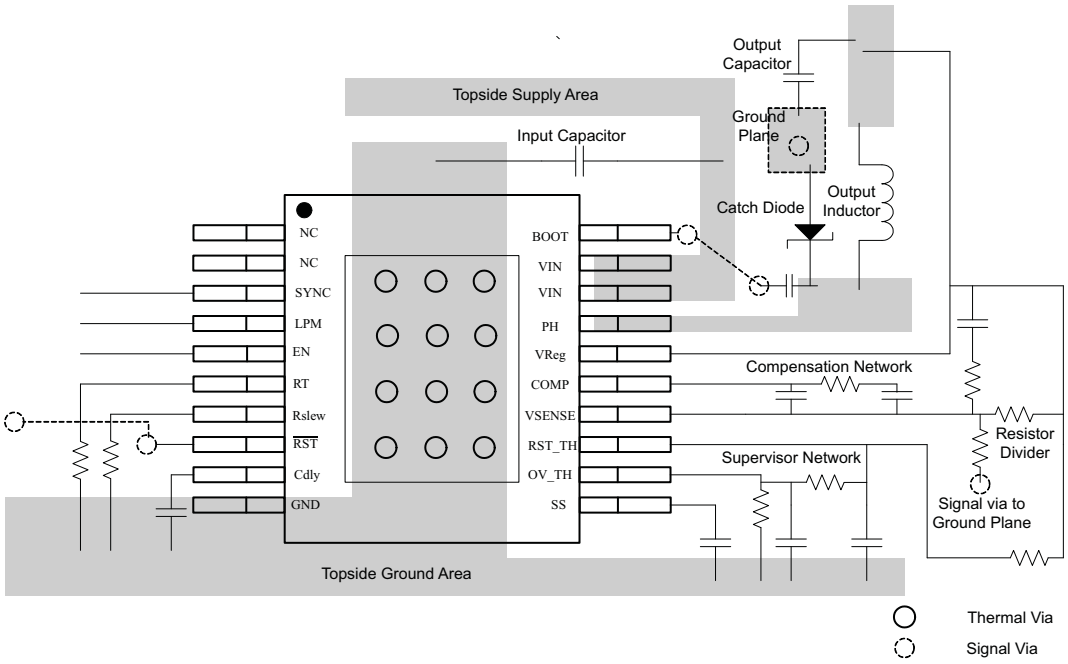


Figure 32. PCB Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS54262QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples

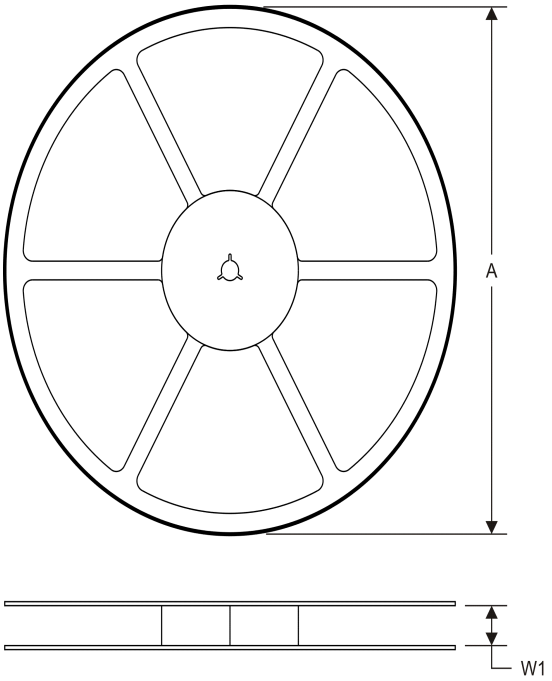
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

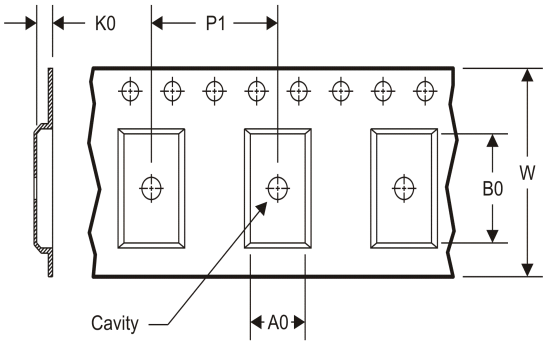
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



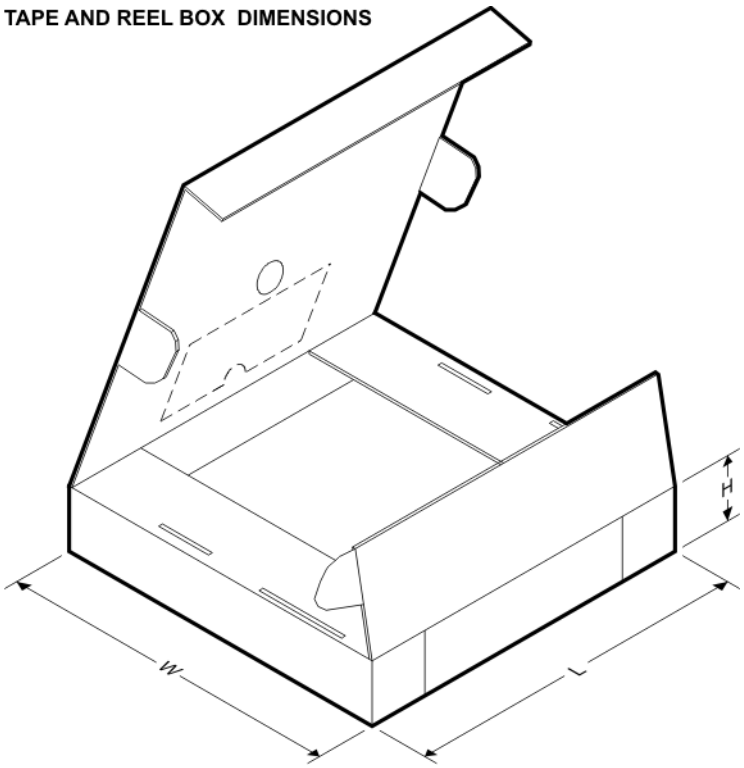
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54262QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

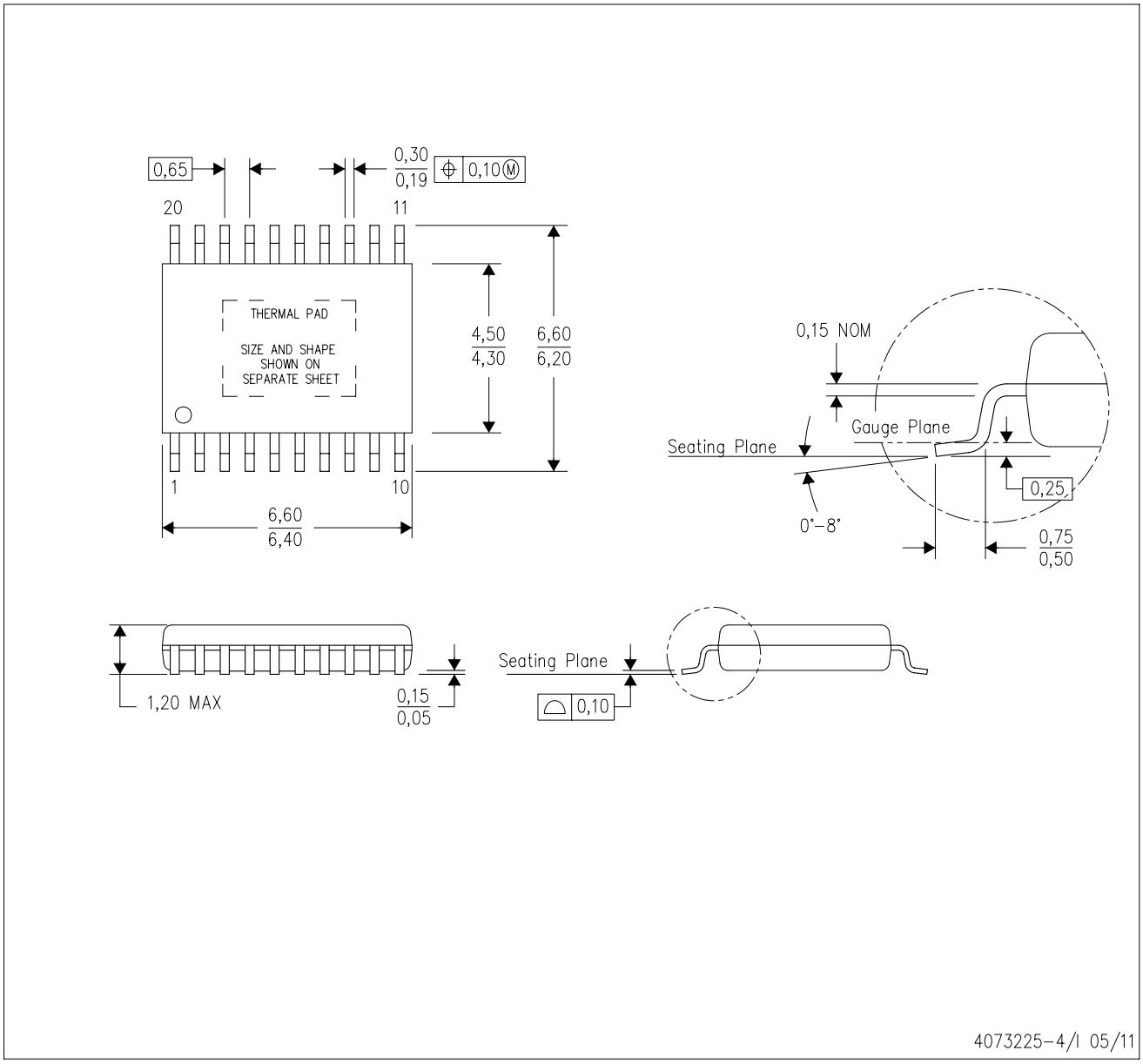
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54262QPWPRQ1	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

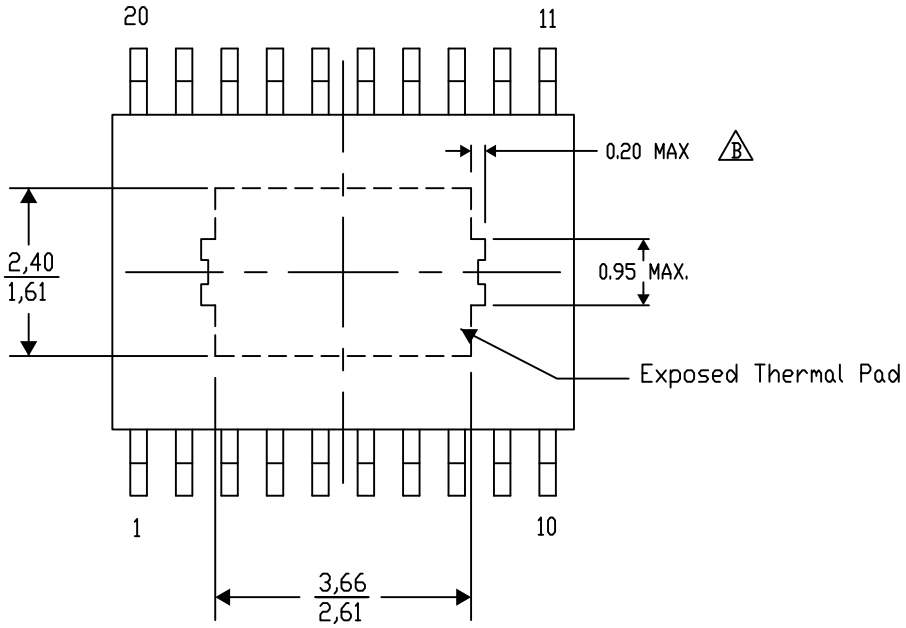
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

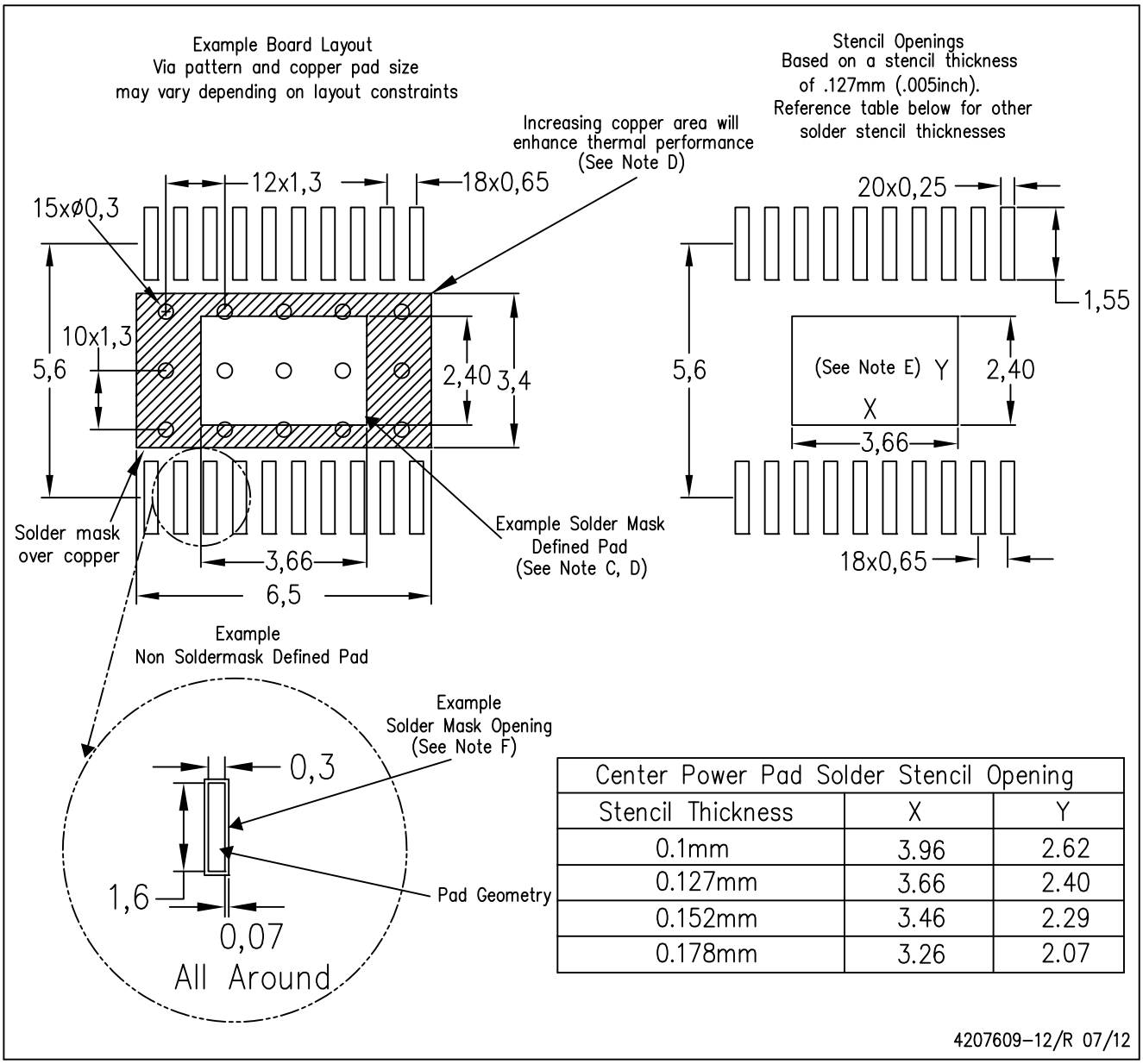
4206332–22/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.96	2.62
0.127mm	3.66	2.40
0.152mm	3.46	2.29
0.178mm	3.26	2.07

4207609–12/R 07/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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