TPS541620 4.5-V to 15-V, Dual 6-A / Single 12-A, Synchronous Step-Down SWIFT™ Converter With Internal Compensation

1 Features

- Integrated 24-mΩ and 10-mΩ MOSFETs with lossless current sensing
- Fixed-frequency, internally-compensated advanced current mode (ACM) control
- Dual output with up to 6 A each output
- Dual-phase, single output for up to 12 A
- Phase interleaving operation for one or two phases
- Synchronization to an external clock using SYNC and CLKO
- 0.5-V to 5.5-V output voltage range
- Four selectable PWM ramp options for each switching frequency to optimize control loop performance
- Soft start time is configurable by an external cap in single-output, multi-phase configuration and is fixed at 1 ms for dual-output configuration
- True differential remote sensing in multi-phase operation
- Independent enable and power good
- Four selectable switching frequency options of 500 kHz, 1 MHz, 1.5 MHz, and 2.0 MHz
- Supports safe pre-biased start-up
- Overtemperature protection with hysteresis
- -40°C to 150°C operation junction temperature
- 3-mm × 5-mm, 25-pin VQFN-HR package with 0.5-mm pitch

2 Applications

- Wireless and wired communications infrastructure equipment
- Ethernet switches and routers
- ASIC, SoC, FPGA, DSP I/O voltage rails
- Industrial test and measurement equipment

3 Description

The TPS541620 is a highly-integrated non-isolated dual DC-DC converter that is capable of high-frequency operation in a 3-mm x 5-mm package. The device can be configured as two single 6-A rails or combined to drive a single 12-A current load. The device implements a fixed-frequency advanced current mode control (ACM) with selectable ramp amplitude configurations to optimize the loop bandwidth. Two mode selection pins (MODE1 and 2) are used to select switching frequency, configuration, clock phase delay, and internal compensation.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS541620	VQFN-HR (25)	3 mm × 5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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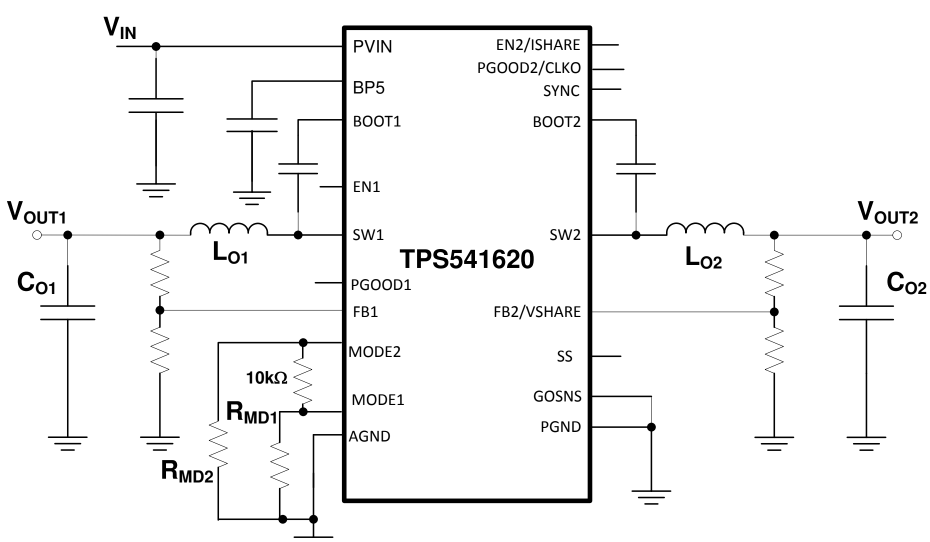

Simplified Schematic (Dual Output)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2021	*	Initial release

5 Pin Configuration and Functions

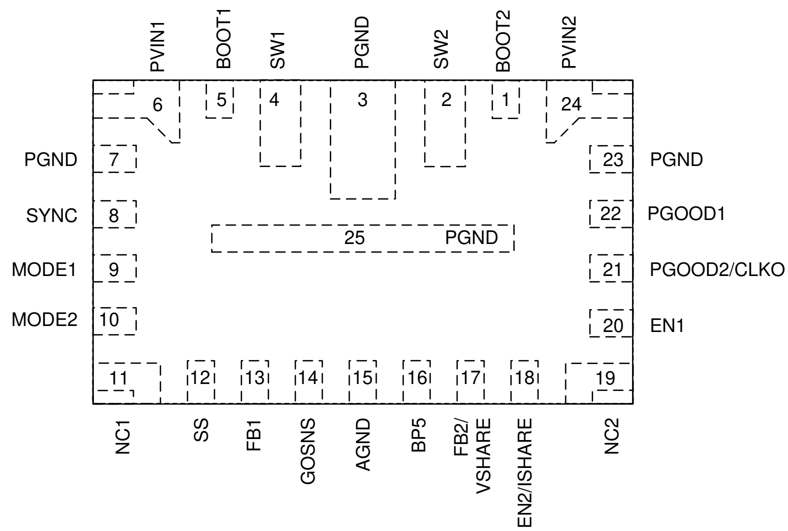

Figure 5-1. 25-Pin VQFN-HR RPB Package (Top View)

Table 5-1. Pin Functions

PIN		I/O/B/P[2]	DESCRIPTION
NAME	NO.		
BOOT2	1	I	Bootstrap pin for the internal flying high-side driver. Connect a typical 100-nF capacitor from this pin to SW2.
SW2	2	B	Channel 2 power stage switch node. Connect this pin to the channel 2 output inductor.
PGND	3, 7, 23, 25	G	Power stage ground return
SW1	4	B	Channel 1 power stage switch node. Connect this pin to the channel 1 output inductor.
BOOT1	5	I	Bootstrap pin for the internal flying high-side driver. Connect a typical 100-nF capacitor from this pin to SW1.
PVIN1	6	I	Power conversion input. Bypass with capacitor from PVIN1 (pin 6) to PGND (pin 7).
SYNC	8	I	Synchronizes to external clock. Tie to BP5 for internal switching frequency. Connect it to an external clock for frequency synchronization.
MODE1	9	I	Pin strap set pin. Connect a resistor from this pin to GND to set supply configurations, dual independent outputs, primary/secondary, and clock delays.
MODE2	10	I	Pin strap set pin. Select from four preselected switching frequencies, each with four settings of compensation.
NC1	11	—	No internal connection
SS	12	O	External soft start for multi-phase configuration only. Place a capacitor from SS to AGND to set output rise time. Float for dual-output configurations. Dual-output mode uses an internal soft start of 1 ms.
FB1	13	I	Feedback input. Connect to the output voltage of channel 1 with a resistor divider for dual-output mode. For multi-phase configuration, FB1 is used for positive input of the remote sense amplifier.
GOSNS	14	I	Connect to ground of the output capacitor as remote sense ground in multi-phase operation. In dual-output mode, simply ground this pin to PGND.
AGND	15	G	Analog ground. Connect to PGND at one single point away from noisy circuitry.
BP5	16	I/O	LDO output. Connect a 1-µF to 4.7-µF capacitor to PGND. BP5 should not be connected to an external load.
FB2/VSHARE	17	I/O	Feedback input. Connect to the output voltage of channel 2 with a resistor divider for dual-output mode. For multi-phase mode, connect to VSHARE of device 2.
EN2/ ISHARE[1]	18	I/O	Enable high to power on. This pin can also be used to externally adjust EN UVLO by connecting a resistor divider between PVIN and AGND.
NC2	19	—	No internal connection

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Table 5-1. Pin Functions (continued)

PIN		I/O/B/P(2)	DESCRIPTION
NAME	NO.		
EN1	20	I	Enable high to power on. This pin can also be used to externally adjust EN UVLO by connecting a resistor divider between PVIN and AGND.
PGOOD2/ CLKO	21	O	Open-drain power-good indicator for channel 2 output
PGOOD1	22	O	Open-drain power-good indicator for channel 1 output
PVIN2	24	I	Power conversion input. Bypass with a capacitor from PVIN2 (pin 24) to PGND (pin 23).

(1) Pin 18 only uses one operating mode for its lifetime.
(2) I = Input, O = Output, B = Bidirectional, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Input Voltage	PVIN	–0.3	16	V
Input Voltage	PVIN to SW1, PVIN to SW2 (10 ns)	–0.3	18	V
Output Voltage	SW1, SW2	–0.3	16	V
Output Voltage	SW1, SW2 transients (10 ns)	–0.3	18	V
Output Voltage	BP5	–0.3	6	V
Input Voltage	BOOT1 – SW1, BOOT2 – SW2	–0.3	6	V
Input Voltage	FB1, FB2/VSHARE	–0.3	6	V
Input Voltage	PGOOD1, PGOOD2/CLKO	–0.3	6	V
Output Voltage	EN1, EN2/ISHARE	–0.3	6	V
Input Voltage	MODE1, MODE2, SS, SYNC	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Input Voltage	PVIN	4.5	15	V
Output Voltage	BP5	–0.1	5.5	V
Input Voltage	BOOT1 - SW1, BOOT2 - SW2	–0.1	5.5	V
Input Voltage	FB1, FB2/VSHARE	–0.1	5.5	V
Output Voltage	PGOOD1, PGOOD2/CLKO	–0.1	5.5	V
Input Voltage	EN1, EN2/ISHARE	–0.1	5.5	V
Input Voltage	MODE1, MODE2, SS, SYNC	–0.1	5.5	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Design the high-side FET to support 100-k hours operation with 0.5% failure rate and 50% switching duty cycle at 0.7*full rated current for T_J = 125°C
(2) Design the low-side FET to support 100-k hours operation with 0.5% failure rate and 96% switching duty cycle at 0.7*full rated current for T_J = 125°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPS541620 RPB (VQFN-HR) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET $R_{DS(ON)}$						
$R_{DS(on)HS}$	High-side FET on-resistance	V_{BST} - V_{SW} = 5 V, T_J = 25°C		24		mΩ
$R_{DS(on)LS}$	Low-side FET on-resistance	BP5 = 5 V, T_J = 25°C		10		mΩ
$t_{DEAD(LtoH)}$	Power stage driver dead-time from low-side off to high-side on(1)	PVIN ≥ 12 V, T_J = 25°C		5		ns
$t_{DEAD(HtoL)}$	Power stage driver dead-time from high-side off to low-side on(1)	PVIN ≥ 12 V, T_J = 25°C		5		ns
R_{SW_disch}	SW discharge FET			27		Ω
INPUT SUPPLY and CURRENT						
V_{PVIN1}, V_{PVIN2}	Power stage voltage		4.5		15	V
$I_{VINSTBY}$	PVIN bias current	T_J = 25°C, EN = 5 V, non-switching		2.5		mA
$I_{VINSTBY}$	PVIN standby current	T_J = 25°C, EN1 = EN2 = 0 V		250		µA
UNDERVOLTAGE LOCKOUT						
V_{PVIN_UVLO}	PVIN UVLO rising threshold	VIN Slew Rate 1 V/1 ms	3.6	3.7	3.9	V
$V_{PVIN\_UVLO\_HYS}$	PVIN UVLO hysteresis			200		mV
V_{BP5}	BP5 regulation voltage	I_{OUT} = 70 mA	4.8	5	5.2	V
$V_{BP5\_UVLO\_RI}$	BP5 rising voltage			3		V
$V_{BP5\_UVLO\_FA}$	BP5 falling voltage			2.7		V
$V_{BP5\_UVLO\_HYS}$	BP5 UVLO hysteresis			300		mV
$V_{DROPOUT}$	LDO dropout voltage	PVIN = 4.5 V, ILOAD = 70 mA			550	mV
INTERNAL REFERENCE VOLTAGE						
Feedback voltage	Feedback voltage	T_J = 25°C		500		mV
Feedback accuracy	Feedback accuracy(1)	T_J = -40°C to 125°C	–1%		1%	
REMOTE SENSE AMPLIFIER						
f_{UGBW}	Unity gain bandwidth			12		MHz
A0	Open loop gain		75			dB
SR	Slew rate			4.7		V/µs
V_{ICM}	Input range		–0.2		0.6	V
V_{OFFSET}	Input offset voltage	0 to 125°C	–1		1	mV
V_{OFFSET}	Input offset voltage	0 to 150°C	–1.5		1.5	mV
EN1 AND EN2 LOGIC THRESHOLD						
$V_{EN\_TO\_SW}$	Enable to start switching	PVIN > 4.0 V, BP5 > 3.0 V		0.3		ms
$V_{EN\_ON\_TH}$	EN rising threshold			1.2	1.3	V
$V_{EN\_OFF\_TH}$	EN falling threshold		1	1.1		V

Over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENHYS}	EN hysteresis			100		mV
I_{EN_pullup}	EN pullup current, EN floating	PVIN = 12 V		1.4		µA
INTERNAL BOOTSTRAP SWITCH						
V_F	BOOTSTRAP voltage drop	I_{boot} = 10 mA			200	mV
V_{BOOT_UVLO}	BOOT UVLO			2.3		V
SWITCHING FREQUENCY						
F_{SW}	F_{SW1}	PVIN = 12 V, V_{OUT} = 1.2 V	450	500	550	kHz
	F_{SW2}	PVIN = 12 V, V_{OUT} = 1.2 V	900	1000	1100	kHz
	F_{SW3}	PVIN = 12 V, V_{OUT} = 1.2 V	1350	1500	1650	kHz
	F_{SW4}	PVIN = 12 V, V_{OUT} = 1.2 V	1800	2000	2200	kHz
t_{on_min}	SW1, SW2 minimum controllable on-time			40		ns
t_{off_min}	SW1, SW2 minimum controllable off-time			150		ns
SYNCHRONIZATION						
$V_{IH(SYNC)}$	High-level input		2			V
$V_{IL(SYNC)}$	Low-level input				0.6	V
D_{SYNC}	Input duty cycle		20%		80%	
$F_{SYNC\ to\ SW}$	Sync to SW variation, % from sync to SW[(1)]		–20%		+20%	
$VCLKO_{High}$	CLKO high-level output	I_O = 20 µA, Cload = 20 pF	2.2			V
VCLKOLow	CLKO low-level output	I_O = 20 µA, Cload = 20 pF			0.4	V
$t_{PSW(CLKO)}$	Pulsewidth output			80		ns
LOOP MANAGER PHASE SHIFT						
tSW12SW2	Phase delay from SW1 to SW2			180		°
$t_{SYNC2SW1(M)}$	PhaseSYNC IN to SW1 delay in 2-phase			216		ns
$t_{SYNC2CLKO(M)}$	PhaseSYNC IN to CLKO delay in 2-phase			53		ns
$t_{CLKO2SW1(M)}$	Phase SW1 to CLKO delay in 2-phase			163		ns
LOOP FOLLOWER PHASE SHIFT						
$t_{SYNC2SW1(S)}$	Phase delay from SYNC IN to SW1			90		°
$t_{SYNC2SW1(S)}$	Phase delay from SYNC IN to SW2			270		°
Tpcsw4, R8 to R11 mode, dual mode	Tpcsw4, R8 to R11 mode, dual mode			163		ns
HIGH SIDE CURRENT DETECTION						
I_{HSOC}	High-side current limit	12 V_{IN}, 1 V_{OUT}, 1 MHz, 0.5µH	8.0	9.0	11.5	A
LOW SIDE CURRENT DETECTION						
I_{LSOC}	Low-side current limit	12 V_{IN}, 1 V_{OUT}, 1 MHz, 0.5µH	6.2	6.8	9	A
I_{LSNOC}	Low-side negative current limit	12 V_{IN}, 1 V_{OUT}, 1 MHz, 0.5µH	-4.2	-3.5	-2.8	A
Low Side Zero Cross	Low-side zero cross		–200			mA
t_{ENTER_HICCUP}	OCP hiccup entry time			16		cycles
t_{HICDLY}	Hiccup delay time	T_{SS} = 1 ms		7		ms
OV / UV PROTECTION						
V_{OVP}	Overvoltage threshold			120%		
t_{OVPDLY}	OVP response time[(1)]			10		µs

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Over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVP}	Undervoltage threshold			80%		
t_{UVPDLY}	UVP response time(1)			16		cycles
THERMAL SHUTDOWN						
T_{SDN}	Built-in thermal shutdown threshold(1)			165		°C
T_{SDN_HYS}	Built-in thermal shutdown hysteresis(1)			20		°C
INTERNAL SOFT START						
$t_{SS\_single\text{-}output}$	Soft start time (from switching to PGOOD high)	Default		1		ms
$t_{SS\_dual\text{-}output}$	Soft start time (from switching to PGOOD high)	Fixed		1		ms
EXTERNAL SOFT START						
I_{C_tSS}	C_{SS} charge current	T_{SS} ≤ 50 ms, C_{SS} < 0.3 µF		2		µA
R_{SS}	Soft-start discharge FET			600		Ω
CURRENT SHARE ACCURACY						
$I_{SHARE(acc)}$	Output current sharing accuracy among stackable devices, defined as the ratio of the current difference between devices to total current(sensing error only)(1)	Load > 0.5 * 6 A		15%		
$I_{SHARE(acc)}$	Output current sharing accuracy among stackable devices, defined as the ratio of the current difference between devices to total current(sensing error only)(1)	Load < 0.5 * 6 A		1		A
V_{ISHARE_L}	Fault voltage falling			200		mV
V_{ISHARE_L}	Fault voltage rising			300		mV
POWER GOOD COMPARATOR						
$V_{PG(thresh)}$	PGOOD1, PGOOD2 threshold	PGOOD out to lower	87%	90%	93%	*V_{REF}
$V_{PG(thresh)}$	PGOOD1, PGOOD2 threshold	PGOOD in from lower	90%	93%	96%	*V_{REF}
$V_{PG(thresh)}$	PGOOD1, PGOOD2 threshold	PGOOD out to higher	107%	110%	113%	*V_{REF}
$V_{PG(thresh)}$	PGOOD1, PGOOD2 threshold	PGOOD in from higher	104%	107%	110%	*V_{REF}
I_{PGD_lkg}	PGOOD1, PGOOD2 leakage current	V(PGOOD1) = V(PGOOD2) = 5.5 V			1	µA
t_{PGDLY}	Delay for PGOOD low to high			50		µs
t_{PGDLY}	Delay for PGOOD high to low			10		µs
V_{PGDLOW}	PGOOD output low voltage	V_{IN} = 4.5 V, V_{OUT} = 0 V, I_{PGOOD} = 6 mA			0.4	V
V_{MINVIN_OUT}	Minimum PVIN for asserted output	V_{PGOOD} ≤ 0.4V			1.5	V

(1) Specified by design. Not production tested.

7 Detailed Description

7.1 Overview

The TPS541620 regulator is an easy-to-use, dual output, synchronous step-down DC-DC converter that operates from 4.5-V to 15-V supply voltage. The device is capable of delivering up to 6-A DC load current per output with exceptional efficiency and thermal performance in a very small solution size. The device is highly configurable where two outputs can be combined to deliver up to 12 A. When the TPS541620 operates in multi-phase mode, phase interleaving enables the following:

- Input and output current and voltage ripple reduction
- Reduced RMS current power dissipation
- Better transient performance
- Use of a small inductor to save board space and cost

The TPS541620 uses a fixed-frequency, internally-compensated advanced current mode control, which reduces design time and requires fewer external components. The switching frequency, internal compensation, and phase operation can be configured using pin strapping. MODE1 (pin 9) configures the phase operation. Table 7-3 shows the resistor values that are required to configure the phase operation and phase offset. The switching frequency can be selected from preset values through pin-strapping on MODE2 (pin 10). Four switching frequency options are available:

- 500 kHz
- 1.0 MHz
- 1.5 MHz
- 2.0 MHz

Each switching frequency has four options of ramp amplitude to optimize the loop bandwidth performance. The TPS541620 is also capable of synchronization to an external clock. The wide switching frequency option allows the device to meet a wide range of design requirements. It can be optimized to a small solution size with higher frequency or to high efficiency with lower switching frequency.

The TPS541620 also features the following:

- Open-drain power-good (PGOOD) flag
- Precision enable
- Internal or adjustable soft start time
- Start-up into pre-bias voltage

It provides a flexible and easy-to-use solution for a wide range of applications. Protection features include the following:

- Thermal shutdown
- BP5 undervoltage lockout
- Cycle-by-cycle current limiting
- Short-circuit hiccup protection

The device pinout is optimized for simple, optimum PCB layout for EMI and thermal performance. The TPS541620 is available in a 3-mm × 5-mm lead-less package.

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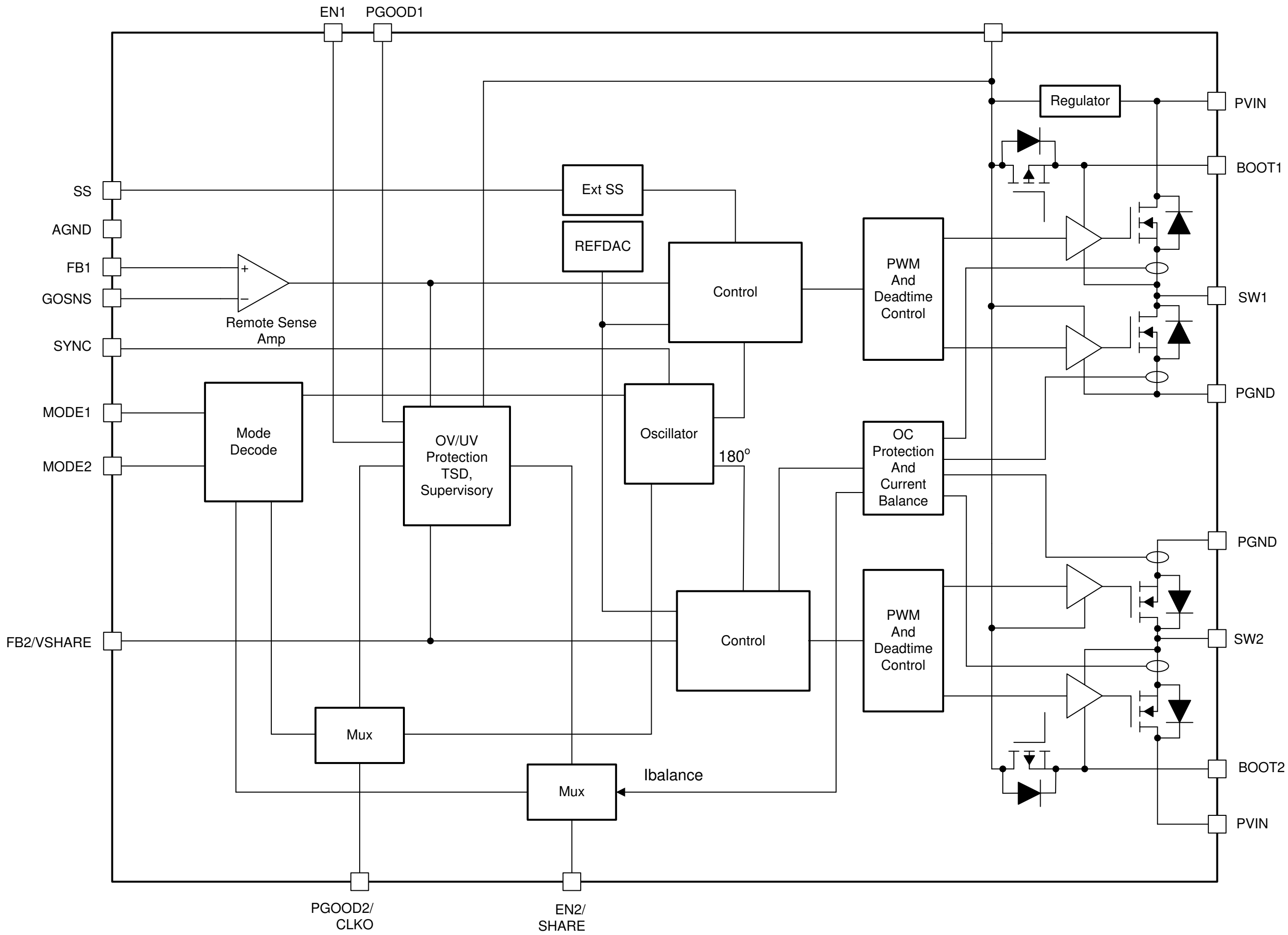
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency, Internal-Compensated Advanced-Current-Mode Control

The TPS541620 synchronous buck converter employs a new control architecture. It supports stable static and transient operation without complex external compensation design. This architecture employs ramp emulation which enables very small duty cycles. The internally-generated ramp is a function of emulating inductor current information, enabling the use of low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). Loop response can be optimized by tuning the amplitude of the internal ramp for different application requirements with various inductor and output capacitor combinations through the MODE2 (pin 10). The TPS541620 is easy to use and allows low external component count for high power density. Fixed-frequency modulation also provides ease-of-filter design to overcome EMI noise.

7.3.2 Enable and UVLO

The precision enable feature of the TPS541620 allows the voltage on the EN1/EN2 pin (V_{EN}) to control the ON/OFF functionality of the device. The EN pin has a 1.4-μA typical internal pullup current source. Floating the EN pin allows the device to start up when a valid input voltage is applied. The TPS541620 switching action and output regulation are enabled when V_{EN} is greater than 1.2 V (typical). While the device is switching, if the EN voltage falls below 1.1 V (typical), the device will stop switching.

It is recommended to enable the device at a voltage greater than the minimum input voltage. Control the turnon and turnoff using a resistor divider on the EN1 (EN2) pin, between VIN and AGND (see Figure 7-1). Set the divider to a voltage greater than the minimum input voltage as shown in Figure 7-2. Select a top enable resistor of 100 kΩ and use Equation 1 for R_{ENB} selection. It is recommended to use divider resistors with 1% tolerance or better and with a temperature coefficient of 100 ppm or lower.

The minimum input voltage of the TPS541620 is 4.5 V, however, the minimum input voltage increases at higher output voltages. Figure 7-2 plots the minimum required input voltage for each of the allowable switching frequencies across the output voltage range. It is recommended to control the turnon and turnoff of the device at an input voltage greater than the minimum shown in Figure 7-2 using a resistor divider on the EN1 (EN2) pin, between VIN and AGND (see Figure 7-1).

$$R_{ENB} = \frac{R_{ENT} \times 1.1}{(V_{IN} - 1.1)} \tag{1}$$

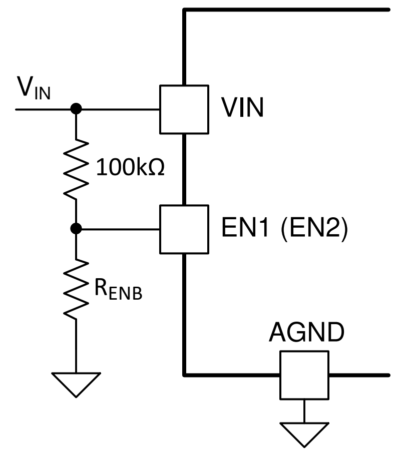


Figure 7-1. Enable ON/OFF Control

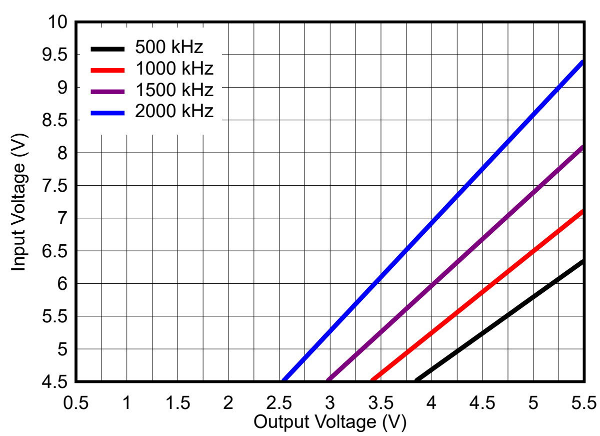


Figure 7-2. Minimum Input Voltage

7.3.3 Internal LDO

The TPS541620 integrates an internal LDO, generating 5 V for control circuitry and MOSFET drivers. The (BP5) LDO output is monitored and generates a power okay signal, enabling internal circuits when the voltage is 3 V or greater. The signal disables internal circuits when the BP5 voltage is 2.7 V or lower. The BP5 pin must have a minimum 1-µF bypass capacitor placed as close as possible to the pin and properly grounded. BP5 is not designed to power external circuitry. The UVLO on BP5 voltage turns off the device when BP5 voltage is below the threshold. It prevents the TPS541620 from operating until the BP5 voltage is enough for the internal circuitry. Hysteresis on UVLO prevents the part from turning off during power up if V_{IN} droops due to momentary input current demands.

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7.3.4 Pre-biased Output Start-up

The device prevents current from being discharged from the output during start-up when a pre-biased output condition exists. If the output is pre-biased, no SW pulses occur until the internal soft-start voltage rises above the error amplifier input voltage (FB pins). As soon as the soft-start voltage exceeds the error amplifier input, SW pulses start, the low-side zero-cross signal is used to shut down the low-side FET for the first eight cycles. This prevents inductor current from reversing and discharging the output voltage. Once the eight cycles are completed, the BOOT to SW cap is charged enough during the off-time periods to turn on the high-side FET completely.

7.3.5 Current Sharing

In instances when a load current higher than 6 A is required by an application, the TPS541620 can be configured to share current. Additionally, the advantage of multi-phase setup is that the output voltage ripple and the input ripple current is reduced by the number of phases in parallel. Pin strapping on the MODE1 pin configures the various modes that current sharing can be enabled as shown in Table 7-3. For applications requiring up to 12 A of load current, the two outputs of the TPS541620 can be connected to enable current sharing between two outputs of a single TPS541620.

7.3.6 Frequency Selection and Minimum On-Time and Off-Time

Switching frequency for the TPS541620 can be configured through the MODE2 pin on the device. The options available to you are the following:

- 500 kHz
- 1 MHz
- 1.5 MHz
- 2.0 MHz

Selecting the appropriate resistor from Table 7-1 sets one of the four options, as well as the ramp capacitor value for compensation.

The device has a minimum on-time of 40 ns (typ.) and a minimum off-time of 150 ns (typ.). Pay attention in applications with minimum duty cycle at high input voltage and maximum duty cycle at low input voltage. The minimum on-time and minimum off-time constrain the output voltage regulation in steady state operation. The device pulse skips if the input voltage, output voltage, and switching frequency require an on-time that is smaller than the minimum controllable on-time of 40 ns. Similarly, the device will operate in dropout when the input voltage, output voltage, and switching frequency require a lower off-time than the controllable off-time of 150 ns. You must always stay away from operating beyond T_{on_min} and T_{off_min} conditions.

7.3.7 Ramp Compensation Selection

Internal ramp voltage is generated from an internal current source charging a capacitor. The current source charges the capacitor with a slope of (VIN-VOUT)/L and discharges with a slope of (VOUT/L) to emulate the inductor ripple current. This ramp is then fed back for control loop regulation and optimization according to required output power stage, duty ratio, and switching frequency. Internal ramp amplitude is set by selecting the appropriate ramp capacitor value. There are four ramp capacitor values available to you:

- 1.5 pF
- 2.5 pF
- 4 pF
- 6 pF

These can be selected through the MODE pins. For the best performance, TI recommendeds using 1.5 pF for output voltage less or equal to 4 V. For output voltage higher than 4 V, use 2.5 pF. In some cases, a feedforward capacitor in parallel with a top-side feedback resistor is recommended to boost phase margin.

Connecting the pin-strapping resistor from MODE2 to ground selects the ramp capacitor value along with other functions. The MODE2 pin is also used to set your desired switching frequency. Every switching frequency opnion (F_{SW}) has four ramp capacitor values to allow you to tune the transient performance. Table 7-1 shows the pin-strapping resistor options for switching frequency and internal ramp capacitor. For dual-output mode operation, which includes an application with two one-phase outputs, MODE1 provides the selection of the internal ramp capacitor for VOUT2 as shown in Table 7-3. VOUT1 ramp is set by MODE2 as shown in Table 7-1.

Table 7-1. MODE2 Pin-Strap Configuration

RESISTOR FROM MODE2 TO AGND (kΩ)	FREQUENCY (kHz)	RAMP CAPACITOR VALUE FOR VOUT1 (pF)
10.7	500	1.5
12.1		2.5
13.7		4
15.4		6
17.4	1000	1.5
19.6		2.5
22.1		4
24.9		6
28.7	1500	1.5
33.2		2.5
38.3		4
45.3		6
53.6	2000	1.5
64.9		2.5
78.7		4
100		6

7.3.8 Soft Start

The soft-start feature is used to prevent inrush current impacting the TPS541620 and its supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. For dual-output applications, the external soft start is disabled and the outputs turn on with an internally-set soft start time of 1 ms. In this situation, leave the SS pin floating. The external soft start is enabled when the device is configured in multi-phase operation. Multi-phase applications that deliver high load current can have a large amount of capacitance at the output. The soft-start time for such applications can be extended by connecting an external capacitor C_{SS} from the SS pin to AGND to make sure there is no sudden current surge. Extended soft-start time further reduces the supply current required to charge up output capacitors and supply any output loading. An internal current source (I_{Ct_SS} = 2 µA) charges C_{SS} and generates a ramp from 0 V to V_{FB} to control the ramp-up rate of the output voltage. The soft-start capacitor C_{SS} is discharged through an internal FET of 600-Ω resistance when V_{OUT} is shut down by fault protection or EN low. The total time required to discharge the soft-start capacitor completely is 500 µs. When a large value of C_{SS} is connected and EN is toggled low only for a short period of time, C_{SS} may not be fully discharged. The next soft-start ramp follows the internal soft-start ramp before reaching the leftover voltage on C_{SS} and then follows the ramp programmed by C_{SS}.

7.3.9 Remote Sense Function

The device supports differential remote sense function for accurate output regulation. In multi-phase configuration, FB1 and GOSNS pins are used for remote sensing purpose. If feedback resistors are required for output voltage programming, the FB1 pin must be connected to the mid-point of the resistor divider. Additionally, the GOSNS pin must always be connected to the load return. If feedback resistors are not required, the FB1 pin must be connected to the positive sensing point of the load. Additionally, the GOSNS pin should always be connected to the load return. The FB1 and GOSNS pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider must use resistor values much less than 100 kΩ to reduce susceptibility to noise. A simple rule of thumb is to use a 10-kΩ lower divider resistor and then size the upper resistor to achieve the desired ratio.

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7.3.10 Adjustable Output Voltage

The voltage regulation loop in the TPS541620 regulates the FB pin voltage to be equal to the internal reference voltage. The output voltage of the TPS541620 is set by a resistor divider to program the ratio from V_{OUT} to V_{FB}. The resistor divider is connected from the output to ground with the mid-point connecting to the FB pin (V_{FB} = 0.5 V).

The internal voltage reference and feedback loop produce precise voltage regulation over temperature. TI recommends using divider resistors with 1% tolerance or better, and with a temperature coefficient of 100 ppm or lower for increased DC accuracy over temperature. Typically, R_{FBT} (top feedback resistor) equal to 10 kΩ to 100 kΩ is recommended. Larger R_{FBT} and R_{FBB} (bottom feedback resistor) values reduce the quiescent current going through the divider, which helps maintain high efficiency at very light load. However, larger divider values also make the feedback path more susceptible to noise. R_{FBB} can be calculated by Equation 2.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \tag{2}$$

7.3.11 Power Good

The power good pins (PGOOD1, PGOOD2) are open-drain outputs that must be connected to a pullup resistor of 10 kΩ to a source less than 5.5 V (for example, BP5) to indicate the output voltage is within the PGOOD window. The PGOOD detection is activated after soft start is completed. When the output voltage falls within a window of ±10% of the target, there is a 50-µs delay after soft start is finished and PGOOD goes high. If the output voltage falls outside of ±10% of target voltage during operation, PGOOD is pulled low after a 10-µs delay. The PGOOD feature is active while the voltage at PVIN pin is either equal to or greater than 1.5 V.

7.3.12 Overcurrent Protection

The device detects low-side (LS) current during off-time and high-side (HS) current during on-time. The device will respond to an overcurrent fault when soft start is done.

Low-side Overcurrent Protection:

The device monitors valley current during HS off-time. If the inductor current is above the valley current limit threshold, the next HS pulse is skipped, the LS FET remains on, and an internal counter increments. This counter counts as long as inductor current is higher than valley at the clock edge. If the current goes below valley at the clock edge, the counter is reset.

If the counter is able to count to 16 cycles without reset, then it is identified as a current limit fault and the device hiccups. The device enters hiccup for seven cycles of internal soft start and then attempts a normal soft start.

High-side Overcurrent Limit:

The device implements a high-side overcurrent limit-to-limit peak current and prevents the inductor from saturation when a short circuit happens. When the device hits peak current limit, the HS FET turns off and the LS FET turns on. Once the inductor current clears the valley limit, the HS FET turns on at the next clock edge.

Negative Overcurrent Protection:

When the inductor current goes below the negative overcurrent threshold, the low-side FET turns off. It turns on again at the next clock pulse.

7.3.13 Overvoltage and Undervoltage Protection

The device includes both output overvoltage protection and output undervoltage protection capability. The device compares the FB voltage to internal preset voltages. If the FB voltage with respect to GOSNS voltage rises above the output overvoltage protection threshold after a 10-µs delay, the device terminates normal switching and enters continuous hiccup process. The device waits for 7 × T_{ss} and tries to restart. Overvoltage protection is enabled both during and after soft start is completed.

If the FB pin voltage with respect to GOSNS falls below the undervoltage protection threshold, the device enters hiccup after 7 × T_{ss} of wait time. Undervoltage protection is enabled after soft start is completed.

7.3.14 Overtemperature Protection

An internal temperature sensor protects the devices from thermal runaway. The internal thermal shutdown threshold, T_{SD}, is fixed at 165°C typical with 20°C hysteresis. When the devices sense a temperature above T_{SD}, power conversion stops until the sensed junction temperature falls by the thermal shutdown hysteresis amount. Then, the device starts up again.

7.3.15 Frequency Synchronization

The TPS541620 device can synchronize to an external clock, which must fall in the ±20% range of the internal frequency setting. For a standalone device, the external clock must be applied to the SYNC pin. A sudden change in synchronization clock frequency causes an associated control loop response. This change results in an overshoot or undershoot on the output voltage. When external sync is lost, the IC switches to its internal preset switching frequency.

When the device is synchronized to an external clock signal, if the external clock signal is missing, the device switches back to 75% of the preset free running frequency for approximately eight cycles. After that, the device runs at its free running frequency.

The following occurs in dual-phase configuration with external clock:

- Both the outputs of the device are tied together.
- Switching frequency is set by the clock received at the SYNC pin of the device.
- Clock phase shift is set by MODE1 pin of the device. See Current Sharing for more details.
- GOSNS functions as the GND remote sense input.

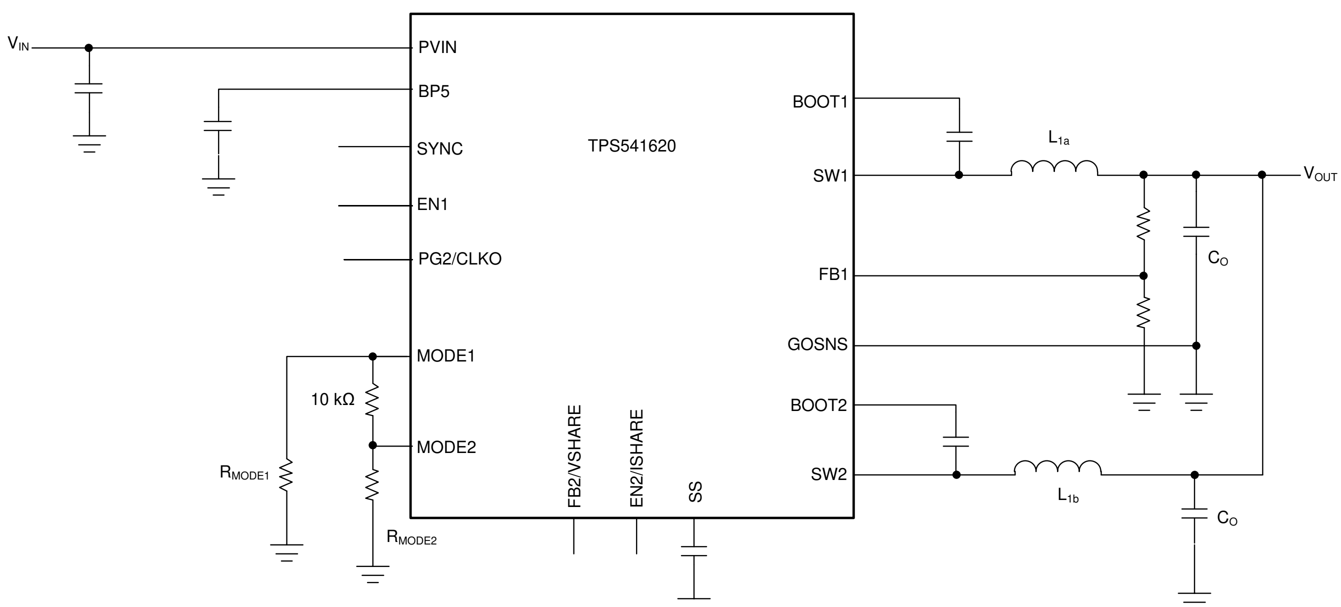

Figure 7-3. Dual-phase Configuration with External Clock

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7.4 Device Functional Modes

7.4.1 Operation Mode

The TPS541620 is a highly-configurable device. It can be configured through pin strapping on the MODE1 and MODE2 pins. Table 7-1, Table 7-2, and Table 7-3 show what aspects of the device can be configured by the respective mode pins.

Table 7-2. MODE1 and MODE2 Pin Functions

PIN	FUNCTION 1	FUNCTION 2
MODE1	Phase setting for single and multi phase operation	Compensation tuning on VOUT2 in dual-output conditions
MODE2	Frequency and compensation tuning on output in multi-phase operation or VOUT1 in dual-output operation	

Table 7-3. MODE1 Pin-Strap Configuration

RESISTOR FROM MODE1 TO AGND (kΩ)	OPERATION MODE	PHASE POSITION FOR CHANNEL 1	PHASE POSITION FOR CHANNEL 2	RAMP CAPACITOR FOR VOUT2 (pF)	NOTES
10.7	In two-phase configuration	0°	180°		Sets phase positions for the two outputs of the device.
15.4	Dual-output independent single phase	0°	180°	1.5	Sets phase position for both channels in dual-output independent single phase operation to 0° and 180°. Sets ramp capacitor value for VOUT2.
17.4				2.5	
19.6				4	
22.1				6	
24.9	Dual-output independent single phase	90° from Sync	270° from Sync	1.5	Sets phase position for both channels in dual output independent single phase operation to 90° and 270°. Sets ramp capacitor value for VOUT2.
28.7				2.5	
33.2				4	
38.3				6	

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS541620 is a synchronous buck regulator designed for 4.5-V to 15-V input and two 6-A loads. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors.

8.2 Typical Application - Dual Independent Outputs

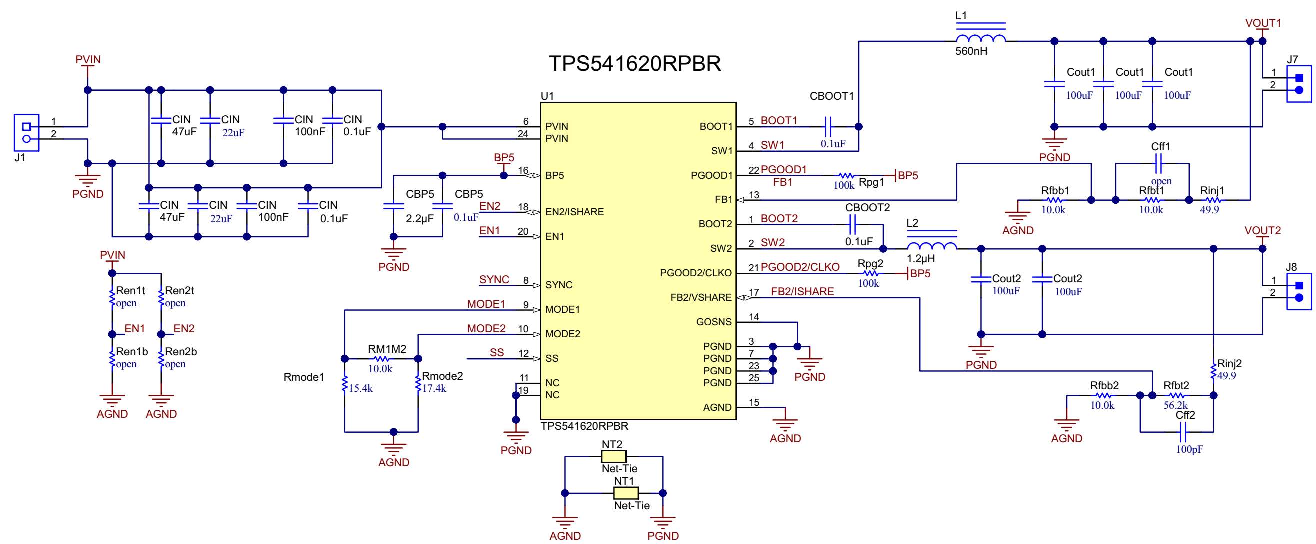

Figure 8-1. 12-V Input, 1.0-V and 3.3-V Dual Output Regulator Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	7 to 15 V, 12 V nominal
Output voltage (V_{OUT1})	1.0 V
Output current rating (I_{OUT1})	6 A
Steady state output ripple voltage	10 mV
Output current load step	3 A
Transient response	± 50 mV (± 5%)
Output voltage (V_{OUT2})	3.3 V
Output current rating (I_{OUT2})	6 A
Steady state output ripple voltage	33 mV
Output current load step	3 A
Transient response	± 165 mV (± 5%)
Switching frequency (f_{SW})	1000 kHz
Soft start time	Internal
Operating temperature	25°C

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8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The first step is to decide on a switching frequency. The TPS541620 can operate at four different frequencies from 500 kHz to 2.0 MHz. f_{SW} is set by the resistor value from the MODE2 pin to ground. Typically, the highest switching frequency possible is desired because it produces the smallest solution size or lower switching frequency for a more efficient converter. The minimum controllable on-time and maximum off-time affect the input voltage range and switching frequency.

The maximum switching frequency for a given application can be limited by the minimum on-time of the regulator and the maximum f_{SW} can be estimated with Equation 3. Using the minimum 50-ns on-time, 15-V maximum input voltage, and the lower voltage of the dual-output 1 V for this application, the maximum switching frequency is 1333 kHz. The minimum regulating input voltage is limited by the maximum off-time, switching frequency, and output voltage. Using the maximum off-time of 150 ns, 7-V minimum input voltage, and the higher voltage of the dual-output 3.3 V for this application with Equation 4, the maximum switching frequency from 3.3 V and maximum off-time is 3524 kHz.

The selected switching frequency must also consider the tolerance of the switching frequency. A switching frequency of 1000 kHz is selected for a good balance of solution size and efficiency. To set the frequency to 1000 kHz, the selected MODE2 resistor is 17.4 kΩ per Table 7-1. To set for dual-output configuration, select a MODE1 resistor is 15.4 kΩ per Table 7-3.

$$fsw = \frac{Vout\,min}{ton \times Vin\,max} = \frac{1\ V}{50\ ns \times 15\ V} = 1333\ kHz \tag{3}$$

$$fsw = \frac{1 - \frac{Vout\,max}{Vin\,min}}{toff} = \frac{1 - \frac{3.3\ V}{7\ V}}{150\ ns} = 3524\ kHz \tag{4}$$

Figure 8-2 shows the maximum recommended input voltage versus output voltage for each FSEL frequency. Figure 8-2 uses the maximum minimum on-time of 50 ns and includes 10% tolerance on the switching frequency.

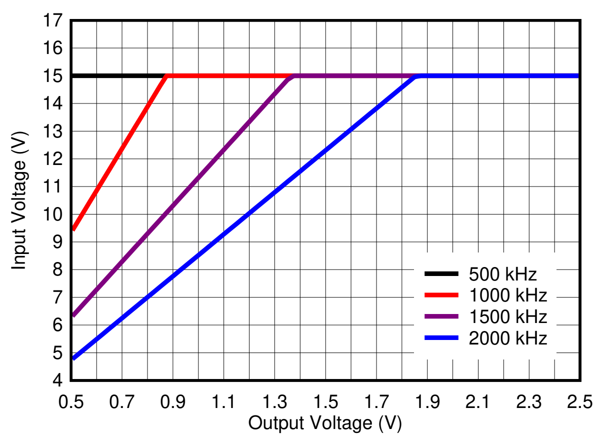

Figure 8-2. Maximum Input Voltage Versus Output Voltage

8.2.2.2 Output Inductor Selection

To calculate the effective value of the output inductor, use Equation 5. K is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Choosing small inductor ripple currents (through a large inductor) can degrade the transient response performance. The inductor ripple, K, is normally 0.1 to 0.4 for the majority of applications, giving a peak-to-peak ripple current range of 0.6 A to 2.4 A. The target Iripple must be 0.3 A or larger.

For this design example, K = 0.3 is used and the inductor values Lo1 and Lo2 are calculated to be 0.506 µH and 1.329 µH, respectively. An inductor with an inductance of 0.56 µH is selected for Vout1 and 1.2 µH for Vout2. It is important that the RMS (Root Mean Square) current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found in Equation 7 and Equation 8, respectively. For Vout1 in this design, the RMS inductor current is 6.019 A and the peak inductor current is 6.833 A. The chosen inductor is a Coilcraft XAL6030-561. For Vout2 in this design, the RMS inductor current is 6.032 A and the peak inductor current is 7.073 A. The chosen inductor for Vout2 is a Coilcraft XAL6030-122. XAL6030-561 has a saturation current rating of 29 A, an RMS current rating of 17 A, and a typical DC series resistance of 3.01 mΩ. The XAL6030-122 has a saturation current rating of 22 A, an RMS current rating of 13 A, and a typical DC series resistance of 6.8 mΩ.

The peak current through the inductor is the inductor ripple current plus the DC output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in Equation 8. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify the current ratings of the inductor based on the switch current limit rather than the steady-state peak inductor current.

$$\mathrm{Lo1} = \frac{(\mathrm{Vin} - \mathrm{Vout})}{\mathrm{K} \times \mathrm{Iout}}\left(\frac{\mathrm{Vout}}{\mathrm{Vin} \times \mathrm{fsw}}\right) = \frac{(12\ \mathrm{V} - 1\ \mathrm{V})}{0.3 \times 6\ \mathrm{A}}\left(\frac{1\ \mathrm{V}}{12\ \mathrm{V} \times 1000\ \mathrm{kHz}}\right) = 0.506\ \mu\mathrm{H}$$

$$\mathrm{Lo2} = \frac{(\mathrm{Vin} - \mathrm{Vout})}{\mathrm{K} \times \mathrm{Iout}}\left(\frac{\mathrm{Vout}}{\mathrm{Vin} \times \mathrm{fsw}}\right) = \frac{(12\ \mathrm{V} - 3.3\mathrm{V})}{0.3 \times 6\ \mathrm{A}}\left(\frac{3.3\ \mathrm{V}}{12\ \mathrm{V} \times 1000\ \mathrm{kHz}}\right) = 1.329\ \mu\mathrm{H} \tag{5}$$

$$\mathrm{Iripple1} = \frac{(\mathrm{Vinmax} - \mathrm{Vout1})}{\mathrm{Lo\_eff} \times \mathrm{N}}\left(\frac{\mathrm{Vout1}}{\mathrm{Vinmax} \times \mathrm{fsw}}\right) = \frac{(15\ \mathrm{V} - 1\ \mathrm{V})}{0.56\ \mu\mathrm{H} \times 1}\left(\frac{1\ \mathrm{V}}{15\ \mathrm{V} \times 1000\ \mathrm{kHz}}\right) = 1.667\ \mathrm{A}$$

$$\mathrm{Iripple2} = \frac{(\mathrm{Vinmax} - \mathrm{Vout2})}{\mathrm{Lo\_eff} \times \mathrm{N}}\left(\frac{\mathrm{Vout2}}{\mathrm{Vinmax} \times \mathrm{fsw}}\right) = \frac{(15\ \mathrm{V} - 3.3\ \mathrm{V})}{1.2\ \mu\mathrm{H} \times 1}\left(\frac{3.3\ \mathrm{V}}{15\ \mathrm{V} \times 1000\ \mathrm{kHz}}\right) = 2.145\ \mathrm{A} \tag{6}$$

$$I_{L1(RMS)} = \sqrt{\left(\frac{I_{OUT1}}{N}\right)^2 + \frac{{I_{RIPPLE1}}^2}{12}} = \sqrt{\left(\frac{6}{1}\right)^2 + \frac{(1.667\ \mathrm{A})^2}{12}} = 6.019\ \mathrm{A}$$

$$I_{L2(RMS)} = \sqrt{\left(\frac{I_{OUT2}}{N}\right)^2 + \frac{{I_{RIPPLE2}}^2}{12}} = \sqrt{\left(\frac{6}{1}\right)^2 + \frac{(2.145\ \mathrm{A})^2}{12}} = 6.032\ \mathrm{A} \tag{7}$$

$$I_{L1(PEAK)} = \frac{I_{OUT1}}{N} + \frac{I_{RIPPLE1}}{2} = 6\ \mathrm{A} + \frac{1.667\ \mathrm{A}}{2} = 6.833\ \mathrm{A}$$

$$I_{L2(PEAK)} = \frac{I_{OUT2}}{N} + \frac{I_{RIPPLE2}}{2} = 6\ \mathrm{A} + \frac{2.145\ \mathrm{A}}{2} = 7.073\ \mathrm{A} \tag{8}$$

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8.2.2.3 Output Capacitor

The two primary considerations for selecting the value of the output capacitor are how the regulator responds to a large change in load current and the output voltage ripple. The third consideration is to ensure converter stability, which is typically met from the first two considerations. The output capacitance needs to be selected based on the most stringent of these criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop needs to sense the change in the output voltage then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically, the loop bandwidth is near $f_{SW}/10$. Equation 9 estimates the minimum output capacitance necessary, where I_{STEP} is the change in output current and V_{TRANS} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 5% change in V_{OUT1} for a load step of 3 A. Therefore, I_{STEP1} is 3 A and V_{TRANS1} is 50 mV. Using this target gives a minimum output capacitance of 95.5 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response. Similarly, I_{STEP2} is 3 A and V_{TRANS2} is 165 mV, which gives a minimum output capacitance of 28.9 µF.

$$C_{OUT1\_LOOP} > \frac{I_{STEP1}}{V_{TRANS1}} \times \frac{1}{2\pi \times \frac{fsw}{10}} = \frac{3\text{ A}}{50\text{ mV}} \times \frac{1}{2\pi \times \frac{1000\text{ kHz}}{10}} = 95.5\ \mu\text{F}$$

$$C_{OUT2\_LOOP} > \frac{I_{STEP2}}{V_{TRANS2}} \times \frac{1}{2\pi \times \frac{fsw}{10}} = \frac{3\text{ A}}{165\text{ mV}} \times \frac{1}{2\pi \times \frac{1000\text{ kHz}}{10}} = 28.9\ \mu\text{F} \tag{9}$$

In addition to the loop bandwidth, it is possible for the inductor current slew rate to limit how quickly the regulator responds to the load step. For low duty cycle applications, the time it takes for the inductor current to ramp down after a load step down can be the limiting factor. Equation 10 estimates the minimum output capacitance necessary to limit the output voltage undershoot after a load step up. Equation 11 estimates the minimum output capacitance necessary to limit the change in the output voltage overshoot after a load step down. Using the selected 0.56-µH inductance gives a minimum capacitance of 4.6 µF for V_{OUT1} to meet the undershoot requirement due to a load step-up. Using the selected 0.56-µH inductance gives a minimum capacitance of 50.4 µF for V_{OUT1} to meet the overshoot requirement due to a load step down. Using the selected 1.2-µH inductance for V_{OUT2} gives a minimum output capacitance of 3.8 µF and 9.9 µF to meet the undershoot and overshoot requirements, respectively.

$$C_{OUT1\_UNDERSHOOT} > \frac{Lo1 \times I_{STEP}^2}{2 \times V_{TRANS} \times (Vin - V_{OUT1})} > \frac{0.56\ \mu\text{H} \times (3\text{ A})^2}{2 \times 50\text{ mV} \times (12\text{ V - 1 V})} = 4.6\ \mu\text{F}$$

$$C_{OUT2\_UNDERSHOOT} > \frac{Lo2 \times I_{STEP}^2}{2 \times V_{TRANS} \times (Vin - V_{OUT2})} > \frac{1.2\ \mu\text{H} \times (3\text{ A})^2}{2 \times 165\text{ mV} \times (12\text{ V - 3.3 V})} = 3.8\ \mu\text{F} \tag{10}$$

$$C_{OUT1\_OVERSHOOT} > \frac{Lo1 \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT1}} = \frac{0.56\ \mu\text{H} \times (3\text{ A})^2}{2 \times 50\text{ mV} \times 1\text{ V}} = 50.4\ \mu\text{F}$$

$$C_{OUT2\_OVERSHOOT} > \frac{Lo2 \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT2}} = \frac{1.2\ \mu\text{H} \times (3\text{ A})^2}{2 \times 165\text{ mV} \times 3.3\text{ V}} = 9.9\ \mu\text{F} \tag{11}$$

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{sw} is the switching frequency, $V_{RIPPLE1}$ is the maximum allowable steady-state output voltage ripple, and $I_{RIPPLE1}$ is the inductor ripple current. In this case, the target maximum steady-state output voltage ripple is 10 mV for V_{OUT1}. Under this requirement, Equation 12 yields 20.8 µF. Similarly, $V_{RIPPLE2}$ is the maximum allowable V_{OUT2} steady-state output voltage ripple, and $I_{RIPPLE2}$ is the inductor ripple current for V_{OUT2}. For 33-mV steady-state output voltage ripple, Equation 12 yields 8.13 µF for V_{OUT2}.

$$C_{OUT1\_RIPPLE} > \frac{I_{RIPPLE1}}{8 \times V_{RIPPLE1} \times f_{SW}} = \frac{1.667\ A}{8 \times 10\ mV \times 1000\ kHz} = 20.8\ \mu F$$
$$C_{OUT2\_RIPPLE} > \frac{I_{RIPPLE2}}{8 \times V_{RIPPLE2} \times f_{SW}} = \frac{2.145\ A}{8 \times 33\ mV \times 1000\ kHz} = 8.13\ \mu F \quad (12)$$

Lastly, if an application does not have a stringent load transient response or output ripple requirement, a minimum amount of capacitance is still required to ensure the control loop is stable with the lowest gain ramp setting on the MODE pin. Equation 13 estimates the minimum capacitance needed for loop stability. Equation 13 sets the minimum amount of capacitance by keeping the LC frequency at a maximum of 1/30th the switching frequency. Equation 13 gives a minimum capacitance of 40.7 µF and 19 µF for V_{OUT1} and V_{OUT2}, respectively.

$$C_{OUT1\_STABILITY} > \left(\frac{15}{\pi \times fsw}\right)^2 \times \frac{1}{Lo1} = \left(\frac{15}{\pi \times 1000\ kHz}\right)^2 \times \frac{1}{0.56\ \mu H} = 40.7\ \mu F$$
$$C_{OUT2\_STABILITY} > \left(\frac{15}{\pi \times fsw}\right)^2 \times \frac{1}{Lo2} = \left(\frac{15}{\pi \times 1000\ kHz}\right)^2 \times \frac{1}{1.2\ \mu H} = 19\ \mu F \quad (13)$$

Equation 14 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and shows that the ESR should be less than 6 mΩ for V_{OUT1}. This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If you are using non-ceramic capacitors as a starting point, the ESR should be below the values calculated in Equation 14 and Equation 15 to meet both the ripple and transient response requirements. For more accurate calculations or if you are using mixed output capacitors, the impedance of the output capacitors should be used to determine if the ripple and transient requirements can be met. Similary, Equation 14 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification. This shows the ESR should be less than 15.4 mΩ for V_{OUT2}. In this case, ceramic capacitors are used and the combined ESR of the ceramic capacitors in parallel is much less than is needed to meet the ripple.

$$R_{ESR1\_RIPPLE} < \frac{V_{RIPPLE1}}{I_{RIPPLE1}} = \frac{10\ mV}{1.667\ A} = 6.00\ m\Omega$$
$$R_{ESR2\_RIPPLE} < \frac{V_{RIPPLE2}}{I_{RIPPLE2}} = \frac{33\ mV}{2.145\ A} = 15.4\ m\Omega \quad (14)$$

$$R_{ESR1\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{50\ mV}{3\ A} = 16.7\ m\Omega$$
$$R_{ESR2\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{165\ mV}{3\ A} = 55\ m\Omega \quad (15)$$

Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheet specifies the RMS value of the maximum ripple current. Equation 16 can be used to calculate the RMS ripple current the output capacitor needs to support.

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$$\mathrm{Ico1rms} = \frac{(\mathrm{Vinmax} - \mathrm{Vout1})}{\sqrt{12} \times \mathrm{Lo1}} \left(\frac{\mathrm{Vout1}}{\mathrm{Vinmax} \times \mathrm{fsw}} \right) = \frac{(15\ \mathrm{V} - 1\ \mathrm{V})}{\sqrt{12} \times 0.56\ \mu\mathrm{H}} \left(\frac{1\ \mathrm{V}}{15\ \mathrm{V} \times 1000\ \mathrm{kHz}} \right) = 0.481\ \mathrm{A}$$

$$\mathrm{Ico2rms} = \frac{(\mathrm{Vinmax} - \mathrm{Vout2})}{\sqrt{12} \times \mathrm{Lo2}} \left(\frac{\mathrm{Vout2}}{\mathrm{Vinmax} \times \mathrm{fsw}} \right) = \frac{(15\ \mathrm{V} - 3.3\ \mathrm{V})}{\sqrt{12} \times 1.2\ \mu\mathrm{H}} \left(\frac{3.3\ \mathrm{V}}{15\ \mathrm{V} \times 1000\ \mathrm{kHz}} \right) = 0.619\ \mathrm{A} \tag{16}$$

For this application, Equation 16 yields 0.481 A and 0.619 A, for V_{OUT1} and V_{OUT2}, respectively. Ceramic capacitors typically have a ripple current rating much higher than this. Select X5R and X7R ceramic dielectrics or equivalent for power regulator capacitors since they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacturer's website. For a V_{OUT1} application example, three 100-µF, 6.3-V, X7S, 0805 ceramic capacitors, each with 2 mΩ of ESR, are used. With the three parallel capacitors, the estimated effective output capacitance after derating using the capacitor manufacturer's website is 240 µF. This is well above the calculated minimum capacitance so this design is expected to meet the transient response requirement with added margin. Figure 8-13 shows the transient response and the output voltage stays within ±4%, below the ±5% target of ±50 mV for V_{OUT1}. For the V_{OUT2} application example, two 100-µF, 6.3-V, X7S, 0805 ceramic capacitorsm each with 2 mΩ of ESRm are used. With the two parallel capacitors the estimated effective output capacitance after derating using the capacitor manufacturer's website is 80 µF. Figure 8-14 shows the transient response and the output voltage stays within ±3%, below the ±5% target of ±165 mV for V_{OUT2}.

8.2.2.4 Input Capacitor

It is required to have input decoupling ceramic capacitors type X5R, X7R, or similar from both the PVIN1 and PVIN2 pins to PGND to bypass the power-stage and be placed as close as possible. A total of at least 10 µF of capacitance is required. Some applications can require a bulk capacitance. At least 1 µF of bypass capacitance is recommended near both VIN pins to minimize the input voltage ripple. A 0.1-µF to 1-µF capacitor must be placed by both PVIN1 and PVIN2 pins 8 and 12 to provide high frequency bypass to reduce the high frequency overshoot and undershoot on the following pins:

- PVIN1
- SW1
- PVIN2
- SW2

The voltage rating of the input capacitor must be greater than the maximum input voltage. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions. The input capacitance required to meet a specific input ripple target can be calculated with Equation 17. A recommended target input voltage ripple is 5% the minimum input voltage, which is 350 mV in this example. The calculated input capacitance is 2.1 µF and 4.3 µF. Use the larger of the two values and distribute evenly between PVIN1 and PVIN2. Since the values are less than 10 µF, 2 × 10 µF are used. This example meets these two requirements with 4 × 10-µF ceramic capacitors and 2 ×100-µF bulk capacitance. The capacitor must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using Equation 18 and Equation 19.

For this example design, a ceramic capacitor with at least a 16-V voltage rating is required to support the maximum input voltage. Two 10-µF, 0805, X7S, 25-V and two 0.1-µF, 0402, X7R 50-V capacitors in parallel have been selected to be placed on both sides of the IC near both PVIN pins to PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 5.4 µF at the nominal input voltage of 12 V. A 100-µF bulk capacitance is also used to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 37. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of I_{OUT1} = 6 A, f_{SW} = 1000 kHz, V_{OUT1} the input voltage ripple with the 12-V nominal input is 350 mV, and the RMS input ripple current with the 7-V minimum input is 2.106 A. Similarly, for V_{OUT2}, the input RMS current is 3.01 A.

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For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in the *How To Select Input Capacitors For A Buck Converter* technical brief is recommended.

$$C_{IN1} > \frac{V_{OUT1} \times I_{OUT1} \times \left(1 - \frac{V_{OUT1}}{V_{IN}(min)}\right)}{N \times f_{SW} \times V_{IN}(min) \times V_{IN\_RIPPLE}} = \frac{1\ V \times 6\ A \times \left(1 - \frac{1\ V}{7\ V}\right)}{1 \times 1000\ kHz \times 7\ V \times 350\ mV} = 2.1\ \mu F$$

$$C_{IN2} > \frac{V_{OUT2} \times I_{OUT2} \times \left(1 - \frac{V_{OUT2}}{V_{IN}(min)}\right)}{N \times f_{SW} \times V_{IN}(min) \times V_{IN\_RIPPLE}} = \frac{3.3\ V \times 6\ A \times \left(1 - \frac{3.3\ V}{7\ V}\right)}{1 \times 1000\ kHz \times 7\ V \times 350\ mV} = 4.3\ \mu F \quad (17)$$

$$I_{CIN1(RMS)} = \sqrt{\frac{V_{OUT1}}{V_{IN}(min)} \times \left(\frac{(V_{IN}(min) - V_{OUT1})}{V_{IN}(min)} \times \left(\frac{I_{OUT1}}{N}\right)^2 + \frac{\left(\frac{Iripple1}{N}\right)^2}{12}\right)} =$$

$$I_{CIN1(RMS)} = \sqrt{\frac{1\ V}{7\ V} \times \left(\frac{(7\ V - 1\ V)}{7\ V} \times \left(\frac{6\ A}{1}\right)^2 + \frac{\left(\frac{1.531}{1}\right)^2}{12}\right)} = 2.11\ A \quad (18)$$

$$I_{CIN2(RMS)} = \sqrt{\frac{V_{OUT2}}{V_{IN}(min)} \times \left(\frac{(V_{IN}(min) - V_{OUT2})}{V_{IN}(min)} \times \left(\frac{I_{OUT2}}{N}\right)^2 + \frac{\left(\frac{Iripple2}{N}\right)^2}{12}\right)} =$$

$$I_{CIN2(RMS)} = \sqrt{\frac{3.3\ V}{7\ V} \times \left(\frac{(7\ V - 3.3\ V)}{7\ V} \times \left(\frac{6\ A}{1}\right)^2 + \frac{\left(\frac{1.454}{1}\right)^2}{12}\right)} = 3.01\ A \quad (19)$$

8.2.2.5 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R_{FB_T1} and R_{FB_B1} from the output node to the FB1 pin. It is recommended to use 1% tolerance or better resistors. For this example design, 10.0 kΩ is selected for R_{FB_B1}. Using Equation 20, R_{FB_T1} is calculated as 10.0 kΩ for V_{OUT1} = 1 V. For this example design, 10.0 kΩ is selected for R_{FB_B2}. Using Equation 20, R_{FB_T2} is calculated as 56.0 kΩ for V_{OUT2} = 3.3 V.

$$R_{fb\_t1} = R_{fb\_b1} \times \left(\frac{V_{OUT1} - V_{FB}}{V_{FB}}\right) = 10\ k\Omega \times \left(\frac{1\ V\ -\ 0.5\ V}{0.5\ V}\right) = 10\ k\Omega$$

$$R_{fb\_t2} = R_{fb\_b2} \times \left(\frac{V_{OUT2} - V_{FB}}{V_{FB}}\right) = 10\ k\Omega \times \left(\frac{3.3\ V\ -\ 0.5\ V}{0.5\ V}\right) = 56\ k\Omega \quad (20)$$

where

- V_{FB} = 0.5 V

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8.2.2.6 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has a threshold for power up when the input voltage is rising. UVLO has another threshold for power down or brownouts when the input voltage is falling. For this example design, the supply is set to turn on and start switching once the input voltage increases above 6 V (UVLO start or enable). After the regulator starts switching, it continues to do so until the input voltage falls below 5.5 V (UVLO stop or disable). In this example, these start and stop voltages set by the EN resistor divider are selected to have more hysteresis than the internally fixed V_{IN} UVLO. Equation 21 can be used to calculate the values for the upper resistor. For these equations to work, V_{START} must be 1.1 × V_{STOP} due to the voltage hysteresis of the EN pin. To set the start voltage, first select the bottom resistor (REN_B). The recommended value is between 1 kΩ and 100 kΩ. This example uses a 10-kΩ resistor.

For the voltages specified, the standard resistor value used for R_{ENT} is 39.2 kΩ and for R_{ENB} is 10 kΩ.

$$R_{EN\_T} = \frac{R_{EN\_B} \times V_{START}}{V_{ENH}} - R_{EN\_B} = \frac{10\ k\Omega \times 6\ V}{1.2\ V} - 10\ k\Omega = 39.9\ k\Omega \tag{21}$$

8.2.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT1 and SW1 and BOOT2 and SW2 pins for proper operation. The capacitor must be rated for 10 V or greater to minimize DC bias derating.

8.2.2.8 BP5 Capacitor Selection

A minimum of 2.2-µF (4.7 µF preferred) ceramic capacitor must be connected between the BP5 pin and PGND for proper operation. The capacitor must be rated for at least 10 V to minimize DC bias derating.

8.2.2.9 PGOOD Pullup Resistor

A 1-kΩ to 100-kΩ resistor can be used to pull up the power good signal when FB conditions are met. The pullup voltage source must be less than the 6-V absolute maximum of the PGOOD pin.

8.2.2.10 Current Limit

The current limit is fixed.

8.2.2.11 Soft-Start Time Selection

When using the TPS541620 in the dual-output configuration, the soft-start time is internally fixed at 1 ms as described in *Section 7.3.8*.

8.2.2.12 MODE1 and MODE2 Pins

To configure the TPS541620 for dual-output mode and a 1.5-pF ramp capacitor on VOUT2, the MODE1 resistor is chosen to be 15.4 kΩ as described in Table 7-3. To set the switching frequency to 1 MHz and a 1.5-pF ramp capacitor for VOUT1, the MODE2 resistor is chosen to be 17.4 kΩ as described in Table 7-1.

8.2.3 Application Curves

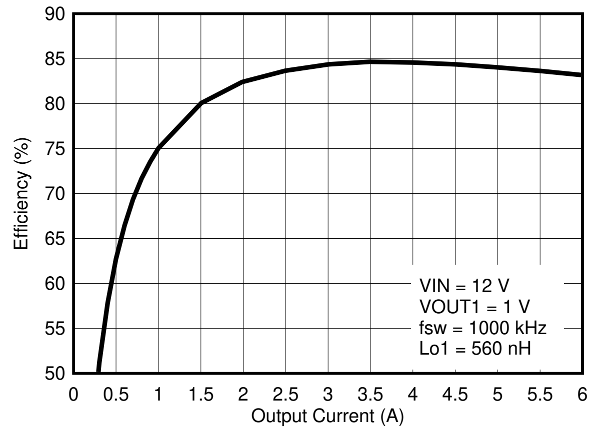

Figure 8-3. V_{OUT1} Efficiency

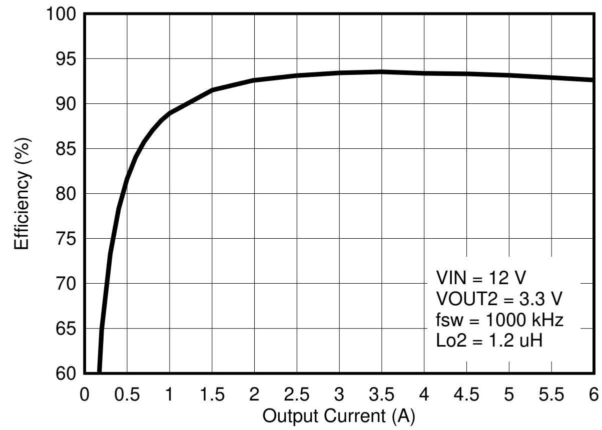

Figure 8-4. V_{OUT2} Efficiency

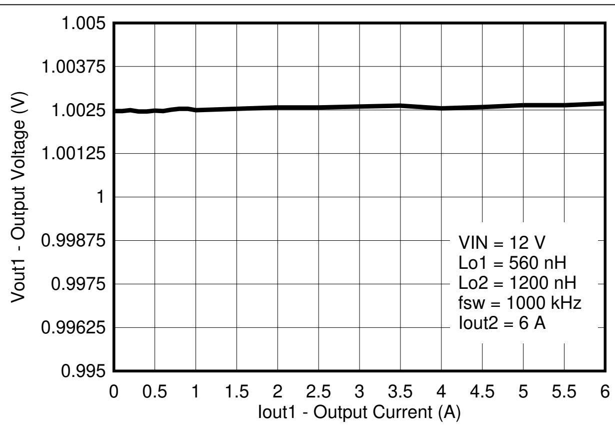

Figure 8-5. V_{OUT1} Load Regulation

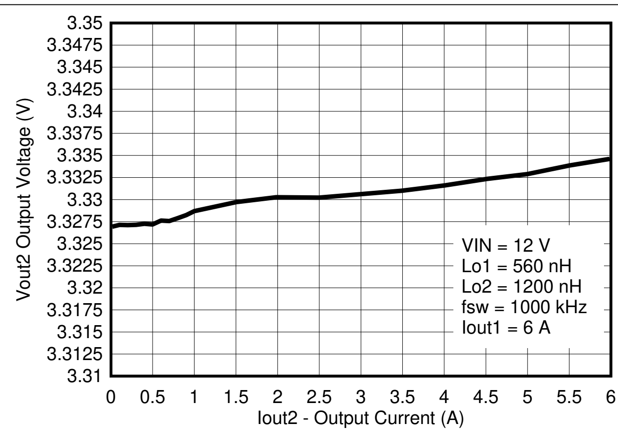

Figure 8-6. V_{OUT2} Load Regulation

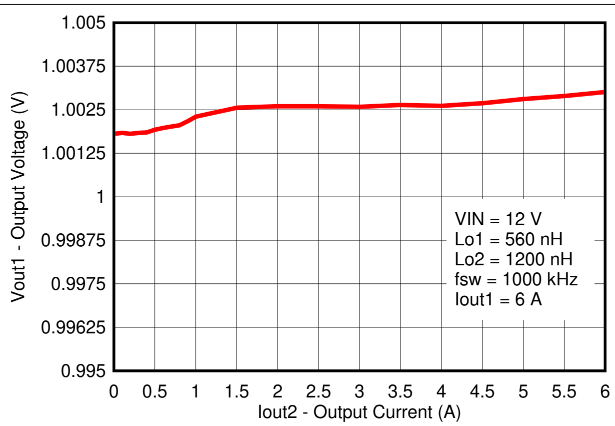

Figure 8-7. V_{OUT1} Cross Regulation

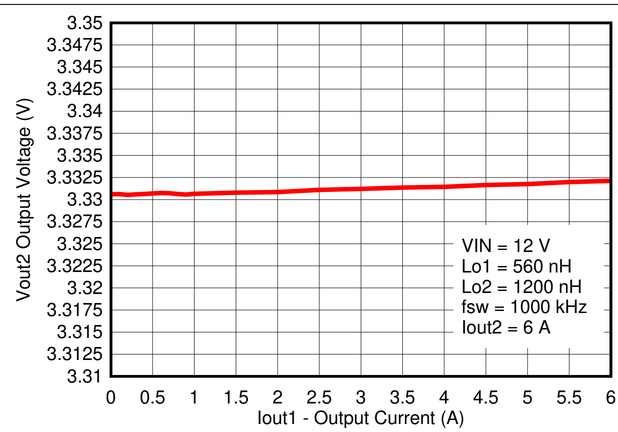

Figure 8-8. V_{OUT2} Cross Regulation

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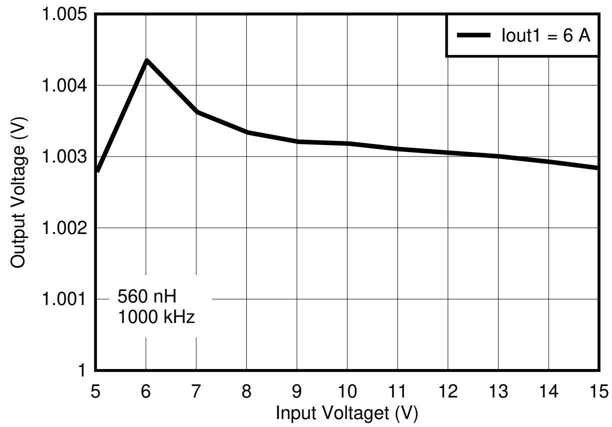

Figure 8-9. Line Regulation V_{OUT1}

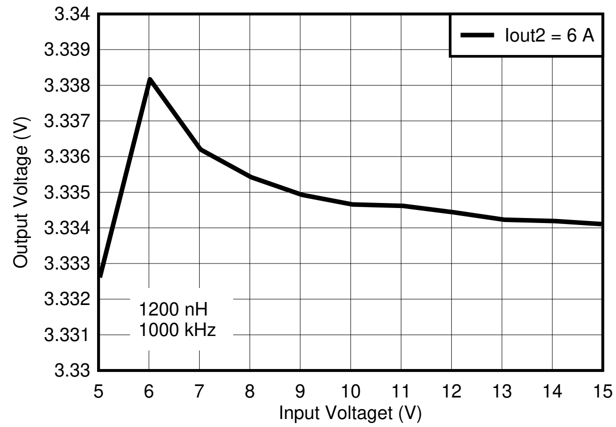

Figure 8-10. Line Regulation V_{OUT2}

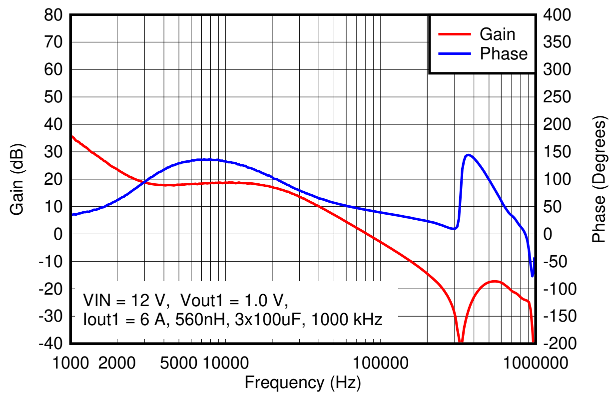

Figure 8-11. V_{OUT1} Bode Plot

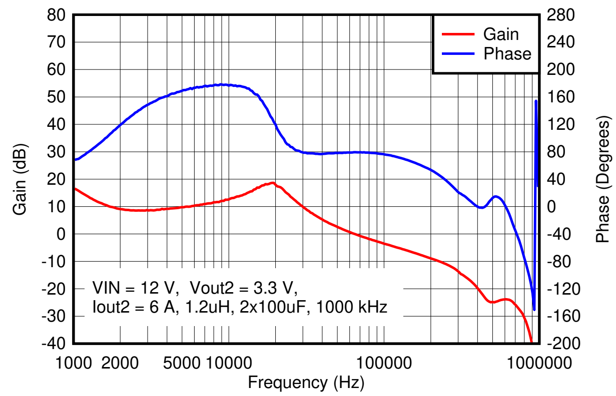

Figure 8-12. V_{OUT2} Bode Plot

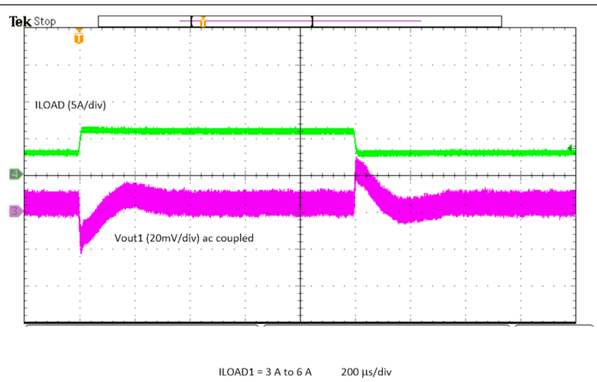

Figure 8-13. V_{OUT1} Load Transient

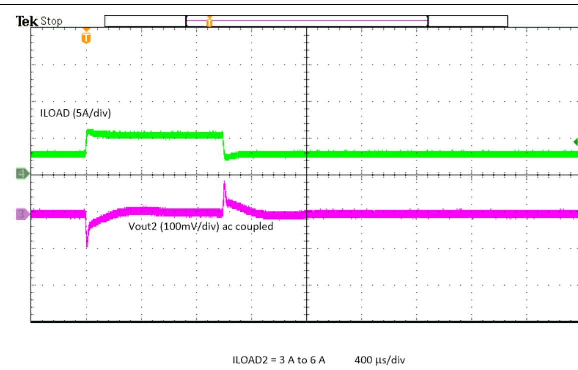

Figure 8-14. V_{OUT2} Load Transient

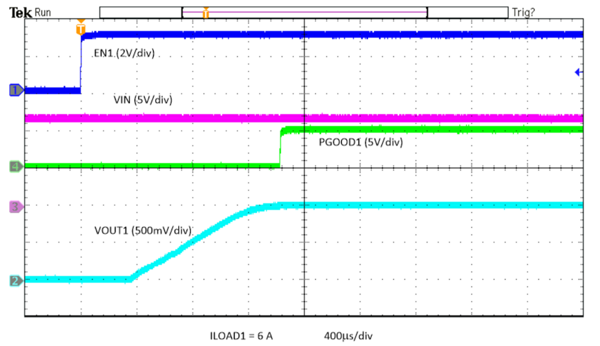

Figure 8-15. Power Up with EN 1

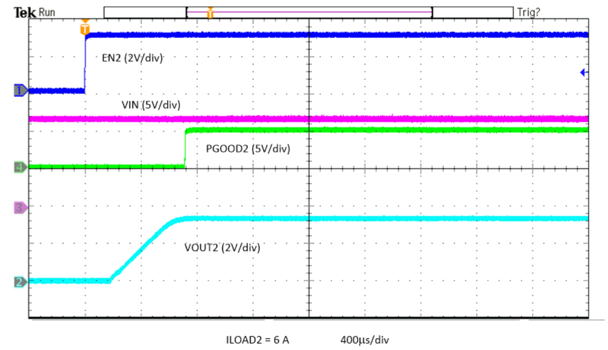

Figure 8-16. Power Up with EN 2

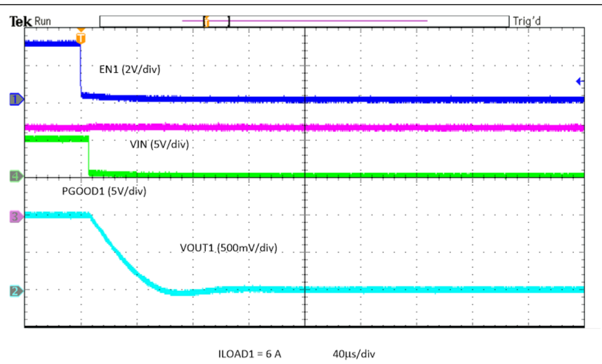

Figure 8-17. Power Down with EN 1

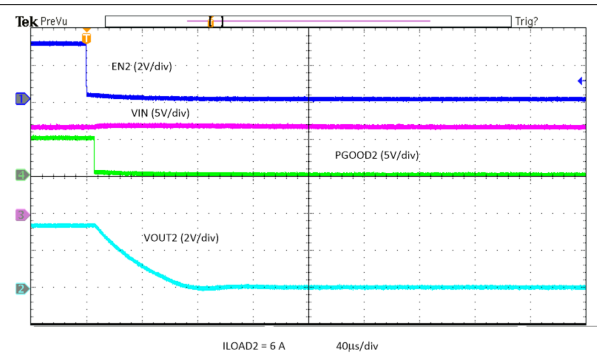

Figure 8-18. Power Down with EN 2

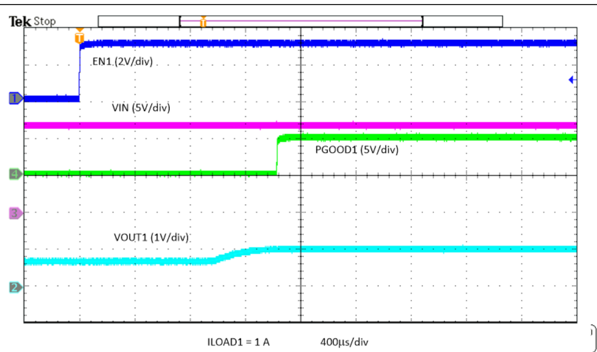

Figure 8-19. Power Up with EN 1 with Pre Bias

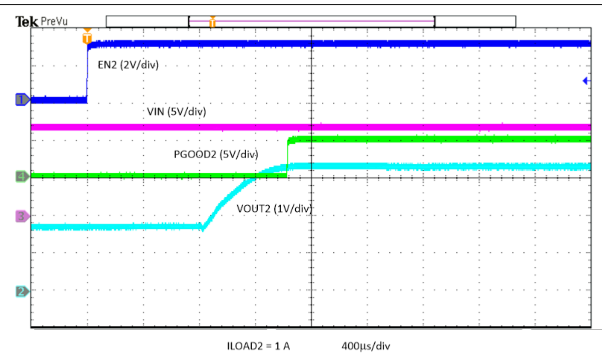

Figure 8-20. Power Up with EN 2 with Pre Bias

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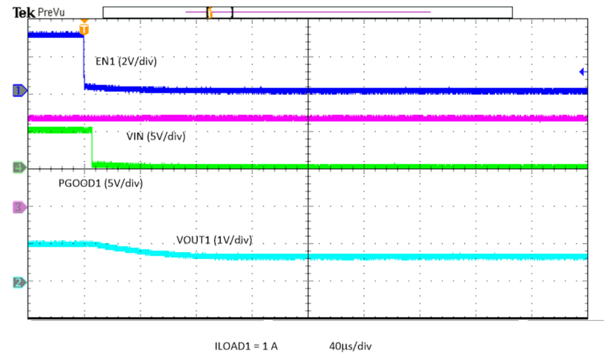

Figure 8-21. Power Down with EN 1 with Pre Bias

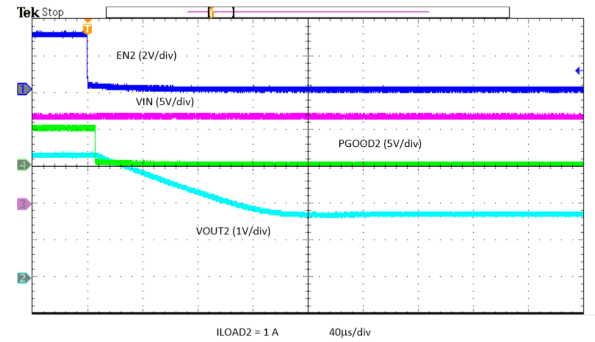

Figure 8-22. Power Down with EN 2 with Pre Bias

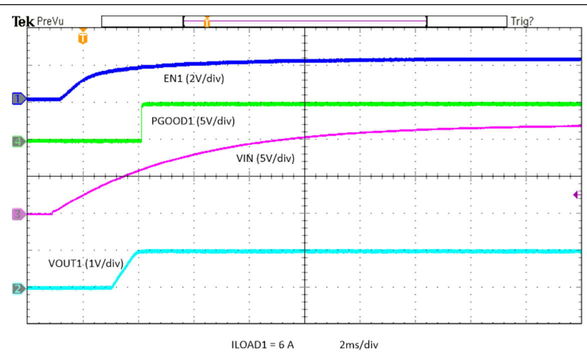

Figure 8-23. Power Up with V_{IN} V_{OUT1}

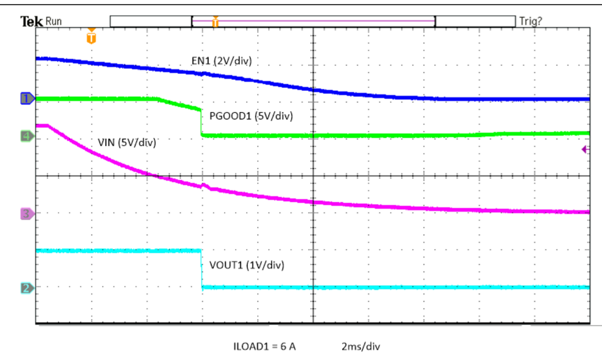

Figure 8-24. Power Down with V_{IN} V_{OUT1}

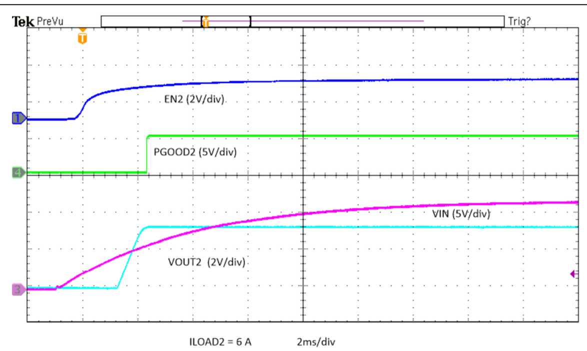

Figure 8-25. Power Up with V_{IN} V_{OUT2}

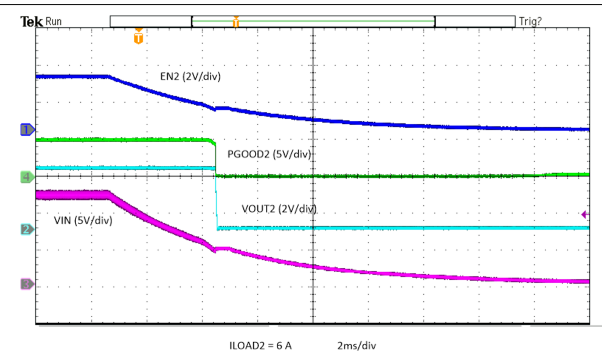

Figure 8-26. Power Down with V_{IN} V_{OUT2}

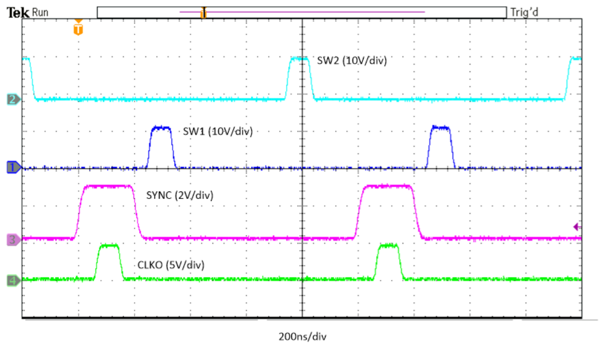

Figure 8-27. Sync In to SW1 and SW2 Delay

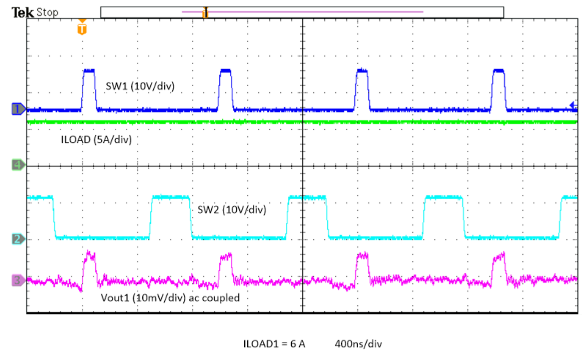

Figure 8-28. V_{OUT1} Output Ripple – 6-A Load

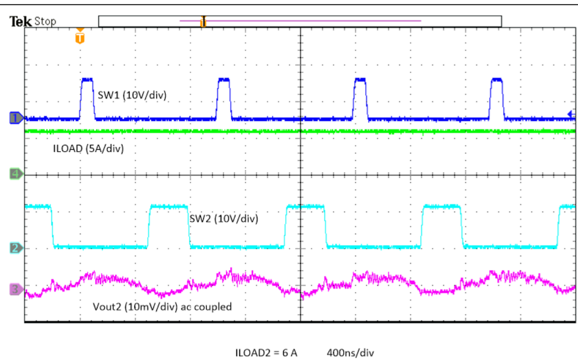

Figure 8-29. V_{OUT2} Output Ripple – 6-A Load

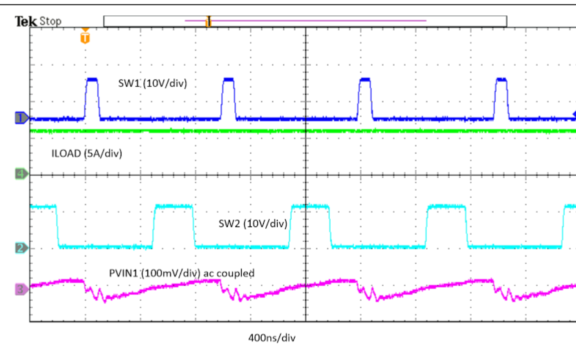

Figure 8-30. Input Ripple PVIN1 – 6-A Load

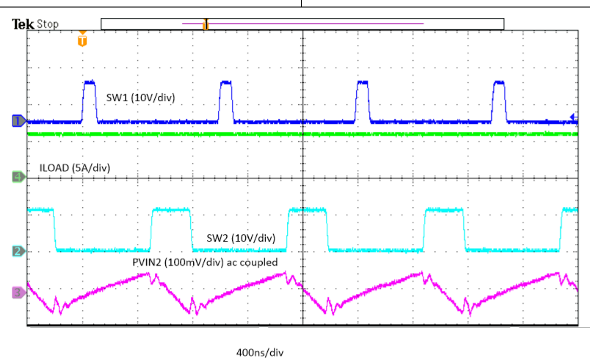

Figure 8-31. Input Ripple PVIN2 – 6-A Load

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8.2.4 Typical Application - 2-Phase Operation

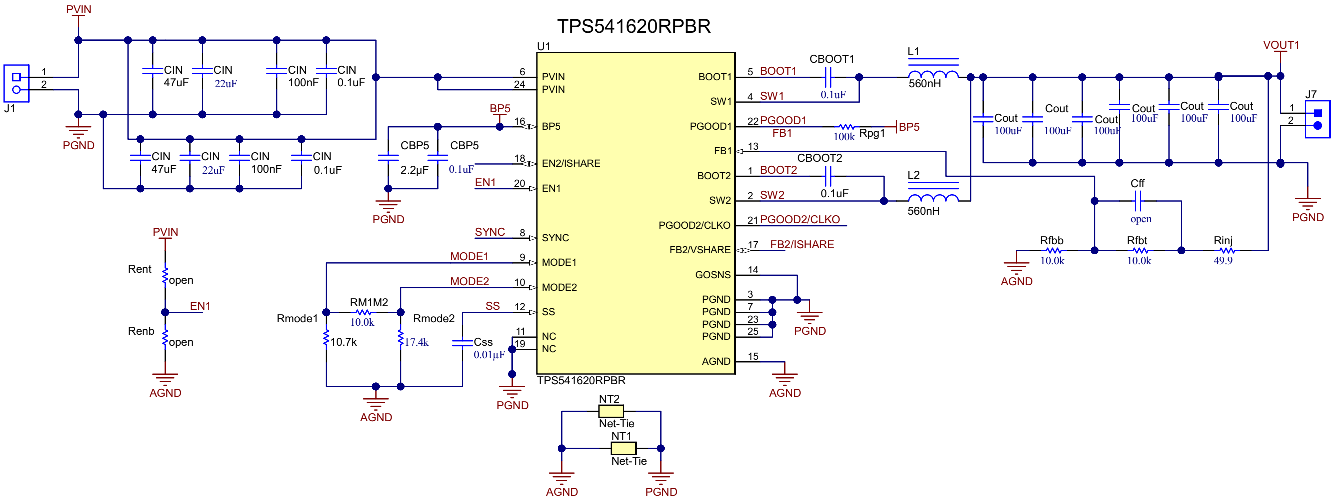

Figure 8-32. 12-V Input, 1.0-V Output 2-Phase Converter Application Schematic

8.2.4.1 Design Requirements

For this design example, use the parameters shown in Table 8-2.

Table 8-2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	7 to 15 V, 12 V nominal
Output voltage (V_{OUT})	1.0 V
Output current rating (I_{OUT})	12 A
Switching frequency (f_{SW})	1000 kHz/phase
Steady state output ripple voltage	10 mV
Output current load step	6 A
Transient response	± 50 mV (± 5%)

8.2.4.2 Detailed Design Procedure

8.2.4.2.1 Switching Frequency

The first step is to decide on a switching frequency. The TPS541620 can operate at four different frequencies from 500 kHz to 2.0 MHz. f_{SW} is set by the resistor value from the MODE2 pin to ground. Typically the highest switching frequency possible is desired because it produces the smallest solution size, or a lower switching frequency is selected for a more efficient converter. The minimum controllable on-time and maximum off-time affect the input voltage range and switching frequency.

The maximum switching frequency for a given application can be limited by the minimum on-time of the regulator and the maximum f_{SW} can be estimated with Equation 22. Using the maximum minimum on-time of 50 ns and 15-V maximum input voltage for this application, the maximum switching frequency is 1333 kHz. The minimum regulating input voltage is limited by the maximum off-time, switching frequency, and output voltage. Using the maximum 150-ns off-time, 7-V minimum input voltage, 1.0-V output voltage for this application, and Equation 23, the maximum switching frequency from 1.0 V and maximum off-time is 5714 kHz.

The selected switching frequency must also consider the tolerance of the switching frequency. A switching frequency of 1000 kHz is selected for a good balance of solution size and efficiency. To set the frequency to 1000 kHz, the selected MODE2 resistor is 17.4 kΩ per Table 7-1.

$$fsw = \frac{Vout\,min}{ton \times Vin\,max} = \frac{1\ V}{50\ ns \times 15\ V} = 1333\ kHz \tag{22}$$

$$fsw = \frac{1 - \frac{Vout\,max}{Vin\,min}}{toff} = \frac{1 - \frac{1.0\ V}{7\ V}}{150\ ns} = 5714\ kHz \tag{23}$$

Figure 8-33 shows the maximum recommended input voltage versus output voltage for each FSEL frequency. Figure 8-33 uses the maximum minimum on-time of 50 ns and includes 10% tolerance on the switching frequency.

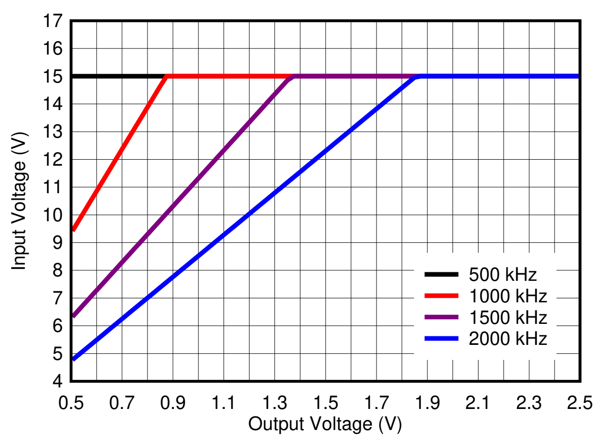

Figure 8-33. Maximum Input Voltage Versus Output Voltage

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8.2.4.2.2 Output Inductor Selection

To calculate the effective value of the output inductor, use Equation 24. K is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Choosing small inductor ripple currents (through a large inductor) can degrade the transient response performance. The inductor ripple, K, is normally from 0.1 to 0.4 for the majority of applications giving a peak-to-peak ripple current range of 0.6 A to 2.4 A. The target Iripple must be 0.3 A or larger.

For this design example, K_{IND} = 0.3 is used and the inductor value Lo_eff is calculated to be 0.255 µH. The per phase value is calculated to 0.51 µH. An inductor with an inductance of 0.56 µH is selected. The inductor ripple current is calculated as 1.674 A using Equation 25. It is important that the RMS (Root Mean Square) current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 26 and Equation 27, respectively. For this design, the RMS inductor current is 6.019 A and the peak inductor current is 6.837 A. The chosen inductor is a Coilcraft XAL6030-561, which has a saturation current rating of 29 A, an RMS current rating of 17 A, and a typical DC series resistance of 3.01 mΩ.

The peak current through the inductor is the inductor ripple current plus the DC output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in Equation 27. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify the current ratings of the inductor based on the switch current limit rather than the steady-state peak inductor current.

$$\begin{aligned} &Lo\_eff = \frac{(Vin - Vout)}{K \times Iout}\left(\frac{Vout}{Vin \times fsw}\right) = \frac{(12\ V - 1\ V)}{0.3 \times 12\ A}\left(\frac{1\ V}{12\ V \times 1000\ kHz}\right) = 0.255\ \mu H \\ &Lo = N \times Lo\_eff = (0.255\ \mu H) \times 2 = 0.509\ \mu H \\ &\text{where} N = 1, 2 \text{or} 4 \end{aligned} \tag{24}$$

$$Iripple = \frac{(Vinmax - Vout)}{Lo\_eff \times N}\left(\frac{Vout}{Vinmax \times fsw}\right) = \frac{(15\ V - 1\ V)}{0.280\ \mu H \times 2}\left(\frac{1\ V}{15\ V \times 1000\ kHz}\right) = 1.667\ A \tag{25}$$

$$I_{L(RMS)} = \sqrt{\left(\frac{I_{OUT}}{N}\right)^2 + \frac{I_{RIPPLE}^2}{12}} = \sqrt{\left(\frac{12\ A}{2}\right)^2 + \frac{(1.667\ A)^2}{12}} = 6.019\ A \tag{26}$$

$$I_{L(PEAK)} = \frac{I_{OUT}}{N} + \frac{I_{RIPPLE}}{2} = \frac{12\ A}{2} + \frac{1.667\ A}{2} = 6.833\ A \tag{27}$$

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8.2.4.2.3 Output Capacitor

The two primary considerations for selecting the value of the output capacitor are how the regulator responds to a large change in load current and the output voltage ripple. The third consideration is to ensure converter stability, which is typically met from the first two considerations. The output capacitance needs to be selected based on the more stringent of these criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop needs to sense the change in the output voltage, then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically, the loop bandwidth is near $f_{SW}/10$. Equation 28 estimates the minimum output capacitance necessary, where I_{STEP} is the change in output current and V_{TRANS} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 6 A. Therefore, I_{TRANS} is 6 A and V_{TRANS} is 50 mV. Using this target gives a minimum capacitance of 191 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

$$C_{OUT\_LOOP} > \frac{I_{STEP}}{V_{TRANS}} \times \frac{1}{2\pi \times \frac{fsw}{10}} = \frac{6\ A}{50\ mV} \times \frac{1}{2\pi \times \frac{1000\ kHz}{10}} = 191\ \mu F \quad (28)$$

In addition to the loop bandwidth, it is possible for the inductor current slew rate to limit how quickly the regulator responds to the load step. For low duty cycle applications, the time it takes for the inductor current to ramp down after a load step down can be the limiting factor. Equation 29 estimates the minimum output capacitance necessary to limit the undershoot of the output voltage after a load step-up. Using the 0.56-µH inductance selected gives a minimum capacitance of 9.2 µF to meet to undershoot requirement. Equation 30 estimates the minimum output capacitance necessary to limit the overshoot of the output voltage after a load step down. Using the 0.56-µH inductance selected gives a minimum capacitance of 100.8 µF to meet the overshoot requirement.

$$C_{OUT\_UNDERSHOOT} > \frac{Lo\_eff \times I_{STEP}^2}{2 \times V_{TRANS} \times (V_{IN} - V_{OUT})}$$

$$C_{OUT\_UNDERSHOOT} > \frac{\frac{0.56\ \mu H}{2} \times (6\ A)^2}{2 \times 50\ mV \times (12\ V - 1\ V)} = 9.2\ \mu F \quad (29)$$

$$C_{OUT\_OVERSHOOT} > \frac{Lo\_eff \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{\frac{0.56\ \mu H}{2} \times (6\ A)^2}{2 \times 50\ mV \times 1\ V} = 100.8\ \mu F \quad (30)$$

Equation 31 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{sw} is the switching frequency, V_{RIPPLE} is the maximum allowable steady-state output voltage ripple, N is the number of phases, and I_{RIPPLE} is the inductor ripple current calculated from Equation 25. In this case, the target maximum steady-state output voltage ripple is 10 mV. Under this requirement, Equation 31 yields 10.4 µF.

$$C_{OUT\_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times N \times f_{SW}} = \frac{1.667\ A}{8 \times 10\ mV \times 2 \times 1000\ kHz} = 10.4\ \mu F \quad (31)$$

Lastly, if an application does not have a stringent load transient response or output ripple requirement, a minimum amount of capacitance is still required to ensure the control loop is stable with the lowest gain ramp setting on the MODE pin. Equation 32 estimates the minimum capacitance needed for loop stability. This

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equation sets the minimum amount of capacitance by keeping the LC frequency at a maximum of 1/30th the switching frequency. Equation 32 gives a minimum capacitance of 81.4 µF.

$$C_{OUT\_STABILITY} > \left(\frac{15}{\pi \times fsw}\right)^2 \times \frac{1}{\frac{Lo}{N}} = \left(\frac{15}{\pi \times 1000\ \text{kHz}}\right)^2 \times \frac{1}{\frac{0.56}{2}\ \mu H} = 81.4\ \mu F \tag{32}$$

Equation 33 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification, showing the ESR should be less than 6 mΩ. This application uses all ceramic capacitors, so the effects of ESR on the ripple and transient were ignored. If you are using non-ceramic capacitors, as a starting point, the ESR should be below the values calculated in Equation 33 and Equation 34, respectively, to meet the ripple and transient requirements. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{10\ \text{mV}}{1.667\ \text{A}} = 6.00\ \text{m}\Omega \tag{33}$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{50\ \text{mV}}{6\ \text{A}} = 8.3\ \text{m}\Omega \tag{34}$$

$$Icorms = \frac{(Vinmax - Vout)}{\sqrt{12} \times Lo}\left(\frac{Vout}{Vinmax \times fsw}\right) = \frac{(15\ \text{V} - 1\ \text{V})}{\sqrt{12} \times 0.56\ \mu H}\left(\frac{1\ \text{V}}{15\ \text{V} \times 1000\ \text{kHz}}\right) = 0.481\ \text{A} \tag{35}$$

In this case, ceramic capacitors are used and the combined ESR of the ceramic capacitors in parallel is much less than is needed to meet the ripple. Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheet specifies the RMS value of the maximum ripple current. Equation 35 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 35 yields 0.481 A, and ceramic capacitors typically have a ripple current rating much higher than this. Select X5R and X7R ceramic dielectrics or equivalent for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacturer's website. For this application example, six 100-µF, 6.3-V, X7S, 0805 ceramic capacitors, each with 2 mΩ of ESR, are used. With the six parallel capacitors, the estimated effective output capacitance after derating using the capacitor manufacturer's website is 240 µF. This is well above the calculated minimum capacitance, so this design is expected to meet the transient response requirement with added margin. Figure 8-38 shows the transient response. The output voltage stays within ±3%, below the ±5% target.

8.2.4.2.4 Input Capacitor

It is required to have input decoupling ceramic capacitors type X5R, X7R, or similar from both the PVIN1 and PVIN2 pins to PGND to bypass the power-stage and placed as close as possible to the IC. A total of at least 10 µF of capacitance is required and some applications can require a bulk capacitance. At least 1 µF of bypass capacitance is recommended near both VIN pins to minimize the input voltage ripple. A 0.1-µF to 1-µF capacitor must be placed by both PVIN1 and PVIN2 pins 8 and 12 to provide high frequency bypass to reduce the high frequency overshoot and undershoot on the following pins:

- PVIN1
- SW1

- PVIN2
- SW2

The voltage rating of the input capacitor must be greater than the maximum input voltage. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions. A recommended target input voltage ripple is 5% of the minimum input voltage, which is 350 mV in this example. The calculated input capacitance is 2.1 µF. Use the larger of the two values and distribute evenly between PVIN1 and PVIN2. Since the values are less than 10 µF, 2 × 10 µF are used. This example meets these two requirements with 4 × 10-µF ceramic capacitors and 2 × 100-µF bulk capacitance. The capacitor must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using Equation 36.

For this example design, a ceramic capacitor with at least a 16-V voltage rating is required to support the maximum input voltage. Two 10-µF, 0805, X7S, 25-V and two 0.1-µF, 0402, X7R 50-V capacitors in parallel have been selected to be placed on both sides of the IC near both PVIN pins to PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 5.4 µF at the nominal input voltage of 12 V. 100-µF bulk capacitance is also used to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 37. The maximum input ripple occurs when operating closest to 50% duty cycle. Using the nominal design example values of I_{outmax} = 12 A, f_{SW} = 1000 kHz, and V_{OUT} = 1 V, the input voltage ripple with the 12-V nominal input is 350 mV and the RMS input ripple current with the 7-V minimum input is 2.106 A.

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in the *How To Select Input Capacitors For A Buck Converter* technical brief is recommended.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}(\min)}\right)}{N \times f_{SW} \times V_{IN}(\min) \times V_{IN\_RIPPLE}} = \frac{1\ V \times 12\ A \times \left(1 - \frac{1\ V}{7\ V}\right)}{2 \times 1000\ kHz \times 7\ V \times 350\ mV} = 2.1\ \mu F \tag{36}$$

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}(\min)} \times \left(\frac{\left(V_{IN}(\min) - V_{OUT}\right)}{V_{IN}(\min)} \times \left(\frac{I_{OUT}}{N}\right)^2 + \frac{(Iripple)^2}{12}\right)} =$$

$$I_{CIN(RMS)} = \sqrt{\frac{1\ V}{7\ V} \times \left(\frac{(7\ V - 1\ V)}{7\ V} \times \left(\frac{12}{2}\right)^2 + \frac{(1.687)^2}{12}\right)} = 2.106\ A \tag{37}$$

8.2.4.2.5 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R_{FB_T} and R_{FB_B} from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. For this example design, 10.0 kΩ is selected for R_{FB_B}. Using Equation 38, R_{FB_T} is calculated as 10.0 kΩ for a 1-V output. This is a standard 1% resistor.

$$R_{fb\_t} = R_{fb\_b} \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) = 10\ k\Omega \times \left(\frac{1\ V\ -\ 0.5\ V}{0.5\ V}\right) = 10\ k\Omega \tag{38}$$

where

- V_{FB} = 0.5 V

8.2.4.2.6 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has a threshold for power up when the input voltage is rising. UVLO has another threshold for power

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down or brownouts when the input voltage is falling. For the example design, the supply is set to turn on and start switching once the input voltage increases above 6 V (UVLO start or enable). After the regulator starts switching, it continues to do so until the input voltage falls below 5.5 V (UVLO stop or disable). In this example, these start and stop voltages set by the EN resistor divider are selected to have more hysteresis than the internally fixed V_{IN} UVLO. Equation 39 can be used to calculate the value for the upper resistor. For these equations to work, V_{START} must be 1.1 × V_{STOP} due to the voltage hysteresis of the EN pin. To set the start voltage, first select the bottom resistor (REN_B). The recommended value is between 1 kΩ and 100 kΩ. This example uses a 10-kΩ resistor.

For the voltages specified, the standard resistor value used for R_{ENT} is 39.2 kΩ and for R_{ENB} is 10 kΩ.

$$R_{EN\_T} = \frac{R_{EN\_B} \times V_{START}}{V_{ENH}} - R_{EN\_B} = \frac{10\ k\Omega \times 6\ V}{1.2\ V} - 10\ k\Omega = 39.9\ k\Omega \quad (39)$$

8.2.4.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT1 and SW1 and BOOT2 and SW2 pins for proper operation. The capacitor must be rated for 10 V or greater to minimize DC bias derating.

8.2.4.2.8 BP5 Capacitor Selection

A 2.2-µF (4.7 µF preferred) ceramic capacitor must be connected between the BP5 pin and PGND for proper operation. The capacitor must be rated for at least 10-V to minimize DC bias derating.

8.2.4.2.9 PGOOD Pullup Resistor

A 1-kΩ to 100-kΩ resistor can be used to pull up the power good signal when FB conditions are met. The pullup voltage source must be less than the 6-V absolute maximum of the PGOOD pin.

8.2.4.2.10 Current Limit

The current limit is fixed.

8.2.4.2.11 Soft-Start Time Selection

The SS pin is used to program different soft-start times in multi-phase mode. In dual-output mode, an internally fixed soft start is used.

This is useful if a load has specific timing requirements for the output voltage of the regulator. A longer soft-start time is also useful if the output capacitance is very large and would require large amounts of current to quickly charge the output capacitors to the output voltage level. The large currents necessary to charge the capacitor can reach the current limit or cause the input voltage rail to sag due excessive current draw from the input power supply. Limiting the output voltage slew rate solves both of these problems. The example design has the soft-start time set to 2.5 ms.

8.2.4.2.12 MODE1 Pin

The MODE1 resistor is set to 10.7 kΩ to select multiphase mode as described by Table 7-3.

8.2.4.3 Application Curves

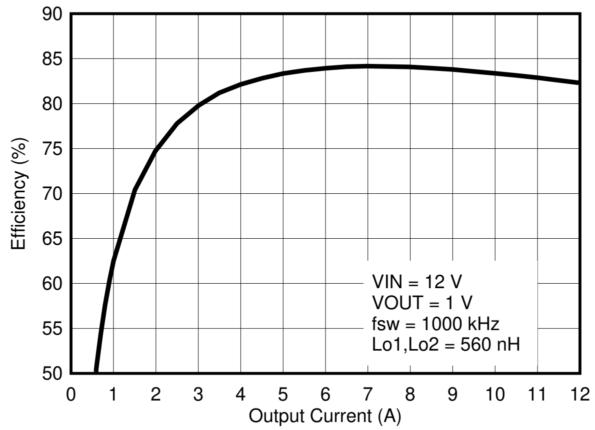

Figure 8-34. Efficiency

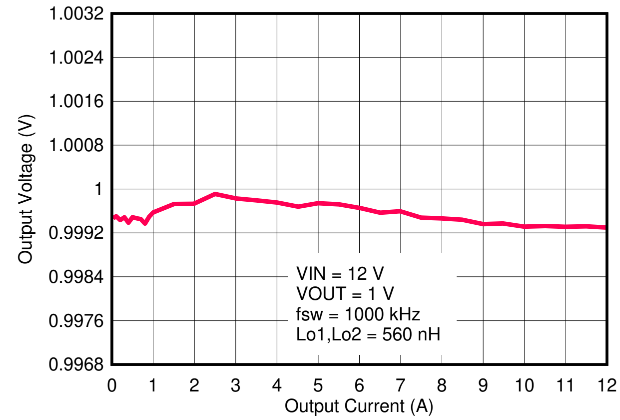

Figure 8-35. Load Regulation

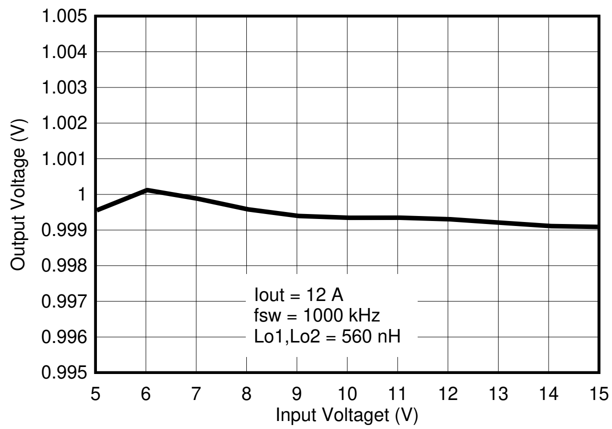

Figure 8-36. Line Regulation

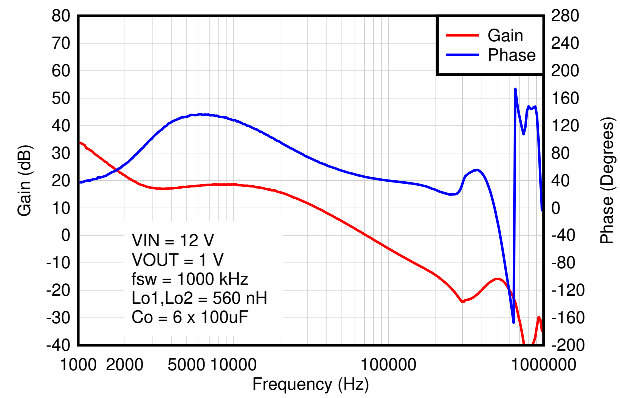

Figure 8-37. Bode Plot

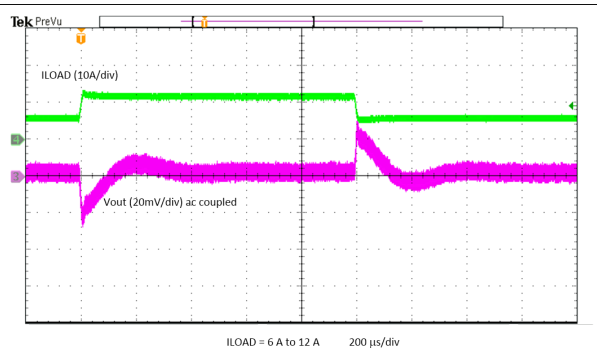

Figure 8-38. Load Transient

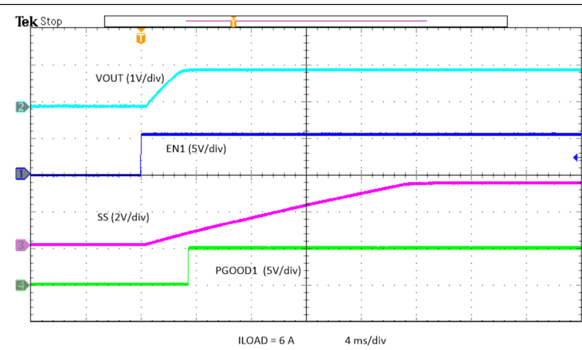

Figure 8-39. Power Up with EN

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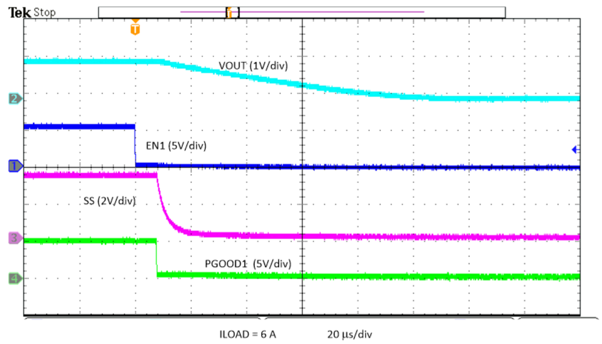

Figure 8-40. Power Down with EN

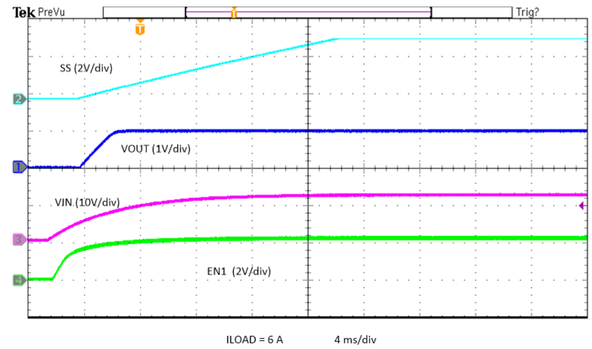

Figure 8-41. Power Up with V_{IN}

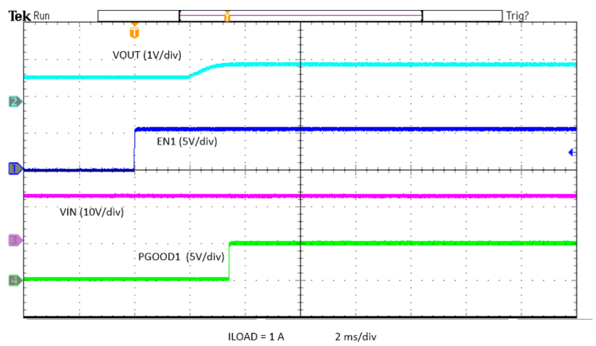

Figure 8-42. Power Up with EN – Prebias

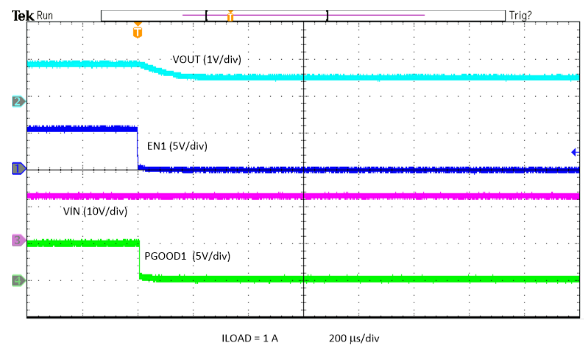

Figure 8-43. Power Down with EN – Prebias

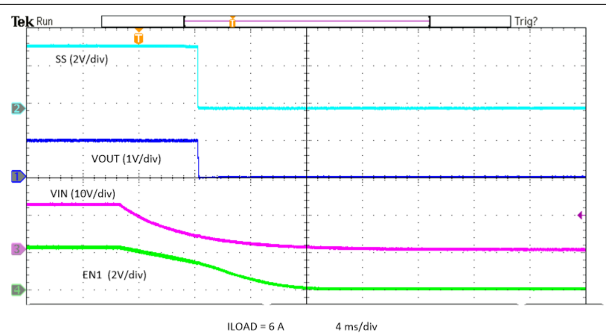

Figure 8-44. Power Down with VIN

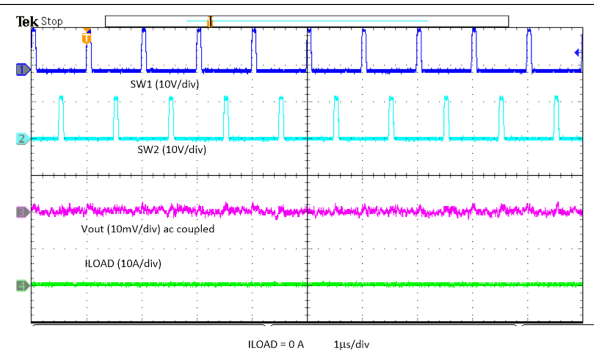

Figure 8-45. Output Ripple – No Load

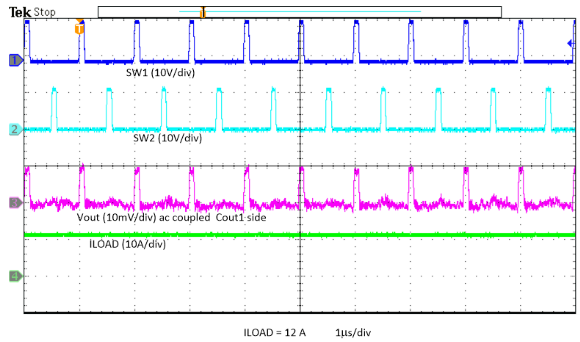

Figure 8-46. Output Ripple – 12-A Load

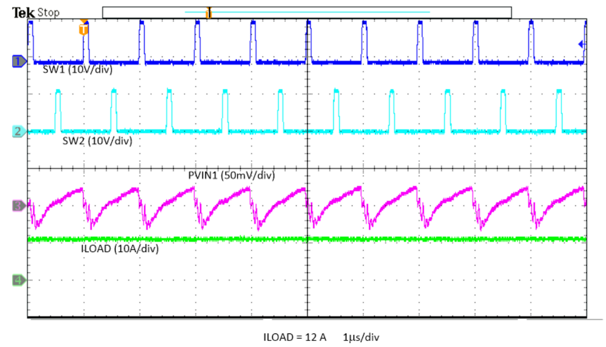

Figure 8-47. Input Ripple PVIN1 – 12-A Load

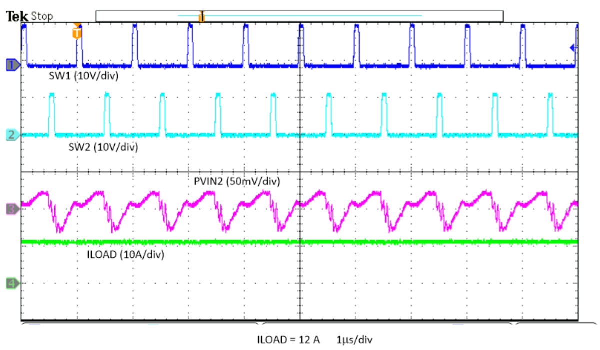

Figure 8-48. Input Ripple PVIN2 - 12-A Load

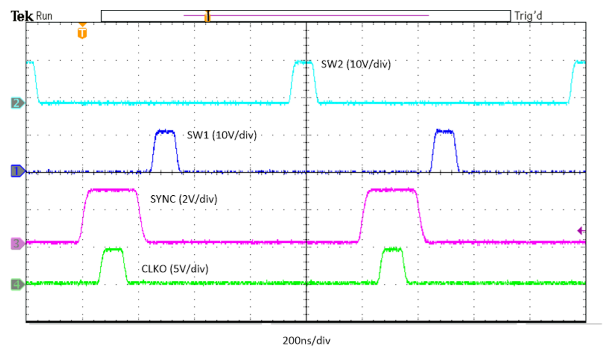

Figure 8-49. Sync In to SW1, SW2 and CLKO Delay

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9 Power Supply Recommendations

The TPS541620 is designed to operate from an input voltage supply range between 4.5 V and 15 V. This supply voltage must be well regulated. Proper bypassing of the input supply is critical for proper electrical performance, as is the PCB layout and the grounding scheme. A minimum of one 22-µF (after derating) ceramic capacitor, type X5R or better, must be placed between VIN and PGND on each side of the device.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. See Figure 10-1 for a PCB layout example. Key guidelines to follow for the layout are:

- VIN, PGND, and SW traces must be as wide as possible to reduce trace impedance and improve heat dissipation.
- Place a 10-nF to 100-nF capacitor from each VIN to PGND pin and place them as close as possible to the device (for applications requiring a DC voltage of 15 V and above, the edge of input bypass capacitor pads must be no more than 8 mils away from the pin) to the device is required. Place the remaining ceramic input capacitance next to these high frequency bypass capacitors.
- Use multiple vias near the PGND pins and use the layer directly below the device to connect them together. This helps to minimize noise and can help heat dissipation.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer.
- Place the inductor as close as possible to the device to minimize the length of the SW node routing.
- Place the BOOT-SW capacitor as close as possible to the BOOT and SW pins. If a boot resistor is needed, the value of the resistor should be no more than 10 Ω.
- Place the BP5 capacitor as close as possible to the BP5 and PGND pins.
- Place the bottom resistor in the FB divider as close as possible to the FB and AGND pins of the IC. Also keep the upper feedback resistor and the feedforward capacitor, if used, near the IC. Connect the FB divider to the output voltage at the desired point of regulation.
- Return the MODE1 and MODE2 resistors to a quiet AGND island.
- Use multiple vias in the AGND island to connect it back to internal PGND layers. Place the vias near the BP5 cap but away from the bottom FB resistor.

10.2 Layout Example

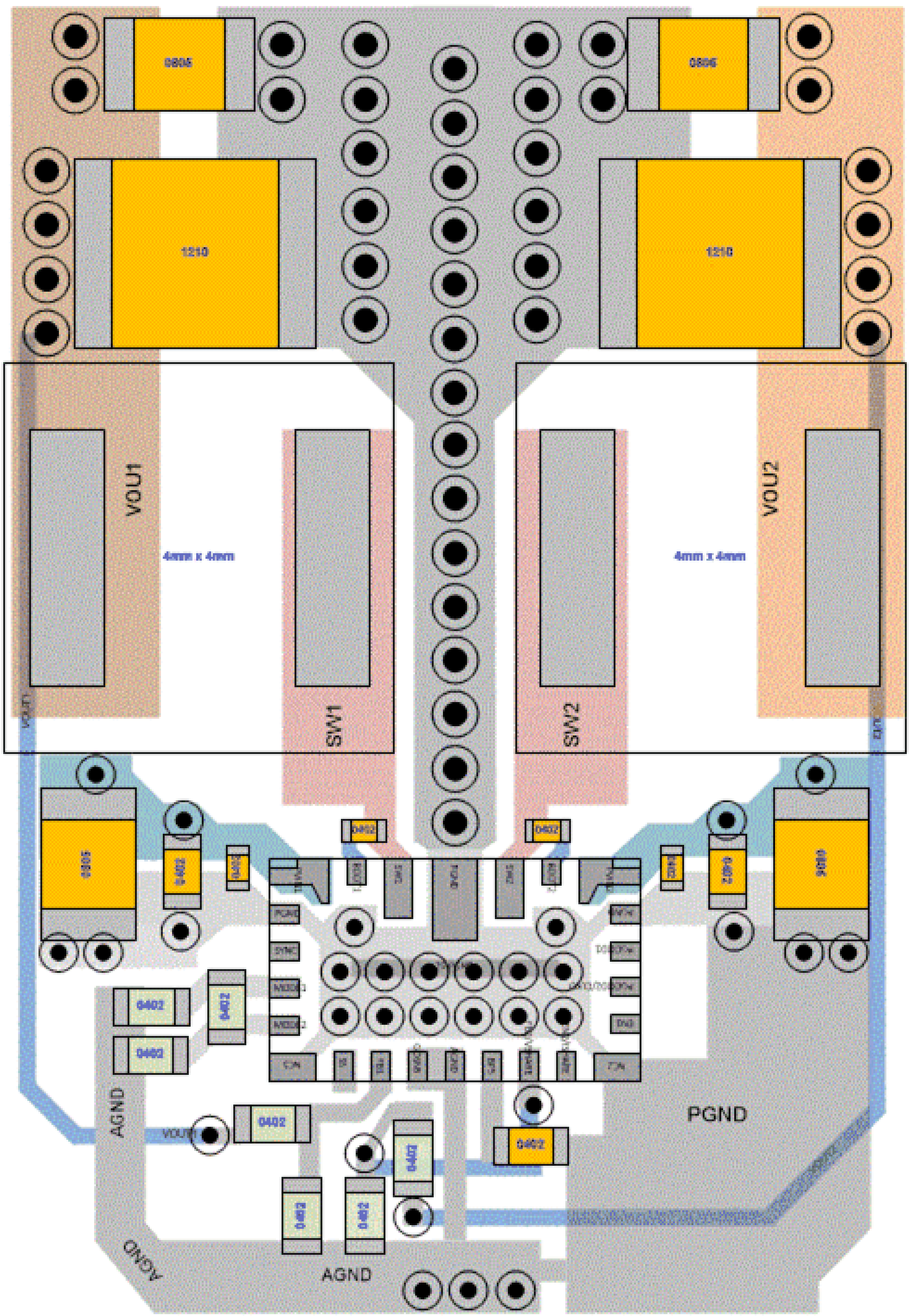

Figure 10-1. Example PCB Layout for Dual-output Configuration

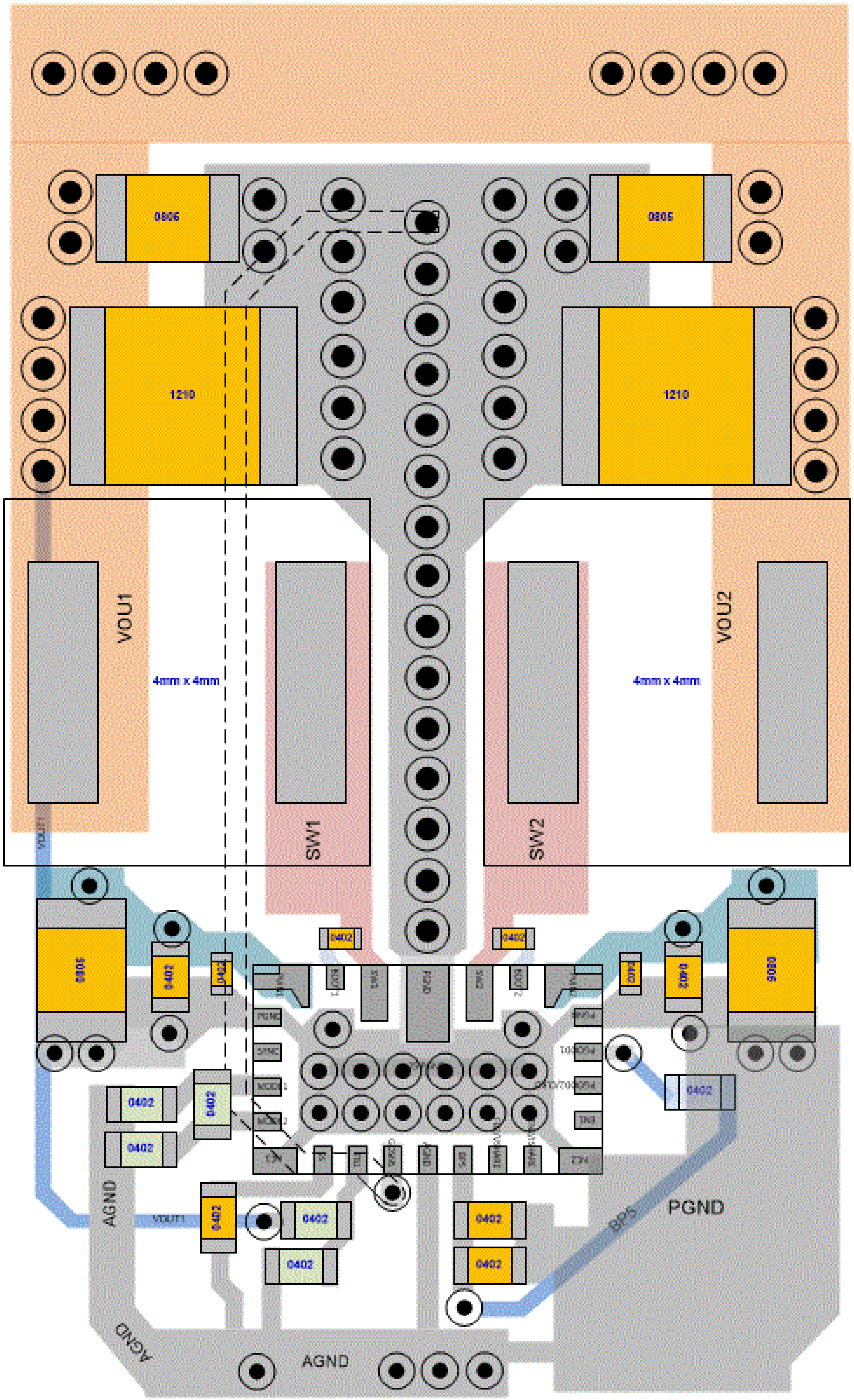

Figure 10-2. Example PCB Layout for Dual-phase Configuration

10.2.1 Thermal Performance

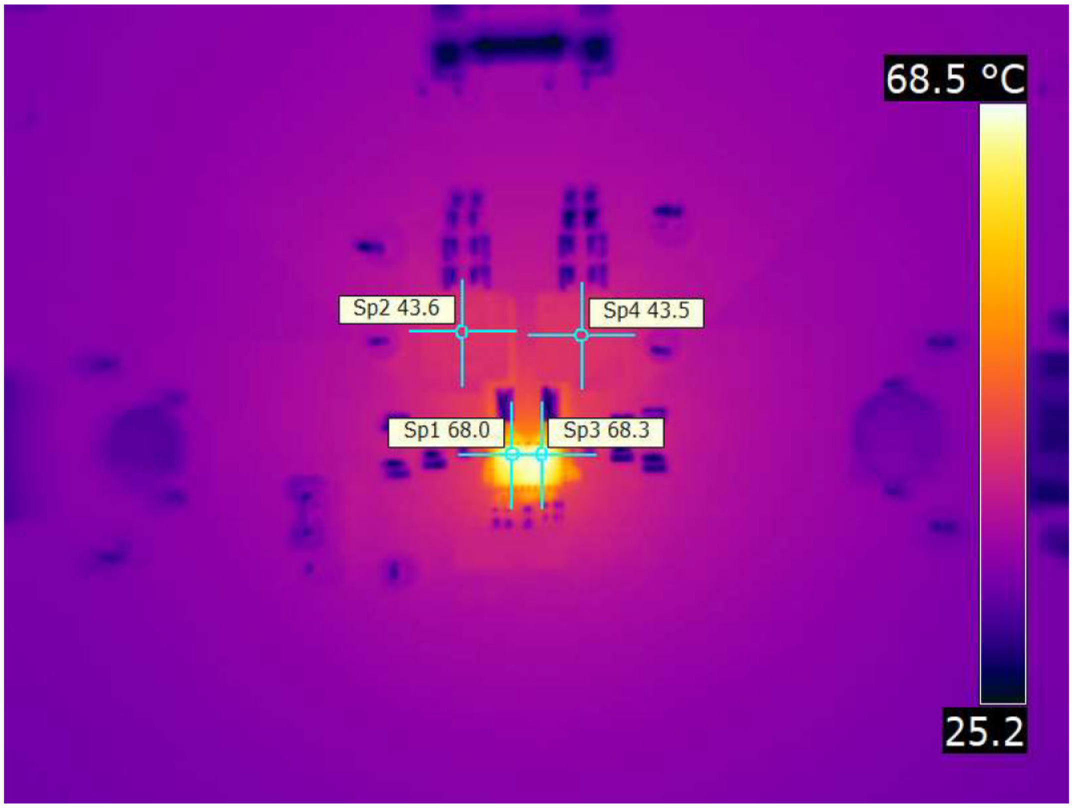

Figure 10-3. Thermal Image at 25°C Ambient - 2-phase Operation, f_{sw} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1 V, I_{OUT} = 12 A, Inductor = 560 nH (3.3 mΩ typical)

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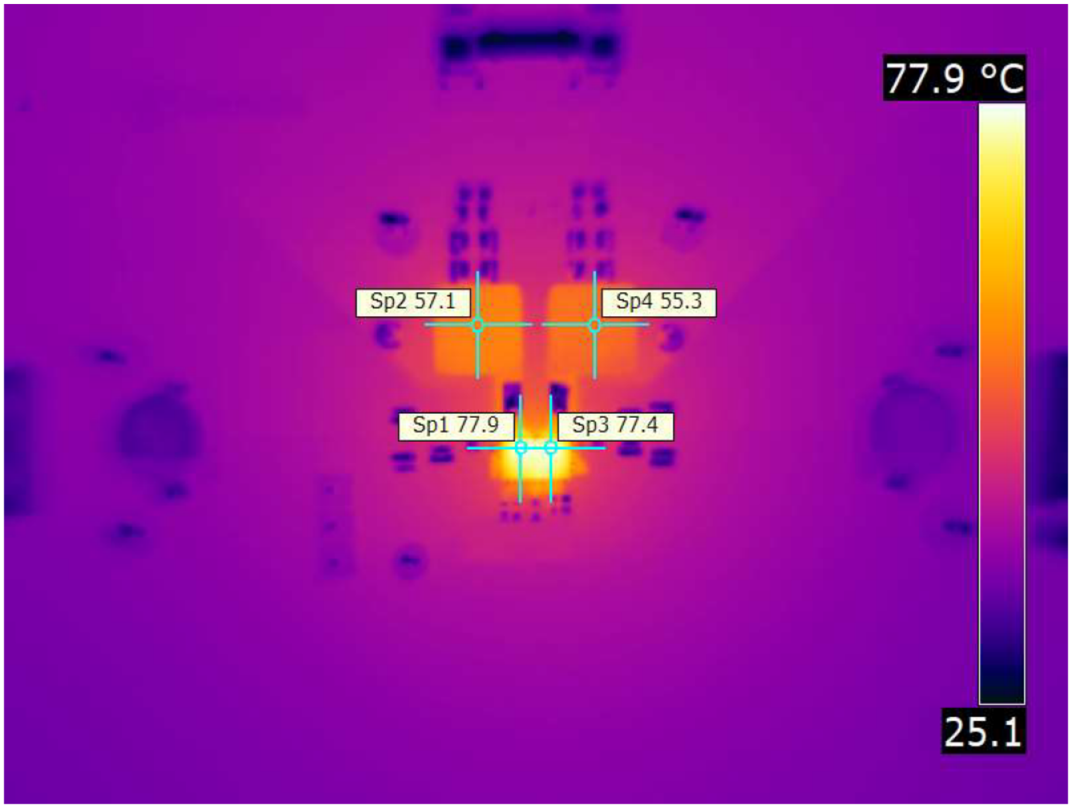

Figure 10-4. Thermal Image at 25°C Ambient - Dual Output Operation, f_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT1} = 1 V, I_{OUT1} = 6 A, L_1 = 560 nH (3.3 mΩ Max), V_{OUT2} = 3.3 V, I_{OUT2} = 6 A, L_2 = 1.2 µH (7.5 mΩ Max)

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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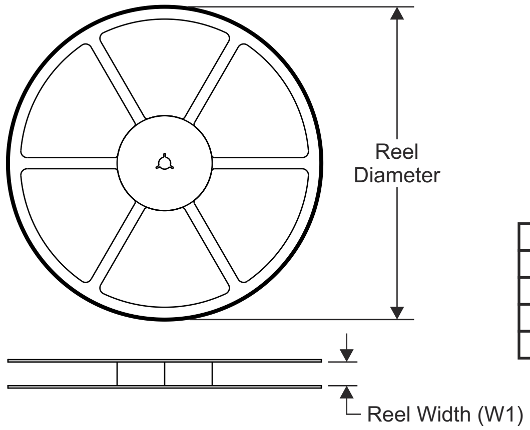
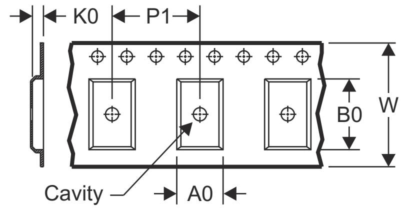
12.1 Tape and Reel Information

REEL DIMENSIONS

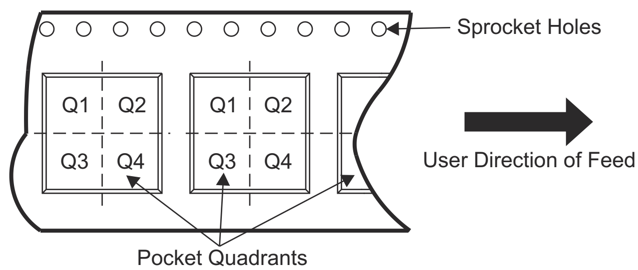


TAPE DIMENSIONS



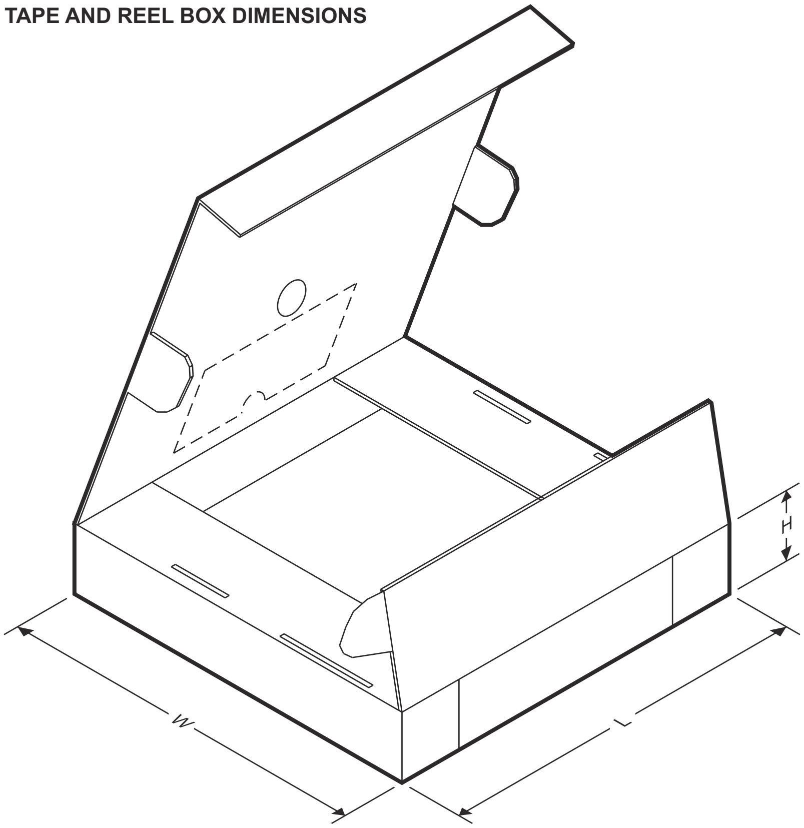
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS541620RPBT	VQFH-HR	RPB	25	250	180.0	12.4	3.8	4.3	1.15	8.0	12	Q1
TPS541620RPBR	VQFH-HR	RPB	25	3000	180.0	12.4	3.8	4.3	1.15	8.0	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS541620RPBT	VQFH-HR	RPB	25	250	195.0	200.0	45.0
TPS541620RPBR	VQFH-HR	RPB	25	3000	195.0	200.0	45.0

ADVANCE INFORMATION

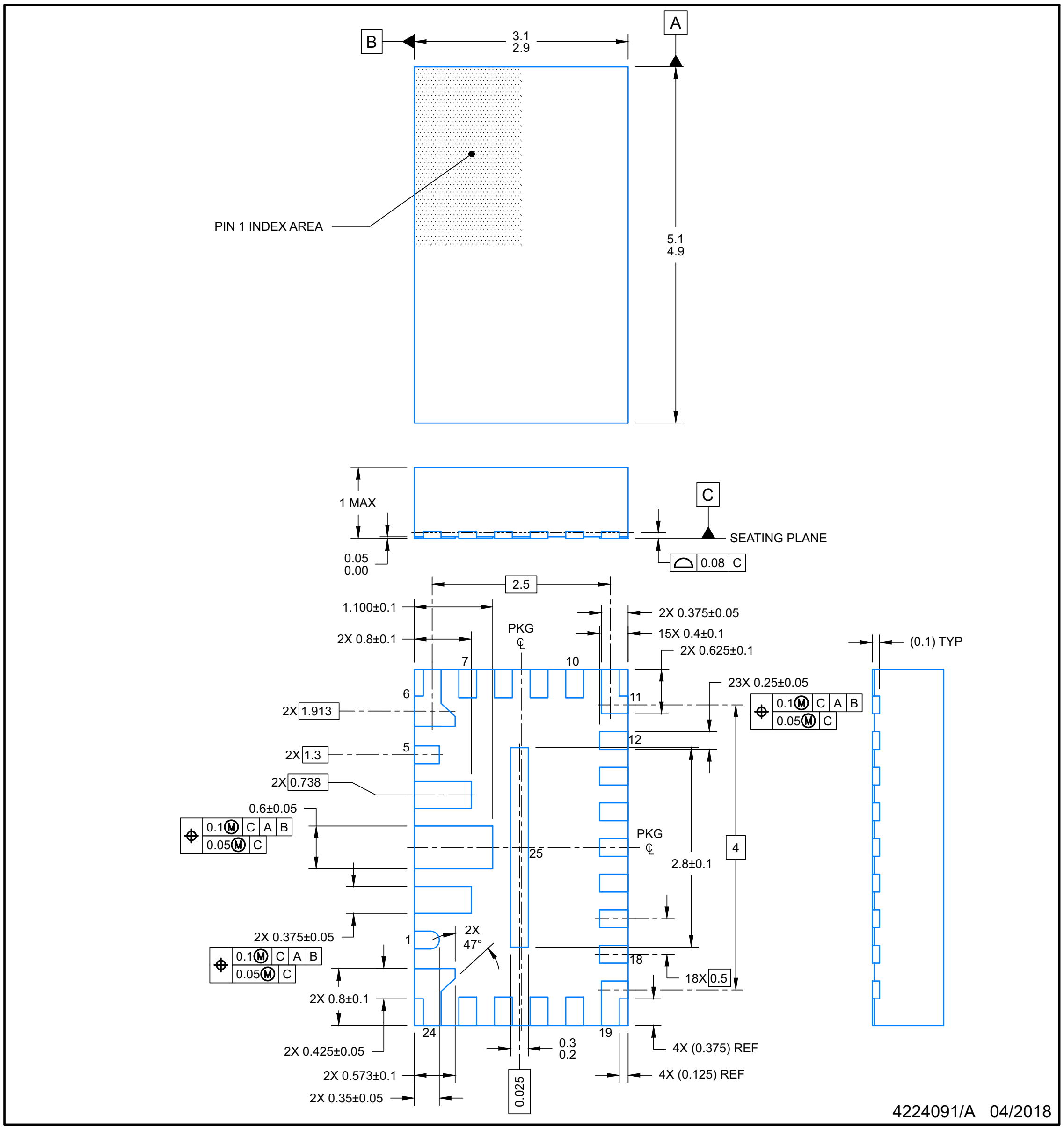
ADVANCE INFORMATION

PACKAGE OUTLINE

RPB0025A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD



NOTES:

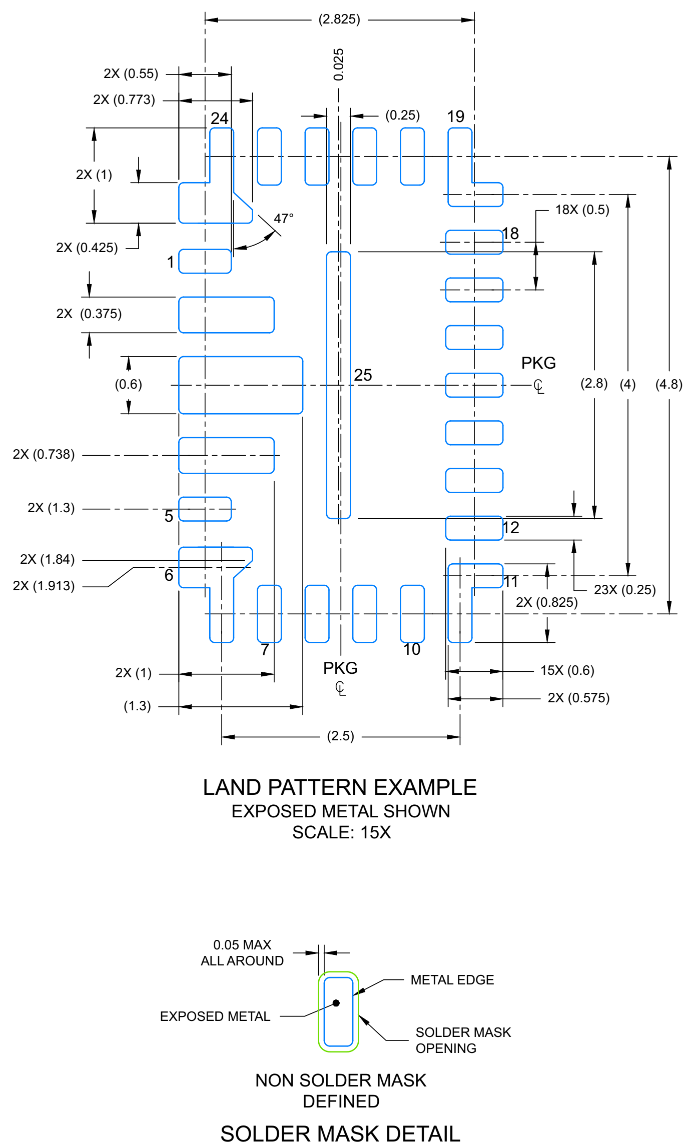
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RPB0025A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD



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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

ADVANCE INFORMATION

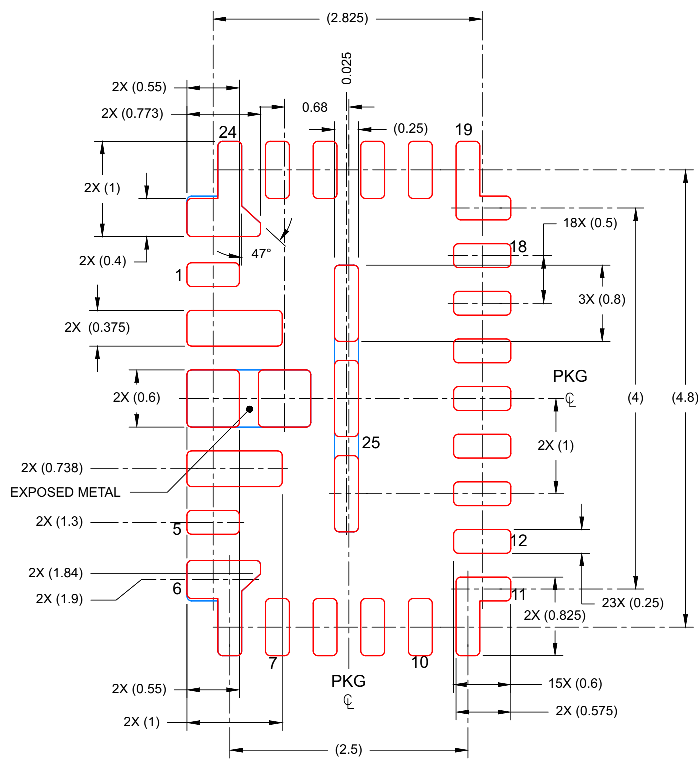
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RPB0025A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
UNDER PACKAGE
PAD 3, 6, 24 & 25: 87%
SCALE: 15X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS541620RPBT	ACTIVE	VQFN-HR	RPB	25	250	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		Samples
TPS541620RPBR	PREVIEW	VQFN-HR	RPB	25	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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