Wide Input 60V, 200mA Synchronous Step-Down DC-DC Converter with Low IQ

Check for Samples: TPS54061

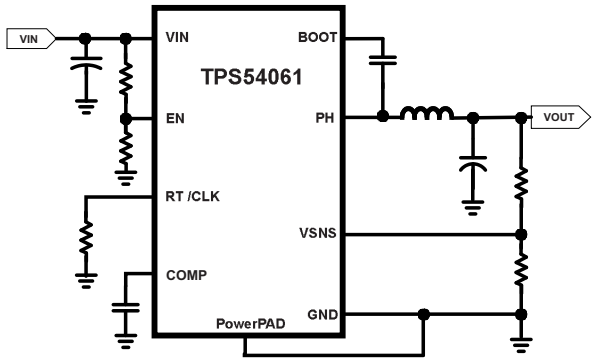
FEATURES

- **Integrated High Side and Low Side MOSFET**
- **Diode Emulation for Improved Light Load Efficiency**
- **Peak Current Mode Control**
- **90 µA Operating Quiescent Current**
- **1.4 µA Shutdown Supply Current**
- **50 kHz to 1100 kHz Adjustable Switching Frequency**
- **Synchronizes to External Clock**
- **Internal Slow Start**
- **0.8 V ±1% Voltage Reference**
- **Stable with Ceramic Output Capacitors or Low Cost Aluminum Electrolytic**
- **Cycle-by-Cycle Current Limit, Thermal, OVP and Frequency Fold Back Protection**
- **VSON-8 Package, 3 mm X 3 mm With Thermal Pad**
- **–40°C to 150°C Operating Junction Temperature**

APPLICATIONS

- **4-20 mA Current-Loop Powered Sensors**
- **Low Power Standby or Bias Voltage Supplies**
- **Industrial Process Control, Metering, and Security Systems**
- **High Efficiency Replacement for High Voltage Linear Regulators**

SIMPLIFIED SCHEMATIC



DESCRIPTION

The TPS54061 device is a 60-V, 200-mA, synchronous step-down DC-DC converter with integrated high side and low side MOSFETs. Current mode control provides simple external compensation and flexible component selection. The non-switching supply current is 90 µA. Using the enable pin, shutdown supply current is reduced to 1.4 µA.

To increase light load efficiency the low side MOSFET emulates a diode when the inductor current reaches zero.

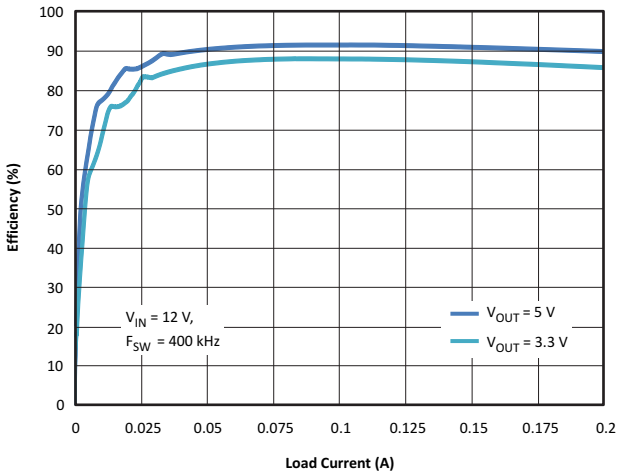
Under voltage lockout is internally set at 4.5 V, but can be increased using two resistors on the enable pin. The output voltage startup ramp is controlled by the internal slow start time.

The adjustable switching frequency range allows efficiency and external component size to be optimized. Frequency foldback and thermal shutdown protects the part during an overload condition.

The TPS54061 enables small designs by integrating the MOSFETs, boot recharge diode, and minimizing the IC footprint with a small 3mm x 3mm thermally enhanced VSON package

The TPS54061 is supported in the Webench™ Designer at www.ti.com.

EFFICIENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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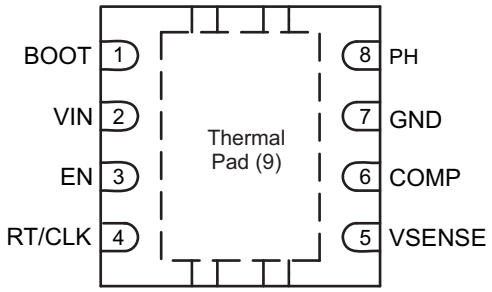
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION(1)

T_J	PACKAGE	PART NUMBER
–40°C to 150°C	VSON-8 DRB	TPS54061DRB

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

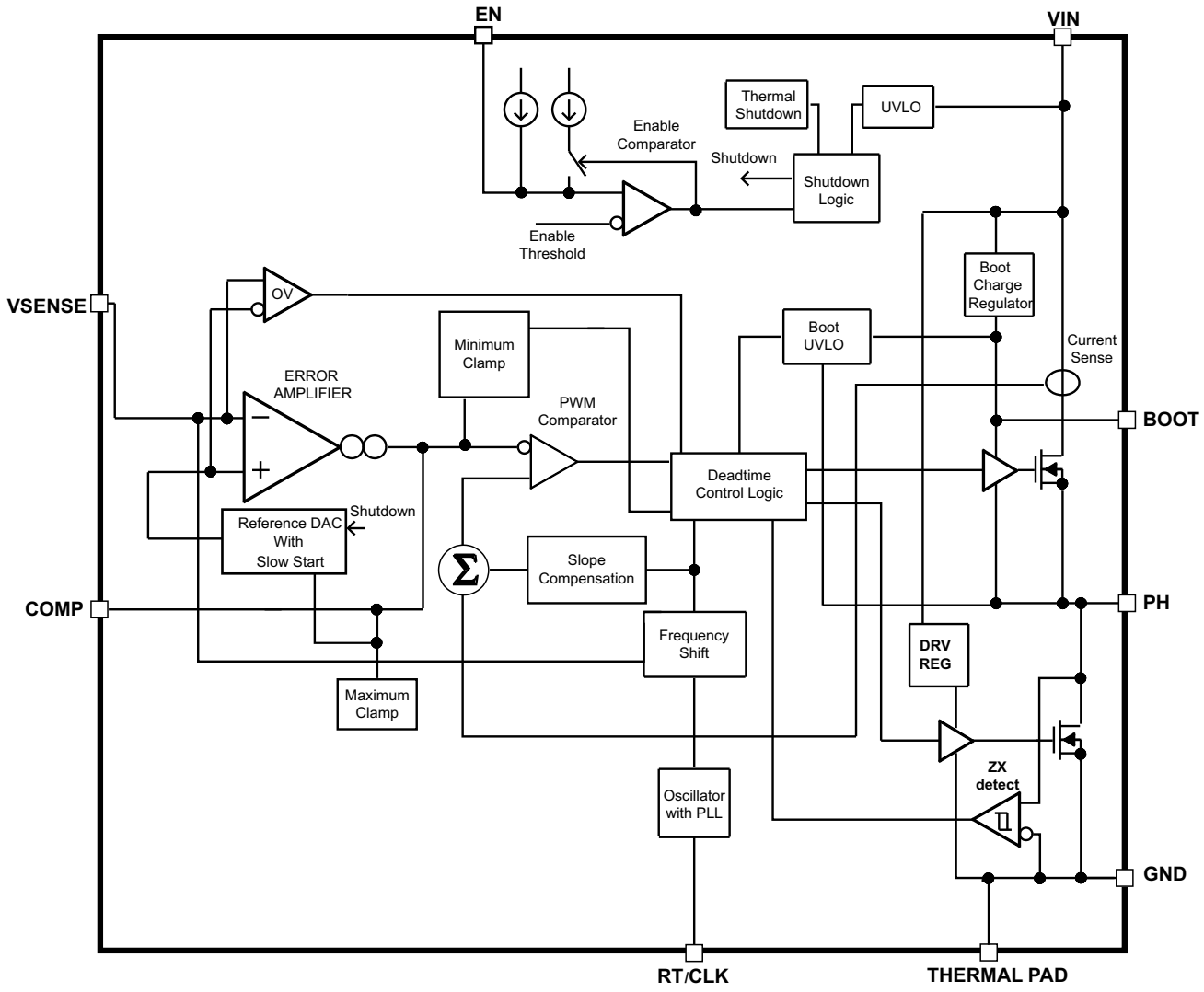
PIN CONFIGURATION
VSON-8 PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
BOOT	1	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
VIN	2	Input supply voltage, 4.7 V to 60 V.
EN	3	Enable pin with internal pull-up current source. Pull below 1.18 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors, see the Enable and Adjusting Undervoltage Lockout section.
RT/CLK	4	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor frequency programming.
VSENSE	5	Inverting input of the transconductance (gm) error amplifier.
COMP	6	Error amplifier output and input to the output switch current comparator. Connect frequency compensation components to this pin.
GND	7	Ground
PH	8	The source of the internal high-side power MOSFET and drain of the internal low side MOSFET
Thermal Pad	9	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage	VIN	–0.3	62	V
	EN(2)	–0.3	8	V
	BOOT-PH		8	V
	BOOT		70	V
	VSENSE	–0.3	6	V
	COMP	–0.3	3	V
	PH	–0.6	62	V
	PH, 10ns Transient	–2	62	V
	RT/CLK	–0.3	6	V
Current	VIN	Internally Limited		A
	BOOT		100	mA
	PH	Internally Limited		A
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CDM) QSS 009-147 (JESD22-C101B.01)		500	V
Operating junction temperature		–40	150	ºC
Storage temperature		–65	150	ºC

(1) The Absolute Maximum Ratings specified in this section will apply to all specifications of this document unless otherwise noted. These specifications will be interpreted as the conditions which may damage the device with a single occurrence.
(2) See Enable and Adjusting Undervoltage Lockout section

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54061	UNITS
		VSON-8	
θ_{JA}	Junction-to-ambient thermal resistance	42.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.0	
θ_{JB}	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS(1)

TEST CONDITIONS: T_J = –40°C to 150°C, VIN = 4.7 To 60 V ((unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage	VIN	4.7		60	V
Shutdown supply current	EN = 0V		1.4		µA
Iq Operating – Non switching	VSENSE = 0.9V, VIN = 12V		90	110	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.23	1.4	V
	Falling	1	1.18		V
Input current	Enable threshold +50 mV		–4.7		µA
	Enable threshold –50 mV		–1.2		µA
Hysteresis			–3.5		µA
Enable high to start switching time			450		µs
VIN					
VIN start voltage	VIN rising		4.5		V
VOLTAGE REFERENCE					
Voltage reference	T_J = 25°C, VIN = 12 V	0.792	0.8	0.808	V
	1mA < I_{OUT} < Minimum Current Limit	0.784	0.8	0.816	
HIGH-SIDE MOSFET					
Switch resistance	BOOT-PH = 5.7V		1.5	3.0	Ω
LOW-SIDE MOSFET					
Switch resistance	VIN = 12V		0.8	1.5	Ω
ERROR AMPLIFIER					
Input Current	VSENSE pin		20		nA
Error amp gm	–2µA < $I_{(COMP)}$ < 2µA, $V_{(COMP)}$ = 1V		108		µMhos
EA gm during slow start	–2µA < $I_{(COMP)}$ < 2µA, $V_{(COMP)}$ = 1V, VSENSE = 0.4V		27		µMhos
Error amp dc gain	VSENSE = 0.8V		1000		V/V
Min unity gain bandwidth			0.5		MHz
Error amp source/sink	$V_{(COMP)}$ = 1V, 100 mV Overdrive		±8		µA
Start Switching Threshold			0.57		V
COMP to Iswitch gm			1.0		A/V
CURRENT LIMIT					
High side sourcing current limit threshold	BOOT-PH = 5.7V	250	350	500	mA
Zero cross detect current			–1.1		mA
THERMAL SHUTDOWN					
Thermal shutdown			176		C
RT/CLK					
Operating frequency using RT mode		50		1100	kHz
Switching frequency	$R_{(RT/CLK)}$ = 120kΩ	425	472	520	kHz
Minimum CLK pulsewidth			40		ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 120kΩ		0.53		V
RT/CLK high threshold				1.8	V
RT/CLK low threshold		0.5			V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor		130		ns
PLL lock in time	Measure at 500 kHz		100		µs

(1) The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it.

ELECTRICAL CHARACTERISTICS(1) (continued)

TEST CONDITIONS: T_J = –40°C to 150°C, VIN = 4.7 To 60 V ((unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PLL frequency range		300		1100	kHz
PH					
Minimum On time	Measured at 50% to 50%, I_{OUT} = 200mA		120		ns
Dead time	VIN = 12V, I_{OUT} = 200mA, One transition		30		ns
BOOT					
BOOT to PH regulation voltage	VIN = 12V		6.0		V
BOOT-PH UVLO			2.9		V
INTERNAL SLOW START TIME					
Slow start time	f_{SW} = 472kHz, RT = 120kΩ, 10% to 90%		2.36		ms

TYPICAL CHARACTERISTICS

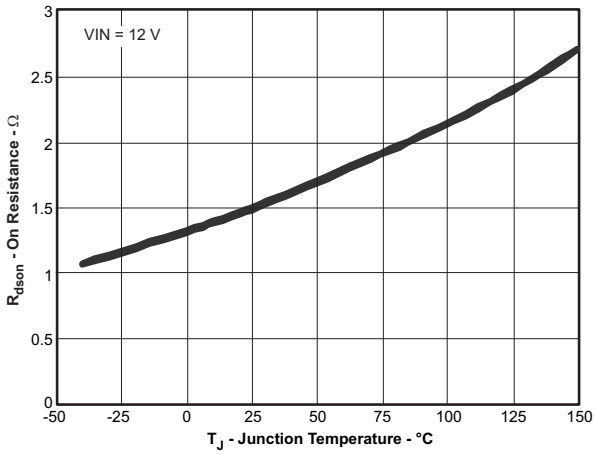


Figure 1. High Side $R_{DS(on)}$ vs Temperature

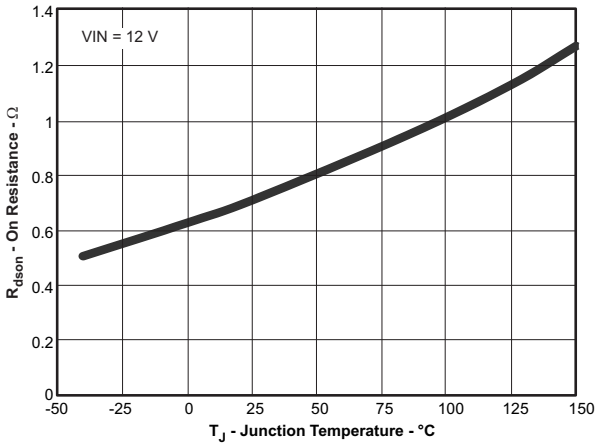


Figure 2. Low Side $R_{DS(on)}$ vs Temperature

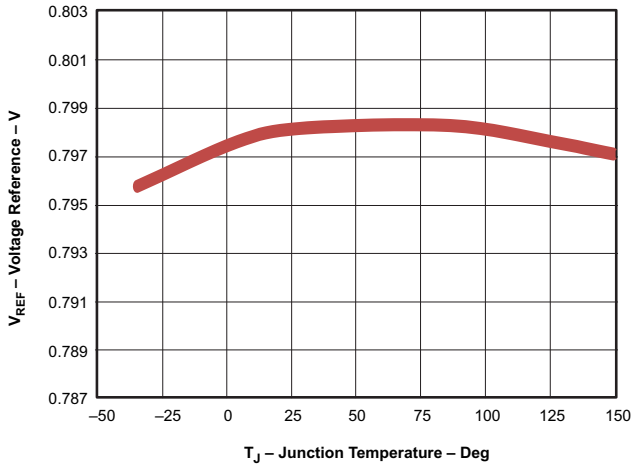


Figure 3. V_{REF} Voltage vs Temperature

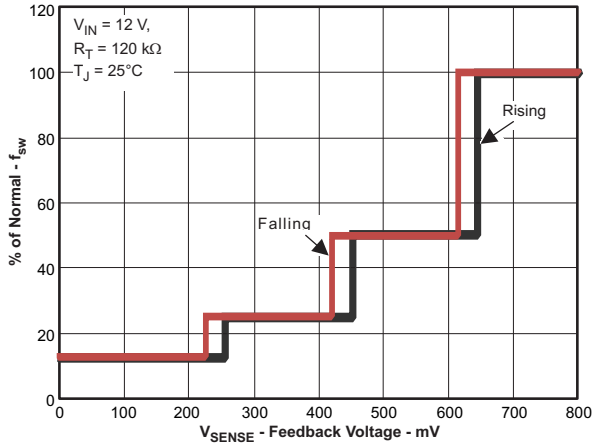


Figure 4. Frequency vs VSENSE Voltage

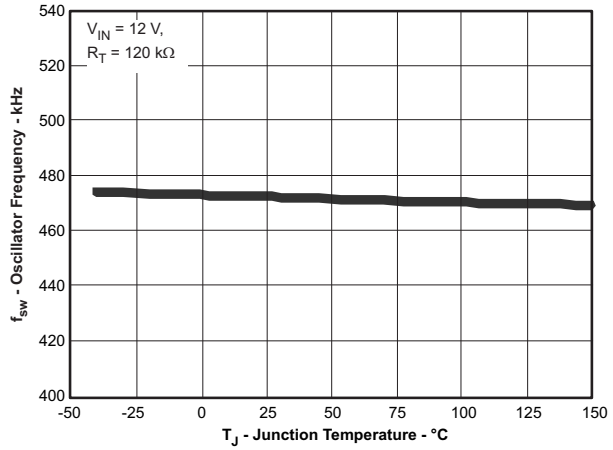


Figure 5. Frequency vs Temperature

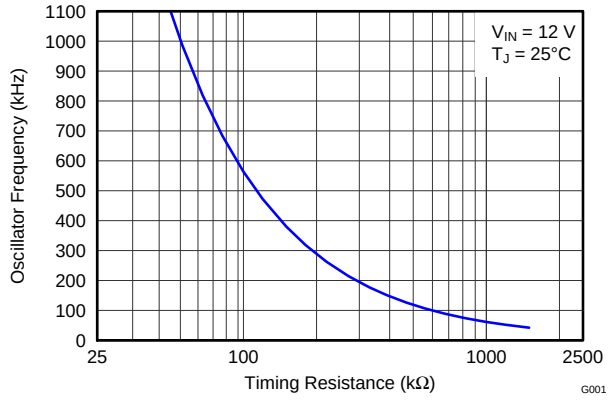


Figure 6. Frequency vs RT/CLK Resistance

TYPICAL CHARACTERISTICS (continued)

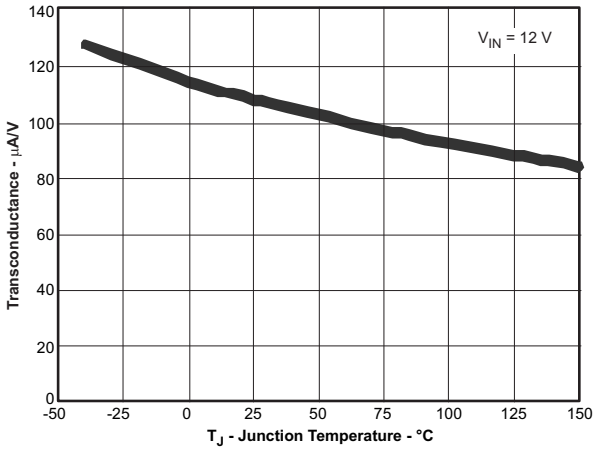


Figure 7. Error Amp Transconductance vs Temperature

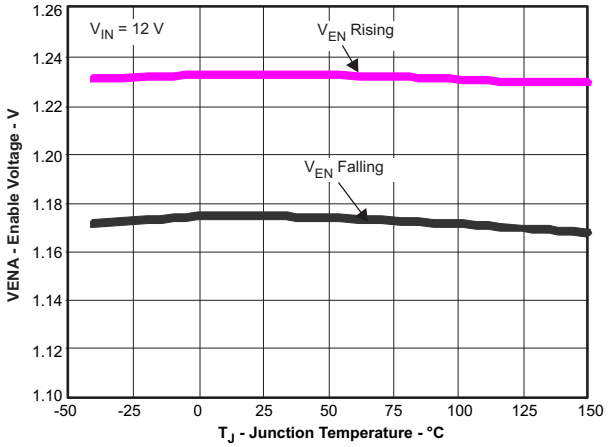


Figure 8. Enable Pin Voltage vs Temperature

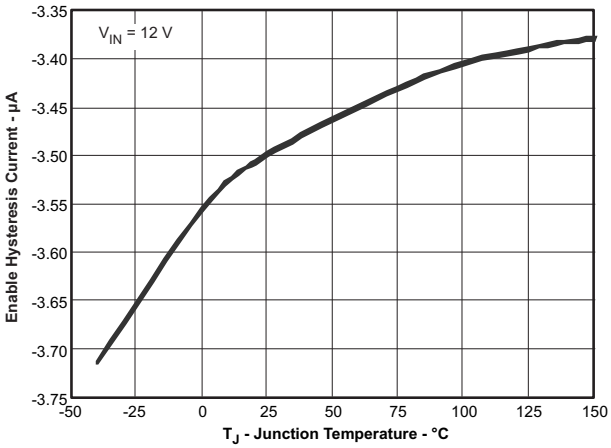


Figure 9. Enable Pin Hysteresis Current vs Temperature

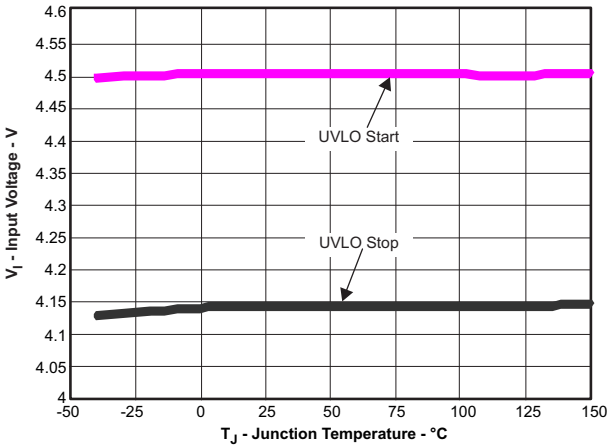


Figure 10. Input Voltage (UVLO) vs Temperature

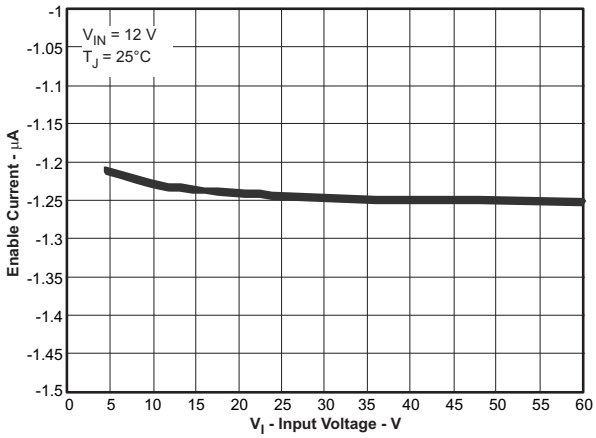


Figure 11. Enable Pin Pull Up Current vs Input Voltage

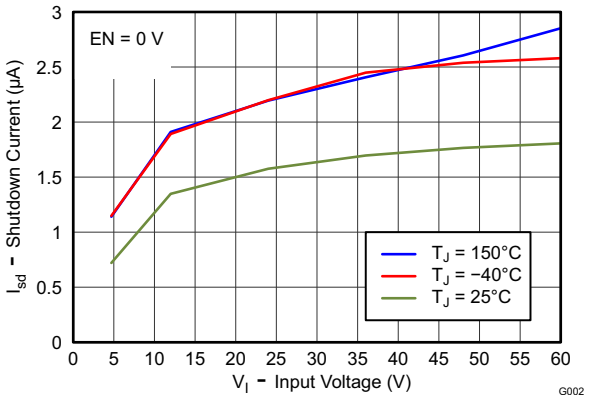


Figure 12. Shutdown Supply Current (VIN) vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

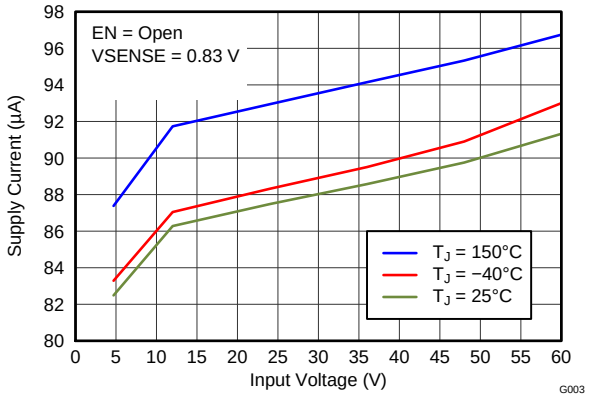


Figure 13. Supply Current (VIN pin) vs Input Voltage

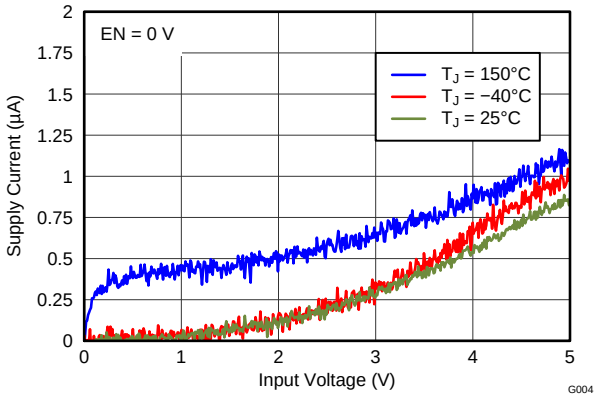


Figure 14. Supply Current (VIN pin) vs Input Voltage (0V to VSTART) EN Pin Low

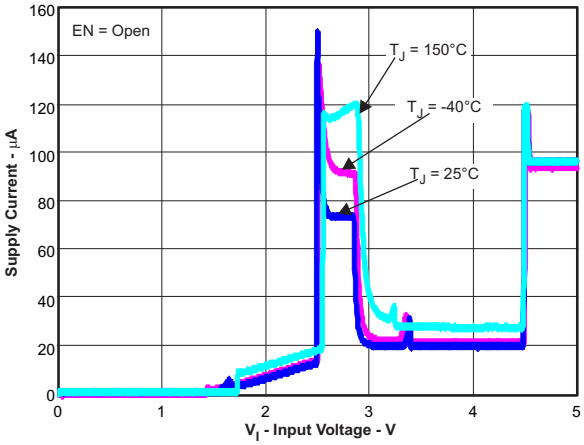


Figure 15. Supply Current (VIN pin) vs Input Voltage (0V to V_{START}) EN Pin Open

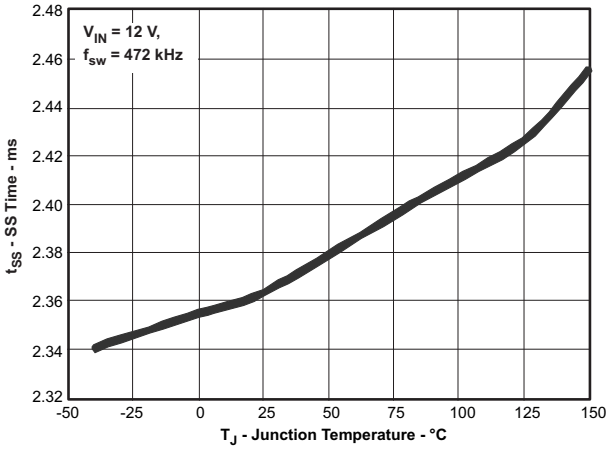


Figure 16. Slow Start Time vs Temperature

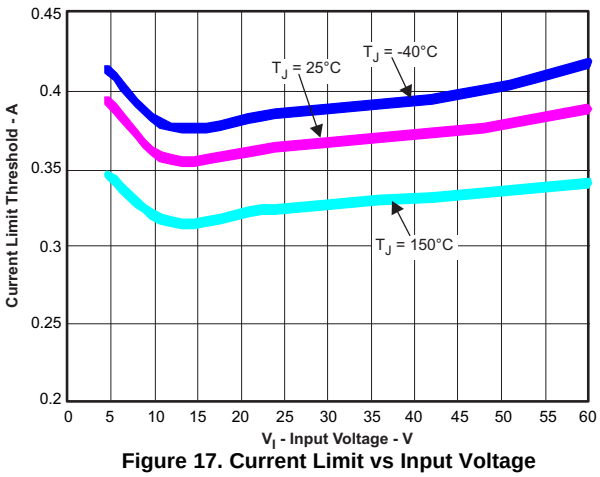


Figure 17. Current Limit vs Input Voltage

OVERVIEW

The TPS54061 device is a 60 V, 200 mA, step-down (buck) regulator with an integrated high side and low side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The switching frequency of 50 kHz to 1100 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54061 has a default start up voltage of approximately 4.5V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN pin is floating the device will operate. The operating current is 90µA when not switching and under no load. When the device is disabled, the supply current is 1.4µA.

The integrated 1.5Ω high side MOSFET and 0.8Ω low side MOSFET allows for high efficiency power supply designs capable of delivering 200 milliamperes of continuous current to a load.

The TPS54061 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The TPS54061 can operate at high duty cycles because of the boot UVLO. The output voltage can be adjusted down to as low as the 0.8 V reference.

The TPS54061 has an internal output OV protection that disables the high side MOSFET if the output voltage is 109% of the nominal output voltage.

The TPS54061 reduces external component count by integrating the slow start time using a reference DAC system.

The TPS54061 resets the slow start times during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54061 uses adjustable fixed frequency, peak current mode control. The output voltage is sensed through external resistors on the VSENSE pin and compared to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the COMP voltage, the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level.

Slope Compensation Output Current

The TPS54061 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations.

Error Amplifier

The TPS54061 uses a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal slow start voltage or the internal 0.8 V voltage reference. The transconductance (gm) of the error amplifier is 108 µA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. The frequency compensation components (capacitor, series resistor and capacitor) are added to the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise voltage reference over temperature by scaling the output of a temperature stable band-gap circuit

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10kΩ for the R_{LS} resistor and use the Equation 1 to calculate R_{HS}.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (1)$$

Enable and Adjusting Undervoltage Lockout

The TPS54061 is enabled when the VIN pin voltage rises above 4.5 V and the EN pin voltage exceeds the EN rising threshold of 1.23V. The EN pin has an internal pull-up current source, I1, of 1.2 µA that provides the default enabled condition when the EN pin floats.

If an application requires a higher input undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 18 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.23 V, an additional 3.5 µA of hysteresis current, Ihys, is sourced out of the EN pin. When the EN pin is pulled below 1.18 V, the 3.5 µA Ihys current is removed. This additional current facilitates adjustable input voltage hysteresis. Use Equation 2 to calculate R_{UVLO1} for the desired input start and stop voltages . Use Equation 3 to similarly calculate R_{UVLO2}.

In applications designed to start at relatively low input voltages (e.g., from 4.7V to 10V) and withstand high input voltages (e.g., from 40V to 60V), the EN pin may experience a voltage greater than the absolute maximum voltage of 8.0V during the high input voltage condition. It is recommended to use a zener diode to clamp the pin voltage below the absolute maximum rating.

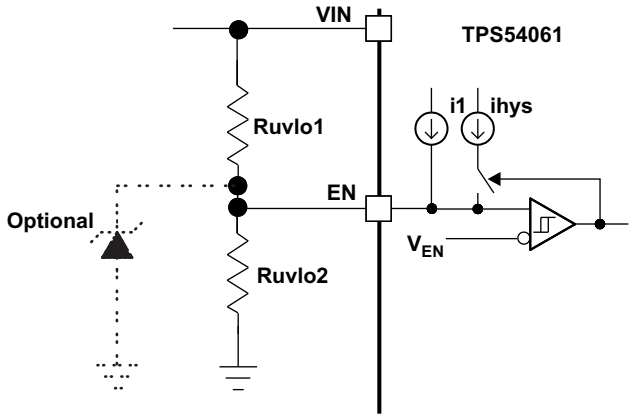


Figure 18. Adjustable Undervoltage Lock Out

$$R_{UVLO}1 = \frac{V_{START}\left(\frac{V_{ENAFALLING}}{V_{ENARISING}}\right) - V_{STOP}}{I1 \times \left(1 - \frac{V_{ENAFALLING}}{V_{ENARISING}}\right) + I_{HYS}} \quad (2)$$

$$R_{UVLO}2 = \frac{R_{UVLO}1 \times V_{ENAFALLING}}{V_{STOP} - V_{ENAFALLING} + R_{UVLO}1 \times \left(I_1 + I_{HYS}\right)} \quad (3)$$

Internal Slow Start

The TPS54061 has an internal digital slow start that ramps the reference voltage from zero volts to its final value in 1114 switching cycles. The internal slow start time is calculated by the following expression:

$$tss(ms) = \frac{1114}{f_{SW}(kHz)} \quad (4)$$

If the EN pin is pulled below the stop threshold of 1.18 V, switching stops and the internal slow start resets. The slow start also resets in thermal shutdown.

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54061 is adjustable over a wide range from 50 kHz to 1100 kHz by varying the resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.53 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 5. To reduce the solution size, one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 120ns and limits the operating frequency for high input voltages. The maximum switching frequency is also limited by the frequency shift circuit. More discussion on the details of the maximum switching frequency is located below.

$$R_T(k\Omega) = \frac{71657}{f_{SW}(kHz)^{1.039}} \quad (5)$$

Selecting the Switching Frequency

The TPS54061 implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and COMP pin voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

To enable higher switching frequency at high input voltages, the TPS54061 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Since the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still have frequency shift protection. During short-circuit events (particularly with high input voltage applications), the control loop has a finite minimum controllable on time and the output has a low voltage. During the switch on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time allowing the current to ramp down.

$$f_{SW}(\text{maxskip}) = \left(\frac{1}{t_{ON}}\right) \times \left(\frac{V_{OUT} + R_{LS} \times I_O + R_{DC} \times I_O}{V_{IN} - I_O \times R_{HS} + I_O \times R_{LS}}\right) \quad (6)$$

$$f_{SW}(\text{shift}) = \left(\frac{f\text{div}}{t_{ON}}\right) \times \left(\frac{V_{OUTSC} + R_{LS} \times I_{CL} + R_{DC} \times I_{CL}}{V_{IN} - I_{CL} \times R_{HS} + I_{CL} \times R_{LS}}\right) \quad (7)$$

Where:

I_O = Output current
I_{CL} = Current Limit
V_{IN} = Input Voltage
V_{OUT} = Output Voltage
V_{OUTSC} Output Voltage during short
R_{DC} = Inductor resistance
R_{HS} = High side MOSFET resistance
R_{LS} = Low side MOSFET resistance
t_{on} = Controllable on time
fdiv = Frequency divide (equals 1, 2, 4, or 8)

Synchronization to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through one of the circuit networks shown in Figure 19. The square wave amplitude must extend lower than 0.5 V and higher than 1.8V on the RT/CLK pin and have high and low states greater than 40ns. The synchronization frequency range is 300 kHz to 1100 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed in such a way that the device will have the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 19 through another resistor (e.g., 50Ω) to ground for clock signal that are not Hi-Z or tristate during the off state. The sum of the resistance should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10pF ceramic capacitor to RT/CLK pin. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5 V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and lock onto the CLK frequency within 100 microseconds. When the device transitions from the PLL mode to the resistor mode, the switching frequency will reduce from the external CLK frequency to 150 kHz, then reapply the 0.5V voltage source and the resistor will then set the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions.

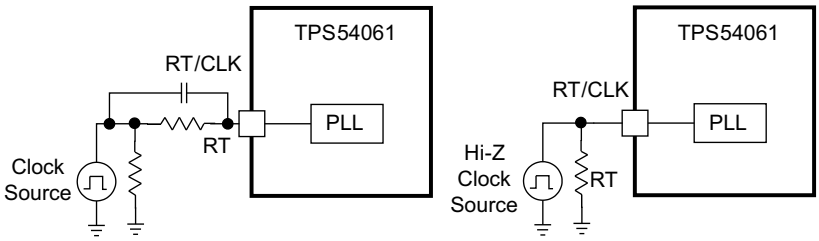


Figure 19. Synchronizing to a System Clock

Overvoltage Protection

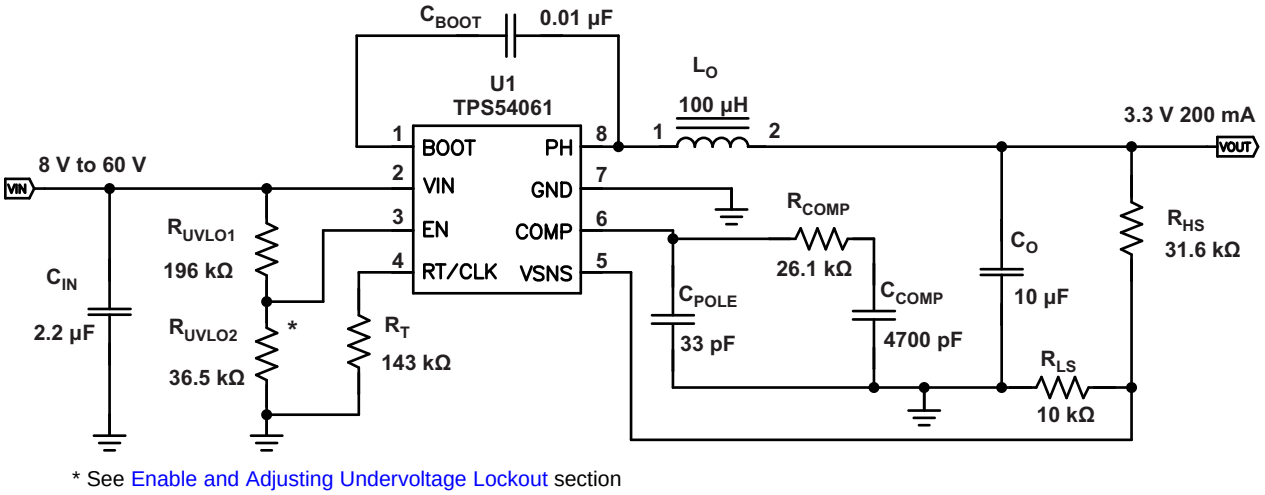
The TPS54061 incorporates an output over-voltage transient protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot.

The OVP feature minimizes the output overshoot when using a low value output capacitor by comparing the VSENSE pin voltage to OVP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVP threshold, the high side MOSFET is disabled to minimize output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high side MOSFET resumes normal operation.

Thermal Shutdown

The device implements an internal thermal shutdown until the junction temperature exceeds 176°C. The thermal shutdown forces the device to stop switching until the junction temperature falls below the thermal trip threshold. Once the die temperature decreases below 176°C, the device reinitiates the power up sequence by restarting the internal slow start.

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE No.1



* See Enable and Adjusting Undervoltage Lockout section

Figure 20. CCM Application Schematic

This example details the design of a continuous conduction mode (CCM) switching regulator design using ceramic output capacitors. If a low output current design is see design procedure Number 2. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	5.0V
Transient Response 50 to 150mA load step	ΔV_{OUT} = 4%
Maximum Output Current	200mA
Input Voltage	24 V nom. 8V to 60V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	7.50V
Stop Input Voltage (falling VIN)	6.50V

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency is limited by the minimum on-time of the internal power switch, the maximum input voltage, the output voltage and the frequency shift limitation.

Equation 6 and Equation 7 must be used to find the maximum switching frequency for the regulator, choose the lower value of the two results. Switching frequencies higher than these values will result in pulse skipping or a lack of overcurrent protection during short circuit conditions. The typical minimum on time, t_{on}min, is 120ns for the TPS54061. To ensure overcurrent runaway does not occur during short circuits in your design, use Equation 7 to determine the maximum switching frequency. With a maximum input voltage of 60V, inductor resistance of 0.77 Ω, high side switch resistance of 3.0 Ω, low side switch resistance of 1.5Ω, a current limit value of 350 mA and a short circuit output voltage of 0.1 V, the maximum switching frequency is 524 kHz and 1003 kHz in each case respectively. A switching frequency of 400 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 5. The switching frequency is set by resistor R_T shown in Figure 20. R_T is calculated to be 142 kΩ. A standard value of 143 kΩ is used.

Output Inductor Selection (LO)

To calculate the minimum value of the output inductor, use Equation 8. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used. Typically it is recommended to use KIND values in the range of 0.2 to 0.4; however, for designs using low ESR output capacitors such as ceramics and low output currents, a KIND value as high as 1 may be used. In a wide input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum. For this design example, use KIND of 0.4 and the minimum inductor value is calculated to be 97 µH. For this design, a standard 100µH value was chosen. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 10 and Equation 11.

For this design, the RMS inductor current is 200 mA and the peak inductor current is 239 mA. The chosen inductor is a Würth 74408943101. It has a saturation current rating of 680 mA and an RMS current rating of 520 mA. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value. The current flowing through the inductor is the inductor ripple current plus the average output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the calculated peak inductor current.

$$L_O\,\text{min} \geq \frac{V_{IN}\,\text{max} - V_{OUT}}{\text{Kind} \times I_O} \times \frac{V_{OUT}}{V_{IN}\,\text{max} \times f_{sw}} \tag{8}$$

$$I_{RIPPLE} \geq \frac{V_{OUT} \times \left(V_{IN}\text{max} - V_{OUT}\right)}{V_{IN}\text{max} \times L_O \times f_{SW}} \tag{9}$$

$$I_L\text{rms} = \sqrt{I_O^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN}\text{max} - V_{OUT}\right)}{V_{IN}\text{max} \times L_O \times f_{SW}}\right)^2} \tag{10}$$

$$I_L\text{peak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \tag{11}$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria. The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current until the regulator increases the inductor current. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also will temporarily not be able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 15 shows the minimum output capacitance necessary to accomplish this, where ΔIout is the change in output current, f_{sw} is the regulators switching frequency and ΔVout is the allowable change in the output voltage.

For this example, the transient load response is specified as a 4% change in Vout for a load step from 50 mA to 150 mA. For this example, ΔI_{OUT} = 0.150 –0.05 = 0.10 and ΔV_{OUT} = 0.04 × 3.3 = 0.132.

Using these values gives a minimum capacitance of 3.79 µF. This does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The low side FET of the regulator emulates a diode so it can not sink current so any stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases, as in Figure 28. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 14 is used to calculate the minimum capacitance input the output voltage overshoot to a desired value, where $_{LO}$ is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, $V_O+\Delta V_O$ is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 150 mA to 50 mA. The output voltage will increase during this load transition and must be limited to 4% of the output voltage to satisy the design goal. This will make $V_O+\Delta V_O$ = 1.04 × 3.3 = 3.432 V. V_O is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 14 yields a minimum capacitance of 2.25 µF.

Equation 13 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{SW} is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. Equation 13 yields 1.48 µF. Equation 16 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 16 indicates the ESR should be less than 0.160 Ω.

The most stringent criteria for the output capacitor is 3.79 µF of capacitance to maintain the output voltage regulation during an load transient.

Additional capacitance de-ratings for aging, temperature and dc bias will increase this minimum value. For this example, 10 µF, 10V X5R ceramic capacitor with 0.003 Ω of ESR in a 1206 package is used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current.

Equation 12 can be used to calculate the RMS ripple current the output capacitor needs to support. For this example, Equation 12 yields 10.23 mA.

$$IC_Orms = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times (V_{IN}max - V_{OUT})}{V_{IN}max \times L_O \times f_{SW}} \right) \quad (12)$$

$$C_O1 \geq \frac{I_{RIPPLE}}{V_{RIPPLE}} \times \left(\frac{1}{8 \times f_{SW}} \right) \quad (13)$$

$$C_O2 \geq L_O \times \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (14)$$

$$C_O3 \geq \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{2}{f sw} \quad (15)$$

$$R_C \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (16)$$

Input capacitor

The TPS54061 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 1µF of effective capacitance. The effective capacitance includes any deration for dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have an rms current rating greater than the maximum rms input current. The input rms current can be calculated using Equation 17. The value of a ceramic capacitor varies significantly over temperature and the dc bias applied to the capacitor. The capacitance variations with temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors

because they have a high capacitance to volume ratio and are fairly stable over temperature. The effective value of a capacitor decreases as the dc bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 60 V voltage rating is required to support the maximum input voltage. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated by rearranging Equation 18.

Using the design example values, Ioutmax = 200 mA, C_{IN} = 2.2 µF, f_{SW} = 400 kHz, yields an input voltage ripple of 56.8 mV and an rms input ripple current of 98.5 mA.

$$IC_{IN}rms = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{INmin}} \times \frac{(V_{INmin} - V_{OUT})}{V_{INmin}}} \quad (17)$$

$$C_{IN} \geq \frac{I_O}{V_{IN}ripple} \times \left(\frac{0.25}{f_{SW}}\right) \quad (18)$$

Bootstrap Capacitor Selection

A 0.01-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10V or higher voltage rating.

Under Voltage Lock Out Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54061. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.50 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.50 V (UVLO stop). The programmable UVLO and enable voltages are set by connecting resistor divider between Vin and ground to the EN pin. Equation 2 and Equation 3 can be used to calculate the resistance values necessary. For example, a 196 kΩ resistor between Vin and EN and a 36.5 kΩ resistor between EN and ground are required to produce the 7.50 and 6.50 volt start and stop voltages. See the Enable and Adjusting Undervoltage Lockout section for additional considerations in high input voltage applications.

Output Voltage and Feedback Resistors Selection

For the example design, 10 kΩ was selected for R_{LS}. Using Equation 1, R_{HS} is calculated as 31.46 kΩ. The nearest standard 1% resistor is 31.6 kΩ.

Closing the Loop

There are several methods used to compensate DC/DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the cross over frequency used in the calculations. This method assume the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, fpole, and the ESR zero, fzero must be calculated using Equation 19 and Equation 20. For Cout, use a derated value of 6.0 µF. Use Equation 21 and Equation 22, to estimate a starting point for the crossover frequency, fco, to design the compensation. For the example design, fpole is 1015 Hz and fzero is 5584 kHz.

Equation 21 is the geometric mean of the modulator pole and the ESR zero and Equation 22 is the mean of modulator pole and the switching frequency. Equation 21 yields 119.2 kHz and Equation 22 gives 17.9 kHz. Use a frequency near the lower value of Equation 21 or Equation 22 for an initial crossover frequency.

For this example, fco of 17.9 kHz is used. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

To determine the compensation resistor, R_{COMP}, use Equation 23. Assume the power stage transconductance, gmps, is 1.00 A/V. The output voltage, Vo, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 3.3 V, 0.8 V and 108 µA/V, respectively.

R_{COMP} is calculated to be 25.9 kΩ, use the nearest standard value of 26.1 kΩ. Use Equation 24 to set the compensation zero equal to the modulator pole frequency. Equation 24 yields a 3790 pF for capacitor C_{COMP} and a 4700 pF is chosen. Use the larger value of Equation 25 and Equation 26 to calculate the C_{POLE} value, to set the compensation pole. Equation 26 yields 30.5 pF so the nearest standard of 33 pF is selected.

$$fpole(Hz) = \frac{1}{\frac{Vout}{Io} \times Co \times 2 \times \pi} \quad (19)$$

$$fzero(Hz) = \frac{1}{R_C \times C_O \times 2 \times \pi} \quad (20)$$

$$fco1(Hz) = \left(fzero \times fpole\right)^{0.5} \quad (21)$$

$$fco2(Hz) = \left(\frac{fsw}{2} \times fpole\right)^{0.5} \quad (22)$$

$$R_{COMP} = \frac{2 \times \pi \times f_{CO} \times C_O}{gmps} \times \frac{V_{OUT}}{V_{REF} \times gmea} \quad (23)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{POLE}} \quad (24)$$

$$C_{POLE1} = \frac{R_C \times C_O}{R_{COMP}} \quad (25)$$

$$C_{POLE2} = \frac{1}{R_{COMP} \times f_{SW} \times \pi} \quad (26)$$

Characteristics

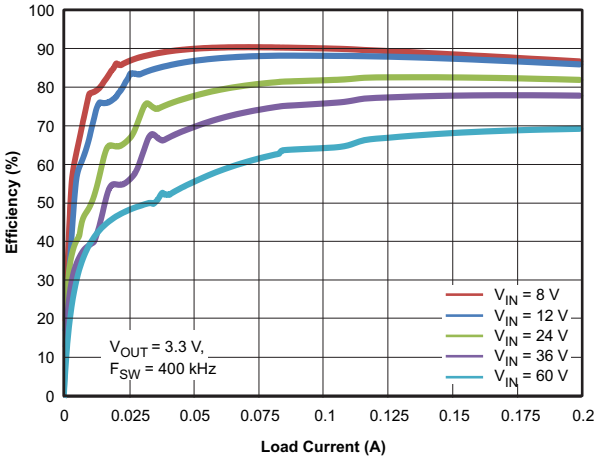


Figure 21. Efficiency vs Output Current

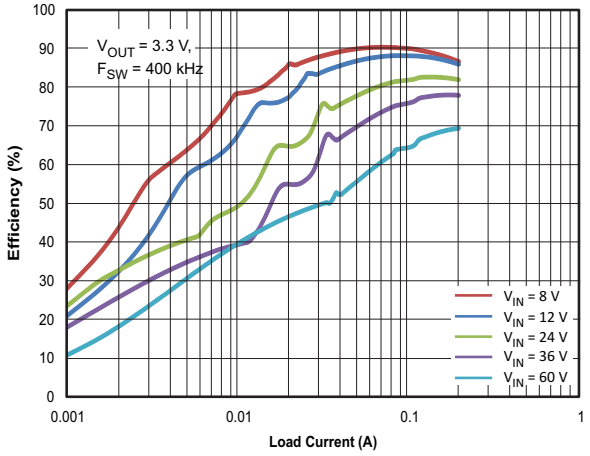


Figure 22. Efficiency vs Output Current

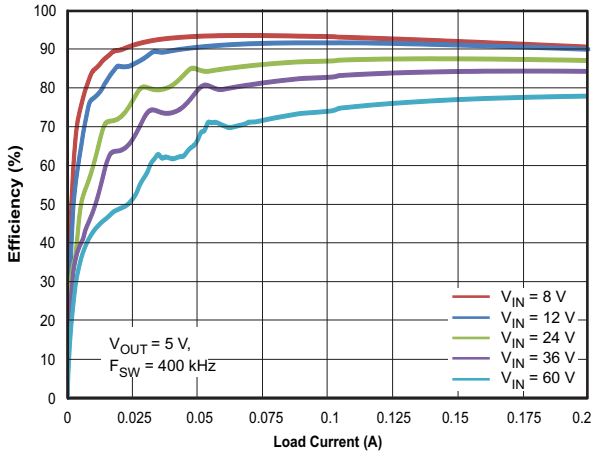


Figure 23. Efficiency vs Output Current

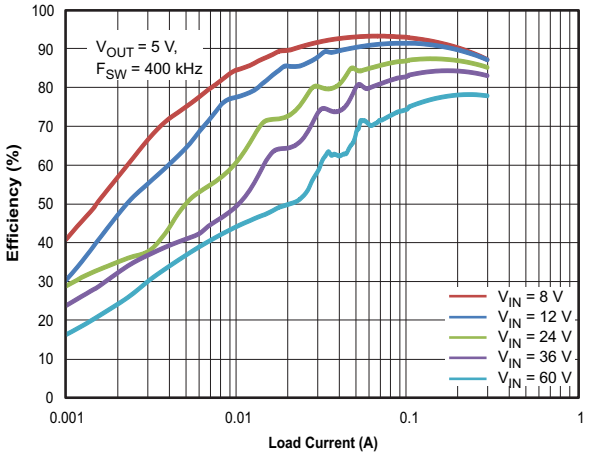


Figure 24. Efficiency vs Output Current

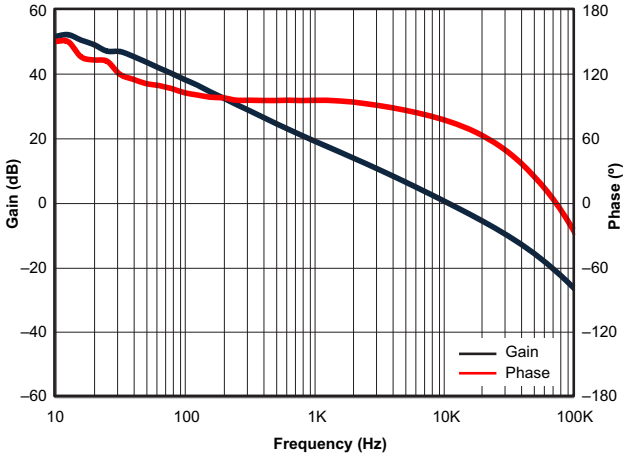


Figure 25. Gain vs Phase

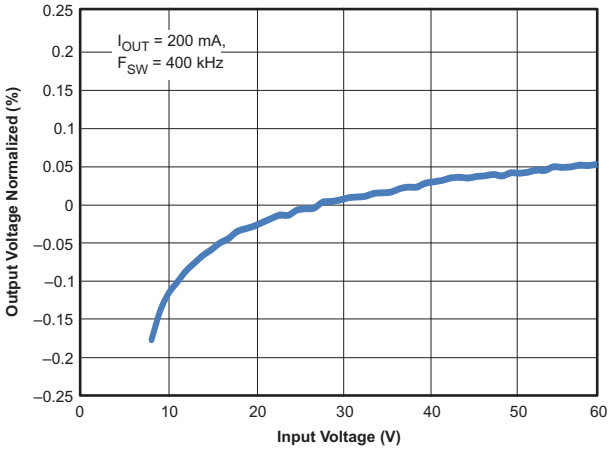


Figure 26. Output Voltage vs Input Voltage

Characteristics (continued)

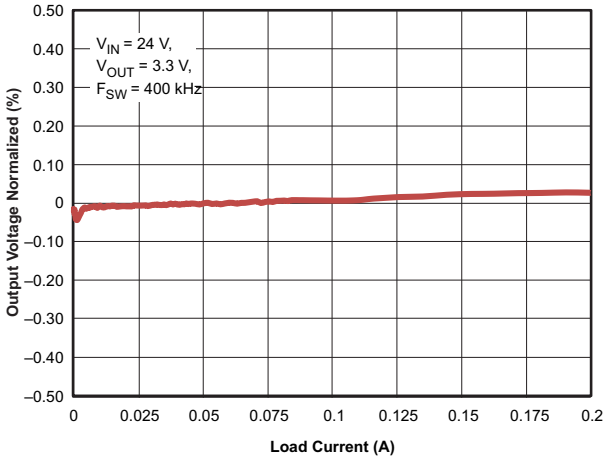


Figure 27. Output Voltage vs Output Current

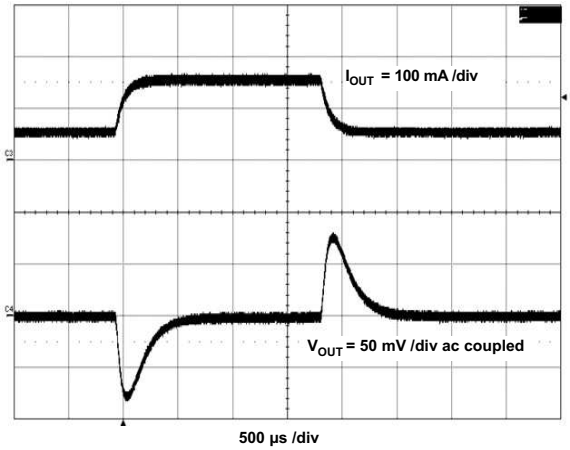


Figure 28. Load Transient

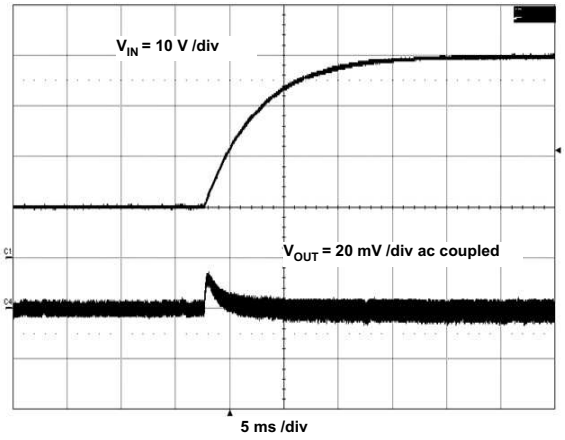


Figure 29. Line Transient

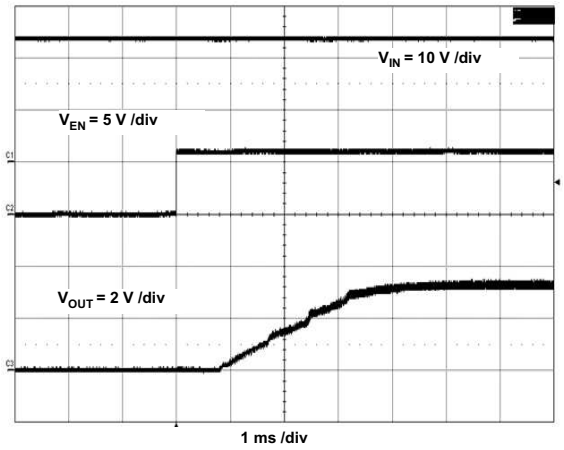


Figure 30. Startup with ENA

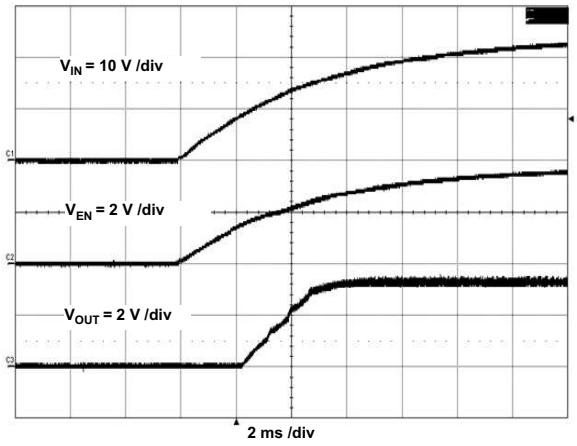


Figure 31. Startup with V_{IN}

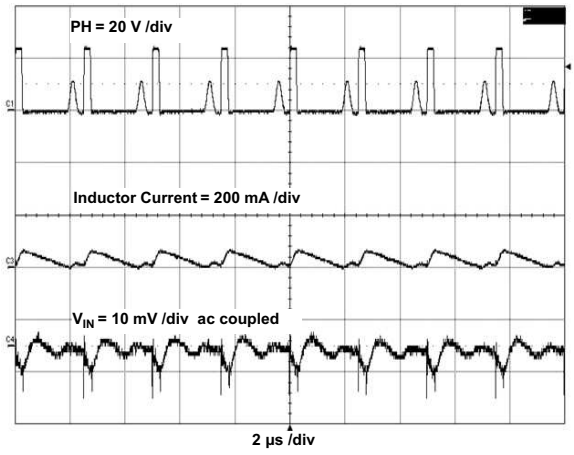


Figure 32. Input Ripple in DCM

Characteristics (continued)

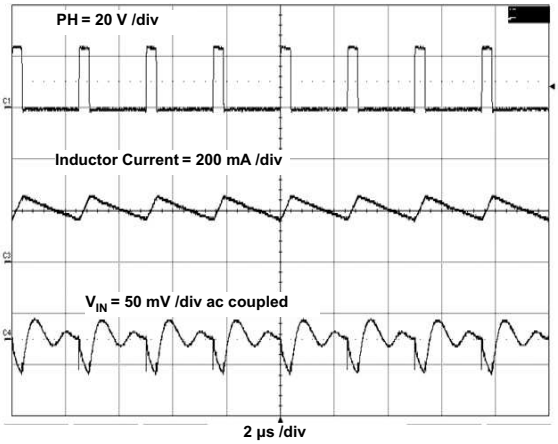


Figure 33. Input Ripple in CCM

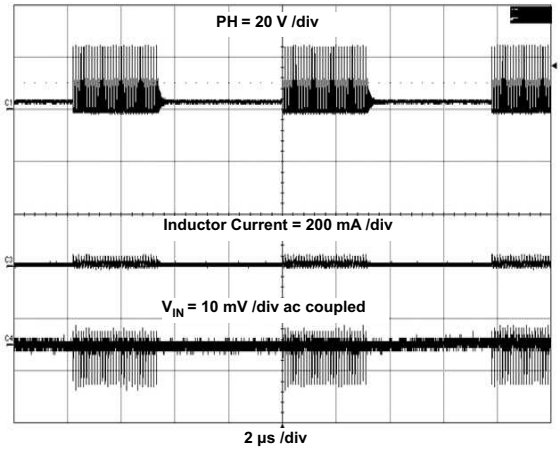


Figure 34. Input Ripple Skip

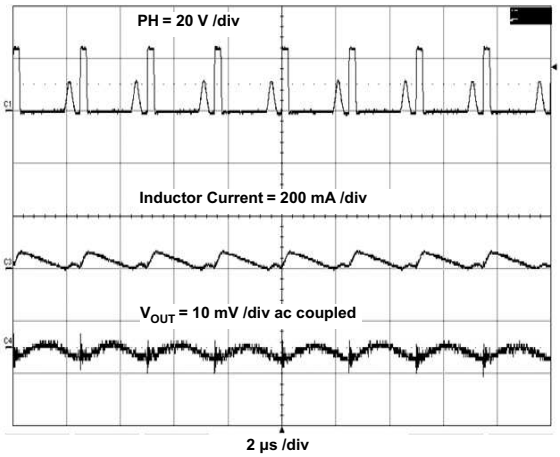


Figure 35. Output Ripple in DCM

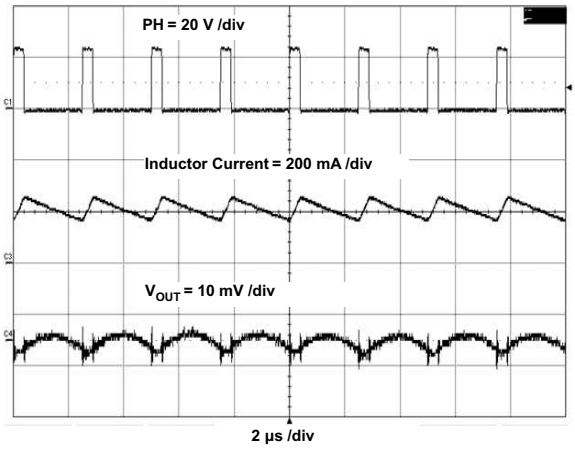


Figure 36. Output Ripple in CCM

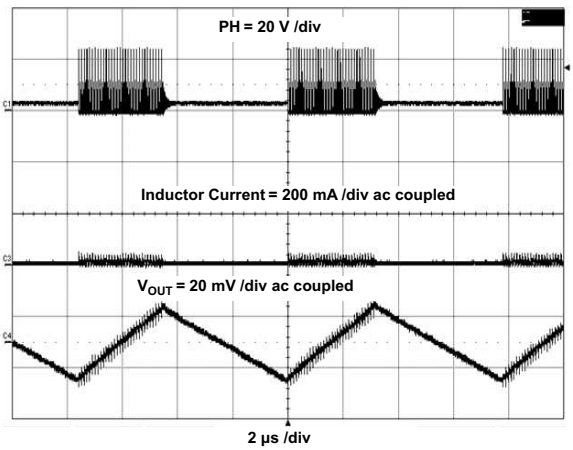


Figure 37. Output Ripple Skip

DESIGN GUIDE – STEP-BY-STEP PROCEDURE Number 2

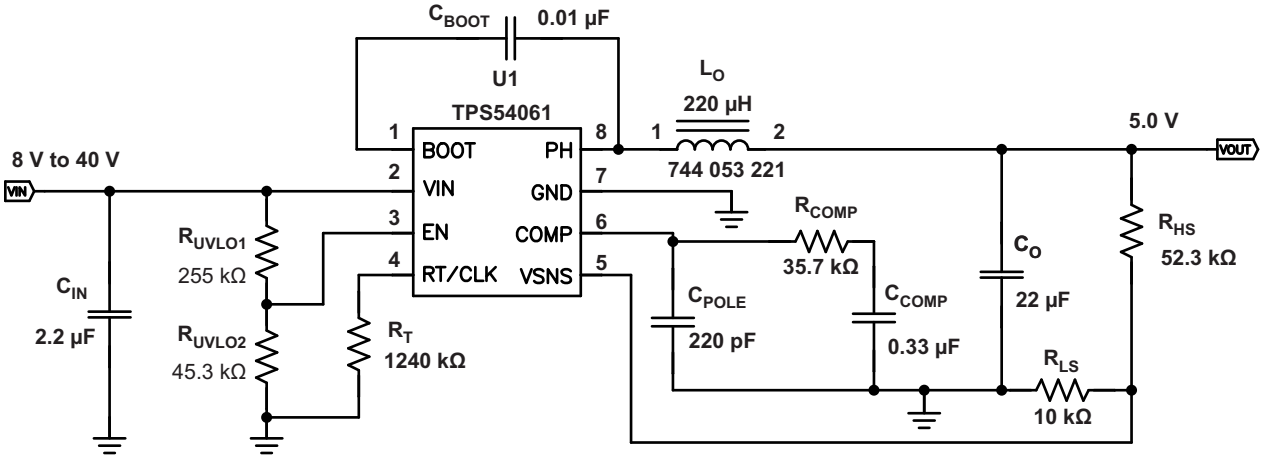


Figure 38. DCM Application Schematic

It is most desirable to have a power supply that is efficient and has a fixed switching frequency at low output currents. A fixed frequency power supply will have a predictable output voltage ripple and noise. Using a traditional continuous conduction mode (CCM) design method to calculate the output inductor will yield a large inductance for a low output current supply. Using a CCM inductor will result in a large sized supply or will affect efficiency from the large dc resistance an alternative is to operate in discontinuous conduction mode (DCM). Use the procedure below to calculate the components values for designing a power supply operating in discontinuous conduction mode. The advantage of operating a power supply in DCM for low output current is the fixed switching frequency, lower output inductance, and lower dc resistance on the inductor. Use the frequency shift and skip equations to estimate the maximum switching frequency.

For Designing an Efficient, Low Output Current Power Supply at a Fixed Switching Frequency

This example details the design of a low output current, fixed switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	5.0 V
Transient Response 37.5 to 75 mA load step	ΔV_{OUT} = 4%
Maximum Output Current	75 mA
Minimum Output Currert	1 mA
Input Voltage	24 V nom. 8 V to 40 V
Output Voltage Ripple	1 % of V_{OUT}
Switching Frequency	50 kHz
Start Input Voltage (rising VIN)	8 V
Stop Input Voltage (falling VIN)	6.8 V

The TPS54061 is designed for applications which require a fixed operating frequency and low output voltage ripple at low output currents, thus, the TPS54061 does not have a pulse skip mode at light loads. Since the device has a minimum controllable on time, there is an output current at which the power supply will pulse skip. To ensure that the supply does not pulse skip at output current of the application the inductor value will be need to be selected greater than a minimum value. The minimum inductance needed to maintain a fixed switching frequency at the minimum load is calculated to be 227 µH using Equation 27. Since the equation is ideal and was derived without losses, assume the minimum controllable light load on time, $t_{onminII}$, is 180 ns. To maintain DCM operation the inductor value and output current need to stay below a maximum value. The maximum inductance is calculated to be 250 µH using Equation 28. A 744053221 inductor from Würth Elektronik is selected. If CCM operation is necessary, use the previous design procedure.

Use Equation 29, to make sure the minimum current limit on the high side power switch is not exceeded at the maximum output current. The peak current is calculated as 244 mA and is lower than the 350 mA current limit. To determine the rms current for the inductor and output capacitor, it is necessary to calculate the duty cycle. The duty cycle, D1, for a step down regulator in DCM is calculated in Equation 30. D1 is the portion of the switching cycle the high side power switch is on, and is calculated to be 0.1345. D2 is the portion of the switching cycle the low side power switch is on, and is calculated to be 0.5111.

Using the Equation 32 and Equation 33, the rms current of the inductor and output capacitor are calculated, to be 0.1078 A and 0.0774 A respectively. Select components that ratings exceed the calculated rms values. Calculate the output capacitance using the Equation 34 to Equation 36 and use the largest value, Vripple is the steady state voltage ripple and deltaV is voltage change during a transient. A minimum of 7.5 µF capacitance is calculated. Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which increases this minimum value. For this example, a 22 µF 10 V X7R ceramic capacitor with 5mΩ ESR is used. To have a low output ripple power supply use a low esr capacitor. Use Equation 37 to estimate the maximum esr for the output capacitor. Equation 38 and Equation 39 estimate the rms current and capacitance for the input capacitor. An rms current of 38.7 mA and capacitance of 1.56 µF is calculated. A 2.2 µF 100V/X7R ceramic is used for this example.

$$L_o\text{min} \geq \left(\frac{V_{IN}\text{max} - V_{OUT}}{V_{OUT}}\right) \times \left(\frac{V_{IN}\text{max}}{2}\right) \times \frac{t_O\text{nmin}^2}{I_O\text{min}} \; x\, f\text{sw} \tag{27}$$

$$L_O\text{max} \leq \left(\frac{V_{IN}\text{min} - V_{OUT}}{2}\right) \times \left(\frac{V_{OUT}}{V_{IN}\text{min}}\right) \times \frac{1}{f_{sw} \times I_O} \tag{28}$$

$$I_L\text{peak} = \left(\frac{2 \times V_{OUT} \times \text{Iomax} \times (V_{IN}\text{max} - V_{OUT})}{V_{IN}\text{max} \times L_O \times f_{sw}}\right)^{0.5} \tag{29}$$

$$D1 = \left(\frac{2 \times V_{OUT} \times I_O \times L_O \times f_{sw}}{V_{IN} \times (V_{IN} - V_{OUT})}\right)^{0.5} \tag{30}$$

$$D2 = \left(\frac{V_{IN} - V_{OUT}}{V_{OUT}}\right) \times D1 \tag{31}$$

$$I_L\text{rms} = I_L\text{peak} \times \left(\frac{D1 + D2}{3}\right)^{0.5} \tag{32}$$

$$I_{CO}\text{rms} = I_L\text{peak} \times \left(\left(\frac{D1 + D2}{3}\right) - \left(\frac{D1 + D2}{4}\right)^2\right)^{0.5} \tag{33}$$

$$C_O1 \leq \frac{I_L\text{peak}}{V_{RIPPLE}} \times \left(\frac{D1 + D2}{8 \times f_{SW}}\right) \tag{34}$$

$$C_O2 \geq L_O \times \frac{\text{Io}^2 - 0^2}{(V_{OUT} + \Delta V)^2 - {V_{OUT}}^2} \tag{35}$$

$$\text{Co3} \geq \frac{I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{f_{co}} \tag{36}$$

$$R_C \leq \frac{V_{RIPPLE}}{I_L\text{peak}} \tag{37}$$

$$I_{CIN}\text{rms} = I_L\text{peak} \times \left(\left(\frac{D1}{3}\right) - \left(\frac{D1}{4}\right)^2\right)^{0.5} \tag{38}$$

$$C_{IN} \geq \frac{I_O}{V_{IN}\text{RIPPLE}} \times \left(\frac{0.25}{f_{SW}}\right) \tag{39}$$

Closing the Feedback Loop

The method presented here is easy to calculate and includes the effect of the slope compensation that is internal to the TPS54061. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater than the modulator pole. Once the output components are determined, use the equations below to close the feedback loop. A current mode controlled power supply operating in DCM has a transfer function which includes an ESR zero and pole as shown in Equation 40. To calculate the current mode power stage gain, first calculate, Kdcm, the DCM gain, and Fm, the modulator gain, using Equation 41 and Equation 42. Kdcm and Fm are 32.4 and 0.475 respectively. The location of the pole and ESR zero are calculated using Equation 43 and Equation 44 . The pole and zero are 491 Hz and 2.8 MHz, respectively. Use the lower value of Equation 45 and Equation 46 as a starting point for the crossover frequency. Equation 45 is the geometric mean of the power stage pole and the esr zero and Equation 46 is the mean of power stage pole and the switching frequency. The crossover frequency is chosen as 5 kHz from Equation 46.

To determine the compensation resistor, R_{COMP}, use Equation 47. Assume the power stage transconductance, gmps, is 1.0 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5.0 V, 0.8 V and 108 µA/V, respectively. R_{COMP} is calculated to be 38.3 kΩ; use the nearest standard value of 35.7 kΩ. Use Equation 48 to set the compensation zero to equalthe modulator pole frequency. Equation 48 yields 290 nF for compensating capacitor C_{COMP}, and a 330 nF is used. Use the larger value of Equation 49 or Equation 50 to calculate the C_{POLE}, which sets the compensation pole. Equation 50 yields 178 pF standard value of 220 pF is selected.

$$Gdcm(s) \approx Fm \times Kdcm \times \frac{1 + \frac{s}{2 \times \pi \times f_{ZERO}}}{1 + \frac{s}{2 \times \pi \times f_{POLE}}} \tag{40}$$

$$Kdcm = \frac{2}{D1} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \left(2 + \frac{Rdc}{\frac{V_{OUT}}{I_O}}\right) - V_{OUT}} \tag{41}$$

$$Fm = \frac{gmps}{\left(\frac{V_{IN} - V_{OUT}}{L_O \times f_{sw}}\right) + 0.380} \tag{42}$$

$$f_{POLE}(Hz) = \frac{1}{\frac{V_{OUT}}{I_O} \times C_O \times 2 \times \pi} \times \left(\frac{2 - \frac{V_{OUT}}{V_{IN}}}{1 - \frac{V_{OUT}}{V_{IN}}}\right) \tag{43}$$

$$f_{ZERO}(Hz) = \frac{1}{R_C \times C_O \times 2 \times \pi} \tag{44}$$

$$f_{CO1}(Hz) = \left(f_{ZERO} \times f_{POLE}\right)^{0.5} \tag{45}$$

$$f_{CO2}(Hz) = \left(f_{SW} \times f_{POLE}\right)^{0.5} \tag{46}$$

$$R_{COMP} = \frac{f_{co}}{Kdcm \times Fm \times f_{POLE}} x \frac{V_{OUT}}{V_{REF} \times gmea} \tag{47}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times Kdcm \times Fm} \tag{48}$$

$$C_{POLE1} = \frac{R_C \times C_O}{R_{COMP}} \tag{49}$$

$$C_{POLE2} = \frac{1}{R_{COMP} \times f_{SW} \times \pi} \tag{50}$$

Characteristics

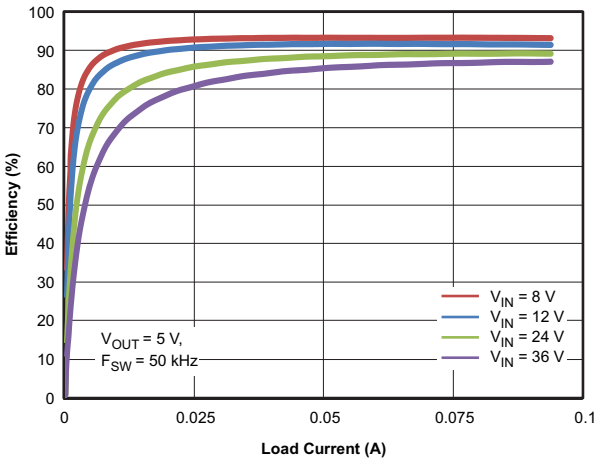


Figure 39. Efficiency vs Load Current

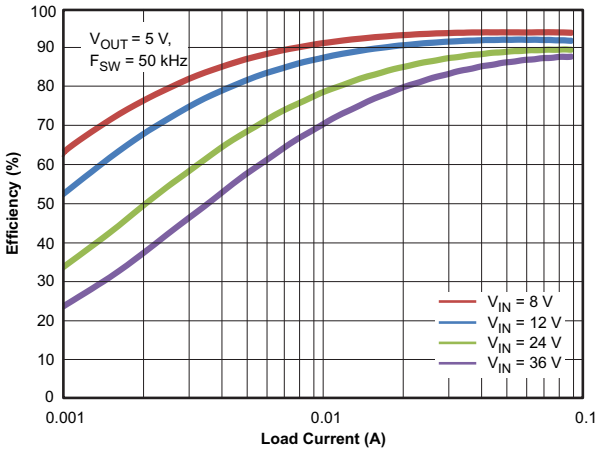


Figure 40. Efficiency vs Load Current

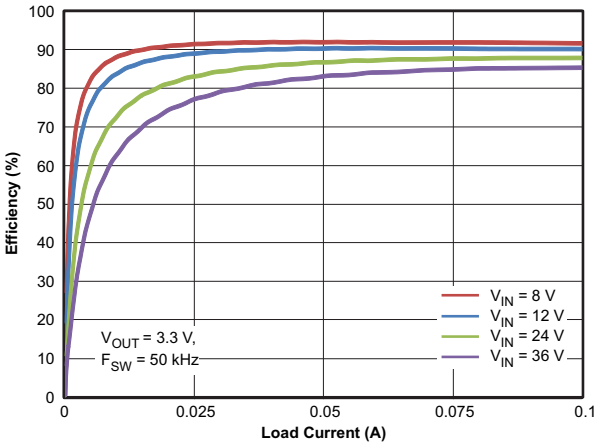


Figure 41. Efficiency vs Load Current

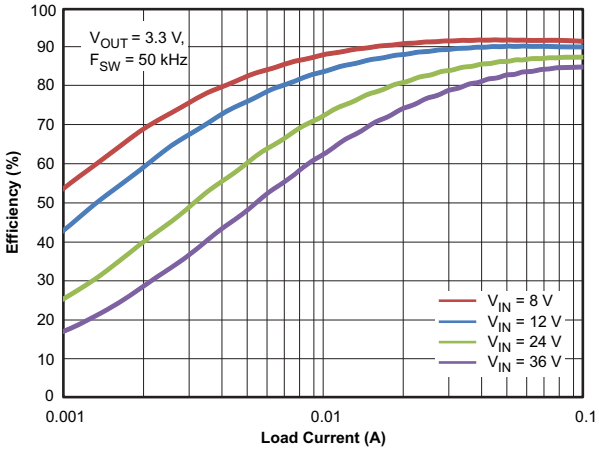


Figure 42. Efficiency vs Load Current

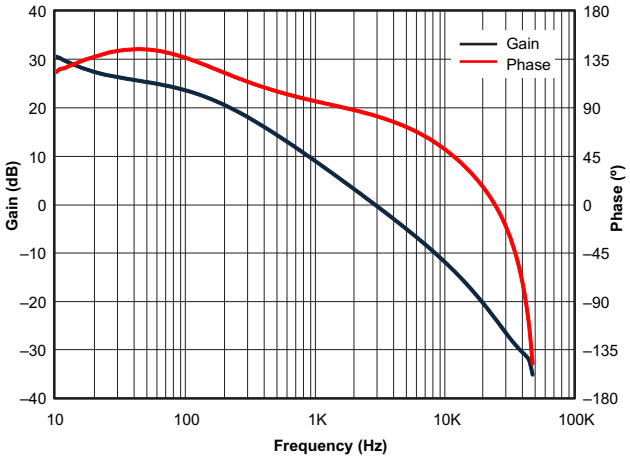


Figure 43. Frequency Response

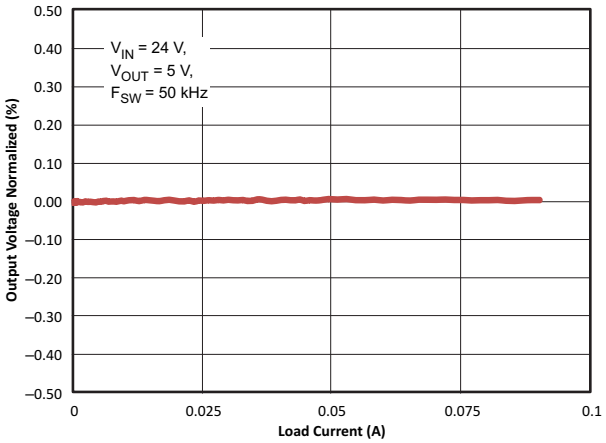


Figure 44. Output Voltage Normalized vs Load Current

Characteristics (continued)

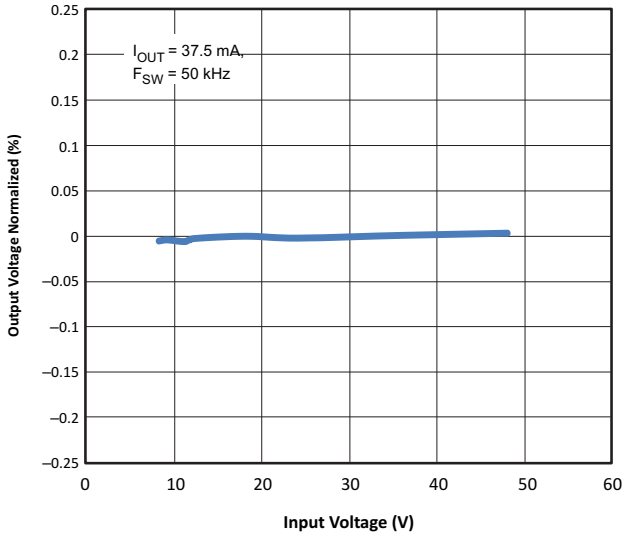


Figure 45. Output Voltage Normalized vs Input Voltage

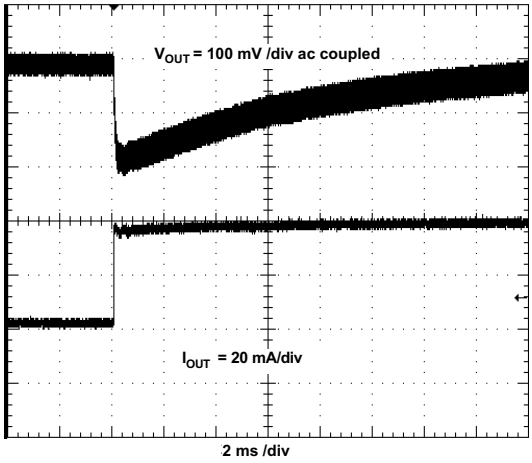


Figure 46. Load Transient

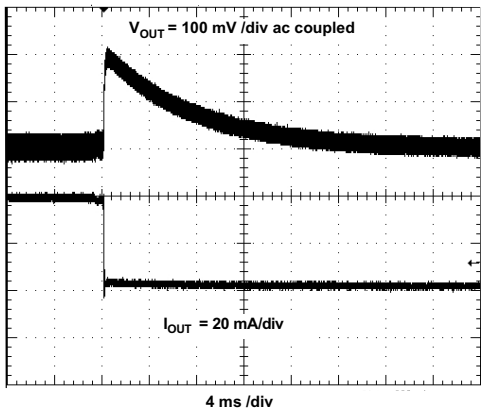


Figure 47. Unload Transient

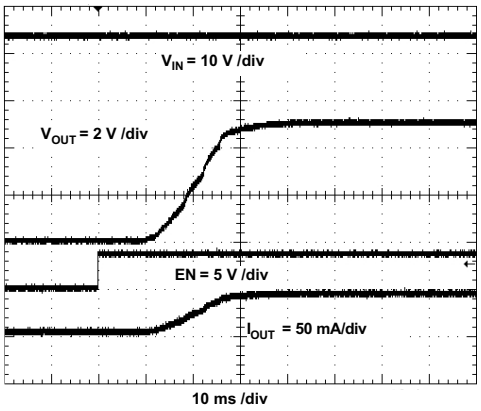


Figure 48. Startup With ENA

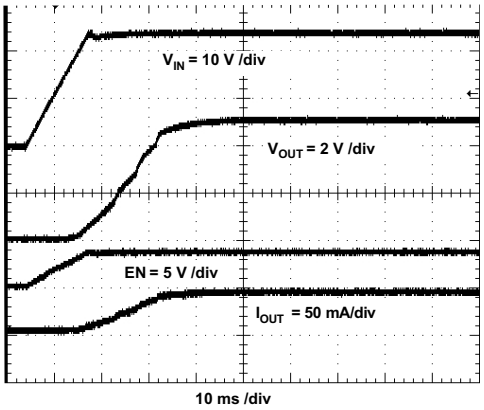


Figure 49. Startup With V_{IN}

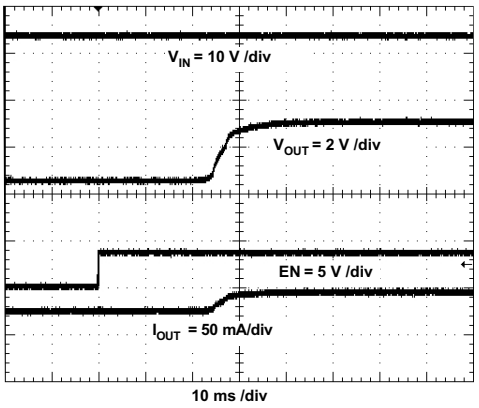


Figure 50. Prebias Startup With ENA

Characteristics (continued)

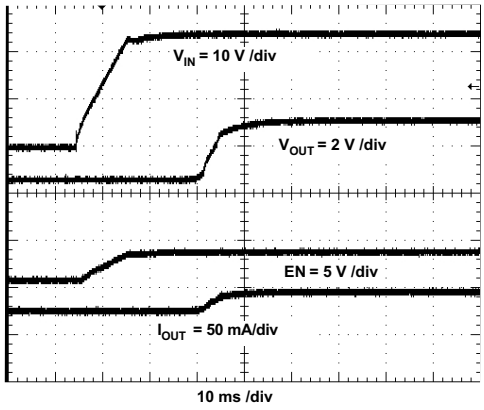


Figure 51. Prebias Startup With V_{IN}

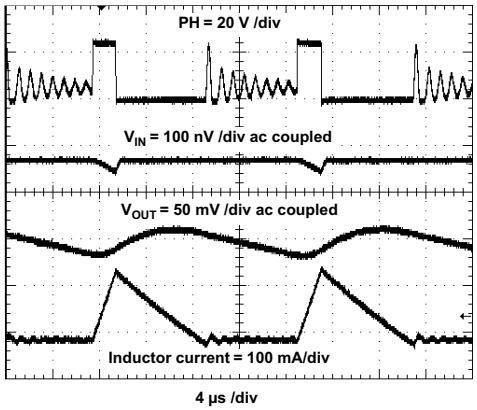


Figure 52. Input and Output Ripple in DCM

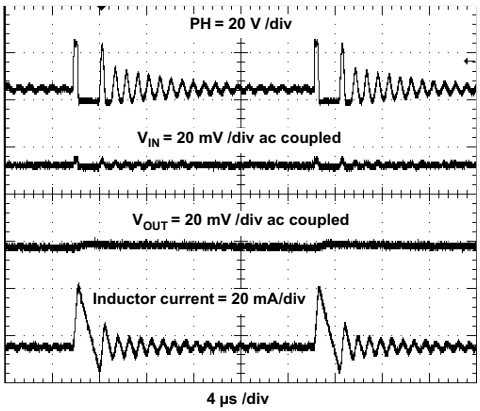


Figure 53. Input and Output Ripple in PSM

Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the GND pin. See Figure 54 for a PCB layout example. Since the PH connection is the switching node and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The RT/CLK pin is sensitive to noise. so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however; this layout has been shown to produce good results and is meant as a guideline.

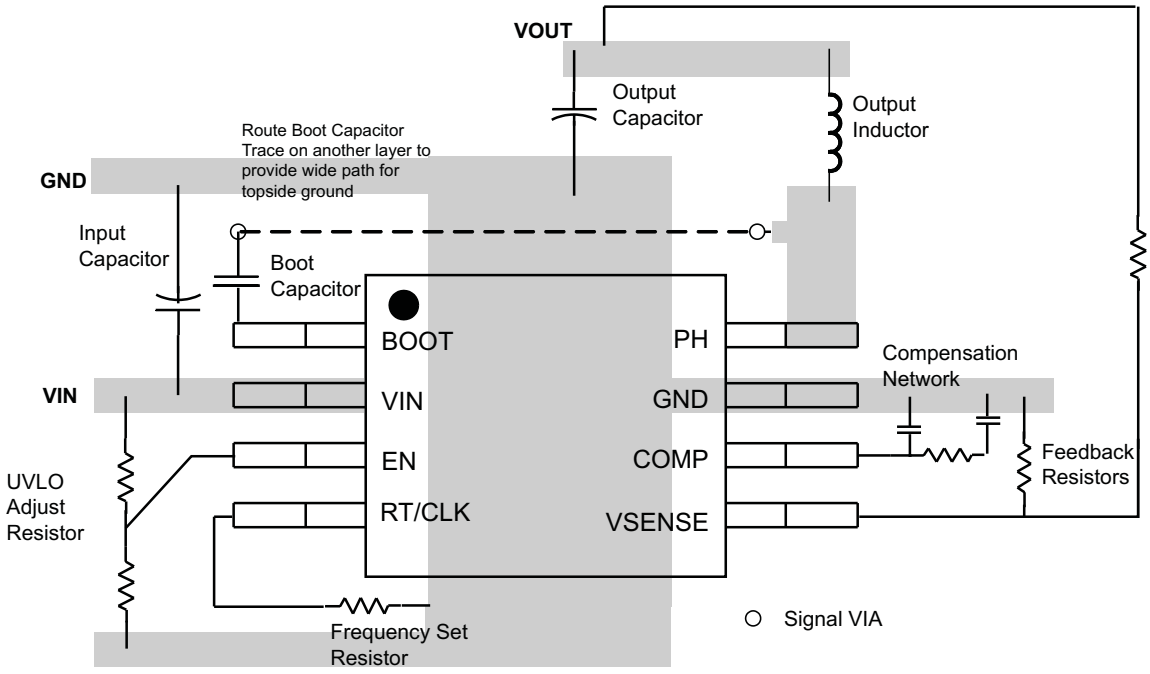


Figure 54. PCB Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS54061DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS54061DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

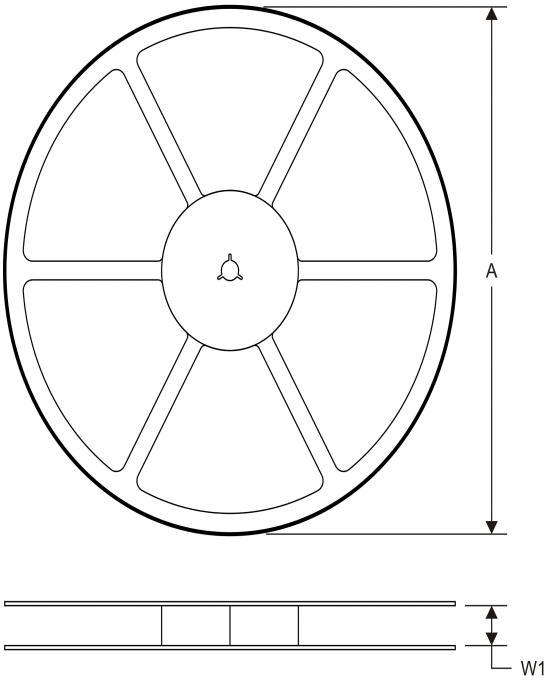
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

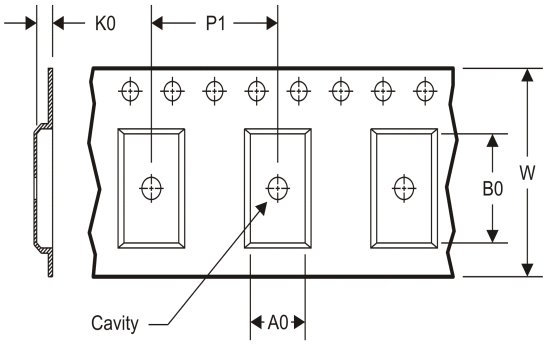
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



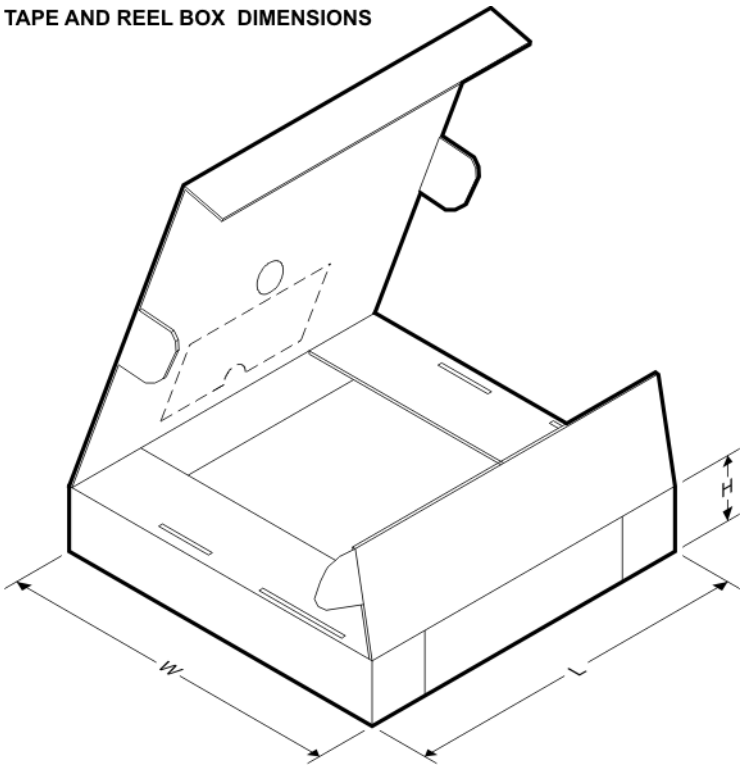
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54061DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54061DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

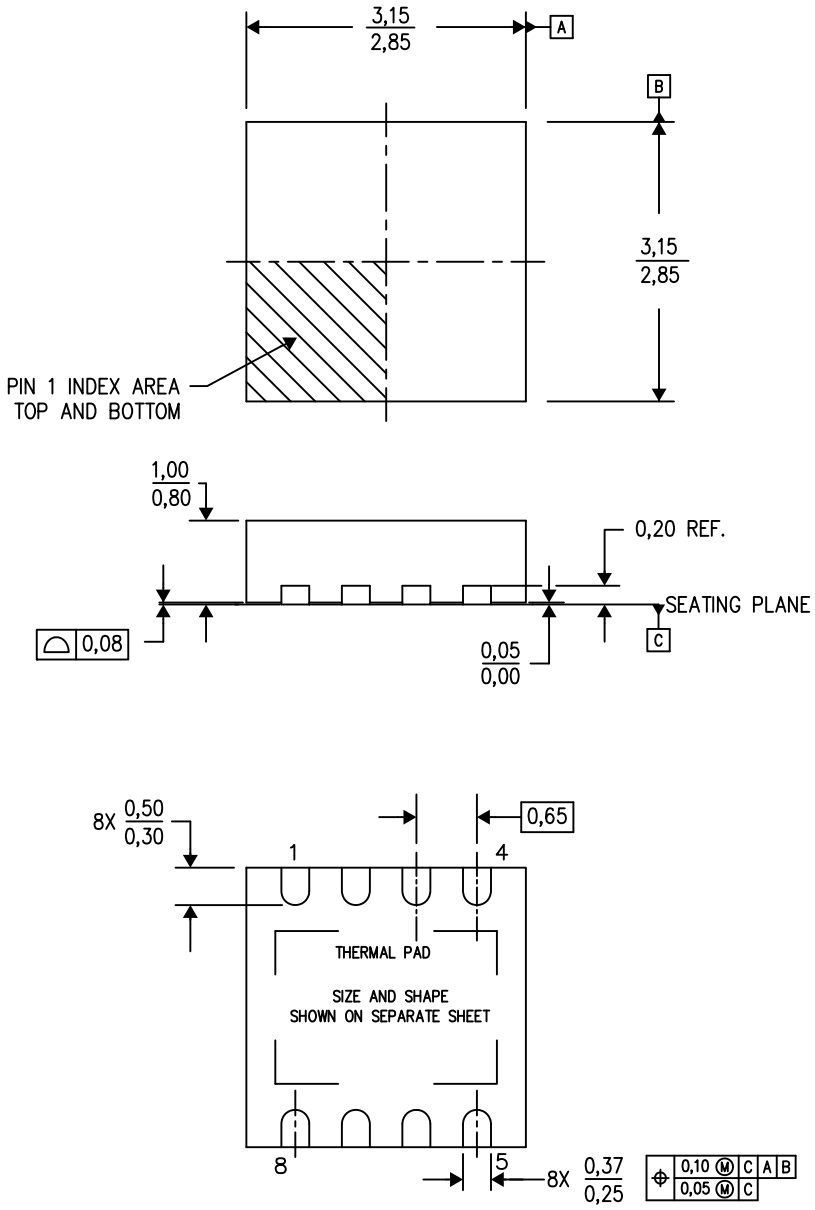
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54061DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS54061DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

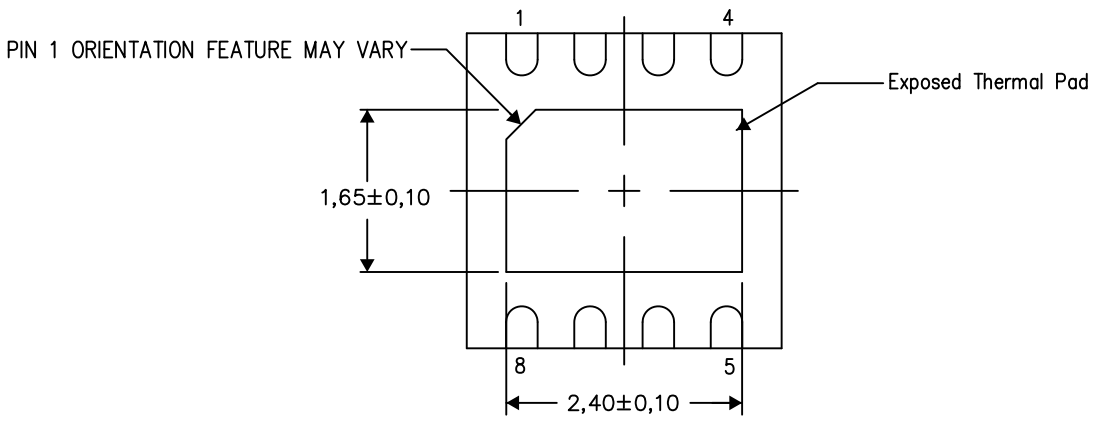
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



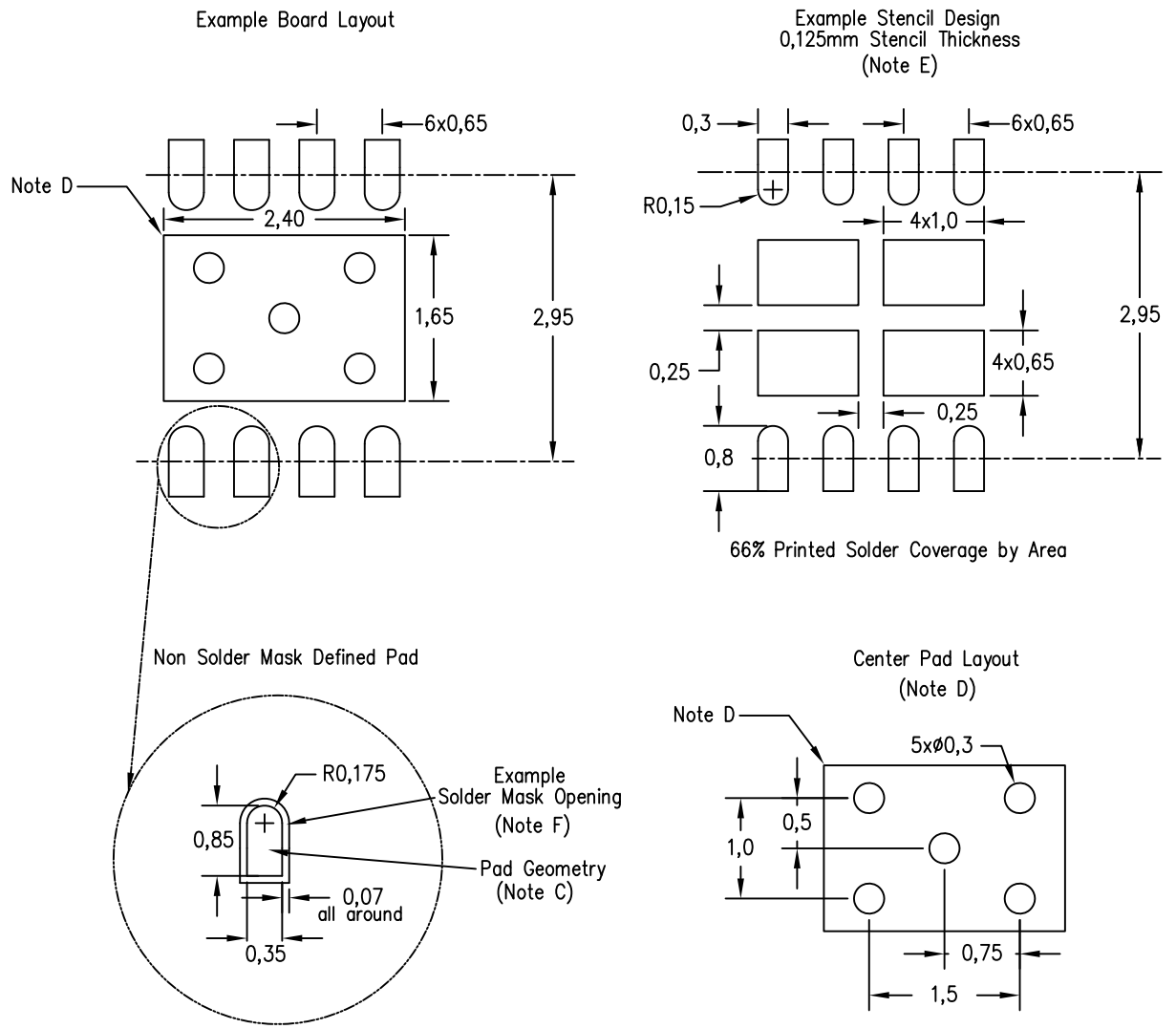
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/M 06/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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