TPS53667 6-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load

Check for Samples: TPS53667

PRODUCT PREVIEW

1 Features

- 8-bit Selectable BOOT Voltage via Pinstrap or NVM: 0.5 V to 2.5 V (down to 5-mV Step)
- 1-, 2-, 3-, 4-, 5-, or 6- Phase Operation
- PMBus™ System Interface for Telemetry of Voltage, Current, Power, Temperature, and Fault Conditions
- 1.8-V and 3.3-V PMBus Bias Compatible
- Fault Reporting: Output Voltage, Output Current, and Temperature
- Configurable with Non-Volatile Memory (NVM) or Resistor Pinstrap
- 16 Levels of Programmable OCP with Pinstrap or NVM
- Fast Transient with DCAP+™Control
- Optimized Efficiency at Light and Heavy Loads
- Support Pre-Bias Startup
- 8 Independent Levels of Overshoot Reduction (OSR) and Undershoot Reduction (USR)
- Driverless Configuration for Efficient High-Frequency Switching
- Compatible with CSD95490BQ5MC NexFET™ Power Stage
- Accurate, Adjustable Voltage Positioning
- 300-kHz to 1-MHz Frequency Selections with Closed-loop Frequency Control
- Patented AutoBalance™ Phase Balancing
- Dynamic Phase Shedding with Programmable Current Threshold
- Conversion Voltage Range: 4.5 V to 17 V
- Small, 6 mm × 6 mm, 40-Pin, QFN, PowerPAD™ Package

2 Applications

- Application-Specific Integrated Circuit (ASIC) Power in Communications Equipment
- High Density Power Solutions
- Server Power
- Smart Power Systems

3 Description

The TPS53667 is a high-current, multi-phase, step-down controller. The device offers built-in non volatile memory (NVM) and PMBus interface. It is fully compatible with the NexFET power stage (CSD95490BQ5MC). The TPS53667 provides 8-bit BOOT voltage selection covering output voltage from 0.5 V to 2.5 V, with steps as small as 5 mV, which is ideal for high current application with accurate output voltage setting. Advanced control features such as D-CAP+ architecture with undershoot reduction (USR) and overshoot reduction (OSR) provide fast transient response, lowest output capacitance, and high efficiency. The TPS53667 also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at light loads. In addition, the TPS53667 supports the PMBus communication interface with systems for telemetry of voltage, current, power, temperature, and fault conditions. Some of the configurations can be programmed by pinstrap or PMBus and stored in non-volatile memory to minimize the external component count.

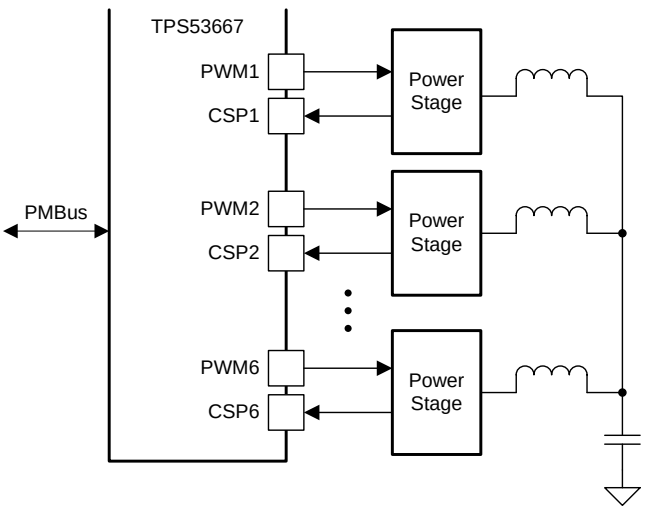
The TPS53667 is offered in a space saving, thermally enhanced 40-pin QFN package and is rated to operate from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53667	QFN (40)	6.00 mm × 6.00 mm

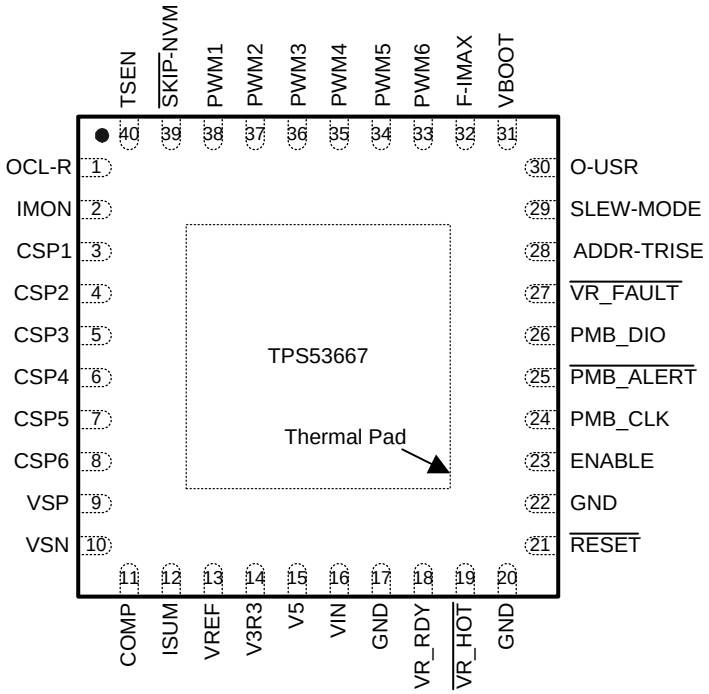
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



4 Pin Configuration and Functions

RTA Package
40-Pin QFN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ADDR-TRISE	28	I	Voltage divider to VREF pin. A resistor ($R_{ADDR-TRISE}$) connected between this pin and GND sets the 3-bits. Bit 2 and bit 1 set the rise slew rate. Bit 0 Selects the LSB of BOOT voltage. The voltage ($V_{ADDR-TRISE}$) sets 4 bits PMBus address. The device latches these settings when V3R3 powers up.
COMP	11	O	Output of the g_M error amplifier. Resistors and capacitors connected between this pin and the VREF pin set the compensation.
CSP1	3	I	Positive current sense inputs. Connect to the IOUT pin of TI smart power stages (ex: CSD95372BQ5MC). Tie CSP6, CSP5, CSP4, CSP3, or CSP2 to the V3R3 pin according to to disable the corresponding phase.
CSP2	4		
CSP3	5		
CSP4	6		
CSP5	7		
CSP6	8		
ENABLE	23	I	VR enable. 1-V I/O level; 100-ns debounce.
F-IMAX	32	I	Voltage divider to VREF pin. A resistor (R_{F-IMAX}) connected between this pin and GND sets the operating frequency of the controller. The voltage level (V_{F-IMAX}) sets the maximum operating current of the converter. The IMAX value is an 8-bit A/D where $V_{F-IMAX} = V_{VREF} \times I_{MAX} / 255$. Both are latched at V3R3 power-up.
GND	17	G	Ground pin.
GND	20	G	Connect these pins to GND. Note this is not IC ground pin.
	22		

(1) I = Input, O = Output, P = Power, I/O = Bi-directional, GND = ground

PRODUCT PREVIEW

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
IMON	2	O	Analog current monitor output. $V_{IMON} = \frac{I_O \times 5m\Omega \times R_{IMON}}{35k\Omega}$
ISUM	12	O	A resistor (R_{ISUM}) connected between this pin and VREF pin determines the droop. $V_{ISUM} = \frac{I_O \times 5m\Omega \times g_{M(isum)} \times R_{ISUM}}{n} + V_{REF}$ (where n is the number of phases)
OCL-R	1	I	A resistor (R_{OCL-R}) connected between this pin and GND and the voltage level (V_{OCL-R})select 1 of 16 OCP levels (per phase current-limit). V_{OCL-R} also sets 1 of 4 RAMP levels. The device latches these settings when V3R3 powers up.
O-USR	30	I	Voltage divider to VREF pin. A resistor (R_{O-USR}) connected between this pin and GND selects 1 of 7 OSR thresholds or OFF. The voltage level (V_{O-USR}))sets 1 of 7 USR levels or OFF. The device latches these settings when V3R3 powers up.
$\overline{\text{PMB\_ALERT}}$	25	O	I^2C PMBus interrupt line. Open drain. 3.3-V and 1.8-V logic level.
PMB_CLK	24	I	I^2C PMBus clock. 3.3-V and 1.8-V logic level.
PMB_DIO	26	I/O	I^2C PMBus digital I/O line. 3.3-V and 1.8-V logic level.
PWM1	38	O	PWM signals for each phase
PWM2	37		
PWM3	36		
PWM4	35		
PWM5	34		
PWM6	33		
$\overline{\text{RESET}}$	21	I	Reset pin. If this pin is low for more than 1000 ns, the controller pulls the output voltage to the V_{BOOT} level.
$\overline{\text{SKIP}}$-NVM	39	O	A resistor ($R_{\overline{SKIP}\text{-NVM}}$) connected between this pin and GND sets either pinstrap or NVM configuration mode. This pin can also connect to the FCCM pin of TI smart power stages (ex: CSD95372BQ5MC) for SKIP or FCCM operation.
SLEW-MODE	29	I	Voltage divider to VREF pin. A resistor ($R_{SLEW-MODE}$) connected between this pin and GND sets 8 slew rates. The voltage level ($V_{SLEW-MODE}$) sets 4-bit operation modes. Bit 7 for DAC mode (1 for VR12.0; 0 for VR12.5). Bit 6 for the 4-phase interleaving mode (1 for 1/3 and 2/4 two phase interleaving; 0 for 4 phase interleaving individually). Bit 4 for enabling dynamic phase add or drop (1 for enable; 0 for disable). Bit 3 sets zero load-line (1 for zero load-line; 0 for non-zero load-line) The device latches these settings when V3R3 powers up.
TSEN	40	I	Connect to the TAO/FAULT pin of TI smart power stages (ex: CSD95372BQ5MC) to sense the highest temperature of the power stages and to sense the fault signal from the power stages.
V3R3	14	O	3.3-V LDO output. Bypass this pin to GND with a ceramic capacitor with a value of 1-µF or larger.
V5	15	P	5-V power input. Bypass this pin to GND with a ceramic capacitor with a value of 1-µF or larger. This pin is used to power all internal analog circuits.
VBOOT	31	I	Voltage divider to VREF pin. A resistor (R_{VBOOT}) connected between this pin and GND sets 3 bits (B[3:1]). The voltage level (V_{VBOOT}) sets 4 bits (B[7:4]). The total 7 bits set 7 of 8 bits of VID of boot voltage (B[7:1]). The device latches these settings when V3R3 powers up.
VIN	16	P	Input voltage supply. This pin is also used for input voltage sensing for on-time control and input undervoltage lockout (UVLO).
VR_RDY	18	O	Power good open-drain output for the controller. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger.
$\overline{\text{VR\_FAULT}}$	27	O	VR fault indicator (open-drain). The failures include shorts of the high-side FETs, over temperature, output overvoltage, and overcurrent conditions of the input. The fault signal should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply. When the failure occurs, the $\overline{\text{VR\_FAULT}}$ pin is LOW. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger.
$\overline{\text{VR\_HOT}}$	19	O	Thermal flag open drain output. Active low. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger.

PRODUCT PREVIEW

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VREF	13	O	1.7-V, 500-µA, LDO reference voltage. Bypass this pin to GND with a ceramic capacitor with a value of 0.33 µF. Connect the VREF pin to the REFIN pin of TI smart power stages (ex: CSD95372BQ5MC) as the current-sense reference voltage.
VSN	10	I	Negative input of the remote voltage sense amplifier. Connect this pin directly to the GND of the load.
VSP	9	I	Positive input of the remote voltage sense amplifier. Connect this pin directly to the load.
Thermal Pad		GND	Thermal pad. Connect the thermal pad to the ground plane with multiple vias.

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.1.2 Development Support

For the Power Stage Designer tool, go to www.ti.com/tool/powerstage-designer.

5.2 Documentation Support

5.2.1 Related Documentation

For related documentation, see the following:

- *CSD95372BQ5MC Synchronous Buck NexFET™ Smart Power Stage* (SLPS417)

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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5.5 Trademarks

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5.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53667RTAR	PREVIEW	WQFN	RTA	40	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 53667	
TPS53667RTAT	PREVIEW	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 53667	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

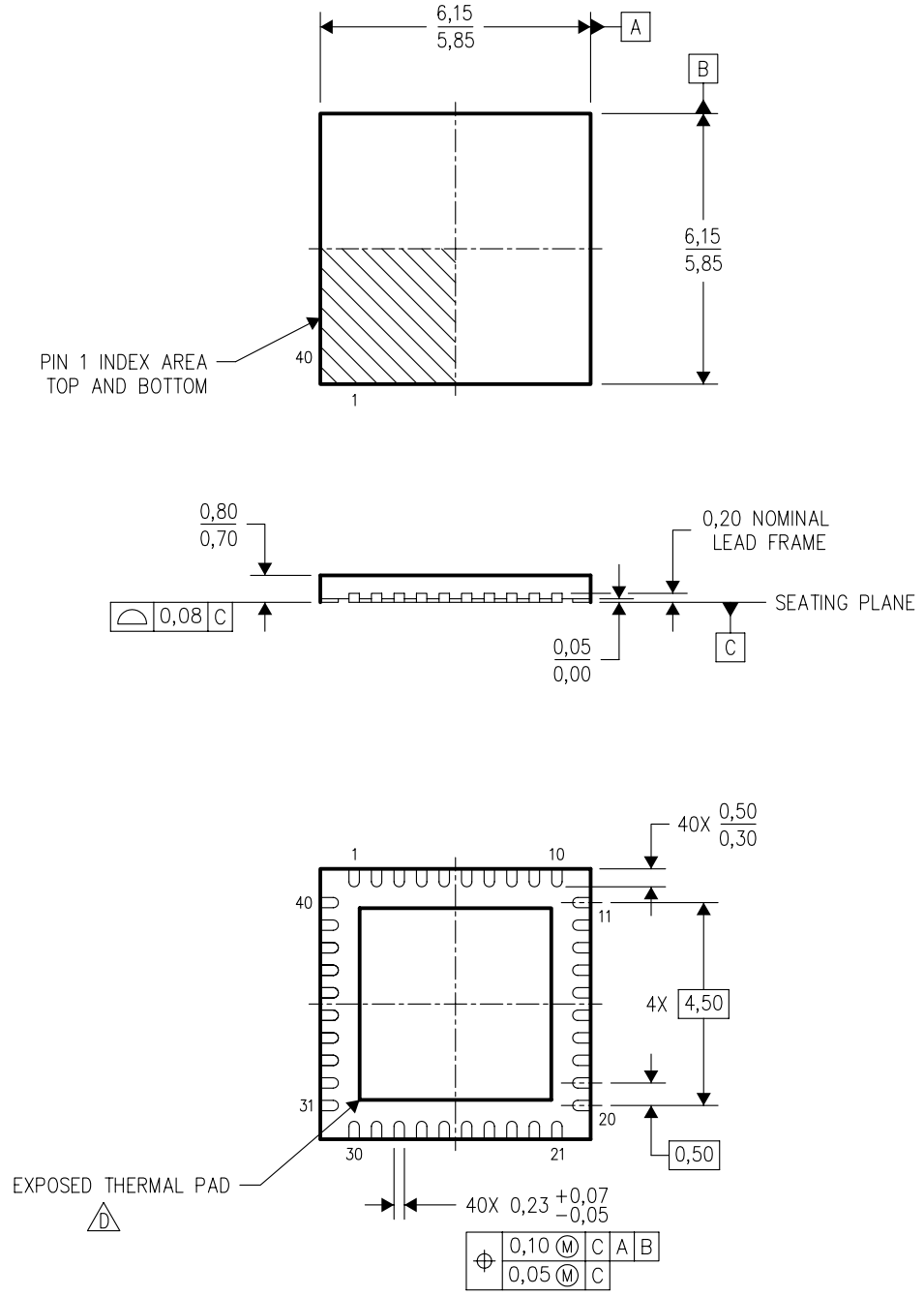
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

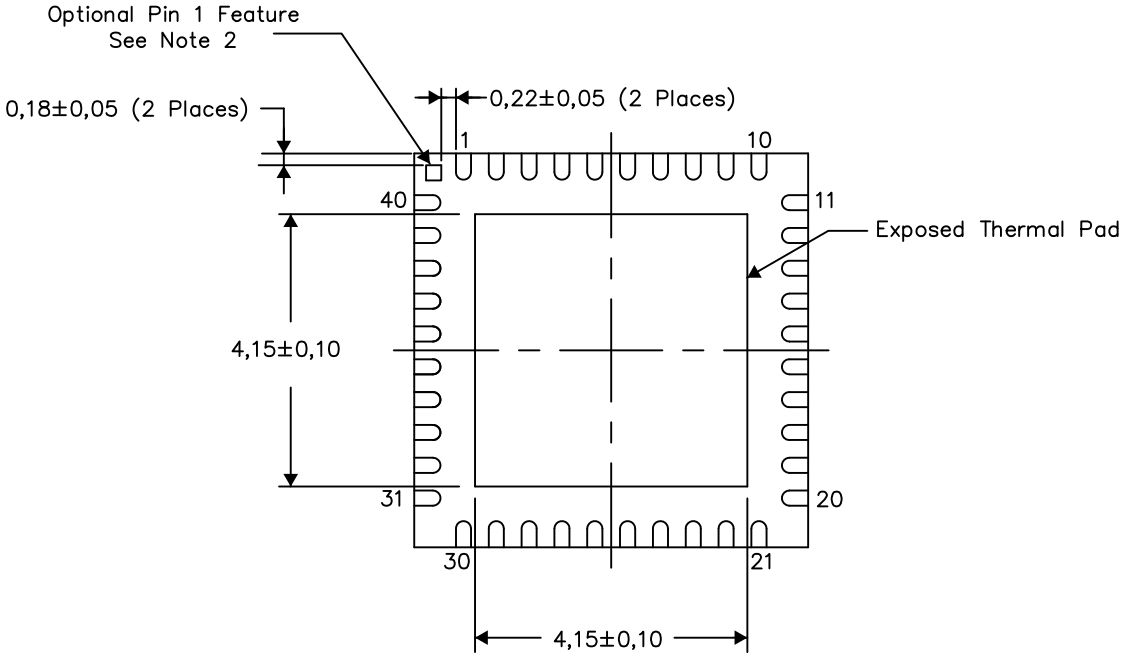
RTA (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

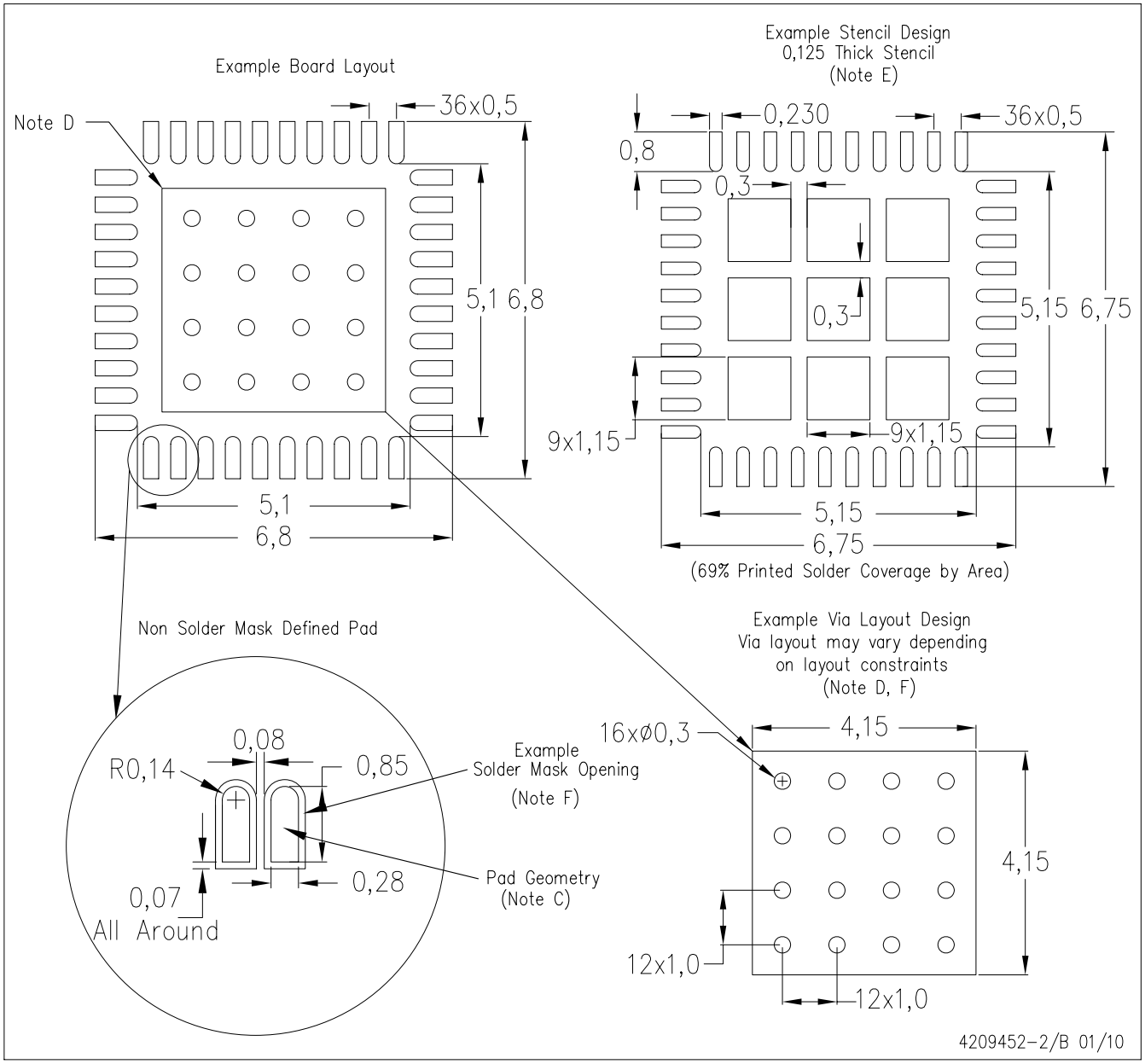
Exposed Thermal Pad Dimensions

4206335–2/F 04/14

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RTA (S–PWQFN–N40)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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