

TPS53219A Wide Input Voltage, Eco-Mode™, Single Synchronous Step-Down Controller

1 Features

- Conversion Input Voltage Range: 3 V to 28 V
- VDD Input Voltage Range: 4.5 V to 25 V
- Output Voltage Range: 0.6 V to 5.5 V
- Wide Output Load Range: 0 A to > 20 A
- Built-In 0.6-V ($\pm 0.8\%$) Reference
- Built-In LDO Linear Voltage Regulator
- Auto-Skip Eco-Mode™ for Light-Load Efficiency
- D-CAP™ Mode with 100-ns Load-Step Response
- Adaptive ON-Time Control Architecture with 8 Selectable Frequency Settings
- 4700ppm/°C $R_{DS(on)}$ Current Sensing
- 0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable Internal Voltage Servo Soft-Start
- Pre-Charged Start-Up Capability
- Built-In Output Discharge
- Open-Drain Power Good Output
- Integrated Boost Switch
- Built-In OVP/UVP/OCV
- Thermal Shutdown (Non-Latch)
- 3-mm x 3-mm QFN, 16-Pin (RGT) Package

2 Applications

- Storage Computers
- Server Computers
- Multi-Function Printers
- Embedded Computing

3 Description

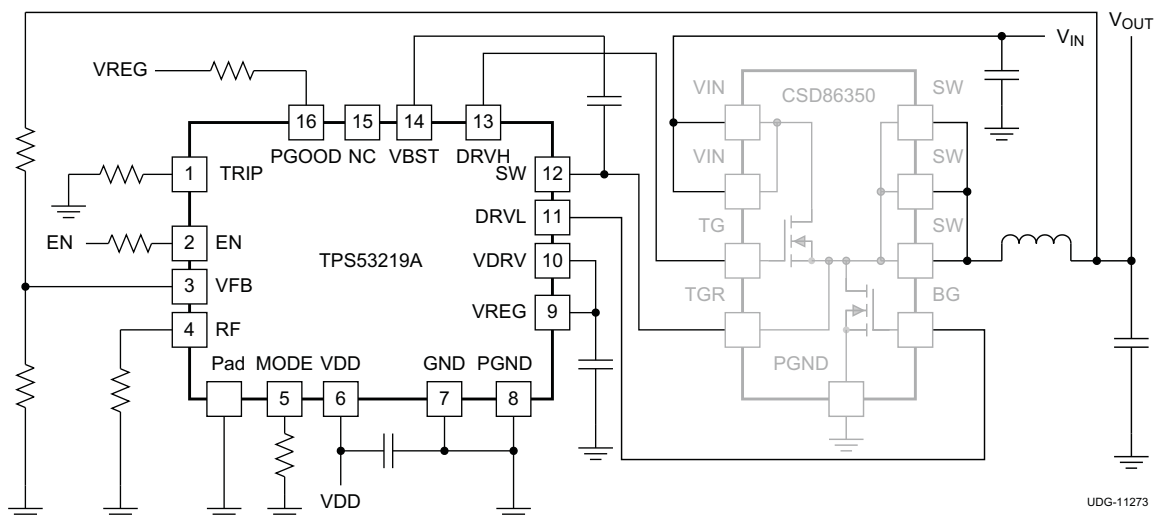
The TPS53219A device is a small-sized single buck controller with adaptive ON-time D-CAP mode control. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supplies in digital consumer products. The small package and minimal pin-count save space on the PCB, while the dedicated EN pin and pre-set frequency selections simplify the power supply design. The skip-mode at light load conditions, strong gate drivers and low-side FET $R_{DS(on)}$ current sensing supports low-loss and high efficiency, over a broad load range. The conversion input voltage (high-side FET drain voltage) range is between 4.5 V and 25 V, and the output voltage range is between 0.6 V and 5.5 V. The TPS53219A is available in a 16-pin, QFN package specified from -40°C to 85°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53219A	QFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



UDG-11273



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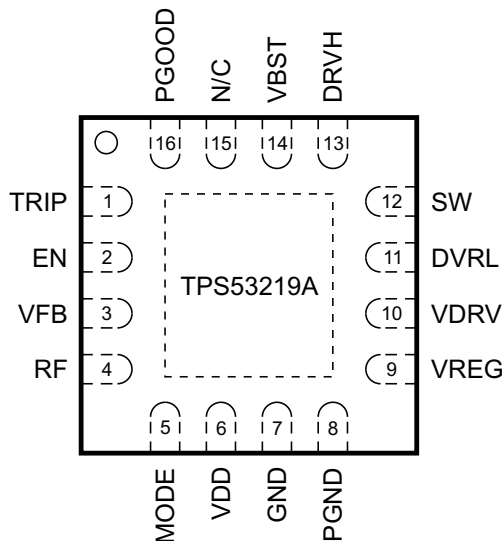
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Added more complete pin descriptions.	3

5 Pin Configuration and Functions

RGT Package
16-Pin QFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DRVH	13	O	High-side MOSFET driver output. The SW node referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node bootstrap flying capacitor.
DRVL	11	O	Synchronous MOSFET driver output. The PGND referenced driver. The gate drive voltage is defined by VDRV voltage.
EN	2	I	Enable pin. Place a 1-kΩ resistor in series with this pin if the source voltage is higher than 5.5 V.
GND	7	G	Ground pin. This is the ground of internal analog circuitry. Connect to GND plane at single point.
MODE	5	I	Soft-start and skip/CCM selection. Connect a resistor to select soft-start time using Table 1. The soft-start time is detected and stored into internal register during start-up.
NC	15	–	No connection.
PAD	–	–	Thermal pad. Use five vias to connect to GND plane.
PGOOD	16	O	Open-drain power good flag. Provides 1-ms start-up delay after the VFB pin voltage falls within specified limits. When VFB goes out specified limits PGOOD goes low after a 2-μs delay.
PGND	8	G	Power ground. Connect to GND plane.
RF	4	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using Table 2. The switching frequency is detected and stored during the start-up.
SW	12	P	Output of converted power. Connect this pin to the output inductor.
TRIP	1	I	OCL detection threshold setting pin. 10 μA at room temp, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL} = V_{TRIP}/8$ ($V_{TRIP} \leq 3$ V, $V_{OCL} \leq 375$ mV)
VBST	14	P	Supply input for high-side FET gate driver (boost terminal). Connect a capacitor from this pin to SW-node. Internally connected to VREG through bootstrap MOSFET switch.
VDD	6	P	Controller power supply input. The input range is from 4.5 V to 25 V.
VDRV	10	I	Gate drive supply voltage input. Connect to VREG if using LDO output as gate drive supply.
VFB	3	I	Output feedback input. Connect this pin to V_{OUT} through a resistor divider.
VREG	9	O	6.2-V LDO output. This is the supply of internal analog circuitry and driver circuitry.

(1) I=Input, O=Output, P=Power, G=Ground

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Input voltage	VBST	-0.3	37	V	
	VBST ⁽²⁾	-0.3	7		
	VDD	-0.3	28		
	SW	DC	-2		30
		Pulse <20ns, E = 5 μJ			-7
VDRV, EN, TRIP, VFB, RF, MODE		-0.3	7		
Output voltage	DRVH	-2	37	V	
	DRVH ⁽²⁾	-0.3	7		
	DRVL, VREG	-0.5	7		
	PGOOD	-0.3	7		
Junction temperature, T _J			150	°C	
Storage temperature, T _{stg}		-55	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage values are with respect to the SW terminal

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VBST	-0.1	34.5	V
	VDD	4.5	25	
	SW	-1	28	
	VBST ⁽¹⁾	-0.1	6.5	
	EN, TRIP, VFB, RF, VDRV, MODE		-0.1	
Output voltage	DRVH	-1	34.5	V
	DRVH ⁽¹⁾	-0.1	6.5	
	DRVL, VREG	-0.3	6.5	
	PGOOD	-0.1	6.5	
Operating free-air temperature, T _A		-40	85	°C

- (1) Voltage values are with respect to the SW terminal.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS53219A	
		RGT (QFN)	
		16 PINS	
Symbol	Description	Value	Unit
R _{θJA}	Junction-to-ambient thermal resistance	51.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	85.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	20.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range, V_{DD} = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VDD}	VDD supply current	VDD current, T _A = 25°C, No Load, V _{EN} = 5 V, V _{VFB} = 0.630 V		420	590	μA
I _{VDDSDN}	VDD shutdown current	VDD current, T _A = 25°C, No Load, V _{EN} = 0 V			10	μA
INTERNAL REFERENCE VOLTAGE						
V _{VFB}	VFB regulation voltage	VFB voltage, CCM condition ⁽¹⁾		600		mV
V _{VFB}	VFB regulation voltage	T _A = 25°C	597	600	603	mV
		0°C ≤ T _A ≤ 85°C	595.2	600	604.8	
		-40°C ≤ T _A ≤ 85°C	594	600	606	
I _{VFB}	VFB input current	V _{VFB} = 0.630 V, T _A = 25°C		0.002	0.2	μA
OUTPUT DRIVERS						
R _{DRVH}	DRVH resistance	Source, I _{DRVH} = -50 mA		1.5	3	Ω
		Sink, I _{DRVH} = 50 mA		0.7	1.8	
R _{DRVL}	DRVL resistance	Source, I _{DRVL} = -50 mA		1.0	2.2	Ω
		Sink, I _{DRVL} = 50 mA		0.5	1.2	
t _{DEAD}	Dead time	DRVH-off to DRVL-on	7	17	30	ns
		DRVL-off to DRVH-on	10	22	35	
LDO OUTPUT						
V _{VREG}	LDO output voltage	0 mA ≤ I _{VREG} ≤ 50 mA	5.76	6.2	6.67	V
I _{VREG}	LDO output current ⁽¹⁾	Maximum current allowed from LDO			50	mA
V _{DO}	LDO drop out voltage	V _{VDD} = 4.5 V, I _{VREG} = 50 mA			364	mV
BOOT STRAP SWITCH						
V _{FBST}	Forward voltage	V _{VREG-VBST} , I _F = 10 mA, T _A = 25°C		0.1	0.2	V
I _{VBSTLK}	VBST leakage current	V _{VBST} = 23 V, V _{SW} = 17 V, T _A = 25°C		0.01	1.5	μA
DUTY AND FREQUENCY CONTROL						
t _{OFF(min)}	Minimum off-time	T _A = 25°C	150	260	400	ns
t _{ON(min)}	Minimum ON-time	V _{IN} = 17 V, V _{OUT} = 0.6 V, R _{RF} = 0 Ω to V _{REG} , T _A = 25°C ⁽¹⁾		35		ns
SOFTSTART						
t _{SS}	Internal soft-start time	0 V ≤ V _{OUT} ≤ 95%, R _{MODE} = 39 kΩ		0.7		ms
		0 V ≤ V _{OUT} ≤ 95%, R _{MODE} = 100kΩ		1.4		
		0 V ≤ V _{OUT} ≤ 95%, R _{MODE} = 200 kΩ		2.8		
		0 V ≤ V _{OUT} ≤ 95%, R _{MODE} = 470 kΩ		5.6		
POWERGOOD						

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, VDD = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V _{THPG}	PG threshold	PG in from lower	92.5%	96%	98.5%	
		PG in from higher	108%	111%	114%	
		PG hysteresis	2.5%	5%	7.8%	
R _{PG}	PG transistor on-resistance		15	30	50	Ω
t _{PG(del)}	PG delay after soft-start		0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS						
V _{EN}	EN voltage threshold enable	-40°C ≤ T _A ≤ 85°C	1.8			V
		0°C ≤ T _A ≤ 85°C	1.7			
	EN voltage threshold disable		0.5			
I _{EN}	EN input current	V _{EN} = 5 V	1			μA
f _{SW}	Switching frequency	R _{RF} = 0 Ω to GND, T _A = 25°C ⁽²⁾	200	250	300	kHz
		R _{RF} = 187 kΩ to GND, T _A = 25°C ⁽²⁾	250	300	350	
		R _{RF} = 619 kΩ to GND, T _A = 25°C ⁽²⁾	350	400	450	
		R _{RF} = Open, T _A = 25°C ⁽²⁾	450	500	550	
		R _{RF} = 866 kΩ to V _{REG} , T _A = 25°C ⁽²⁾	580	650	720	
		R _{RF} = 309 kΩ to V _{REG} , T _A = 25°C ⁽²⁾	670	750	820	
		R _{RF} = 124 kΩ to V _{REG} , T _A = 25°C ⁽²⁾	770	850	930	
		R _{RF} = 0 Ω to V _{REG} , T _A = 25°C ⁽²⁾	880	970	1070	
VO DISCHARGE						
I _{Dischg}	VO discharge current	V _{EN} = 0 V, V _{SW} = 0.5 V	5	13		mA
PROTECTION: CURRENT SENSE						
I _{TRIP}	TRIP source current	V _{TRIP} = 1 V, T _A = 25°C	9	10	11	μA
TC _{ITRIP}	TRIP current temp. coef.	T _A = 25°C ⁽¹⁾	4700			ppm/°C
V _{TRIP}	Current limit threshold setting range	V _{TRIP-GND} voltage	0.2	3		V
V _{OCL}	Current limit threshold	V _{TRIP} = 3 V	355	375	395	mV
		V _{TRIP} = 1.6 V	185	200	215	
		V _{TRIP} = 0.2 V	17	25	33	
V _{OCLN}	Negative current limit threshold	V _{TRIP} = 3 V	-406	-375	-355	mV
		V _{TRIP} = 1.6 V	-215	-200	-185	
		V _{TRIP} = 0.2 V	-33	-25	-17	
V _{AZC(adj)}	Auto zero cross adjustable range	Positive	3	15		mV
		Negative		-15	-3	
PROTECTION: UVP AND OVP						
V _{OVP}	OVP trip threshold voltage	OVP detect	115%	120%	125%	
t _{OVP(del)}	OVP propagation delay time	VFB delay with 50-mV overdrive	1			μs
V _{UVP}	Output UVP trip threshold voltage	UVP detect	65%	70%	75%	
t _{UVP(del)}	Output UVP propagation delay time		0.8	1	1.2	ms
t _{UVP(en)}	Output UVP enable delay time	from EN to UVP workable, R _{MODE} = 39 kΩ	2.00	2.55	3	ms
UVLO						
V _{UVVREG}	VREG UVLO threshold	Wake up	4	4.18	4.5	V
		Hysteresis	0.25			
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾	145			°C
		Hysteresis ⁽¹⁾	10			

 (2) Not production tested. Test conditions are V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 10 A and using the application circuit shown in Figure 18 and Figure 22.

6.6 Typical Characteristics

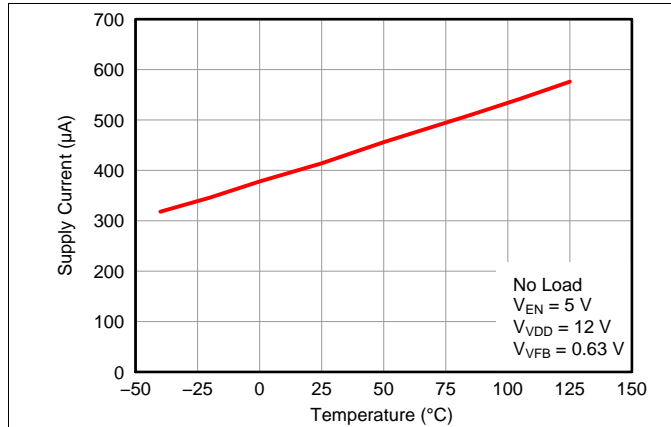


Figure 1. VDD Supply Current vs Temperature

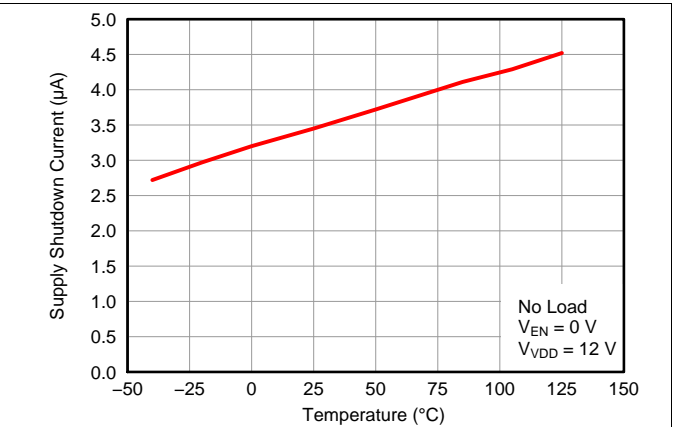


Figure 2. VDD Shutdown Current vs Temperature

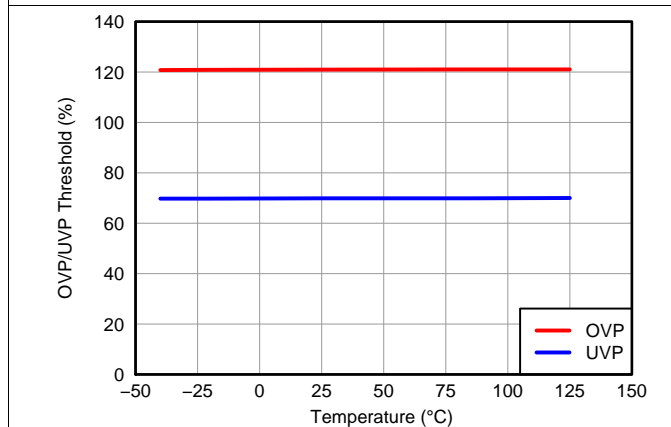


Figure 3. OVP/UVP Threshold vs Temperature

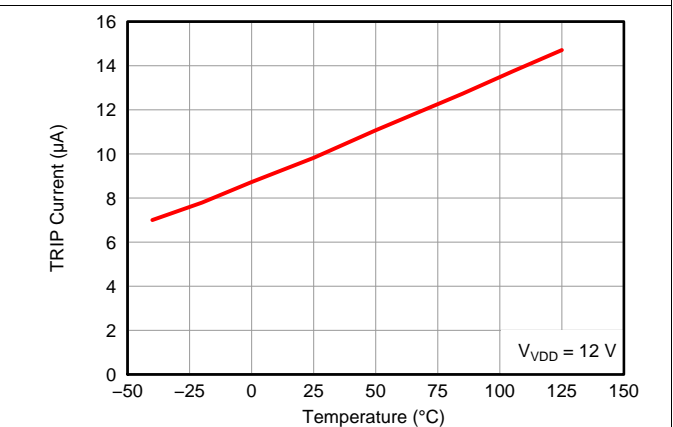


Figure 4. TRIP Pin Current vs Temperature

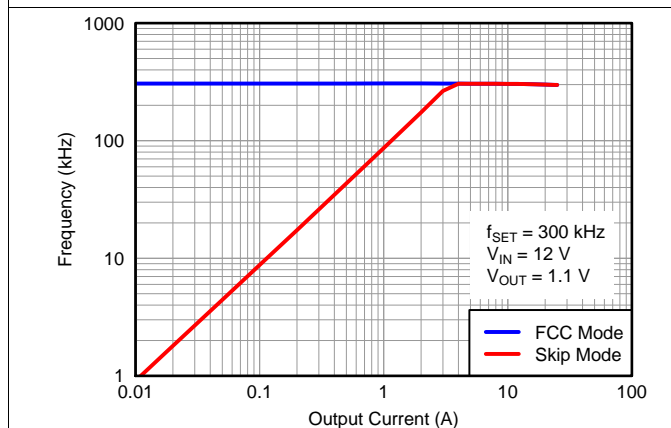


Figure 5. Switching Frequency vs Output Current

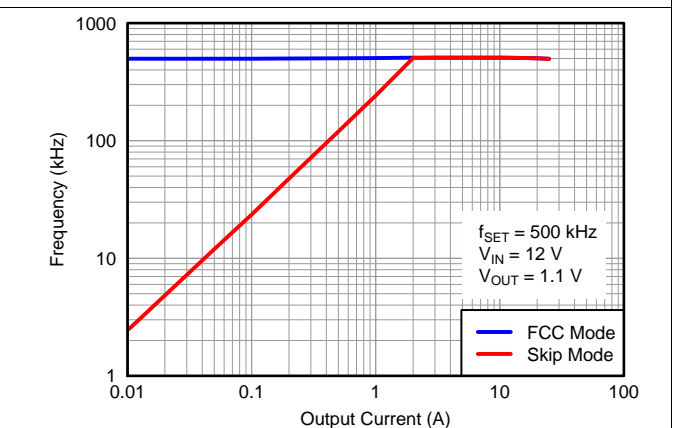


Figure 6. Switching Frequency vs Output Current

Typical Characteristics (continued)

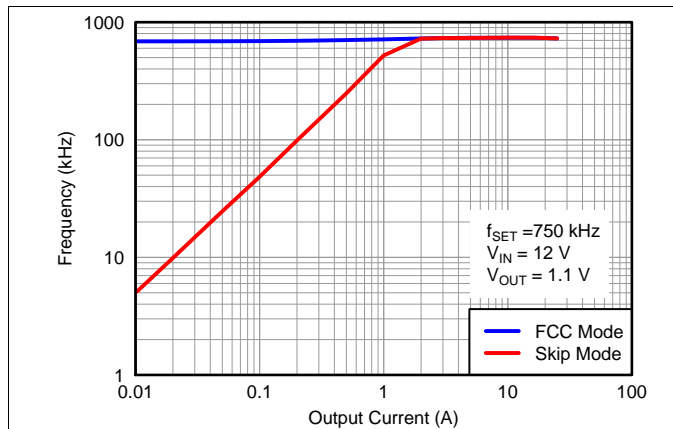


Figure 7. Switching Frequency vs Output Current

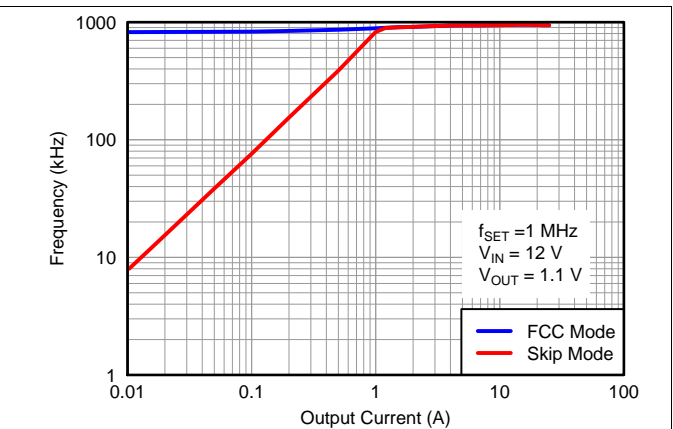


Figure 8. Switching Frequency vs Output Current

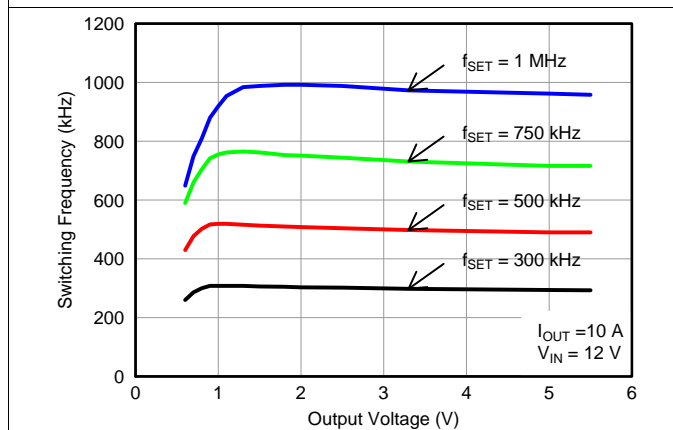


Figure 9. Switching Frequency vs Output Voltage

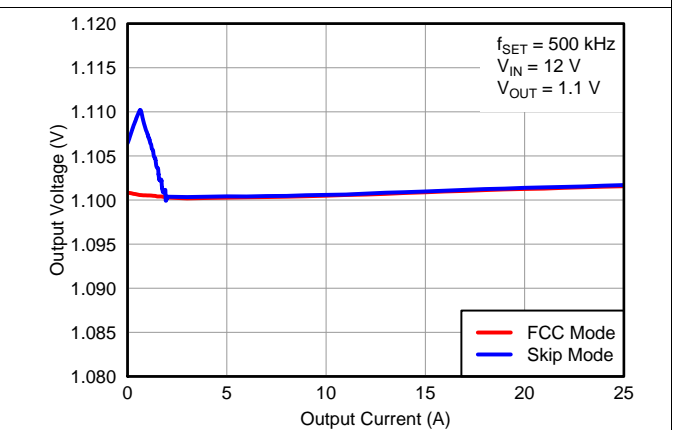


Figure 10. Output Voltage vs Output Current

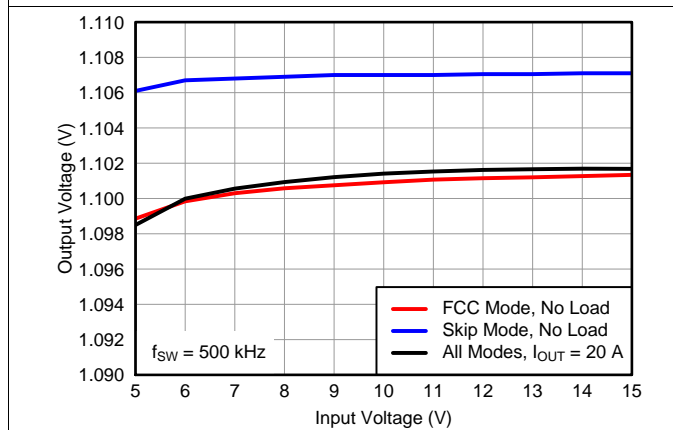


Figure 11. Output Voltage vs Input Voltage

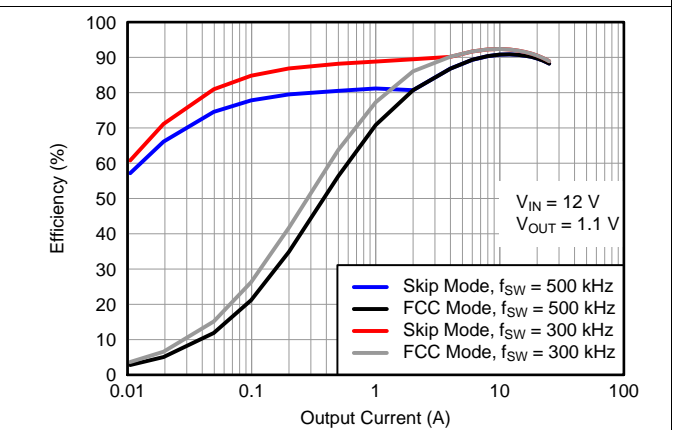


Figure 12. Efficiency vs Output Current

Typical Characteristics (continued)

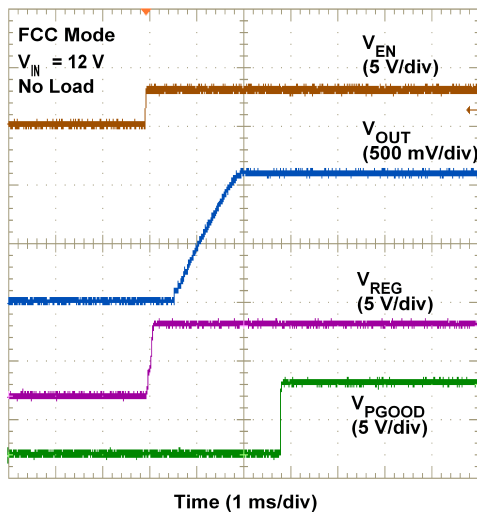


Figure 13. Start-Up Waveform

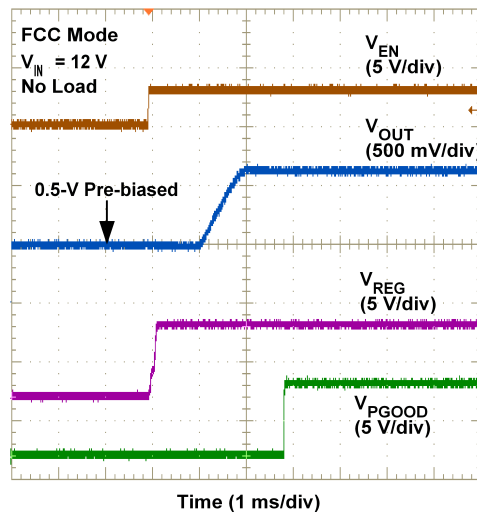


Figure 14. Prebias Start-Up Waveform

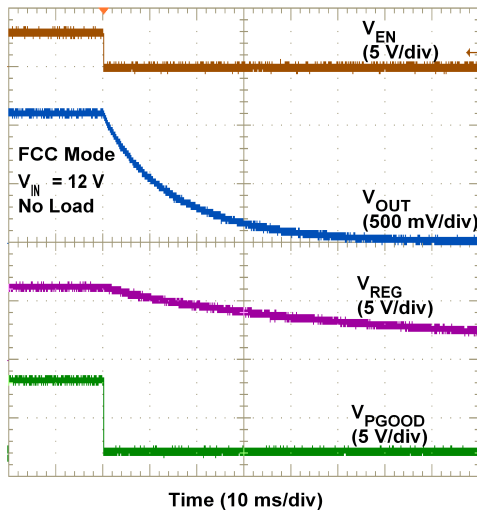


Figure 15. Turnoff Waveform

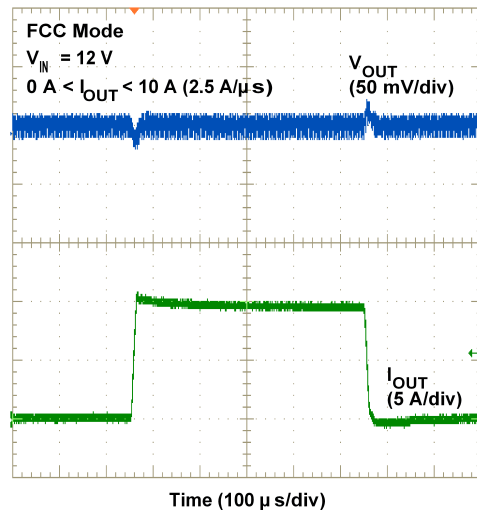


Figure 16. Load Transient Response

7 Detailed Description

7.1 Overview

The TPS53219A is a high-efficiency, single-channel, synchronous buck regulator controller suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive ON-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC–DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V up to 28 V. The D-CAP mode uses the ESR of the output capacitors to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive ON-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

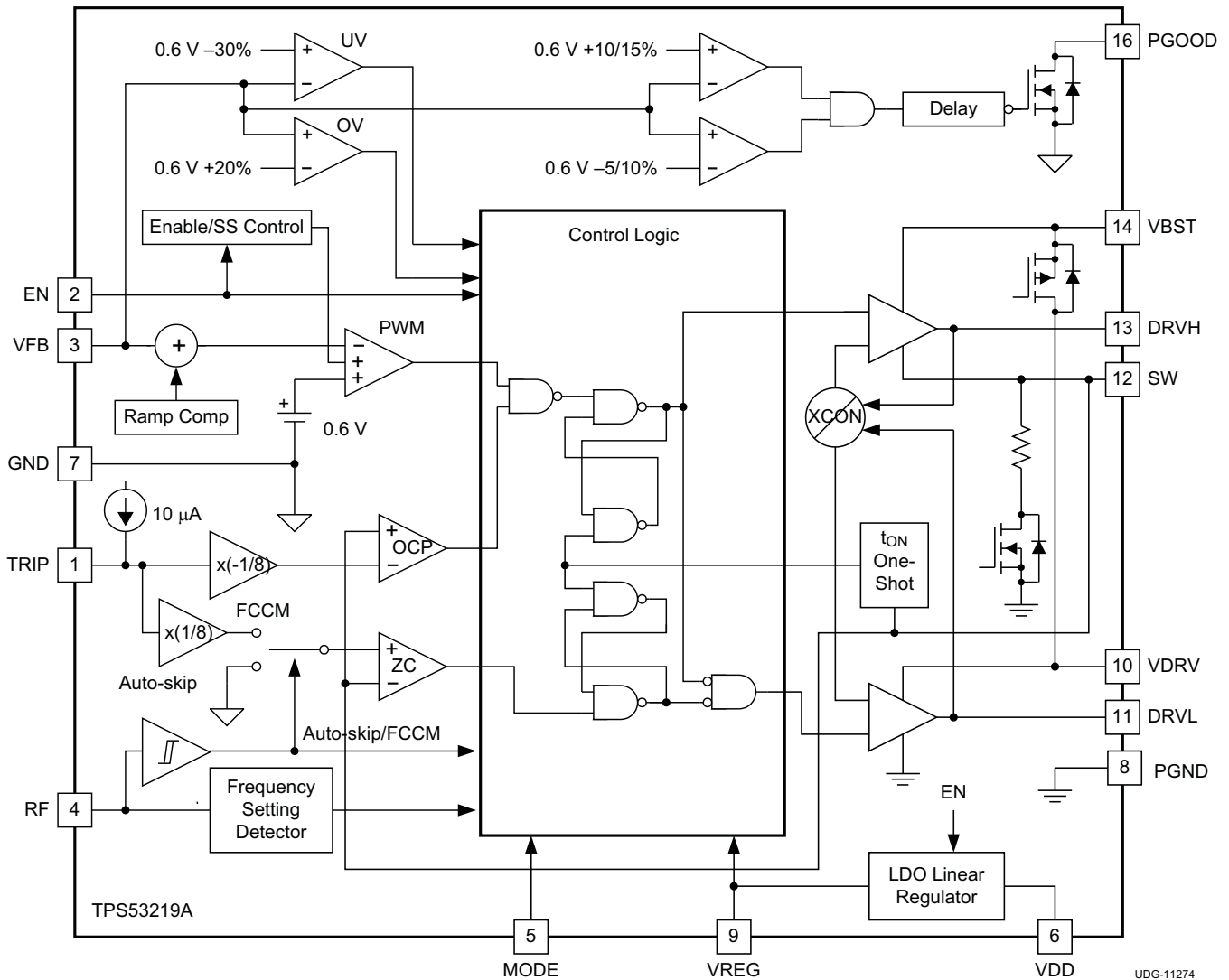
The TPS53219A has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in [Table 1](#). The strong gate drivers allow low $R_{DS(on)}$ FETs for high-current applications.

When the device starts (either by EN or VDD UVLO), the TPS53219A sends out a current that detects the resistance connected to the MODE pin to determine the soft-start time. After that (and before V_{OUT} start to ramp up) the MODE pin becomes a high-impedance input to determine skip mode or FCCM mode operation. When the voltage on the MODE pin is higher than 1.3 V, the converter enters into FCCM mode. If the voltage on MODE pin is less than 1.3 V, then the converter operates in skip mode.

TI recommends to connect the MODE pin to the PGOOD pin if FCCM mode is desired. In this configuration, the MODE pin is connected to the GND potential through a resistor when the device is detecting the soft-start time thus correct soft-start time is used. The device starts up in skip mode and only after the PGOOD pin goes high does the device enter into FCCM mode. When the PGOOD pin goes high there is a transition between skip mode and FCCM. A minimum off-time of 60 ns on DRV1 is provided to avoid a voltage spike on the DRV1 pin caused by parasitic inductance of the driver loop and gate capacitance of the low-side MOSFET.

For proper operation, the MODE pin must not be connected directly to a voltage source.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Soft-Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.4 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 6.2 V at the VREG pin. The controller then uses the first 250 μ s to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. However, switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Table 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device goes into Forced CCM after PGOOD becomes high.

When the EN voltage is higher than 5.5 V, a 1-kΩ series resistor is needed for EN pin

7.3.2 Adaptive ON-Time D-CAP Control and Frequency Selection

The TPS53219A does not have a dedicated oscillator that determines switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the ON-time one-shot timer. The adaptive ON-time control adjusts the ON-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$).

This makes the switching frequency fairly constant in steady-state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in [Table 2](#). Leaving the resistance open sets the switching frequency to 500 kHz.

Table 2. Resistor and Switching Frequency

RESISTOR (R _{RF}) CONNECTIONS	SWITCHING FREQUENCY (kHz)
0 Ω to GND	250
187 kΩ to GND	300
619 kΩ to GND	400
Open	500
866 kΩ to VREG	650
309 kΩ to VREG	750
124 kΩ to VREG	850
0 Ω to VREG	970

The OFF-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a *set* signal to terminate the OFF-time (turn off the low-side MOSFET and turn on high-side MOSFET). The *set* signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

7.3.3 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP mode can be simplified as shown in Figure 17.

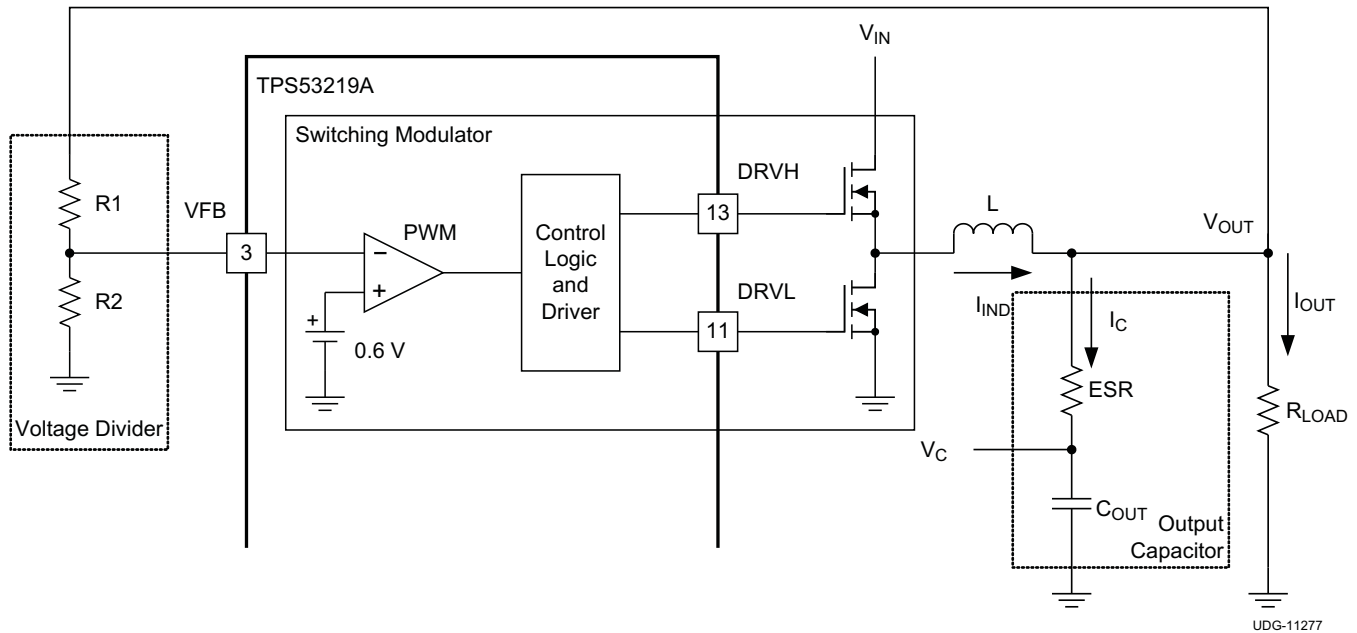


Figure 17. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times \text{ESR} \times C_{\text{OUT}}} \quad (1)$$

For the loop stability, the 0-dB frequency, f_0 , defined below must be lower than $\frac{1}{4}$ of the switching frequency.

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{4} \quad (2)$$

According to Equation 2, the loop stability of D-CAP mode modulator is mainly determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance on the order of several 100 μF and ESR in range of 10 $\text{m}\Omega$. These yields an f_0 on the order of 100 kHz or less and a more stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and require special care when used with this modulator. An application circuit for ceramic capacitor is described in section [External Parts Selection With All Ceramic Output Capacitors](#).

7.3.4 Ramp Signal

The TPS53219A adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in [Small Signal Model](#), the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with -7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady-state.

During skip mode operation, when the switching frequency is lower than 70% of the nominal frequency (because of longer OFF-time), the ramp signal exceeds 0 mV at the end of the OFF-time but is clamped at 3 mV to minimize DC offset.

7.3.5 Adaptive Zero Crossing

The TPS53219A has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

7.3.6 Output Discharge Control

When EN becomes low, the TPS53219A discharges output capacitor using internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the *OFF* state. The typical discharge resistance is 40 Ω. The soft discharge occurs only as EN becomes low. After VREG becomes low, the internal MOSFET turns off and the discharge function becomes inactive.

7.3.7 Low-Side Driver

The low-side driver is designed to drive high-current low- $R_{DS(on)}$ N-channel MOSFETs. The drive capability is represented by its internal resistance, which is 1.0 Ω for VDRV to DRV1 and 0.5 Ω for DRV1 to GND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. The bias voltage VDRV can be delivered from 6.2-V VREG supply or from external power source from 4.5 V to 6.5 V. The instantaneous drive current is supplied by an input capacitor connected between the VDRV and PGND pins.

The average low-side gate drive current is calculated in [Equation 3](#).

$$I_{GL} = C_{GL} \times V_{VDRV} \times f_{SW} \quad (3)$$

When VDRV is supplied by external voltage source, the device continues to be supplied by the VREG pin. There is no internal connection from VDRV to VREG.

7.3.8 High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFETs. When configured as a floating driver, the bias voltage is delivered from the VDRV pin supply. The average drive current is calculated using [Equation 4](#).

$$I_{GH} = C_{GH} \times V_{VDRV} \times f_{SW} \quad (4)$$

The instantaneous drive current is supplied by the flying capacitor between VBST and SW pins. The drive capability is represented by internal resistance, which is 1.5 Ω for VBST to DRVH and 0.7 Ω for DRVH to SW.

The driving power which needs to be dissipated from TPS53219A package.

$$P_{DRV} = (I_{GL} + I_{GH}) \times V_{VDRV} \quad (5)$$

7.3.9 Power Good

The TPS53219A has a power-good output that indicates *high* when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% or –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay. The power-good output is an open-drain output and must be pulled up externally.

In order for the PGOOD logic to be valid, the VDD input must be higher than 1 V. To avoid invalid PGOOD logic before the TPS53219A is powered up, TI recommends that the PGOOD pin be pulled up to VREG (either directly or through a resistor divider if a different pullup voltage is desired) because VREG remains low when the device is powered off. The pullup resistance can be chosen from a standard resistor value between 1 kΩ and 100 kΩ.

7.3.10 Current Sense and Overcurrent Protection

TPS53219A has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost-effective solution, TPS53219A supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP} . The TRIP terminal sources I_{TRIP} current, which is 10 μ A typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in [Equation 6](#).

NOTE

The V_{TRIP} is limited up to approximately 3 V internally.

$$V_{TRIP} \text{ (mV)} = R_{TRIP} \text{ (k}\Omega\text{)} \times I_{TRIP} \text{ (}\mu\text{A)} \quad (6)$$

The inductor current is monitored by the voltage between GND pin and SW pin so that SW pin should be connected to the drain terminal of the low-side MOSFET properly. I_{TRIP} has 4700-ppm/ $^{\circ}$ C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. The GND pin is used as the positive current-sensing node. The GND pin should be connected to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP} , can be calculated as shown in [Equation 7](#).

$$I_{OCP} = \frac{V_{TRIP}}{(8 \times R_{DS(on)})} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{(8 \times R_{DS(on)})} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (7)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7-ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

During the CCM, the negative current limit (NCL) protects the external FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity.

NOTE

The threshold still represents the valley value of the inductor current.

7.3.11 Overvoltage and Undervoltage Protection

TPS53219A monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS53219A latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7-ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after an hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

7.3.12 UVLO Protection

The TPS53219A uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is non-latch protection.

7.3.13 Thermal Shutdown

The TPS53219A uses temperature monitoring. If the temperature exceeds the threshold value (typically 145 $^{\circ}$ C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Light Load Condition in Auto-Skip Operation

While the MODE pin is pulled low through R_{MODE}, TPS53219A automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The ON-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation I_{O(LL)} (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as shown in [Equation 8](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency (8)

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the I_{O(LL)} given in [Equation 8](#). For example, it is 60 kHz at I_{O(LL)}/5 if the frequency setting is 300 kHz.

7.4.2 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53219A device is a small-sized, single-buck controller with adaptive ON-time DCAP mode control.

8.2 Typical Applications

8.2.1 Typical Application With Power Block

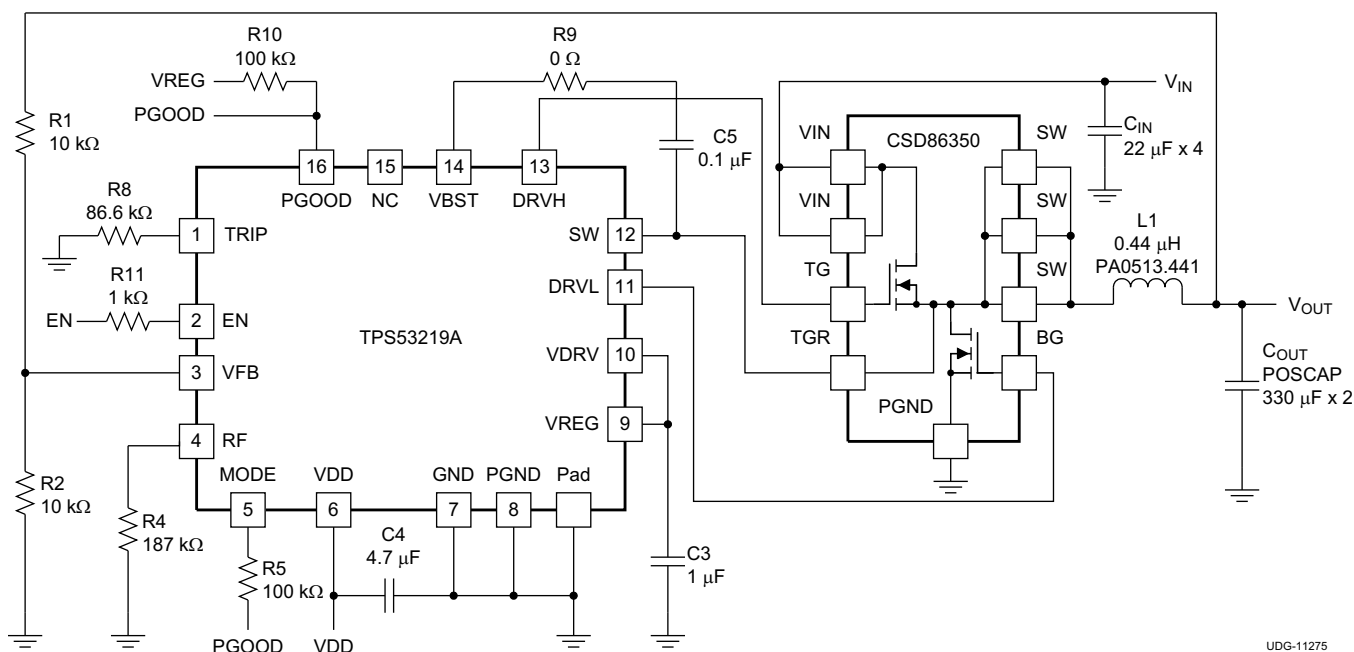


Figure 18. Typical Application Circuit Diagram With Power Block

8.2.1.1 Design Requirements

This design uses the parameters listed in Table 3.

Table 3. Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Voltage range	5	12	18	V
I_{MAX}	Maximum input current	$V_{IN} = 5\text{ V}$, $I_{OUT} = 25\text{ A}$		10	A
	No load input current	$V_{IN} = 12\text{ V}$, $I_{OUT} = 0\text{ A}$ with auto-skip mode		1	mA
OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage			1.2	V
	Output voltage regulation	Line regulation, $5\text{ V} \leq V_{IN} \leq 14\text{ V}$ with FCCM		0.2%	
		Load regulation, $V_{IN} = 12\text{ V}$, $0\text{ A} \leq I_{OUT} \leq 25\text{ A}$ with FCCM		0.5%	

Typical Applications (continued)
Table 3. Design Specifications (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RIPPLE}	Output voltage ripple	V _{IN} = 12 V, I _{OUT} = 25 A with FCCM		10		mV _{PP}
I _{LOAD}	Output load current		0		25	A
I _{OVER}	Output overcurrent			32		
t _{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f _{SW}	Switching frequency			500		kHz
η	Peak efficiency	V _{IN} = 12 V, V _{OUT} = 1.2 V, I _{OUT} = 4 A		91%		
	Full load efficiency	V _{IN} = 12 V, V _{OUT} = 1.2 V, I _{OUT} = 8 A		91.5%		
T _A	Operating temperature			25		°C

8.2.1.2 Detailed Design Procedure
8.2.1.2.1 External Components Selection

Selecting external components is a simple process using D-CAP Mode.

1. Choose the inductor

The inductance should be determined to give the ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

$$L = \frac{1}{I_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{I_{\text{OUT(max)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (9)$$

The inductor also requires a low DCR to achieve good efficiency. It also requires enough room above the peak inductor current before saturation. The peak inductor current can be estimated in [Equation 10](#).

$$I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{8 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (10)$$

2. Choose the output capacitor

When organic semiconductor capacitors or specialty polymer capacitors are used, for loop stability, capacitance and ESR should satisfy [Equation 2](#). For jitter performance, [Equation 11](#) is a good starting point to determine ESR.

$$\text{ESR} = \frac{V_{\text{OUT}} \times 10\text{mV} \times (1-D)}{0.6\text{V} \times I_{\text{IND(ripple)}}} = \frac{10\text{mV} \times L \times f_{\text{SW}}}{0.6\text{V}} = \frac{L \times f_{\text{SW}}}{60} \quad (\Omega)$$

where

- D is the duty factor
- the required output ripple slope is approximately 10 mV per t_{sw} (switching period) in terms of VFB terminal voltage

3. Determine the value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in [Figure 17](#). R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is between 10 kΩ and 20 kΩ. Determine R1 using [Equation 12](#).

$$R1 = \frac{V_{\text{OUT}} - \left(\frac{I_{\text{IND(ripple)}} \times \text{ESR}}{2} \right) - 0.6}{0.6} \times R2 \quad (12)$$

8.2.1.3 Application Curves

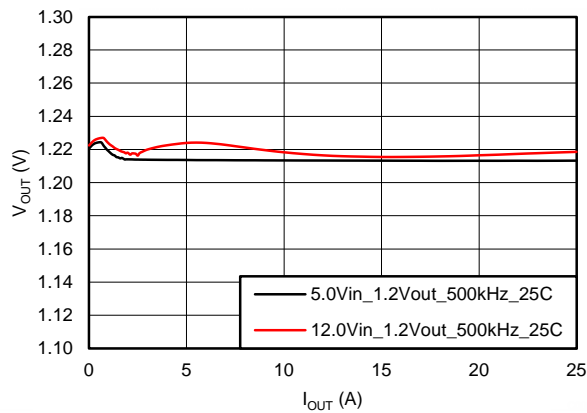


Figure 19. Load Regulation Performance

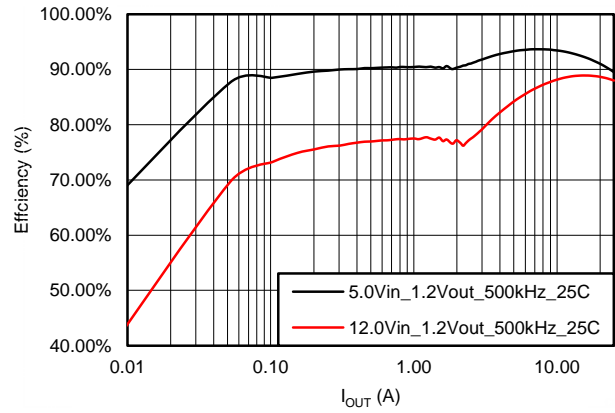


Figure 20. Efficiency Performance

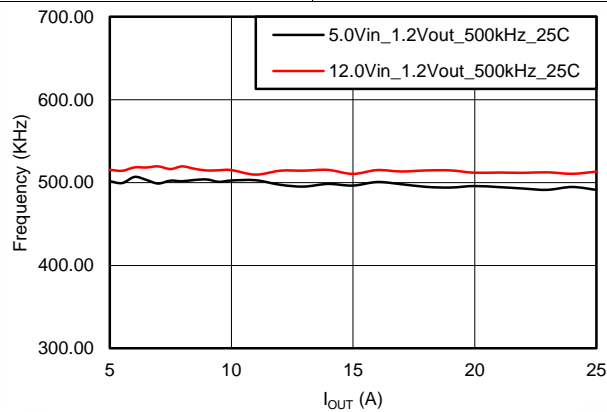


Figure 21. Switching Frequency Performance

8.2.2 Typical Application With Ceramic Output Capacitors

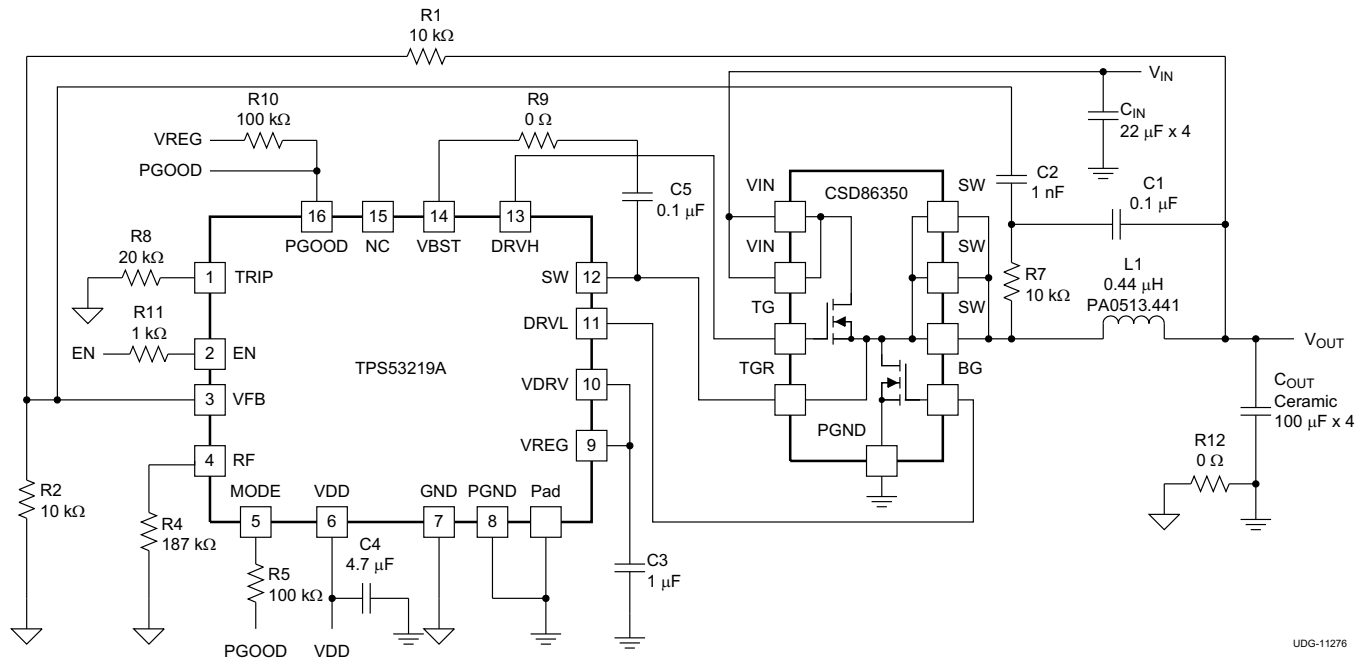


Figure 22. Typical Application Circuit Diagram With Ceramic Output Capacitors

8.2.2.1 Design Requirements

This design uses the parameters listed in [Table 4](#).

Table 4. Design Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Voltage range		5	12	18	V
I_{MAX}	Maximum input current	$V_{IN} = 5\text{ V}$, $I_{OUT} = 8\text{ A}$		2.5		A
	No load input current	$V_{IN} = 12\text{ V}$, $I_{OUT} = 0\text{ A}$ with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.2		V
	Output voltage regulation	Line regulation, $5\text{ V} \leq V_{IN} \leq 14\text{ V}$ with FCCM		0.2%		
		Load regulation, $V_{IN} = 12\text{ V}$, $0\text{ A} \leq I_{OUT} \leq 8\text{ A}$ with FCCM			0.5%	
V_{RIPPLE}	Output voltage ripple	$V_{IN} = 12\text{ V}$, $I_{OUT} = 8\text{ A}$ with FCCM		10		mV _{PP}
I_{LOAD}	Output load current		0		8	A
I_{OVER}	Output overcurrent			25		A
t_{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			500	1000	kHz
η	Peak efficiency	$V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 4\text{ A}$		91%		
	Full load efficiency	$V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 8\text{ A}$		91.5%		
T_A	Operating temperature			25		°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 External Parts Selection With All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 2 cannot be satisfied. The ripple injection approach as shown in Figure 22 is implemented to increase the ripple on the VFB pin and make the system stable. C2 can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

The increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from V_{OUT} and they can be calculated using Equation 13 and Equation 14.

$$V_{INJ(SW)} = \frac{(V_{IN} - V_{OUT})}{R7 \times C1} \times \frac{D}{f_{SW}} \quad (13)$$

$$V_{INJ(OUT)} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (14)$$

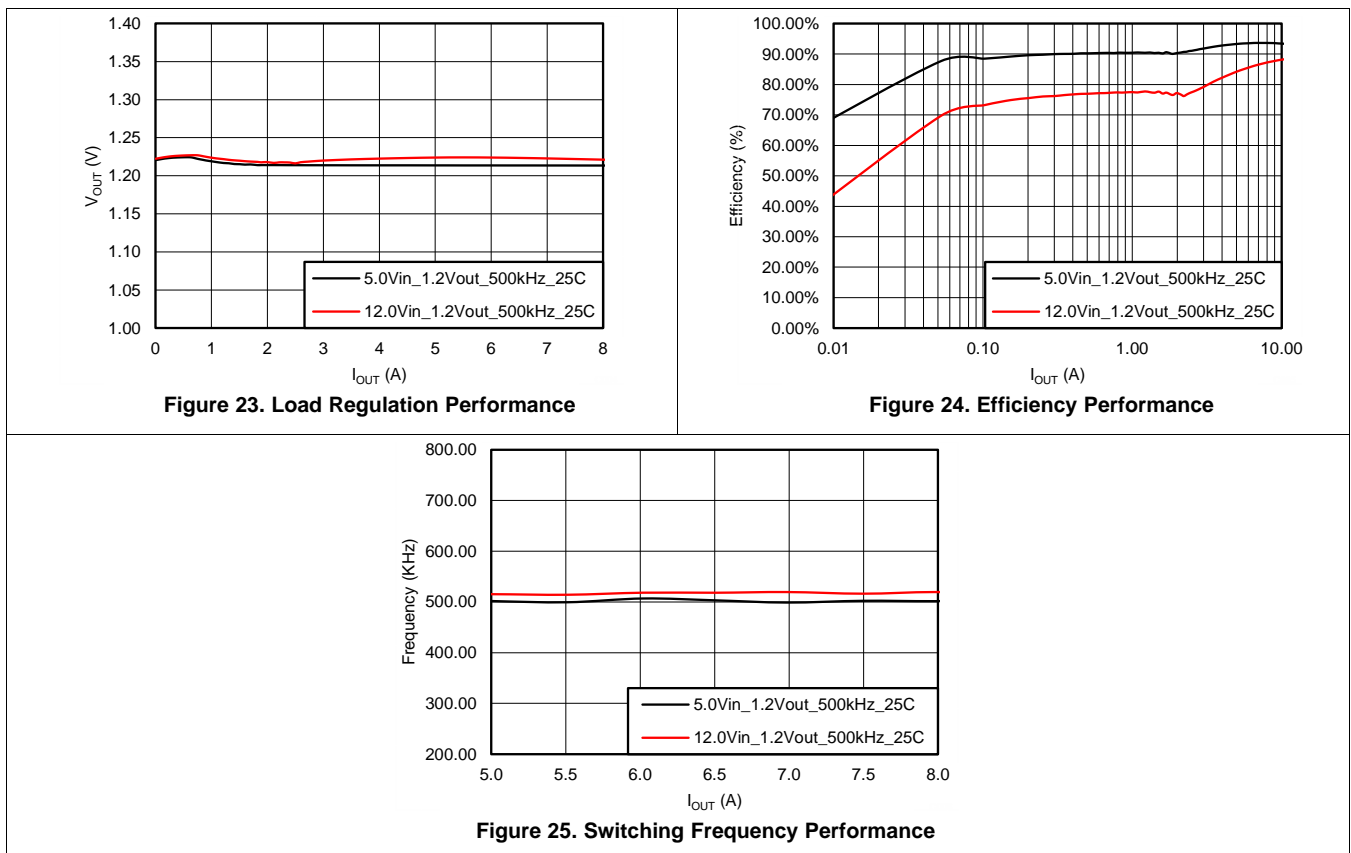
The DC value of VFB can be calculated by Equation 15.

$$V_{FB} = 0.6 + \frac{(V_{INJ(SW)} + V_{INJ(OUT)})}{2} \quad (15)$$

And the resistor divider value can be determined by Equation 16.

$$R1 = \frac{(V_{OUT} - V_{FB})}{V_{FB}} \times R2 \quad (16)$$

8.2.2.3 Application Curves



9 Power Supply Recommendations

The TPS53219A is a small-sized single-buck controller with adaptive ON-time D-CAP mode control. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supplies in digital consumer products.

10 Layout

10.1 Layout Guidelines

Certain points must be considered before starting a layout work using the TPS53219A.

- Inductors, V_{IN} capacitors, V_{OUT} capacitors and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to power ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layers as ground planes and shield feedback trace from power traces and components.
- The DC–DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
 - The most important loop to minimize the area of is the path from the V_{IN} capacitors through the high and low-side MOSFETs, and back to the capacitors through ground. Connect the negative node of the V_{IN} capacitors and the source of the low-side MOSFET at ground as close as possible.
 - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitors, and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitors at ground as close as possible.
 - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from VDRV capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND of the device, and back to source of the low-side MOSFET through ground. Connect negative node of VDRV capacitor, source of the low-side MOSFET and PGND of the device at ground as close as possible.
- Because the TPS53219A controls output voltage referring to voltage across V_{OUT} capacitor, the high-side resistor of the voltage divider should be connected to the positive node of V_{OUT} capacitor at the regulation point. The low-side resistor should be connected to the GND (analog ground of the device). The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid vias between these resistors and the device.
- Connect the overcurrent setting resistors from the TRIP pin to GND and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to GND should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to GND, or to the PGOOD pin, and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to GND should avoid coupling to a high-voltage switching node.
- Connect all GND (analog ground of the device) trace together and connect to power ground or ground plane with a single via or trace or through a 0- Ω resistor at a quiet point
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace (width) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in [Figure 22](#)) from the terminal of ceramic output capacitor. The AC-coupling capacitor (C7 in [Figure 22](#)) can be placed near the device.

10.2 Layout Example

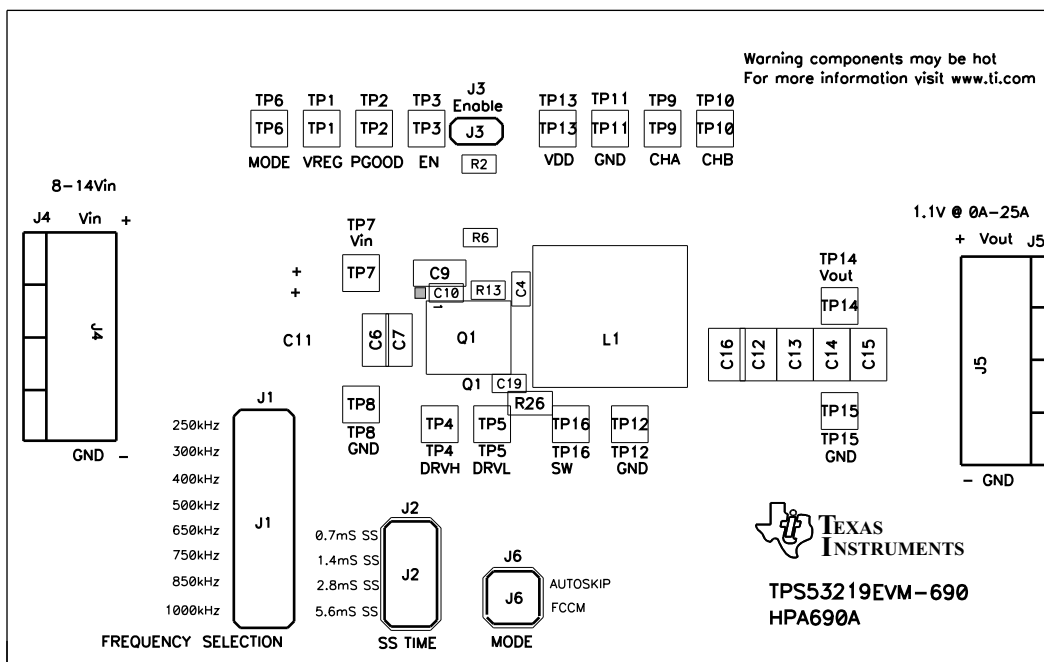


Figure 26. TPS53219EVM-690 Top Layer Assembly Drawing, Top View

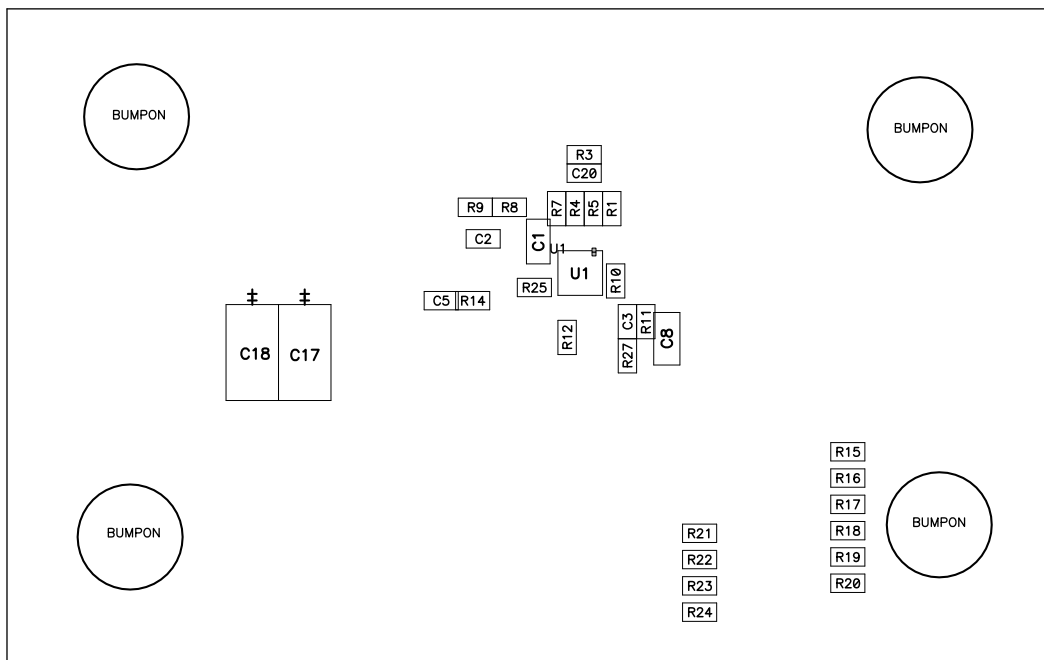
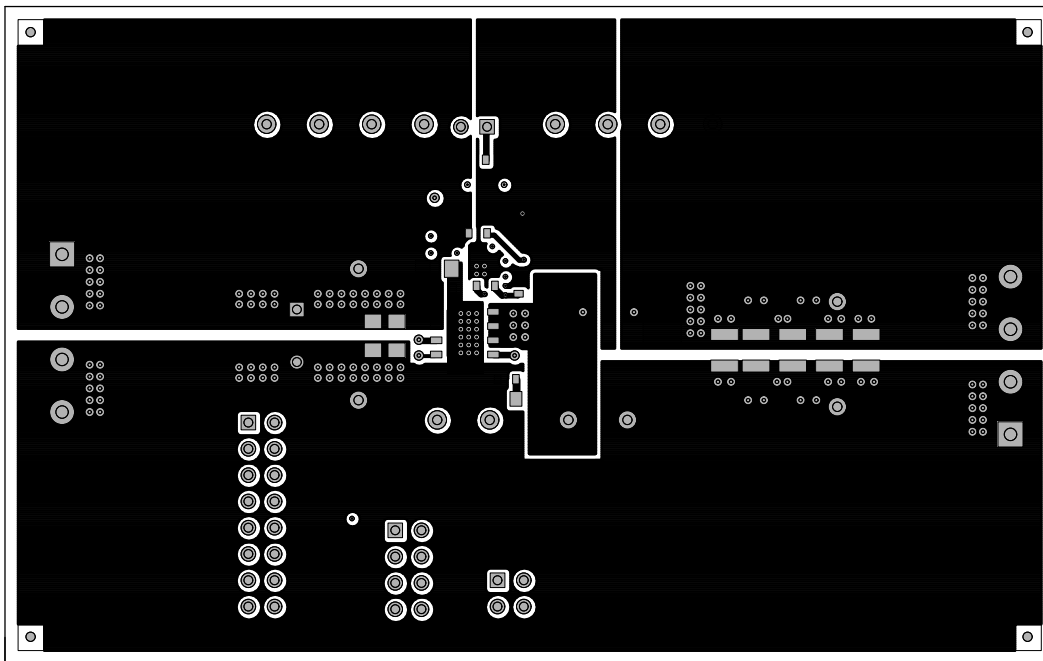
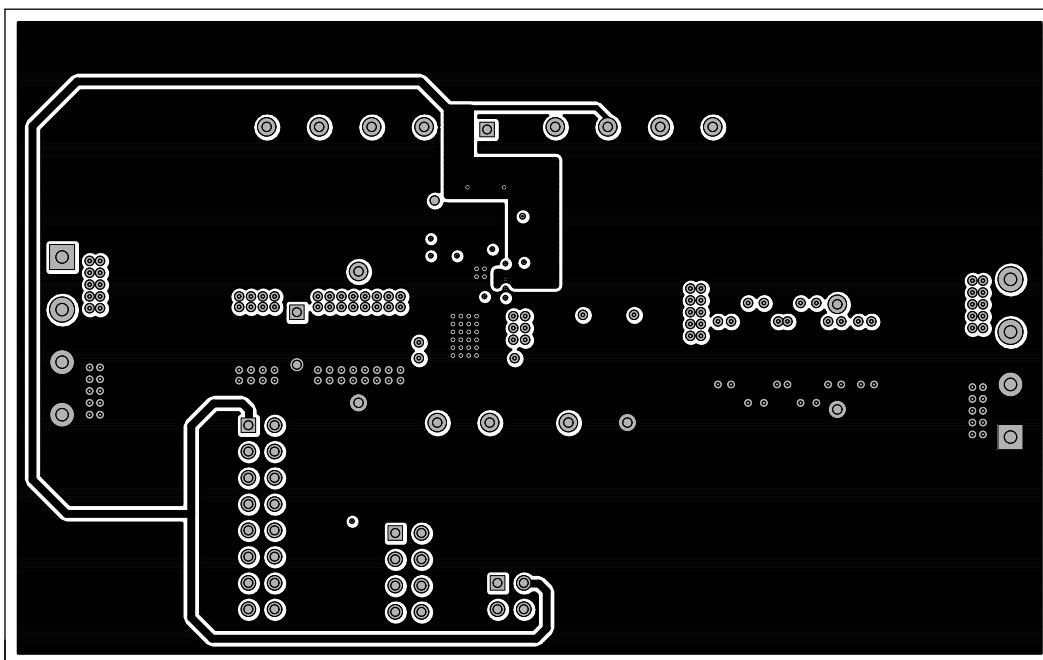


Figure 27. TPS53219EVM-690 Bottom Assembly Drawing, Bottom View

Layout Example (continued)

Figure 28. TPS53219EVM-690 Top Copper, Top View

Figure 29. TPS53219EVM-690 Layer-2 Copper, Top View

Layout Example (continued)

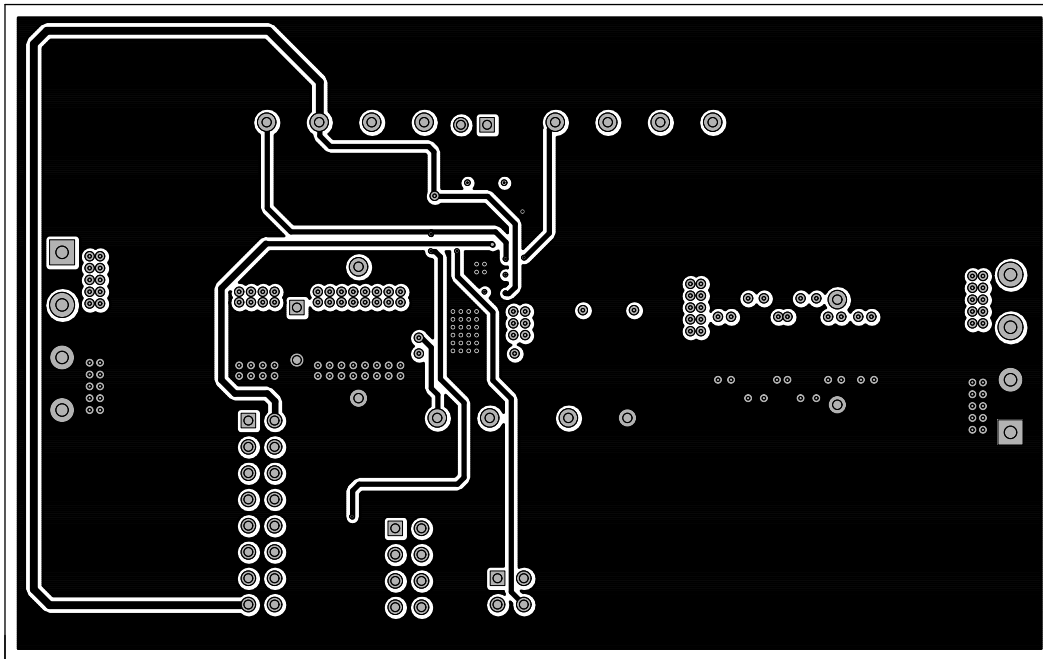


Figure 30. TPS53219EVM-690 Layer-3 Copper, Top View

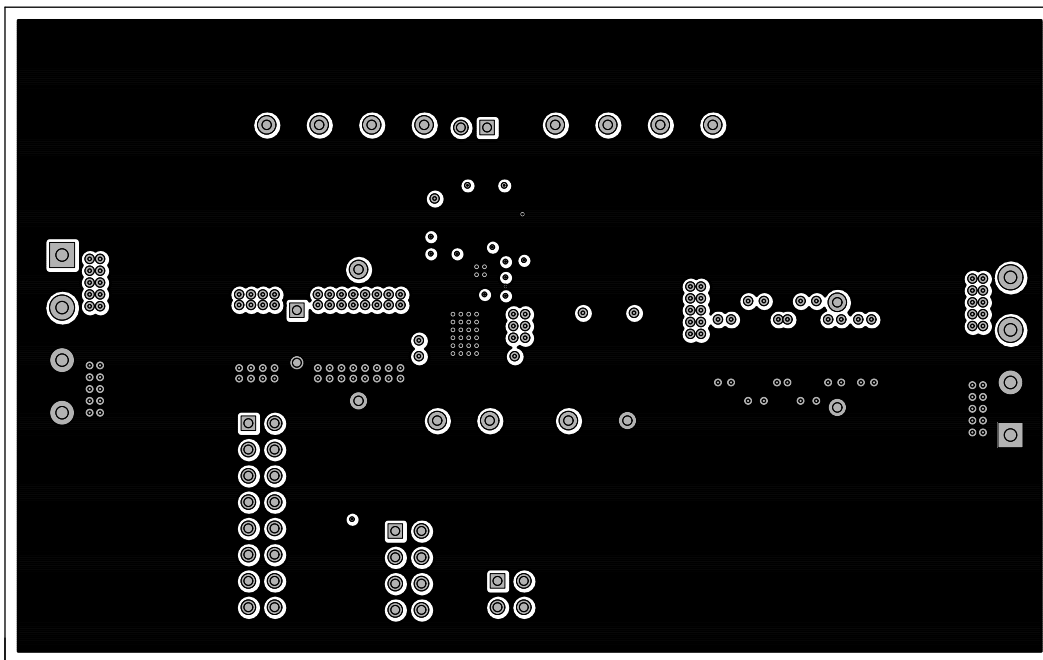


Figure 31. TPS53219EVM-690 Layer-4 Copper, Top View

Layout Example (continued)

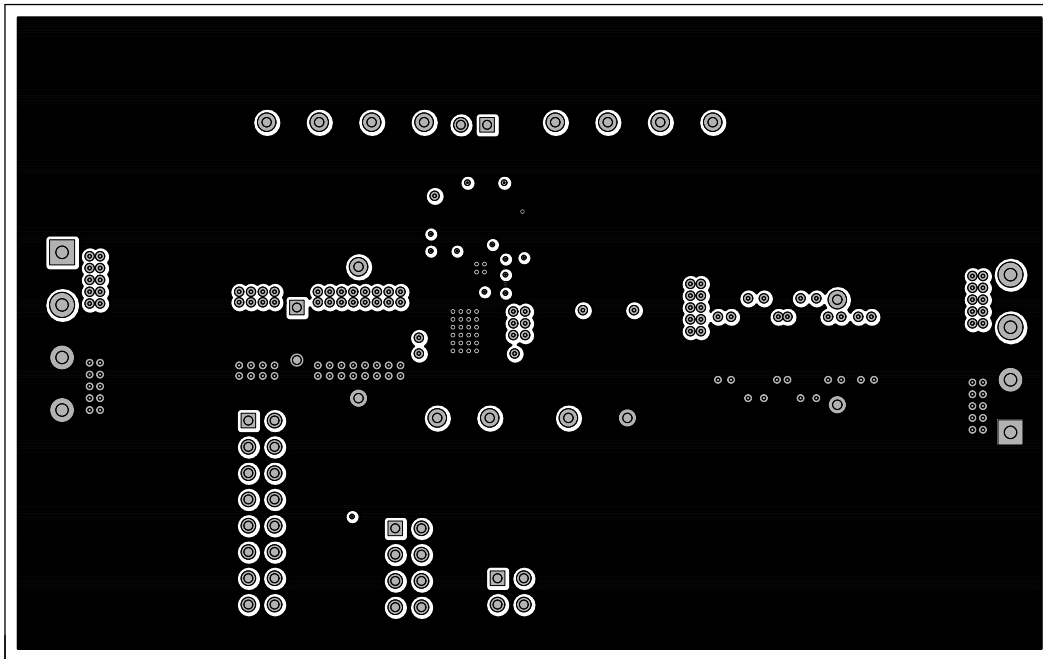


Figure 32. TPS53219EVM-690 Layer-5 Copper, Top View

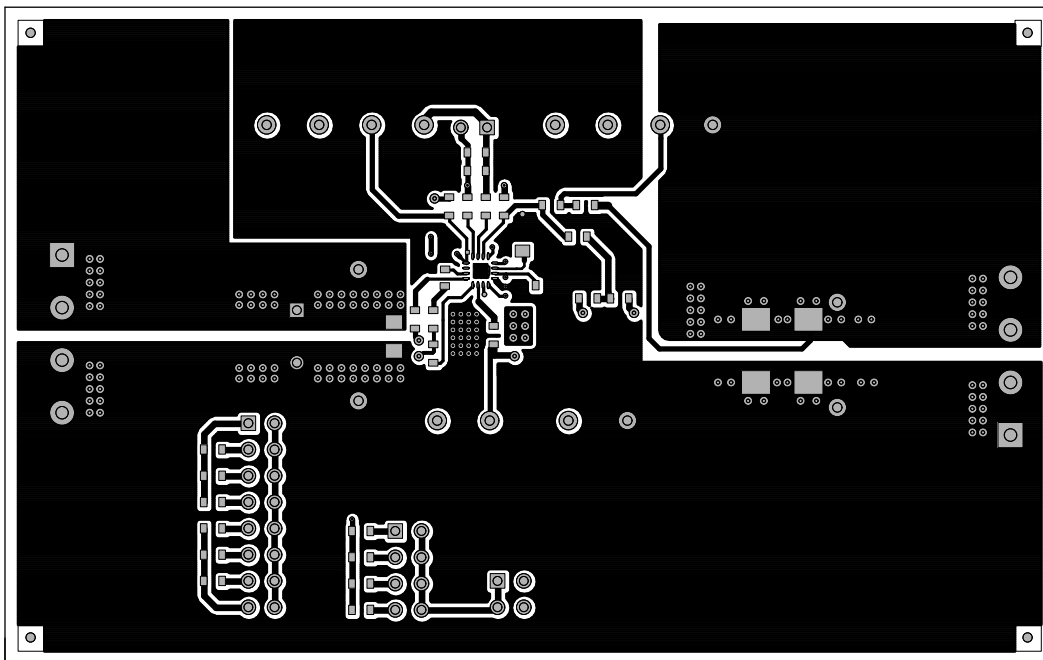


Figure 33. TPS53219EVM-690 Bottom Layer Copper, Top View

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

Eco-Mode, D-CAP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53219ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3219A	Samples
TPS53219ARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3219A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53219ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53219ARGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53219ARGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPS53219ARGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

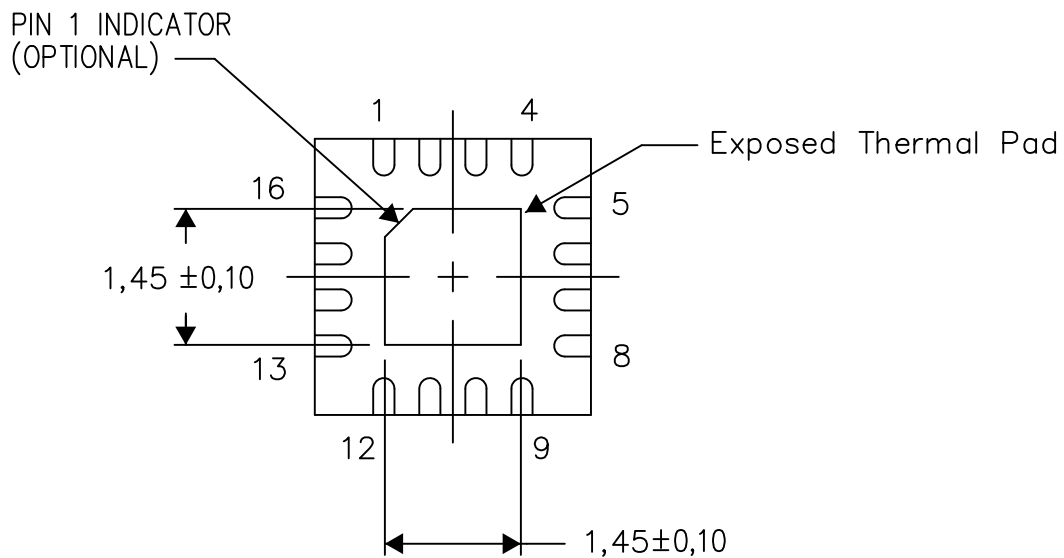
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

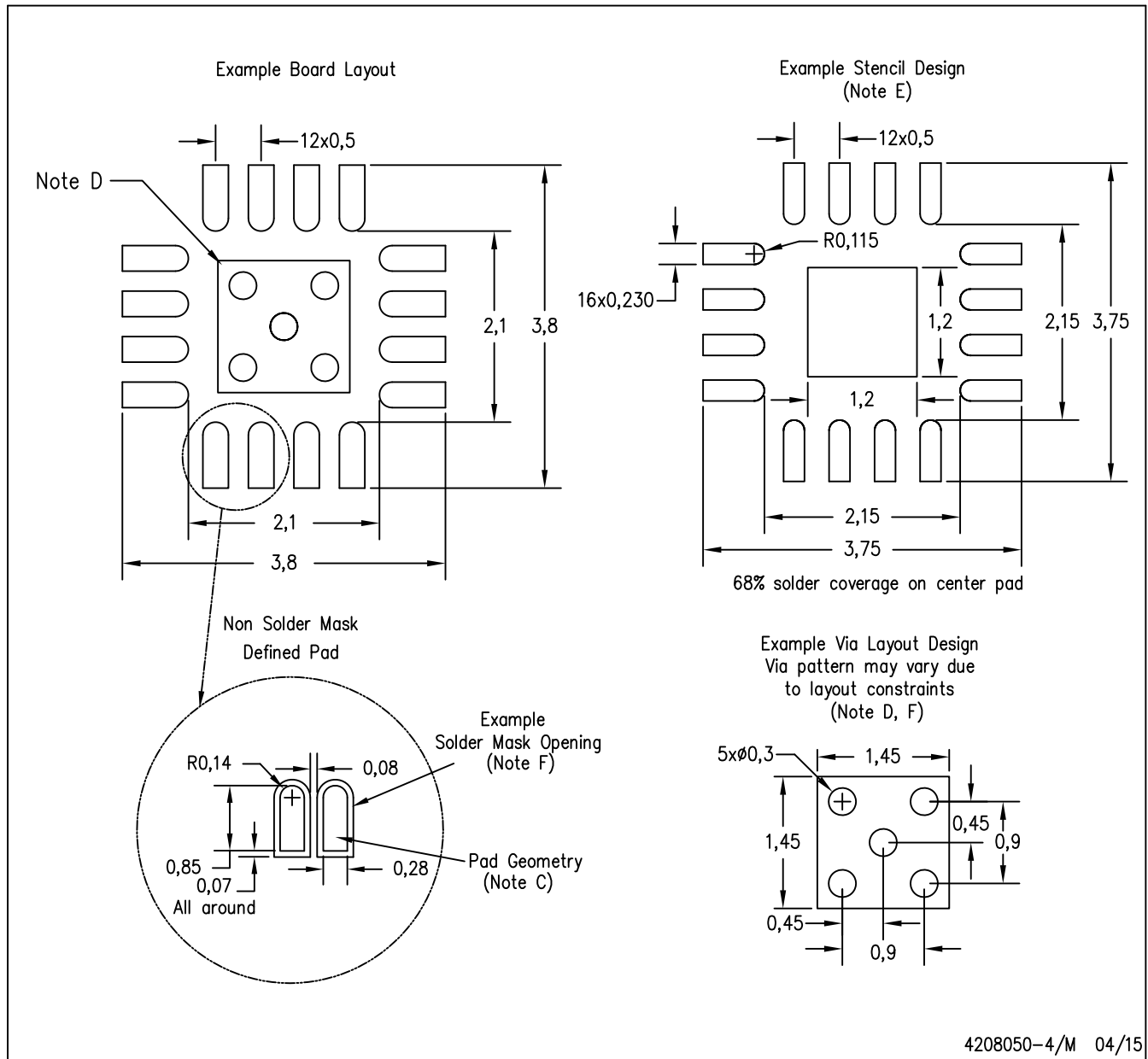
Exposed Thermal Pad Dimensions

4206349-2/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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