Low Quiescent Current Synchronous Boost DC-DC Controller with Wide V_{IN} Range

Check for Samples: TPS43060, TPS43061

FEATURES

- 58 V Maximum Output Voltage
- 4.5 V to 38 V (40 V Abs Max) V_{IN} Range
- TPS43060: 7.5 V Gate Drive Optimized for Standard Threshold MOSFETs
- TPS43061: 5.5 V Gate Drive Optimized for Low Qg NexFETs™
- Current-Mode Control with Internal Slope Compensation
- Adjustable Frequency from 50kHz to 1MHz
- Synchronization Capability to External Clock
- Adjustable Soft-Start Time
- Inductor DCR or Resistor Current Sensing
- Output Voltage Power-Good Indicator
- ±0.8% Feedback Reference Voltage
- 5 µA Shutdown Supply Current
- 600 µA Operating Quiescent Current
- Integrated Bootstrap Diode (TPS43061)
- Cycle-by-Cycle Current Limit and Thermal Shutdown
- Adjustable UVLO and Output Overvoltage Protection
- Small 16-Pin WQFN (3 mm x 3 mm) Package with PowerPAD™
- -40°C to 150°C Operating T_J Range

APPLICATIONS

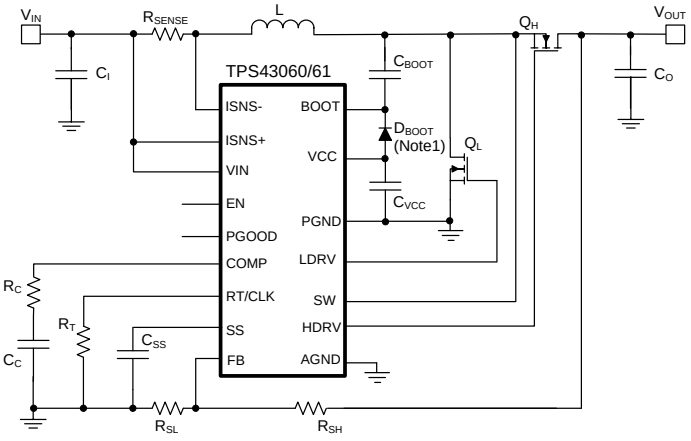
- Thunderbolt Port for PCs
- Automotive Power Systems
- Synchronous Flyback
- GaN RF Power Amplifiers
- Tablet Computer Accessories
- Battery Powered Systems
- 5 V, 12 V, and 24 V DC Bus Power Systems

DESCRIPTION

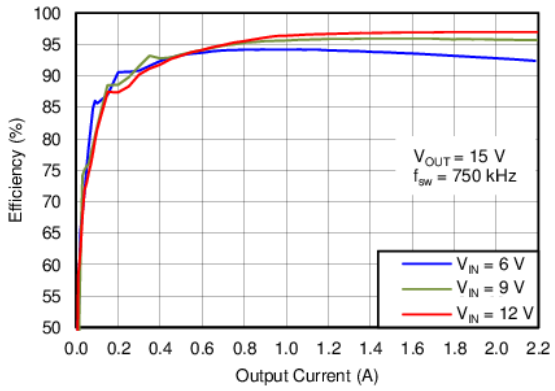
The TPS43060 and TPS43061 are low I_Q current-mode synchronous boost controllers with wide input voltage range from 4.5 V to 38 V (40 V abs max) and boosted output range up to 58 V. Synchronous rectification enables high efficiency for high current applications, and lossless inductor DCR sensing further improves efficiency. The resulting low power losses combined with a 3 mm x 3 mm WQFN-16 package with PowerPAD™ supports high power-density and high reliability boost converter solutions over extended (-40°C to 150°C) temperature range.

The TPS43060 includes a 7.5 V gate drive supply which is suitable to drive a broad range of MOSFETs. The TPS43061 has a 5.5 V gate drive supply and driver strength optimized for low Qg NexFET™. In addition, TPS43061 provides an integrated bootstrap diode for the high side gate driver to reduce external parts count.

SIMPLIFIED SCHEMATIC



Note 1: D_{BOOT} is required for TPS43060, but optional for TPS43061.



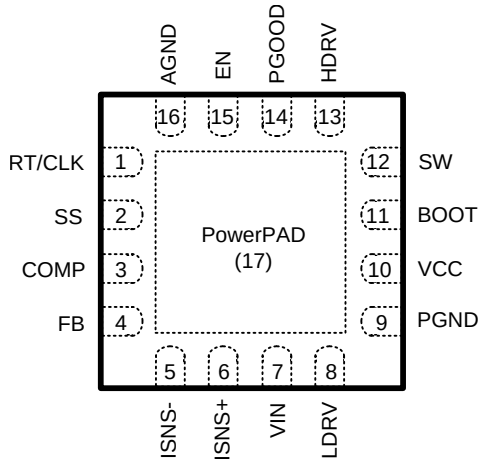
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFETs, PowerPAD are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

WQFN-16 PACKAGE
(TOP VIEW)



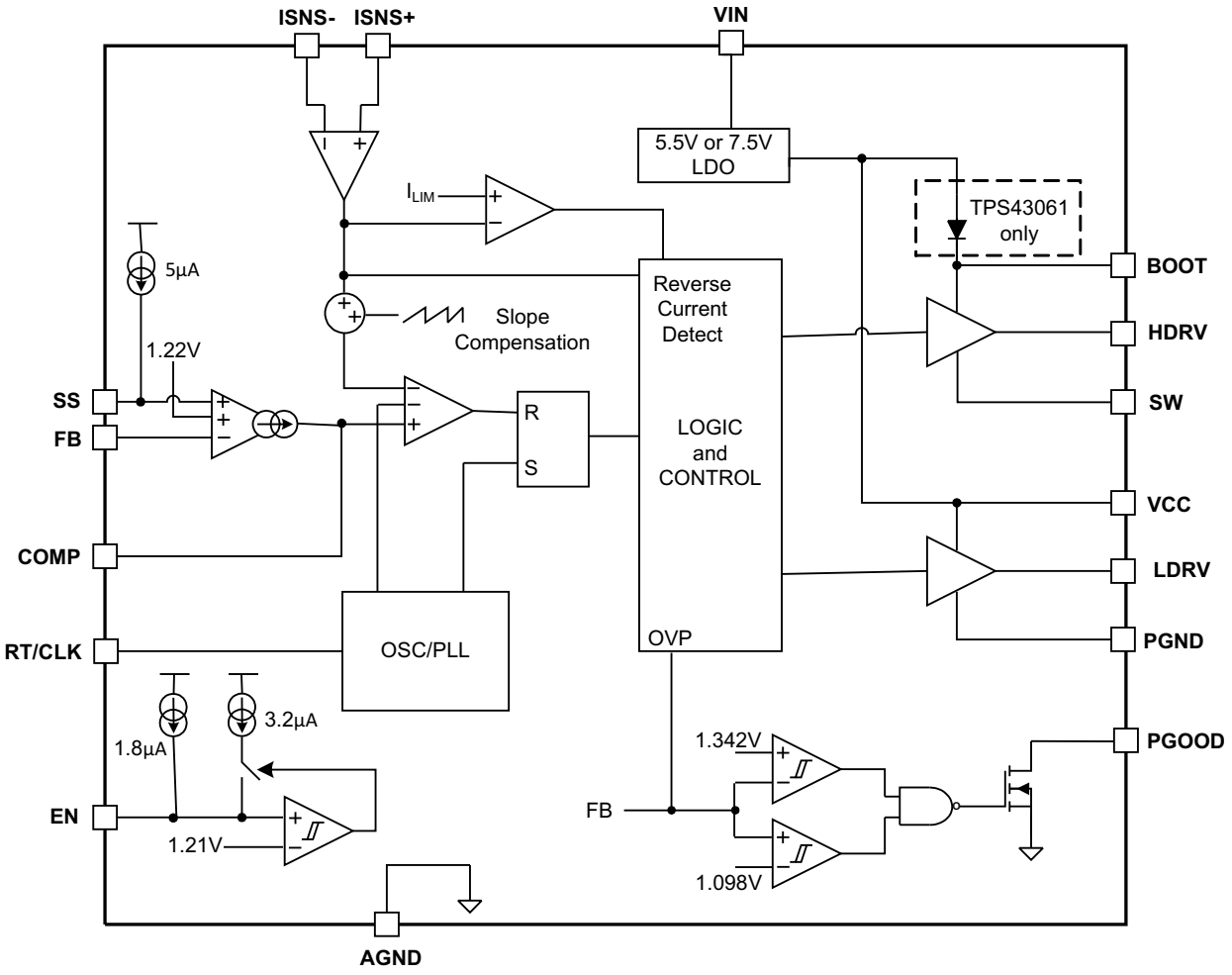
PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Resistor Timing and External Clock. An external resistor from this pin to the AGND pin programs the switching frequency between 50 kHz and 1MHz. Driving the pin with an external clock between 300 kHz to 1 MHz will synchronize the switching frequency to the external clock.
SS	2	Soft-start programming pin. A capacitor between the SS pin and AGND pin sets soft-start time.
COMP	3	Output of the internal transconductance error amplifier. The feedback loop compensation network is connected from this pin to AGND.
FB	4	Error amplifier input and feedback pin for voltage regulation. Connect this pin to the center tap of a resistor divider to set the output voltage.
ISNS-	5	Inductor current sense comparator inverting input pin. This pin is normally connected to the inductor side of the current sense resistor.
ISNS+	6	Inductor current sense comparator non-inverting input pin. This pin is normally connected to the VIN side of the current sense resistor.
VIN	7	The input supply pin to the IC. Connect VIN to a supply voltage between 4.5 V and 38 V. It is acceptable for the voltage on the VIN pin to be different from the boost power stage input, ISNS+ and ISNS- pins.
LDRV	8	Low side gate driver output. Connect this pin to the gate of the low side N-channel MOSFET. When VIN bias is removed, an internal 200 kΩ resistor pulls LDRV to PGND.
PGND	9	Power ground of the IC. Connect this pin to the source of the low-side MOSFET. PGND should be connected to AGND via a single point on printed circuit board.
VCC	10	Output of an internal LDO and power supply for internal control circuits and gate drivers. VCC is typically 7.5V for the TPS43060 and 5.5 V for the TPS43061. Connect a low ESR ceramic capacitor from this pin to PGND. The recommended capacitance range is from 0.47 µF to 10µF.
BOOT	11	Bootstrap capacitor node for high-side MOSFET gate driver. Connect the bootstrap capacitor from this pin to the SW pin. For the TPS43060, also connect a bootstrap diode from VCC to BOOT.
SW	12	Switching node of the boost converter. Connect this pin to the junction of the drain of the low side MOSFET, the source of high side synchronous MOSFET and the inductor.
HDRV	13	High side gate driver output. Connect this pin to the gate of the high side synchronous rectifier MOSFET. When VIN bias is removed, this pin is connected to SW through an internal 200 kΩ resistor.
PGOOD	14	Power good indicator. This pin is an open-drain output. A 10 kΩ pull-up resistor is recommended between PGOOD and VCC or an external logic supply pin.

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NAME	NO.	
EN	15	Enable pin with internal pull-up current source. Floating this pin will enable the IC. Pull below 1.2 V to enter low current standby mode. Pull below 0.4 V to enter shutdown mode. The EN pin can be used to implement adjustable undervoltage lockout (UVLO) using two resistors.
AGND	16	Analog signal ground of the IC. AGND should be connected to PGND at a single point on printed circuit board.
PowerPAD	17	The PowerPAD should be connected to AGND. If possible, use thermal vias to connect to an internal ground plane for improved power dissipation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage	Input: VIN, EN, ISNS+,ISNS-	-0.3	40	V
	DC Voltage: SW	-0.6	60	V
	Transient Voltage (10ns max): SW	-2	60	V
	FB, RT/CLK, COMP, SS	-0.3	3.6	V
	BOOT, HDRV Voltage with Respect to Ground		65	V
	BOOT, HDRV Voltage with Respect to SW Pin		8	V
	VCC, PGOOD, LDRV	-0.3	8	V
Electrostatic Discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CDM) QSS 009-147 (JESD22-C101B.01)		500	V
Operating Junction Temperature Range		-40	+150	°C
Storage Temperature Range		-65	+150	°C

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		WQFN (16-PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	65.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	42.3	
θ_{JB}	Junction-to-board thermal resistance	18	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	17.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	22.7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	4.5		38	V
V_{OUT}	Output voltage range	V_{IN}		58	V
V_{EN}	EN voltage range	0		38	V
V_{CLK}	External switching frequency logic input range	0		3.6	V
T_J	Operating junction temperature	-40		+150	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 4.5 to 38 V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = 25ºC

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY AND ENABLE							
V_{IN}	Input voltage range			4.5		38	V
V_{UV}	Input undervoltage threshold		V_{IN} falling	3.7	3.9	4	V
			V_{IN} rising	3.9	4.1	4.3	V
V_{hys}	Undervoltage lockout hysteresis				200		mV
I_Q	Operating quiescent current into V_{IN}		Device non-switching, R_T = 115 kΩ, V_{FB} = 2 V		600	800	µA
I_{SD}	Shutdown current		V_{EN} = 0.4V		1.5	5	µA
V_{EN}	EN pin voltage threshold to standby		V_{EN} ramping down	0.4	0.7	0.9	V
	EN pin voltage threshold to enable the device		V_{EN} ramping up	1.12	1.21	1.29	V
	EN pin voltage threshold to disable the device		V_{EN} ramping down	1	1.14	1.28	V
I_{EN}	EN pin pull-up current		V_{EN} = 1 V		1.8		µA
	EN pin hysteresis current		V_{EN} = 1. 3V		3.2	4.6	µA
t_{EN}	EN to start switching time		C_{VCC} = 0.47 µF		125		µs
V_{CC}	V_{CC} voltage	TPS43060	V_{IN} = 12 - 38 V, I_{VCC} = 0 µA		7.5		V
			V_{IN} = 4.5 V, I_{VCC} = 0 µA		4.5		V
		TPS43061	V_{IN} = 12 - 38 V, I_{VCC} = 0 µA		5.5		V
			V_{IN} = 4.5 V, I_{VCC} = 0 µA		4.5		V
I_{VCC}	V_{CC} pin maximum output current			50			mA
VOLTAGE REFERENCE AND ERROR AMPLIFIER							
V_{REF}	Feedback Voltage Reference		T_J = 25°C	1.21	1.22	1.23	V
			T_J = -40°C to 150°C	1.195	1.22	1.244	
I_{FB}	Error Amplifier input bias current				20		nA
I_{COMP}	COMP pin sink current		V_{FB} = V_{REF} + 250 mV, V_{COMP} = 1.5 V		160		µA
	COMP pin source current		V_{FB} = V_{REF} - 250 mV, V_{COMP} = 1.5 V		160		µA
V_{CLAMP}	COMP pin clamp voltage		High clamp, V_{FB} = 1V		2.1		V
			Low clamp, V_{FB} = 1.5 V		0.7		
	COMP pin threshold		Duty cycle = 0%		1		V
G_{ea}	Error amplifier transconductance				1.1		m-mho
R_{ea}	Error amplifier output resistance				10		MΩ
F_{ea}	Error amplifier crossover frequency				2		MHz
CURRENT SENSE							
V_{CSmax}	Maximum current sense threshold		At 0% Duty Cycle	64	73	82	mV
	Maximum current sense threshold		At Max Duty Cycle	50	61	72	mV
V_{RCsns}	Reverse current sense threshold				3.8		mV
I_{SNS+}	Sense+ pin current				70		µA
I_{SNS-}	Sense- pin current				70		µA
RT/CLK							
f_{SW}	Switching frequency		Operating frequency range using resistor timing mode	50		1000	kHz
			R_T = 115 kΩ	450	500	550	kHz
			R_T = 75 kΩ	675	750	825	kHz
$V_{RT/CLK}$	RT/CLK pin voltage				0.5		V
$t_{CLK-min}$	Minimum input clock pulse width		P_{LL} = 500 kHz		14	60	ns

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 4.5 to 38 V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = 25ºC

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
v_{CLK-H}	RT/CLK high threshold				1.78	2	V
f_{CLK}	RT/CLK low threshold			0.4	1.35		V
	PLL frequency sync range			300		1000	kHz
t_{PLLIN}	PLL lock in time				100	250	µs
$t_{PLLEXIT}$	Last RT/CLK falling edge to return to resistor timing mode if CLK is not present				140	250	µs
POWER SWITCH DRIVERS							
R_{LDRV}	LDRV pull-up resistance	TPS43060	V_{IN} = 12 V - 40 V		2		Ω
			V_{IN} = 4.5 V		3		
		TPS43061	V_{IN} = 12 V - 40 V		2.5		Ω
			V_{IN} = 4.5 V		3		
	LDRV pull-down resistance	TPS43060	V_{IN} = 12 V - 40 V		1.2		Ω
			V_{IN} = 4.5 V		2		
		TPS43061	V_{IN} = 12 V - 40 V		1.6		Ω
			V_{IN} = 4.5 V		2		
R_{HDRV}	HDRV pull-up resistance	TPS43060	V_{IN} = 12 V - 40 V		2		Ω
			V_{IN} = 4.5 V		2.8		
		TPS43061	V_{IN} = 12 V - 40 V		5		Ω
			V_{IN} = 4.5 V		5.5		
	HDRV pull-down resistance	TPS43060	V_{IN} = 12 V - 40 V		1.2		Ω
			V_{IN} = 4.5 V		1.9		
		TPS43061	V_{IN} = 12 V - 40 V		3		Ω
			V_{IN} = 4.5 V		3.7		
t_{HR}	High side gate rise time, 10% to 90%	TPS43060	C_{LOAD} = 2.2 nF, V_{IN} = 12 V - 40 V		15		ns
		TPS43061			20		
t_{HF}	High side gate fall time, 90% to 10%	TPS43060	C_{LOAD} = 2.2 nF, V_{IN} = 12 V - 40 V		10		ns
		TPS43061			15		
t_{LR}	Low side gate rise time, 10% to 90%	TPS43060	C_{LOAD} = 2.2 nF, V_{IN} = 12 V - 40 V		15		ns
		TPS43061			20		
t_{LF}	Low side gate fall time, 90% to 10%	TPS43060	C_{LOAD} = 2.2 nF, V_{IN} = 12 V - 40 V		10		ns
		TPS43061			15		
V_F	BOOT diode forward voltage drop	TPS43061	I_F = 10 mA, T_A = 25ºC		0.75		V
I_{BOOT}	BOOT pin leakage current	TPS43061	V_r = 60 V		0.1		µA
t_{ON}	LDRV minimum on pulse width		f_{SW} = 500 kHz		100		ns
t_{OFF}	LDRV minimum off pulse width		f_{SW} = 500 kHz		250		ns
t_{delay}	Time delay between LDRV fall(50%) to HDRV rise (50%), $t_{non-overlap1}$	TPS43060, C_{LOAD} = open, f_{SW} = 500 kHz	V_{IN} = 12V		65		ns
			V_{IN} = 4.5V		75		ns
		TPS43061, C_{LOAD} = open, f_{SW} = 500 kHz	V_{IN} = 12V		65		ns
			V_{IN} = 4.5V		75		ns
	Time delay between HDRV fall (50%) to LDRV rise (50%), $t_{non-overlap2}$	TPS43060, C_{LOAD} = open, f_{SW} = 500 kHz	V_{IN} = 12V		65		ns
			V_{IN} = 4.5V		75		ns
		TPS43061, C_{LOAD} = open, f_{SW} = 500 kHz	V_{IN} = 12V		65		ns
			V_{IN} = 4.5V		75		ns

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 4.5 to 38 V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = 25ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD, SS AND OVP						
P_{GDL}	PGOOD low threshold	V_{FB} with respect to Feedback Voltage Reference, V_{FB} falling	86%	90%	93%	
	PGOOD low hysteresis	V_{FB} with respect to Feedback Voltage Reference		2%		
P_{GDH}	PGOOD high threshold	V_{FB} with respect to Feedback Voltage Reference, V_{FB} rising	107%	110%	114%	
	PGOOD high hysteresis	V_{FB} with respect to Feedback Voltage Reference		2%		
P_{GDSC}	PGOOD sink current	V_{PGOOD} = 0.4 V	1.8	4		mA
P_{GDLK}	PGOOD pin leakage current	V_{PGOOD} = 7 V		100		nA
V_{IN_PGD}	Minimum V_{IN} for valid PGOOD			2.5	4.3	V
I_{SS}	Soft-start bias current	V_{SS} = 0 V		5		µA
R_{SS}	Soft-start discharge resistance			250		Ω
V_{OVP}	OVP threshold	V_{FB} with respect to Feedback Voltage Reference, V_{FB} rising	104%	107%	110%	
	OVP hysteresis	V_{FB} with respect to Feedback Voltage Reference		2%		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown set threshold			165		°C
T_{hyst}	Thermal shutdown hysteresis			15		°C

TYPICAL CHARACTERISTICS

V_{IN} = 12 V, f_{SW} = 500 kHz, T_A = 25ºC (unless otherwise noted)

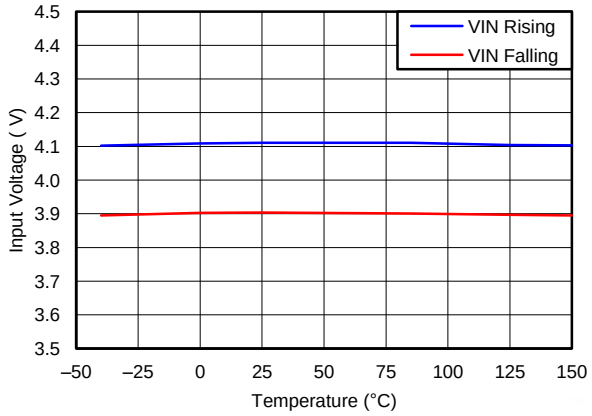


Figure 1. Input Start and Stop Voltage vs Temperature

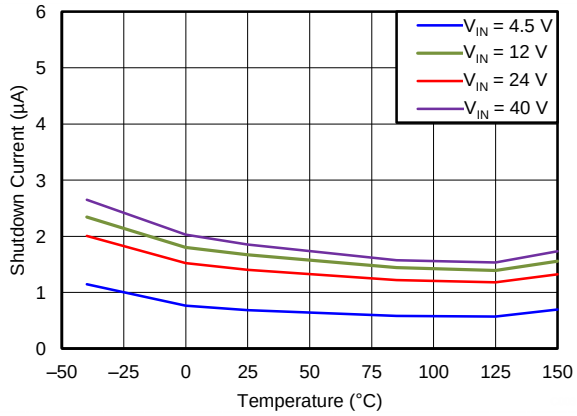


Figure 2. Shutdown Supply Current vs Temperature

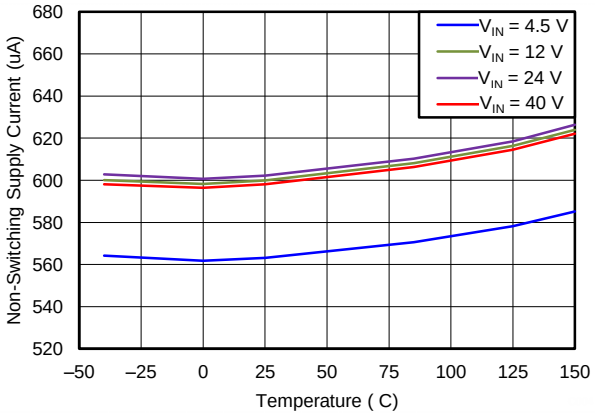


Figure 3. Non-Switching Supply Current vs Temperature

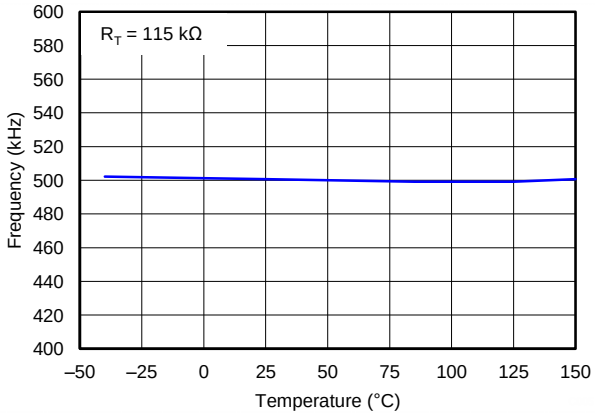


Figure 4. Frequency vs Temperature

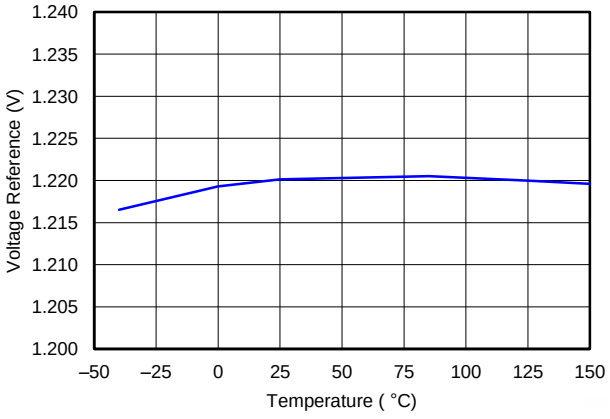


Figure 5. Feedback Voltage Reference vs Temperature

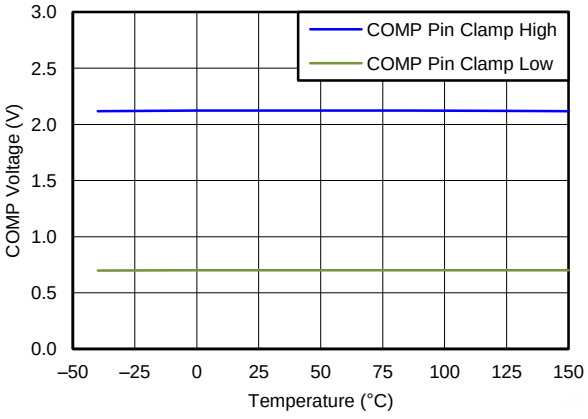


Figure 6. COMP Clamp Voltage vs Temperature

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, f_{SW} = 500 kHz, T_A = 25ºC (unless otherwise noted)

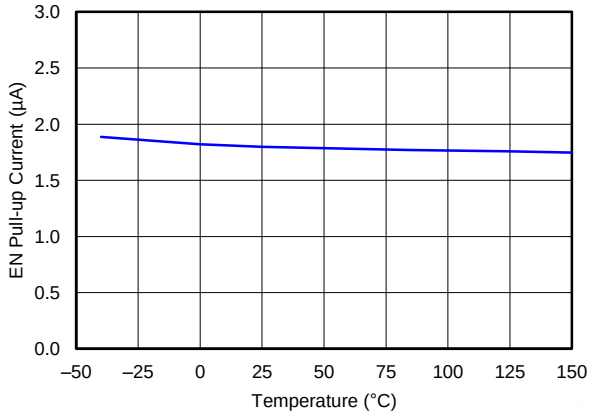


Figure 7. EN Pull-Up Current vs Temperature

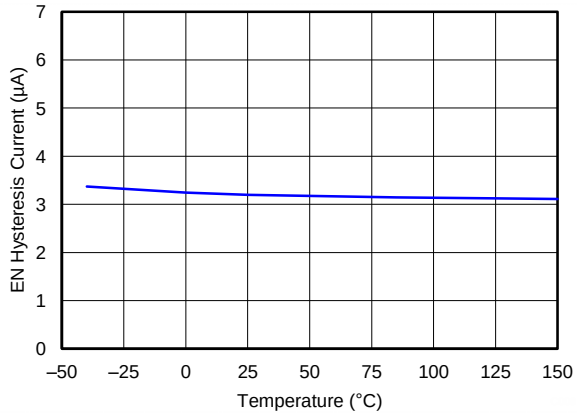


Figure 8. EN Hysteresis Current vs Temperature

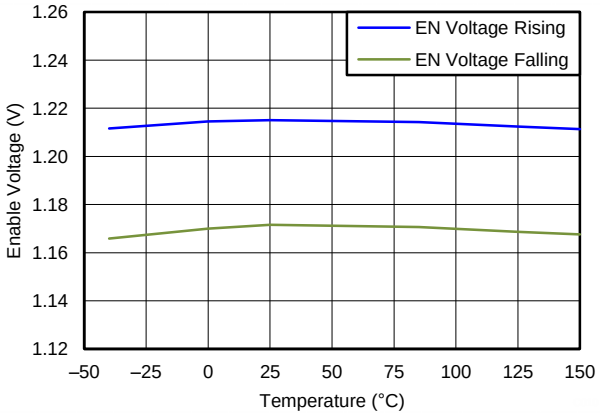


Figure 9. Enable Threshold vs Temperature

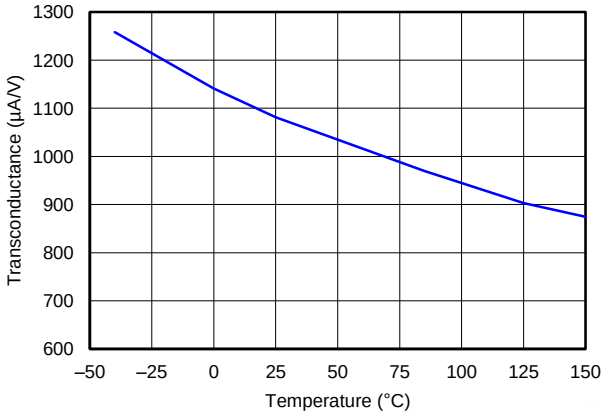


Figure 10. Error Amplifier Transconductance vs Temperature

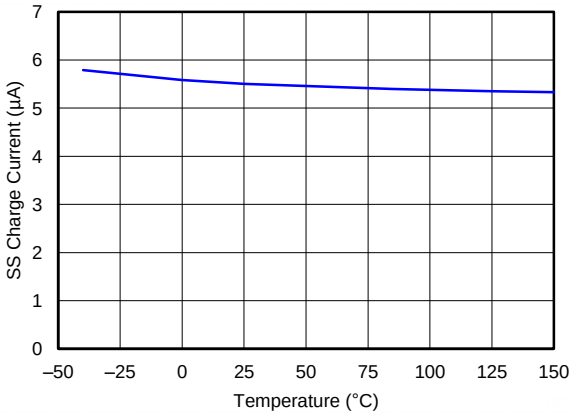


Figure 11. SS Charge Current vs Temperature

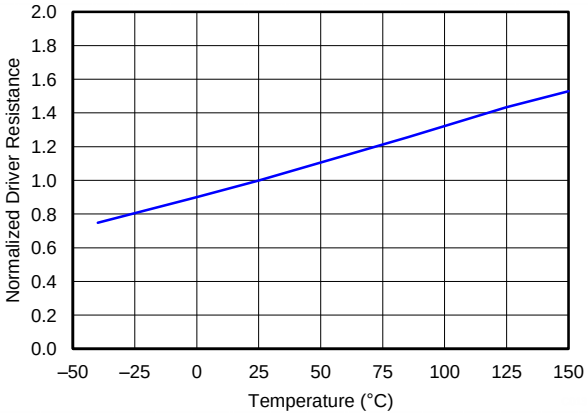


Figure 12. Gate Driver Output Resistance vs Temperature

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, f_{SW} = 500 kHz, T_A = 25ºC (unless otherwise noted)

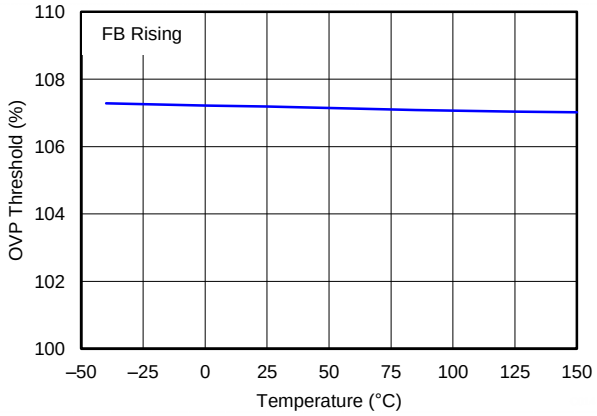


Figure 13. OVP Threshold vs Temperature

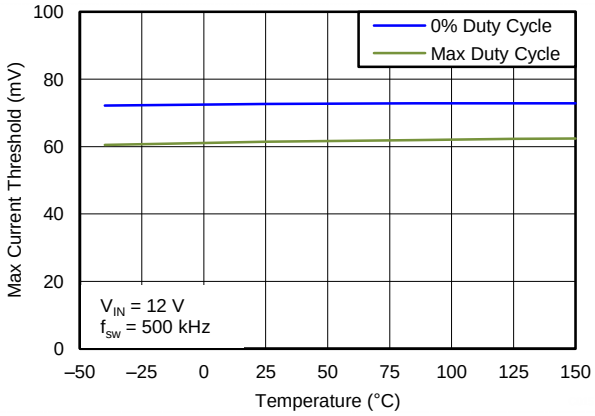


Figure 14. Maximum Current Sense Threshold vs Temperature

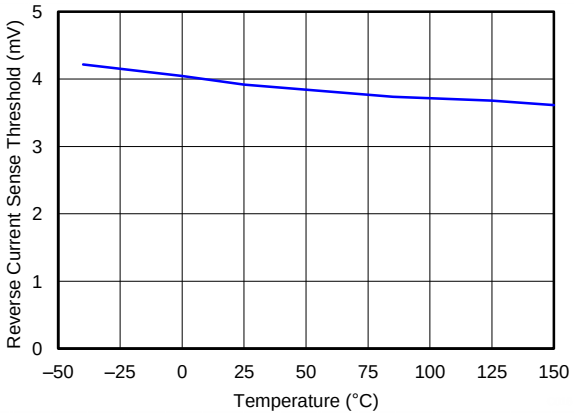


Figure 15. Reverse Current Sense Threshold vs Temperature

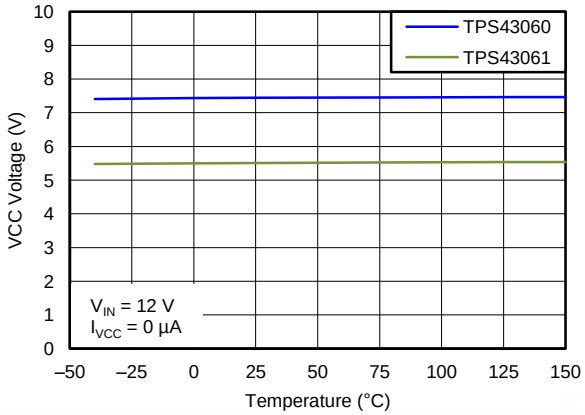


Figure 16. VCC Voltage vs Temperature

DETAILED DESCRIPTION

OPERATION

The TPS43060 and TPS43061 are high-performance wide input range synchronous boost controllers that accept a 4.5 V to 38 V (40 V abs max) input and support output voltages up to 58 V. The devices have gate drivers for both the low side N-channel MOSFET and the high side synchronous rectifier N-channel MOSFET. Voltage regulation is achieved employing constant frequency current mode pulse width modulation (PWM) control. The switching frequency is set either by an external timing resistor or by synchronizing to an external clock signal. The switching frequency is programmable from 50 kHz to 1 MHz in the resistor programmed mode or can be synchronized to an external clock between 300 kHz to 1 MHz.

The PWM control circuitry turns on the low side MOSFET at the beginning of each oscillator clock cycle, as the error amplifier compares the output voltage feedback signal at the FB pin to the internal 1.22 V reference voltage. The low side MOSFET is turned-off when the inductor current reaches a threshold level set by the error amplifier output. After the low side MOSFET is turned off, the high side synchronous MOSFET is turned on until the beginning of the next oscillator clock cycle or until the inductor current reaches the reverse current sense threshold. The input voltage is applied across the inductor and stores the energy as inductor current ramps up during the portion of the switching cycle when the low side MOSFET is on. Meanwhile the output capacitor supplies load current. When the low side MOSFET is turned off by the PWM controller, the inductor transfers stored energy via the synchronous MOSFET to replenish the output capacitor and supply the load current. This operation repeats every switching cycle.

The devices feature internal slope compensation to avoid sub-harmonic oscillation that is intrinsic to peak current mode control at duty cycles higher than 50%. They also feature adjustable soft-start time, optional lossless inductor DCR current sensing, an output power good indicator, cycle-by-cycle current limit and over-temperature protection.

SWITCHING FREQUENCY

The switch frequency is set by a resistor (RT) connected to the RT/CLK pin of the TPS43060 and TPS43061. The relationship between the timing resistance RT and frequency is shown in the Figure 17. The resistor value required for a desired frequency can be calculated using Equation 1.

$$R_T(k\Omega) = \frac{57500}{f_{sw}(kHz)} \quad (1)$$

Figure 17. Frequency vs RT Resistance

The device switching frequency can be synchronized to an external clock that is applied to the RT/CLK pin. The external clock should be in the range of 300 kHz to 1 MHz. The required logic levels of the external clock are shown in the specification table. The pulse width of the external clock should be greater than 20ns to ensure proper synchronization. A resistor between 57.5 kΩ and 1150 kΩ must always be connected from the RT/CLK pin to ground when the converter is synchronized to an external clock. Do not leave this pin open.

LOW DROPOUT REGULATOR

The TPS43060 and TPS43061 contain a low dropout regulators that provides bias supply for the controller and the gate driver. The output of the LDO of TPS43060 and TPS43061 are regulated to 7.5 V and 5.5 V, respectively. When the input voltage is below the V_{CC} regulation level the V_{CC} output tracks V_{IN} with a small dropout voltage. The output current of the V_{CC} regulator should not exceed 50 mA. The value of the V_{CC} capacitance depends on the total system design, and its startup characteristics. The recommended range of values for the V_{CC} capacitor is from 0.47 µF to 10 µF.

INPUT UNDERVOLTAGE (UV)

An undervoltage detection circuit prevents mis-operation of the device at input voltages below 3.9 V (typical). When the input voltage is below the VIN UV threshold, the internal PWM control circuitry and gate drivers are turned off. The threshold is set below minimum operating voltage of 4.5 V to ensure that a transient VIN dip will not cause the device to reset. For input voltages between the UV threshold and 4.5 V, the device attempts to operate, but the electrical specifications are not ensured. The EN pin can be used to achieve adjustable UVLO if the desired start-up threshold is higher than 3.9 V. Details are provided in the following section.

ENABLE AND ADJUSTABLE UNDERVOLTAGE LOCKOUT (UVLO)

The EN pin voltage must be greater than 1.21 V (typical) to enable TPS43060 and TPS43061. The device enters a shutdown mode when the EN voltage is less than 0.4 V. In shutdown mode, the input supply current for the device is less than 5 µA. The EN pin has an internal 1.8 µA pull-up current source that provides the default enabled condition when the EN pin floats. When the EN pin voltage is higher than the shutdown threshold but less than 1.21 V, the devices are in standby mode.

Adjustable input UVLO can be accomplished using the EN pin. As shown in Figure 18, a resistor divider from the VIN pin to AGND sets the UVLO level. Once EN pin voltage crosses the 1.21 V (typical) threshold voltage an additional 3.2 µA hysteresis current is sourced out of the EN pin. When EN pin voltage falls below 1.14 V (typical), the hysteresis current is removed. The addition of hysteresis current at the EN threshold facilitates adjustable input voltage hysteresis. R_{UVLO_H} and R_{UVLO_L} are calculated using Equation 2 and Equation 3 respectively.

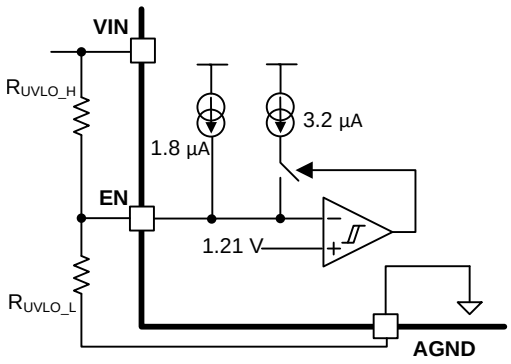


Figure 18. Adjustable UVLO using EN pin

$$R_{UVLO\_H} = \frac{V_{START} \times \left(\frac{V_{EN\_DIS}}{V_{EN\_ON}} \right) - V_{STOP}}{I_{EN\_pup} \times \left(1 - \frac{V_{EN\_DIS}}{V_{EN\_ON}} \right) + I_{EN\_hys}} \quad (2)$$

$$R_{UVLO\_L} = \frac{R_{UVLO\_H} \times V_{EN\_DIS}}{V_{STOP} - V_{EN\_DIS} + R_{UVLO\_H} \times \left(I_{EN\_pup} + I_{EN\_hys} \right)} \quad (3)$$

Where

- V_{START} is the desired turn-on voltage at the VIN pin

- V_{STOP} is the desired turn-off voltage at the VIN pin
- V_{EN_ON} is EN pin voltage threshold to enable the device, 1.21V (typical)
- V_{EN_DIS} is EN pin voltage threshold to disable the device, 1.14V (typical)
- I_{EN_hys} is the hysteresis current inside the device, 3.2µA (typical)
- I_{EN_pup} is the internal pull-up current at EN pin, 1.8µA (typical)

VOLTAGE REFERENCE AND SETTING OUTPUT VOLTAGE

An internal voltage reference provides a precise 1.22 V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor R_{SH} and R_{SL} according to Equation 4.

$$V_{OUT} = 1.22V \times \left(\frac{R_{SH}}{R_{SL}} + 1 \right) \tag{4}$$

MINIMUM ON-TIME AND PULSE SKIPPING

The TPS43060 and TPS43061 also feature a minimum on-time of 100 ns for the low-side gate driver. This minimum on-time determines the minimum duty cycle of the PWM for any set switching frequency. When the voltage regulation loop requires a minimum on-time pulse width less than 100 ns, the controller enters pulse-skipping mode. In this mode, the devices hold the power switch off for multiple switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the DC-DC converter operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in Figure 27.

ZERO-CROSS-DETECTION and DUTY CYCLE

The TPS43060 and TPS43061 feature zero-cross-detection which turns off high side driver when the sensed current falls below the reverse current sense threshold (3.8 mV typical), then the converter runs in discontinuous conduction mode (DCM). The duty cycle is dependent on the mode in which the converter is operating. The duty cycle in DCM varies widely with changes of the load. In CCM, where the inductor maintains a minimum dc current, the duty cycle is related primarily to the input and output voltages as computed in Equation 5.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

When the converter operates in DCM, the duty cycle is a function of the load, input and output voltages, inductance and switching frequency in Equation 6.

$$D = \frac{2 \times V_{OUT} \times I_{OUT} \times L \times f_{SW}}{V_{IN}^{\ 2}} \tag{6}$$

Equation 5 and Equation 6 provide an estimation of the duty cycle. A more accurate duty cycle can be calculated by including the voltage drops of the external MOSFETs, sense resistor and DCR of the inductor.

MINIMUM OFF-TIME and MAXIMUM DUTY CYCLE

The low side driver LDRV of TPS43060 and TPS43061 has a minimum off-time of 250 ns or 5% of the switching cycle period whichever is longer. Figure 19 shows Maximum duty cycle vs. Switching Frequency. The maximum duty cycle limits the maximum achievable step-up ratio in a Boost converter. When the converter operates in CCM, the step-up ratio of the boost converter can be calculated using Equation 7.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \tag{7}$$

For instance, if the maximum duty cycle is 90%, the achievable maximum output voltage to input voltage ratio is limited to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - 90\%} = 10 \tag{8}$$

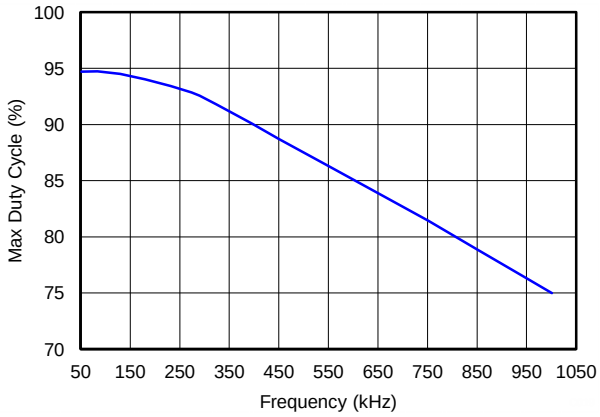


Figure 19. Maximum Duty Cycle vs Frequency

SOFT-START

The TPS43060 and TPS43061 have a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (5 µA typical) charges the capacitor (C_{SS}) on the SS pin. When the SS pin voltage is less than the internal 1.22 V reference, the device regulates the FB pin voltage to the SS pin voltage rather than the internal 1.22 V reference voltage. Once the SS pin voltage exceeds the reference voltage the device regulates the FB pin voltage to 1.22V. The soft-start time of the output voltage can be calculated using Equation 9.

$$t_{ss} = C_{ss} \frac{1.22V}{5\mu A} \tag{9}$$

POWER GOOD

The TPS43060 and TPS43061 PGOOD pin indicates when the output voltage is within pre-determined limits of the desired regulated output voltage by monitoring the FB pin voltage. The PGOOD pin is driven by the open-drain signal of an internal MOSFET. When the output voltage of the power converter is not within ±10% of the output voltage set point, the PGOOD MOSFET turns on and pulls the PGOOD pin low. Otherwise, the PGOOD MOSFET stays off and the PGOOD pin can be pulled up by an external resistor to a voltage supply up to 8V.

OVERVOLTAGE PROTECTION

The TPS43060 and TPS43061 integrate an overvoltage protection (OVP) circuit that turns off the low side MOSFET when the output voltage reaches the OVP threshold which is internally fixed to 107% of the output voltage set point. The low side MOSFET resumes normal PWM control when the output voltage drops below 105% of the output voltage set point. The OVP circuit protects the power MOSFETs and minimizes the output voltage overshoot during transients or fault conditions.

OVERCURRENT PROTECTION AND CURRENT SENSE RESISTOR SELECTION

The TPS43060 and TPS43061 provide cycle-by-cycle current limit protection that turns off the low side MOSFET when the inductor current reaches the current limit threshold. The cycle-by-cycle current limit circuitry is reset at the beginning of the next switching cycle. During an overcurrent event, the output voltage begins to droop as a function of the load on the output.

A slope compensation ramp is added to the current sense ramp to prevent sub-harmonic oscillations at high duty cycle. The slope compensation reduces the overcurrent limit threshold (maximum current sense threshold) with increasing duty cycle as detailed in Figure 20.

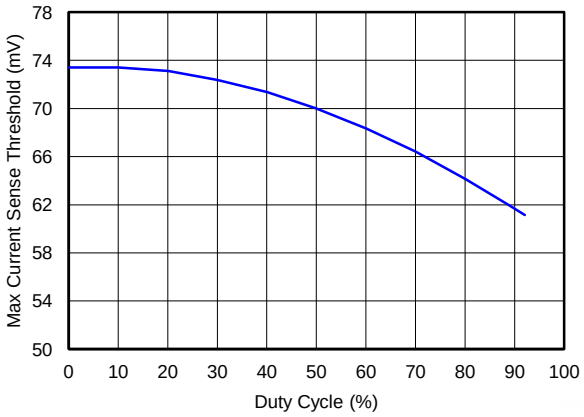


Figure 20. OverCurrent Limit Threshold with Respect to Duty Cycle

The maximum current sense threshold V_{CSmax} sets the maximum peak inductor current which is the sum of maximum average inductor (input) current I_{ave_max} and half the peak-to-peak inductor ripple ΔI_L. The sense resistor value should be chosen based on the desired maximum input current and the ripple current, and can be calculated using Equation 10.

$$R_{SENSE} = \frac{V_{CS\,max}}{I_{ave\_max} + \frac{\Delta I_L}{2}} \tag{10}$$

GATE DRIVERS

The TPS43060 and TPS43061 contain powerful high-side and low-side gate drivers supplied by the V_{CC} bias regulator. The nominal V_{CC} voltage of the TPS43060 and TPS43061 is 7.5 V and 5.5 V respectively. The TPS43061 gate drivers operate from a 5.5 V V_{CC} supply, with drive strength optimized for low Qg NexFETs™. It also features an integrated bootstrap diode for the high side gate driver to reduce the external part count. The TPS43060 gate drivers operate from a 7.5 V V_{CC} supply, which is suitable to drive a wide range of standard MOSFETs. The TPS43060 requires an external bootstrap diode from VCC to BOOT to charge the bootstrap capacitor. It also requires a 2Ω resistor connected in series with the VCC pin to limit the peak current drawn through the internal circuitry when the external bootstrap diode is conducting. See the ELECTRICAL CHARACTERISTICS table for typical rise and fall times and the output resistance of the gate drivers.

The LDRV and HDRV outputs are controlled with an adaptive dead-time control that ensures that both the outputs are never high at the same time. This minimizes any cross conduction and protects the power converter. The typical dead-time from LDRV fall to HDRV rise is 65 ns.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the TPS43060 and TPS43061 when the junction temperature exceeds the thermal shutdown threshold (165°C typical). The device will restart when the junction temperature drops by 15°C.

DESIGN GUIDE – TPS43061 STEP-BY-STEP DESIGN PROCEDURE

The following section provides a step-by-step design guide of a high-frequency, high-power-density synchronous boost converter with the TPS43061 controller combined with a NexFET™ power block. This design procedure is also applicable to the TPS43060. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. For this example, we will start with the following known parameters.

Table 1. Key Parameters of the Boost Converter Example

Input voltage (V_{IN})	6 V to 12.6 V, 9 V nominal
Output voltage (V_{OUT})	15 V
Maximum output current (I_{OUT})	2 A
Transient response to 0.5 A to 1.5 A load step (ΔV_{OUT})	4% of V_{OUT} = 0.6 V
Output voltage ripple (V_{RIPPLE})	0.5% of V_{OUT} = 0.075 V
Start input voltage (V_{START})	5.34 V
Start input voltage (V_{STOP})	4.3 V

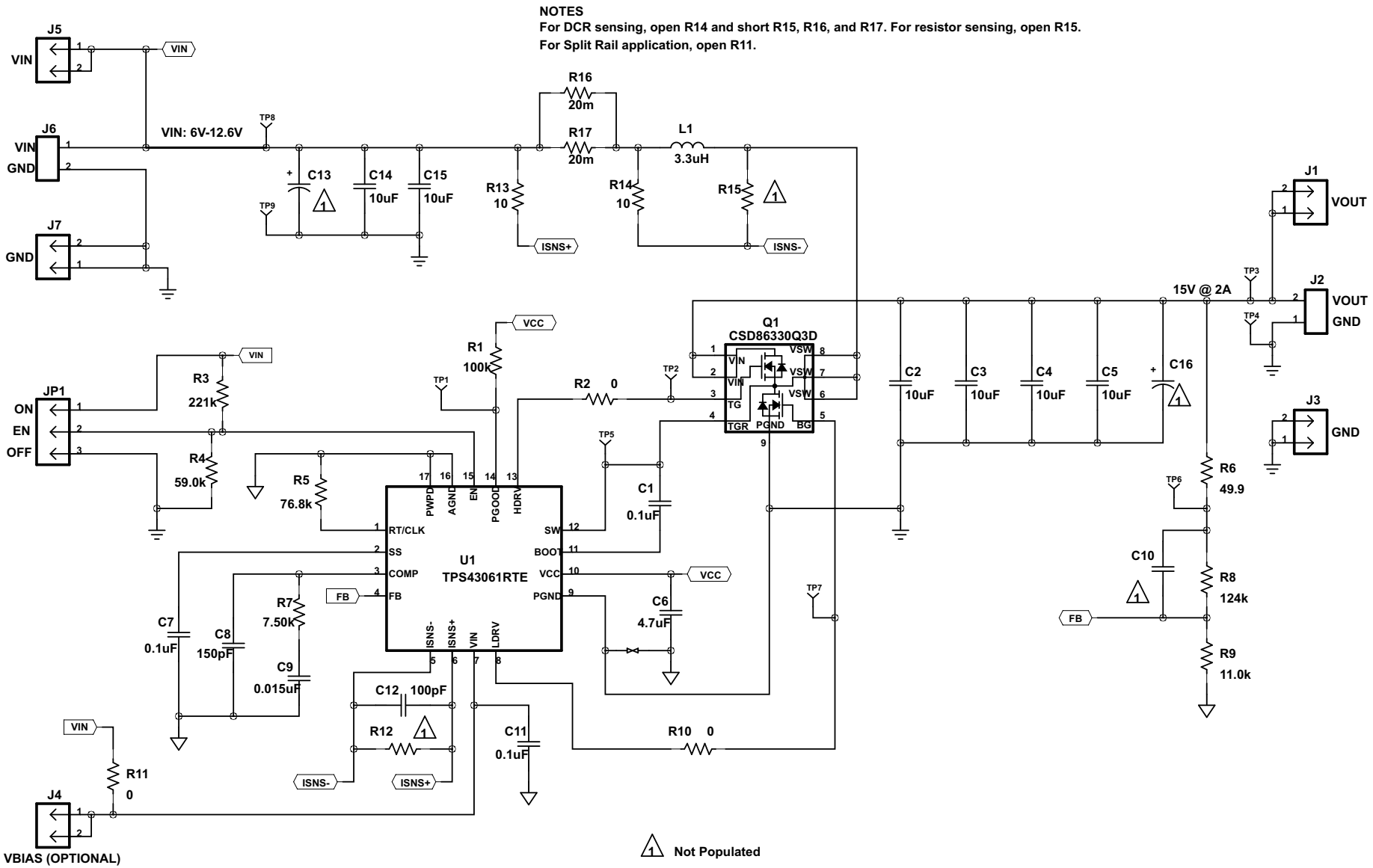


Figure 21. The Schematic of Synchronous Boost Converter using TPS43061

SELECTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency of the power converter. There are tradeoffs to consider when selecting a higher or lower switching frequency. Typically, the designer uses the highest switching frequency possible since this results in the smallest solution size. A higher switching frequency allows for lower value inductors and smaller output capacitors compared to a power converter that switches at a lower frequency. A lower switching frequency will produce a larger solution size but typically has a better efficiency. Setting the frequency for the minimum tolerable efficiency will produce the optimum solution size for the application.

The switching frequency can also be limited by the minimum on-time and off-time of the controller based on the input voltage and the output voltage of the application. To determine the maximum allowable switching frequency, first estimate the continuous conduction mode (CCM) duty cycle using Equation 11 with the minimum and maximum input voltages. Equation 12 and Equation 13 should then be used to calculate the upper limit of switching frequency for the regulator. Choose the lower value result from these two equations. Switching frequencies higher than the calculated values will result in either pulse skipping if the minimum on-time restricts the duty cycle or insufficient boost output voltage if the PWM duty cycle is limited by the minimum off-time.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{11}$$

$$f_{SW}ontime = \frac{D\min}{ton\min} = \frac{20\%}{100ns} = 2MHz \tag{12}$$

$$f_{SW}offtime = \frac{(1 - D\max)}{toffmin} = \frac{(1 - 60\%)}{250ns} = 1.6MHz \tag{13}$$

The typical minimum on-time and off-time of the device are 100 ns and 250 ns respectively. For this design, the duty cycle is estimated at 20% and 60% with the maximum input voltage and minimum input voltage respectively. When operating at switching frequencies less than 200 kHz the minimum off time starts to increase and is equal to 5% the switching period. The estimated allowed maximum switching frequency based on Equation 12 and Equation 13 is 1.6 MHz. When operating near the estimated maximum duty cycle more accurate estimations of the duty cycle should be made by including the voltage drops of the external MOSFETs, sense resistor and DCR of the inductor.

A switching frequency of 750 kHz is chosen as a compromise between efficiency and small solution size. To determine the timing resistance for a given switching frequency use either Equation 14 or the curve in Figure 17. The switching frequency is set by resistor R5 shown in Figure 21. For 750 kHz operation, the closest standard value resistor is 76.8 kΩ.

$$R_T(k\Omega) = \frac{57500}{f_{SW}(kHz)} = \frac{57500}{750(kHz)} = 76.7k\Omega \tag{14}$$

INDUCTOR SELECTION

The selection of the inductor affects the steady-state operation as well as transient behavior and loop stability. These factors make it an important component in a switching power supply design. The three most important inductor specifications to consider are inductor value, DC resistance (DCR), and saturation current rating. Let the parameter K_{IND} represent the ratio of inductor peak-peak ripple current to the average inductor current. In a boost topology the average inductor current is equal to the input current. The current delivered to the output is the input current modulated at the duty cycle of the PWM. The inductor ripple current contributes to the output current ripple that must be filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor. The value of K_{IND} in the design using low ESR output capacitors, such as ceramics, can be relatively higher than that in the design using higher ESR output capacitors. Higher values of K_{IND} lead to discontinuous mode (DCM) operation at moderate to light loads.

To calculate the minimum value of the output inductor, use Equation 16 or Equation 17. In a boost topology maximum current ripple occurs at 50% duty cycle. Use Equation 16 if the design will operate with 50% duty cycle. If not, use Equation 17. In Equation 17, use the input voltage value that is nearest to 50% duty cycle operation.

For this design example, Equation 15 produces the estimated maximum input current (I_{IN}) of 5 A. In reality this will be higher because the simplified equations do not include the efficiency losses of the power supply. Using K_{IND} = 0.3 with Equation 16, the minimum inductor value is calculated to be 3.33µH. The nearest standard value of 3.3 µH is chosen. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 18 and Equation 19, respectively. The calculated RMS inductor current is 5.0A and the peak inductor current is 5.73 A. The chosen inductor is a Vishay IHLP2525CZER3R3M1 which has an RMS current rating of 6 A, a saturation current rating of 10 A and 30 mΩ DCR.

$$I_{IN} = \frac{I_{OUT}}{(1 - D\max)} = \frac{2A}{(1 - 60\%)} = 5A \tag{15}$$

$$L \geq \frac{V_{OUT}}{I_{IN} \times K_{IND}} \times \frac{1}{4 \times f_{SW}} = \frac{15V}{5A \times 0.3} \times \frac{1}{4 \times 750kHz} = 3.33\mu H \tag{16}$$

$$L \geq \frac{V_{IN}}{I_{IN} \times K_{IND}} \times \frac{D}{f_{SW}} \tag{17}$$

$$I_L rms = \sqrt{\left(\frac{I_{OUT}}{1 - D\max}\right)^2 + \left(\frac{V_{IN}\min \times D\max}{\sqrt{12} \times L \times f_{SW}}\right)^2} = \sqrt{\left(\frac{2A}{1 - 60\%}\right)^2 + \left(\frac{6V \times 60\%}{\sqrt{12} \times 3.3\mu H \times 750kHz}\right)^2} = 5A \tag{18}$$

$$I_L peak = \frac{I_{OUT}}{1 - D\max} + \frac{V_{IN}\min \times D\max}{2 \times L \times f_{SW}} = \frac{2A}{1 - 60\%} + \frac{6V \times 60\%}{2 \times 3.3\mu H \times 750kHz} = 5.73A \tag{19}$$

Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults or transient load conditions the inductor current can increase above the peak inductor current calculated above. The above equations also do not include the efficiency of the regulator. For this reason a more conservative design approach is to choose an inductor with a saturation current rating greater than the typical switch current limit set by the current sense resistor or the inductor DC resistance if lossless DCR sensing is used.

SELECTING THE CURRENT SENSE RESISTOR

The external current sense resistor sets the cycle-by-cycle peak current limit. The peak current limit should be set to assure the maximum load current can be supported at the minimum input voltage. The typical over current threshold voltage (V_{CS}) with respect to duty cycle is shown in Figure 20. In this design example, the typical current limit threshold voltage at the 60% maximum duty cycle is 68 mV.

When selecting the current limit for the design, a 20% margin is recommended from the calculated peak current limit in Equation 19 to allow for load and line transients and the efficiency loss of the design. The recommended current sense resistance is calculated with Figure 20. In this example the minimum resistance is calculated at 9.89 mΩ and two 20 mΩ resistors in parallel are used. The sense resistors must be rated for the power dissipation calculated in Equation 22. Using the maximum current limit threshold of 82 mV according to the electrical specification table, the maximum power loss in the current sense resistor is 0.672 W. Two 0.5 W rated sense resistors are used in parallel in this design.

$$V_{CS\max} typ = 68mV \tag{20}$$

$$R_{CS} = \frac{V_{CS\max} typ}{1.2 \times I_L peak} = \frac{68mV}{1.2 \times 5.73A} = 9.89m\Omega \tag{21}$$

$$P_{RCS} = \frac{(V_{CS\max}\max)^2}{R_{CS}} = \frac{(82mV)^2}{10m\Omega} = 0.672W \tag{22}$$

The 10 Ω series resistors R13 and R15 with the 100 pF capacitor C12 filter high frequency switching noise from the ISNS pins.

OUTPUT CAPACITOR SELECTION

In a boost topology the current supplied to the output capacitor is discontinuous and proper selection of the output capacitor is important for filtering the high di/dt path of the supply. There are two primary considerations for selecting the value of the output capacitor. The output capacitor determines the output voltage ripple, and how the supply responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these two criteria.

The desired response to a large change in load current is the first criteria. A PWM controller cannot immediately respond to a fast increase or decrease in the load current. The response time is determined by the loop bandwidth. The output capacitor must supply the increased load current or absorb the excess inductor current until the controller responds. Equation 23 estimates the minimum output capacitance needed for the desired ΔV_{OUT} for a given ΔI_{OUT}. The loop bandwidth (f_{BW}) is typically limited by the Right Half Plane Zero (RHPZ) of the boost topology. The maximum recommended bandwidth can be calculated from Equation 41 and Equation 42. See the compensation section for more information. In this example, to limit the voltage deviation to 600 mV from a 1 A load step with a 14.5 kHz maximum bandwidth, a minimum of 18.3 µF output capacitance is needed. This value does not take into account the ESR of the output capacitor which can typically be ignored when using ceramic capacitors.

The output capacitor absorbs the ripple current through the synchronous switch to limit the output voltage ripple. Equation 24 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this example, a minimum of 21.3 µF is needed. Again this value does not take into account the ESR of the output capacitor.

$$C_{OUT} > \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} = \frac{1A}{2\pi \times 14.5kHz \times 0.6V} = 18.3\mu F \quad (23)$$

$$C_{OUT} > \frac{D\max \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} = \frac{60\% \times 5A}{750kHz \times 0.075V} = 21.3\mu F \quad (24)$$

The most stringent criteria for the output capacitor is 21.3 µF required to limit the output voltage ripple. When using ceramic capacitors for switching power supplies, high quality type X5R or X7R are recommended. They have a high capacitance to volume ratio and are fairly stable over temperature. Capacitance de-ratings for aging, temperature and dc bias increase the minimum value required. The voltage rating must be greater than the output voltage with some tolerance for output voltage ripple and overshoot in transient conditions. For this example 4 x 10 µF, 25 V ceramic capacitors with 5 mΩ of ESR are used. The estimated derated capacitance is 22 µF, approximately equal to the calculated minimum.

MOSFET SELECTION - NexFET™ POWER BLOCK

The TPS43061 5.5V gate drive is optimized for low Qg NexFET power devices. NexFET power blocks with both the high-side and low-side MOSFETs integrated are ideal for high power density designs. This design example uses the CSD86330Q3D. Two primary considerations when selecting the power MOSFETs are the average gate drive current required and the estimated MOSFET power losses.

The average gate drive current must be less than the 50 mA (minimum) VCC supply current limit. This current is calculated using Equation 25. With the selected power block and 5.5V VCC, the low-side FET has a total gate charge of 11 nC and the high-side FET has a total gate charge of 5 nC. The required gate drive current is 12 mA.

$$I_{GD} = (Qg_{HS} + Qg_{LS}) \times f_{SW} = (5nC + 11nC) \times 750kHz = 12mA \quad (25)$$

The target efficiency of the design dictates the acceptable power loss in the MOSFETs. The two largest components of power loss in the low-side FET are switching and conduction losses. Both losses are highest at the minimum input voltage when low-side FET current is maximum. The conduction power loss in the low-side FET can be calculated with Equation 26. Switching losses occur during the turn-off and turn-on time of the MOSFET. During these transitions, the low-side FET experiences both the input current and output voltage. The switching loss can be estimated with Equation 27. The low-side FET of the CSD86330Q3D has $R_{DS(on)LS}$ = 4.2 mΩ, gate to drain charge Q_{gd} = 1.6 nC, output capacitance C_{OSS} = 680 pF, series gate resistance R_G = 1.2 Ω, and gate to source voltage threshold $V_{GS(th)}$ = 1.1 V. The conduction power losses are estimated at 0.042 W and the switching losses are estimated at 0.070 W.

$$P_{CONDLS} = D\max \times I_L rms^2 \times Rdson_{LS} = 60\% \times 5.0A^2 \times 4.2m\Omega = 0.042W \quad (26)$$

$$P_{SW} = \frac{f_{SW}}{2} \times \left(C_{OSS} \times {V_{OUT}}^2 + V_{OUT} \times \frac{I_{OUT}}{1 - D\max} \times \frac{Q_{gd} \times R_G}{VCC - V_{GS(th)}} \right)$$
$$= \frac{750kHz}{2} \times \left(680\,pF \times 15V^2 + 15V \times \frac{2A}{1 - 60\%} \times \frac{1.6nC \times 1.2\Omega}{5.5V - 1.1V} \right) = 0.070W \quad (27)$$

Two power losses in the high-side FET to consider are the dead time body diode loss and the FET conduction loss. The conduction loss is highest at the minimum PWM duty cycle. The conduction power loss in the high-side FET can be calculated with Equation 28. Dead time losses are caused by conduction in the body diode of the high-side FET during the delay time between the LDRV and HDRV signals. The dead time loss varies mainly with switching frequency. The dead time losses are estimated with Equation 29. The high-side FET of the CSD86330Q3D has $R_{DS(ON)HS}$ = 8 mΩ and body diode forward voltage drop V_{SD} = 0.75 V. The conduction power losses are estimated at 0.080 W and the dead time losses are estimated at 0.366 W. For designs targeting highest efficiency, dead time losses can be reduced by adding a Schottky diode in parallel with the high-side FET to reduce the diode forward voltage drop during the dead time.

$$P_{CONDHS} = (1 - D\max) \times I_L rms^2 \times R_{DS(on)HS} = (1 - 60\%) \times 5.0A^2 \times 8m\Omega = 0.080W \quad (28)$$

$$P_{DT} = V_{SD} \times I_L rms \times \left(t_{non-overlap1} + t_{non-overlap2} \right) \times f_{SW}$$
$$= 0.75V \times 5A \times (65ns + 65ns) \times 750kHz = 0.366W \quad (29)$$

BOOTSTRAP CAPACITOR SELECTION

A capacitor must be connected between the BOOT and SW pins for proper operation. This capacitor provides the instantaneous charge and gate drive voltage needed to turn on the high-side FET. A ceramic with X5R or better grade dielectric is recommended. Use Equation 30 to calculate the minimum bootstrap capacitance to limit the BOOT capacitor ripple voltage to 250 mV. In this example with the selected high-side FET the minimum calculated capacitance is 0.042 µF and a 0.1 µF capacitor is used. The capacitor should have a 10 V or higher voltage rating.

$$C_{BOOT} = \frac{Qg_{HS}}{\Delta V_{BOOT}} = \frac{5nC}{250mV} = 0.042\mu F \quad (30)$$

VCC CAPACITOR

An X5R or better grade ceramic bypass capacitor is required for the internal VCC regulator at the VCC pin with a recommended range of 0.47 µF to 10 µF. A capacitance of 4.7 µF is used in this example. The capacitor should have a 10 V or higher voltage rating.

INPUT CAPACITOR

The TPS43060 and TPS43061 require a high quality 0.1 µF or higher ceramic type X5R or X7R bypass capacitor at the VIN pin for proper decoupling. Based on the application requirements additional bulk capacitance may be needed to meet input voltage ripple and, or transient requirements. The minimum capacitance for a specified input voltage ripple is calculated using Equation 31. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the RMS current calculated with Equation 32. If ceramic input capacitors are used they should be high quality ceramic, type X5R or X7R.

For this example design, the capacitors must be rated for at least 12 V to support the maximum input voltage. Designing for a 45 mV input voltage ripple (0.5% the nominal input voltage), the minimum input capacitance is 10.8 µF. The input capacitor must also be rated for 0.42 A RMS current. The capacitors selected are 2 x 10 µF, 25 V ceramic capacitors with 5 mΩ of ESR. The estimated voltage de-rated total capacitance is 15 µF.

$$C_{IN} > \frac{I_{RIPPLE}}{4 \times f_{SW} \times V_{INRIPPLE}} = \frac{1.46A}{4 \times 750kHz \times 0.045V} = 10.8\mu F \quad (31)$$

$$I_{CIN} rms = \frac{I_{RIPPLE}}{\sqrt{12}} = \frac{1.46A}{\sqrt{12}} = 0.42A \quad (32)$$

OUTPUT VOLTAGE AND FEEDBACK RESISTORS SELECTION

The voltage divider of R8 and R9 sets the output voltage. To balance power dissipation and noise sensitivity, R9 should be selected between 10 kΩ and 100 kΩ. For the example design, 11 kΩ was selected for R9. Using Equation 33, R8 is calculated as 124.2 kΩ. The nearest standard 1% resistor 124 kΩ is used.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - V_{FB}}{V_{FB}} = 11.0k\Omega \times \frac{15V - 1.22V}{1.22V} = 124.2k\Omega \quad (33)$$

Where R_{LS} = R9 and R_{HS} = R8.

SETTING THE SOFT-START TIME

The soft-start capacitor determines the amount of time allowed for the output voltage to reach its nominal programmed value during power up. This is especially useful if a load requires a controlled voltage slew rate. A controlled start-up time is necessary with large output capacitance to limit the current into the capacitor during start-up. Large currents to charging the capacitor during start-up could trigger the devices current limit. Excessive current draw from the input power supply may also cause the input voltage rail to sag. The soft-start capacitor can be sized to limit in-rush current or output voltage overshoot during startup. Use Equation 34 to calculate the required capacitor for a desired soft-start time. In this example application for a desired soft-start time of 20 ms, a 0.082 µF capacitance is calculated, and the nearest standard value of 0.1 µF capacitor is chosen.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} = \frac{20ms \times 5\mu A}{1.22V} = 0.082\mu F \quad (34)$$

UNDERVOLTAGE LOCKOUT SET POINT

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider connected to the EN pin of the TPS43060 and TPS43061. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The necessary voltage divider resistors are calculated with Equation 35 and Equation 36. If the application does not require an adjustable UVLO, the EN pin can be left floating or tied to the VIN pin.

For the example design, the supply should start switching once the input voltage increases to 5.34 V (V_{START}). After start-up, it should continue to operate until the input voltage falls to 4.3 V (V_{STOP}). To produce the desired start and stop voltages, resistor divider values R3 = 221 kΩ between VIN and EN and a R4 = 59 kΩ between EN and GND are used.

$$R_{UVLO\_H} = \frac{V_{START} \times \left(\frac{V_{EN\_DIS}}{V_{EN\_ON}}\right) - V_{STOP}}{I_{EN\_pus} \times \left(1 - \frac{V_{EN\_DIS}}{V_{EN\_ON}}\right) + I_{EN\_hys}} = \frac{5.34V \times \left(\frac{1.14V}{1.21V}\right) - 4.3V}{1.8\mu A \times \left(1 - \frac{1.14V}{1.21V}\right) + 3.2\mu A} = 221.26k\Omega \quad (35)$$

$$R_{UVLO\_L} = \frac{R_{UVLO\_H} \times V_{EN\_DIS}}{V_{STOP} - V_{EN\_DIS} + R_{UVLO\_H} \times \left(I_{EN\_pup} + I_{EN\_hys}\right)} = \frac{221k\Omega \times 1.14V}{4.3V - 1.14V + 221k\Omega \times (1.8\mu A + 3.2\mu A)}$$

$$= 59k\Omega \quad (36)$$

POWER GOOD RESISTOR SELECTION

The PGOOD pin is an open drain output requiring a pull-up resistor connected to a voltage supply of no more than 8 V. A value between 10 kΩ and 100 kΩ is recommended. If the Power Good indicator feature is not needed, this pin can be grounded or left floating.

THE CONTROL LOOP COMPENSATION

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation internal to the device. Since the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and ESR zero of the output capacitor. In this simplified model, the DC gain (Adc), modulator pole (f_{Pmod}), and the ESR zero (f_{Zmod}) are calculated with Equation 37 to Equation 39. Use the de-rated value of C_{OUT}, which is 22 µF in this example. In a

boost topology the maximum crossover frequency is typically limited by the right-half plane zero (RHPZ). The RHPZ can be estimated with Equation 40. The compensation design should be done at the minimum input voltage when the RHPZ is at the lowest frequency. The crossover frequency should also be limited to less than 1/5 of the switching frequency. Equation 41 and Equation 42 are used to calculate the maximum recommended crossover frequency. For this example design, Adc = 11.3 V/V, f_{Pmod} = 0.97 kHz, f_{Zmod} = 1.45 MHz, f_{RHPZ} = 57.9 kHz, $f$co1 = 14.5 kHz, and $f$co2 = 150 kHz. The target fco is 14.5 kHz.

$$Adc = \frac{3}{40} \times \frac{V_{IN}\,\text{min}}{2 \times R_{SENSE} \times I_{OUT}} = \frac{3}{40} \times \frac{6V}{2 \times 10m\Omega \times 2A} = 11.3\frac{V}{V} \tag{37}$$

$$f_{P\text{mod}} = \frac{1}{2\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} = \frac{1}{2\pi \times \frac{15V}{2A} \times 22\mu F} = 0.97kHz \tag{38}$$

$$f_{Z\text{mod}} = \frac{1}{2\pi \times ESR \times C_{OUT}} = \frac{1}{2\pi \times 5m\Omega \times 22\mu F} = 1.45MHz \tag{39}$$

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}}}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 = \frac{\frac{15V}{2A}}{2\pi \times 3.3\mu H} \times \left(\frac{6V}{15V}\right)^2 = 57.9kHz \tag{40}$$

$$fco1 < \frac{f_{RHPZ}}{4} = \frac{57.9kHz}{4} = 14.5kHz \tag{41}$$

$$fco2 < \frac{f_{SW}}{5} = \frac{750kHz}{5} = 150kHz \tag{42}$$

The compensation components can now be calculated. A resistor in series with a capacitor creates a compensating zero. A capacitor in parallel to these two components can be added to form a compensating pole. To determine the compensation resistor (R7) use Equation 43. R7 is calculated to be 7.45 kΩ and a standard 1% value of 7.50 kΩ is selected. Use Equation 44 to set the compensation zero to 1/10 the target crossover frequency. C9 is calculated at 0.0147 µF and a standard value of 0.015 µF is used.

$$R7 = R_{COMP} = \frac{40}{3} \times \frac{2\pi \times C_{OUT} \times R_{SENSE} \times V_{OUT} \times fco \times (R_{SH} + R_{SL})}{R_{SL} \times V_{IN}\,\text{min} \times Gea}$$

$$= \frac{40}{3} \times \frac{2\pi \times 22\mu F \times 10m\Omega \times 15V \times 14.5kHz \times (124k\Omega + 11k\Omega)}{11k\Omega \times 6V \times 1100\frac{\mu A}{V}} = 7.45k\Omega \tag{43}$$

$$C9 = C_{COMP} = \frac{1}{2\pi \times \frac{fco}{10} \times R_{COMP}} = \frac{1}{2\pi \times \frac{14.5kHz}{10} \times 7.50k\Omega} = 0.0147\mu F \tag{44}$$

A compensation pole can be implemented if desired with capacitor C8 in parallel with the series combination of R7 and C9. Use the larger value calculated from Equation 45 and Equation 46. The selected value of C8 is 150 pF for this example.

$$C_{HF} = \frac{C_{OUT} \times ESR}{R_{COMP}} = \frac{22\mu F \times 5m\Omega}{7.50k\Omega} = 14.7\,pF \tag{45}$$

$$C_{HF} = \frac{1}{20\pi \times fco \times R_{COMP}} = \frac{1}{20\pi \times 14.5kHz \times 7.50k\Omega} = 150\,pF \tag{46}$$

DISCONTINUOUS CONDUCTION MODE, PULSE-SKIP MODE AND NO LOAD INPUT CURRENT

The reverse current sensing of the TPS43060/61 allows the power supply to operate discontinuous conduction mode (DCM) at light loads for higher efficiency. The supply enters DCM when the inductor current ramps to zero at the end of a PWM cycle and the reverse current sense turns off the high-side FET for the remainder of the cycle. In DCM the duty cycle is a function of the load, input and output voltages, inductance and switching frequency as computed in Equation 47. The load current at which the inductor current falls to zero and the converter enters DCM can be calculated using Equation 48. Additionally after the converter enters DCM, decreasing the load further reduce the duty cycle. If the DCM on-time reaches the minimum on-time of the TPS43060 and TPS43061, the converter begins pulse skipping to maintain output voltage regulation. Pulse skipping can increase the output voltage ripple.

In this example with the 9 V nominal input voltage, the estimated load current where the converter enters DCM operation is 0.44 A. The measured boundary is 0.36 A. In most designs the converter enters DCM at lower load currents because Equation 48 does not account for the efficiency losses.. The design example power supply enters pulse-skip mode when the output current is lower than 12 mA and the input current draw is 1.3 mA with no load.

$$D = \frac{\sqrt{2 \times (V_{OUT} - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \tag{47}$$

$$I_{OUT}crit = \frac{(V_{OUT} - V_{IN}) \times {V_{IN}}^2}{2 \times {V_{OUT}}^2 \times f_{SW} \times L} = \frac{(15V - 9V) \times 9V^2}{2 \times 15V^2 \times 750kHz \times 3.3\mu H} = 0.44A \tag{48}$$

LAYOUT

Layout is a critical portion of a good power converter design. There are several signal paths conducting fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. Guidelines are as follows and the EVM layouts can be used as reference.

- The high speed switching current path includes the high-side FET, low-side FET and output capacitors. This is a critical loop to minimize to reduce noise and achieve best performance.
- Components connected to noise sensitive circuitry should be located as close to the TPS43060 and TPS43061 as possible, and be connected the AGND pin. This includes components connected to FB, COMP, SS, RT/CLK, and VCC pins.
- The PowerPAD should be connected to the quiet analog ground for the AGND pin to limit internal noise. For thermal performance, multiple vias directly under the device should be used to connect to any internal ground planes.
- Components in the power conversion path should be connected to the PGND. This includes the bulk input capacitors, output capacitors, low-side FET and EN UVLO resistors.
- A single connection must connect the quiet AGND to the noisy PGND near the PGND pin.
- The low ESR ceramic bypass capacitor for the VIN pin should be connected to the quiet AGND as close as possible to the TPS43060 and TPS43061.
- The distance between the inductor, low-side FET and high-side FET should be minimized to reduce noise. This connection is the high speed switching voltage node.
- The high-side and low-side FETs should be placed close to the device to limit the trace length required for the HDRV and LDRV gate drive signals.
- The bypass capacitor between the ISNS+ and ISNS- pins should be placed next to the TPS43060 and TPS43061. Minimize the distance between the device and the sense resistors.

THERMAL CONSIDERATIONS

The TPS43060 and TPS43061 junction temperature should not exceed 150°C under normal operating conditions. This restriction limits the power dissipation of the device. Power dissipation of the controller includes gate drive power loss and bias power loss of the internal VCC regulator. The TPS43060 and TPS43061 are packaged in a thermally enhanced WQFN package which includes a PowerPAD™ that improves the thermal capabilities. The thermal resistance of the WQFN package depends on the PCB layout and the PowerPAD connection. As mentioned in the layout considerations, the PowerPAD must be soldered to the analog ground on the PCB with thermal vias underneath the PowerPAD to achieve good thermal performance.

For best thermal performance pcb copper area should be sized to improve thermal capabilities of the components in the power path dissipating the most power. This includes the sense resistors, inductor, low-side FET and high-side FET. Manufacturer guidelines for the selected external FETs should be followed.

CHARACTERISTICS OF THE TPS43061 BOOST CONVERTER EXAMPLE

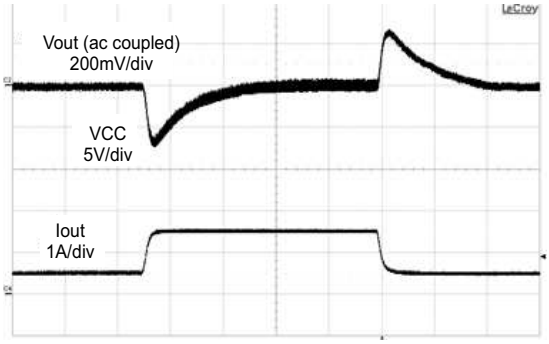


Figure 22. Load Transient

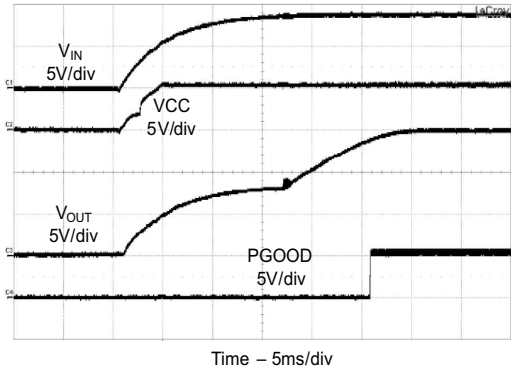


Figure 23. Start-up with VIN

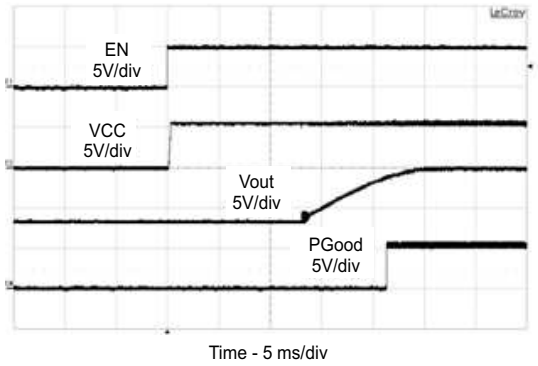


Figure 24. Start-up with EN

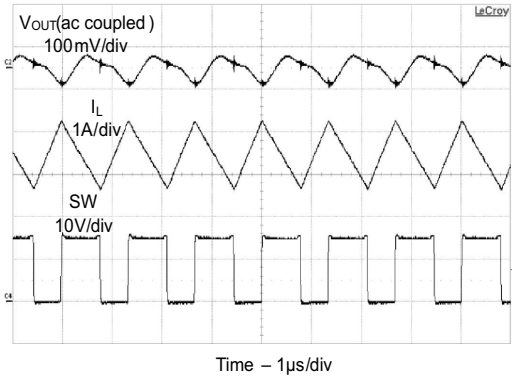


Figure 25. Output Ripple in CCM

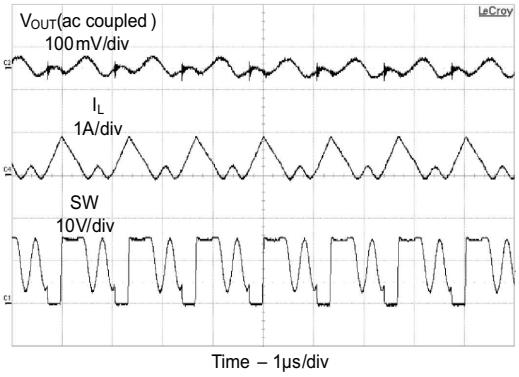


Figure 26. Output Ripple in DCM

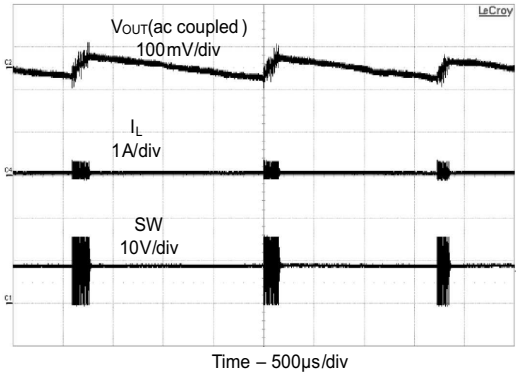


Figure 27. Output Ripple in Pulse-Skipping Mode

CHARACTERISTICS OF THE TPS43061 BOOST CONVERTER EXAMPLE (continued)

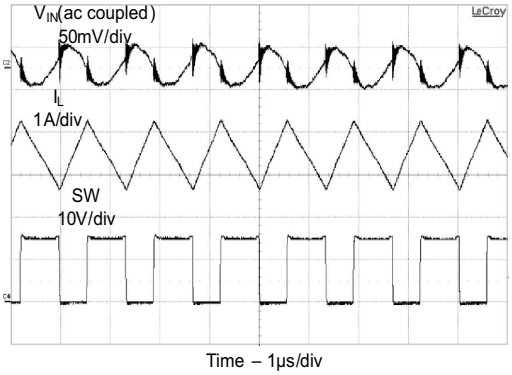


Figure 28. Input Ripple in CCM

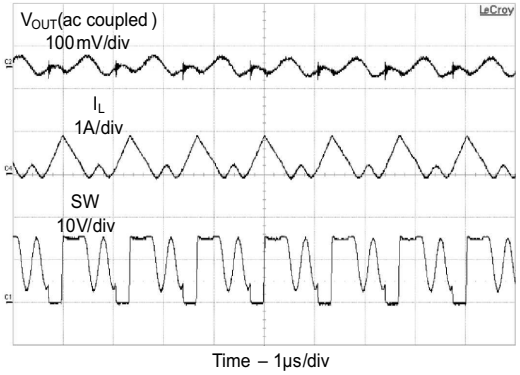


Figure 29. Input Ripple in DCM

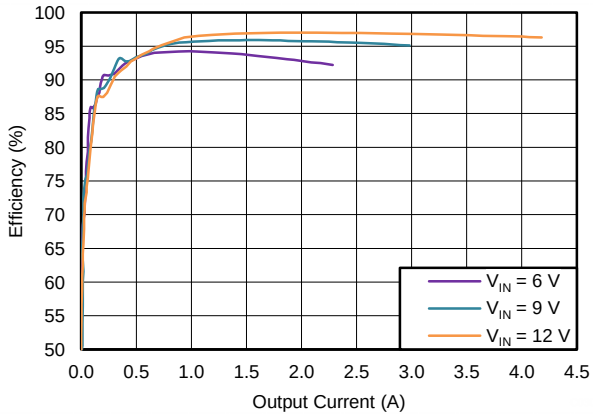


Figure 30. Efficiency vs Output Current

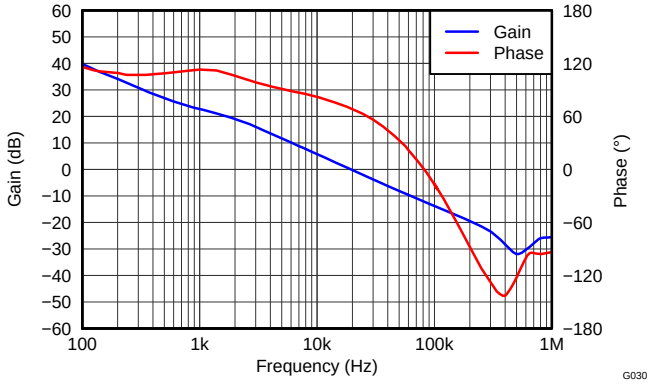


Figure 31. Loop Gain and Phase

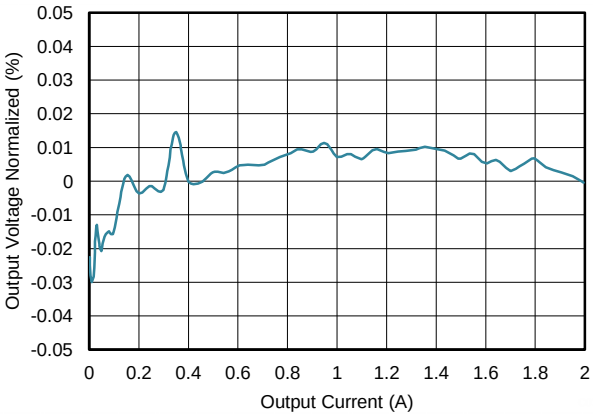


Figure 32. Load Regulation

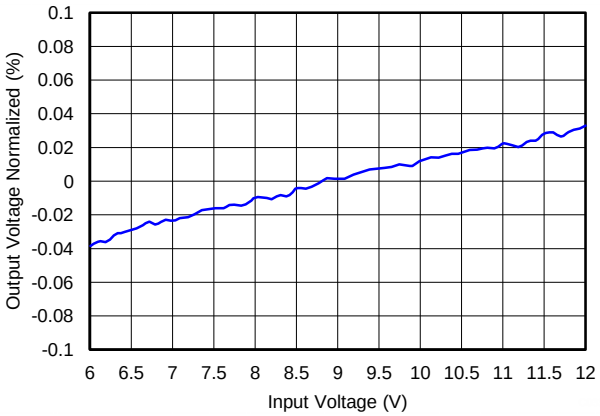


Figure 33. Line Regulation

HIGH EFFICIENCY 40V SYNCHRONOUS BOOST CONVERTER USING TPS43060

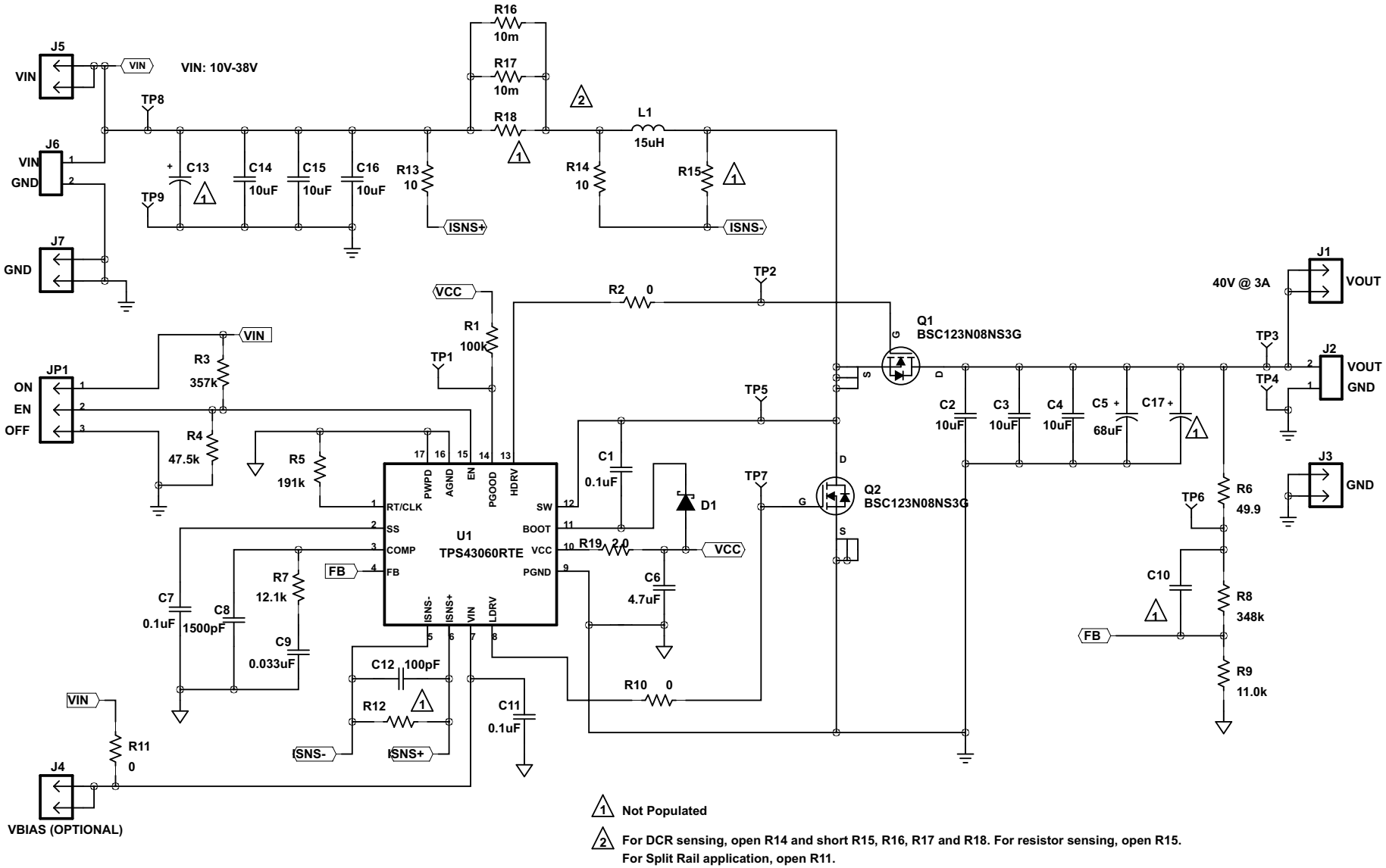


Figure 34. High Voltage Synchronous Boost Converter using TPS43060

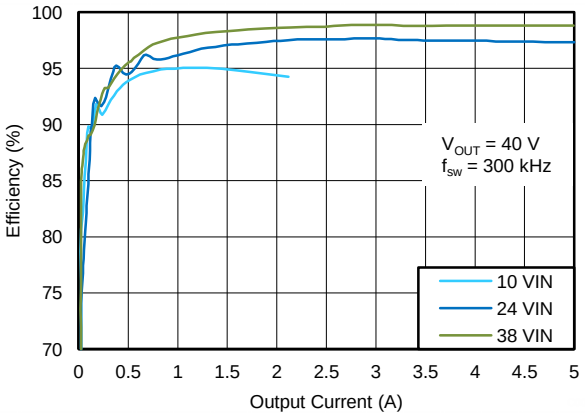


Figure 35. The Efficiency of High Voltage Boost Converter Using TPS43060

The design procedure of TPS43061 is also applicable to the TPS43060; however, several difference should be noted. Unlike the TPS43061, which has 5.5 V gate drive supply and is optimized for low Qg NexFETs™, the TPS43060 has a 7.5 V gate drive supply and is suitable to drive standard threshold MOSFETs. The TPS43060 requires an external bootstrap diode (D1 as shown in Figure 34) from VCC to BOOT to charge the bootstrap capacitor, and the external diode should have a breakdown voltage rating greater than the output voltage. In addition, the TPS43060 also requires a 2Ω resistor (R19 shown in Figure 34) connected in series with the VCC pin to limit the peak current drawn through the internal circuitry when the external bootstrap diode is conducting.

REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Changed the devices From: Preview To: Production 1

Changes from Revision A (December 2012) to Revision B **Page**

- Aligned package description throughout datasheet. 1
- Removed ordering information table. 2

Changes from Revision B (August 2013) to Revision C **Page**

- Changed Equation 3 12
- Deleted sections LAYOUT CONSIDERATIONS and THERMAL CONSIDERATIONS 15
- Changed Equation 13 from Dmin to (1-Dmax), 60% to (1-60%) and 2.4 MHz to 1.6 MHz 18
- Changed 2 MHz to 1.6 MHz in para below Equation 13 18
- Changed in Equation 28 - DS(on)LS to DS(on)HS 21
- Changed in Equation 29 - from (60 ns + 65 ns) to (65 ns _65 ns) 21
- Changed in paragraph above Equation 37 - 1.93 kHz to 0.97 kHz 23
- Changed in Equation 38 - from 1.93 kHz to 0.97 kHz 23
- Changed in paragraph above Equation 43 - 7.44 kΩ to 7.45 kΩ 23
- Changed in Equation 43 - 21 µF to 22 µF, 20mΩ to 10mΩ, 19.3kHz to 14.5kHz, = 7.44 to = 7.45, and deleted 3/40 factor from denominator 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS43060RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	43060	Samples
TPS43060RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	43060	Samples
TPS43061RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	43061	Samples
TPS43061RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	43061	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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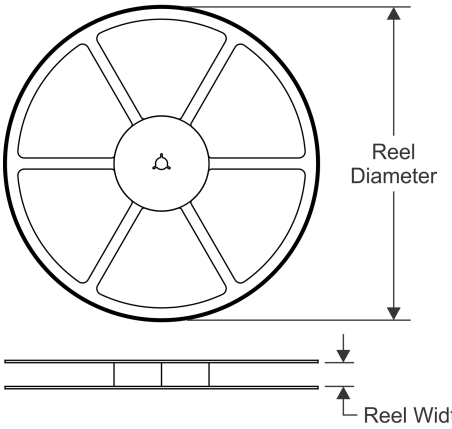
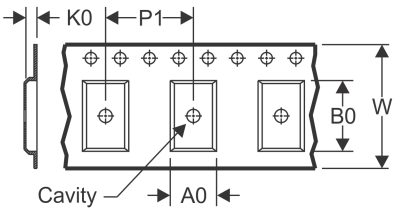
TAPE AND REEL INFORMATION

REEL DIMENSIONS

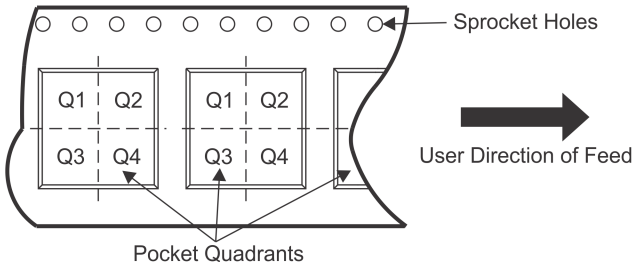


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

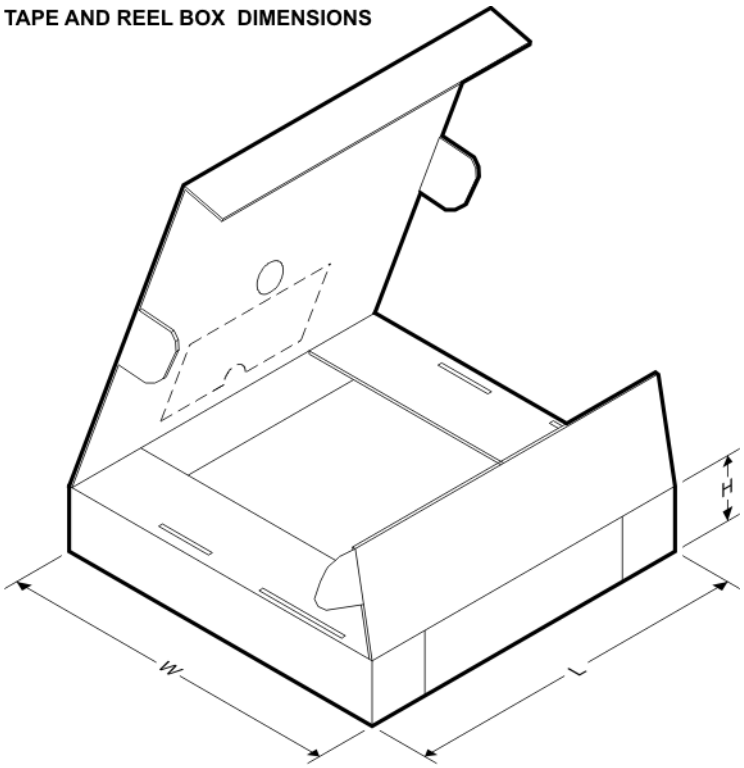
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43060RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS43060RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS43061RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS43061RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

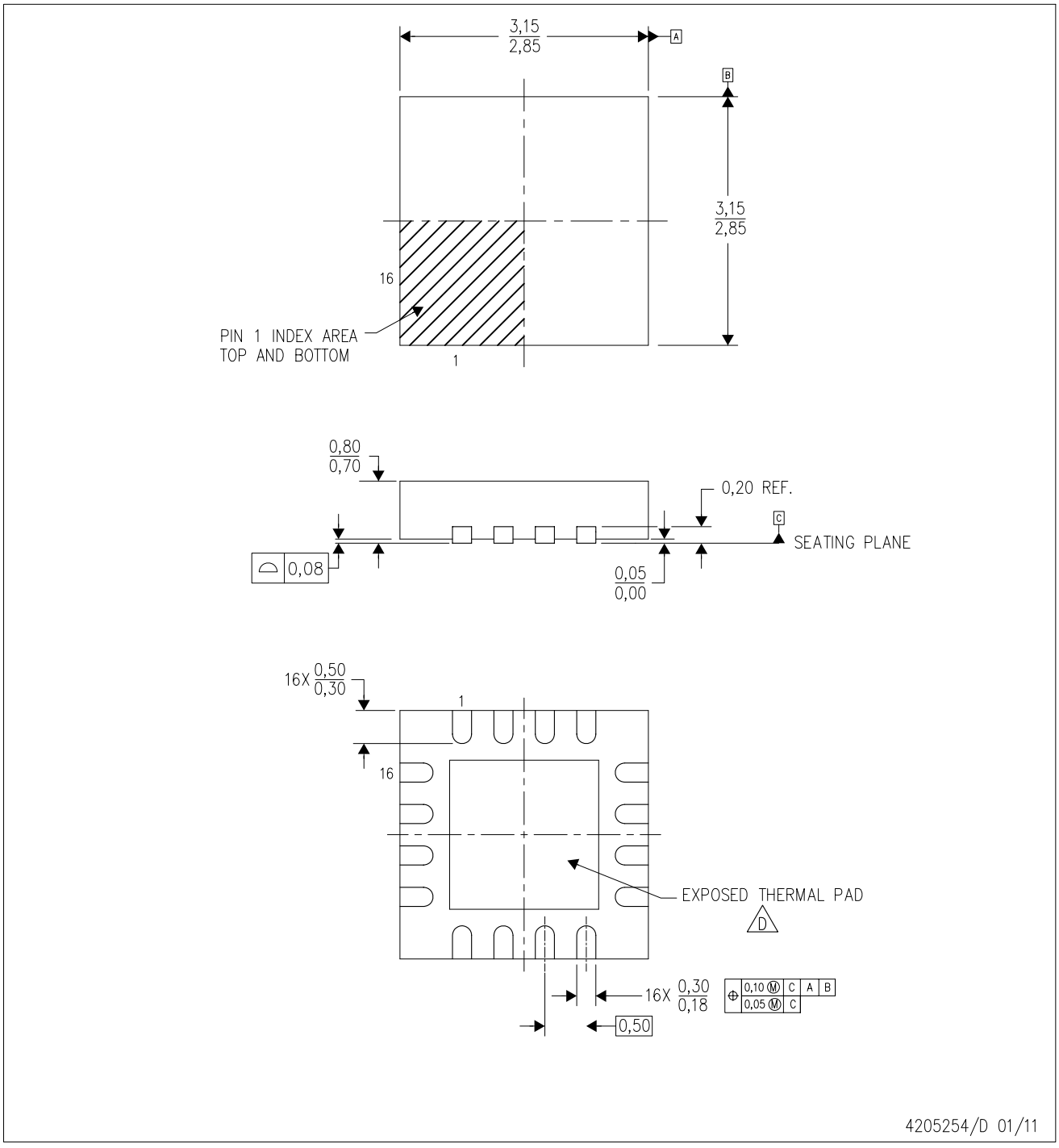
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43060RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS43060RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS43061RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS43061RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

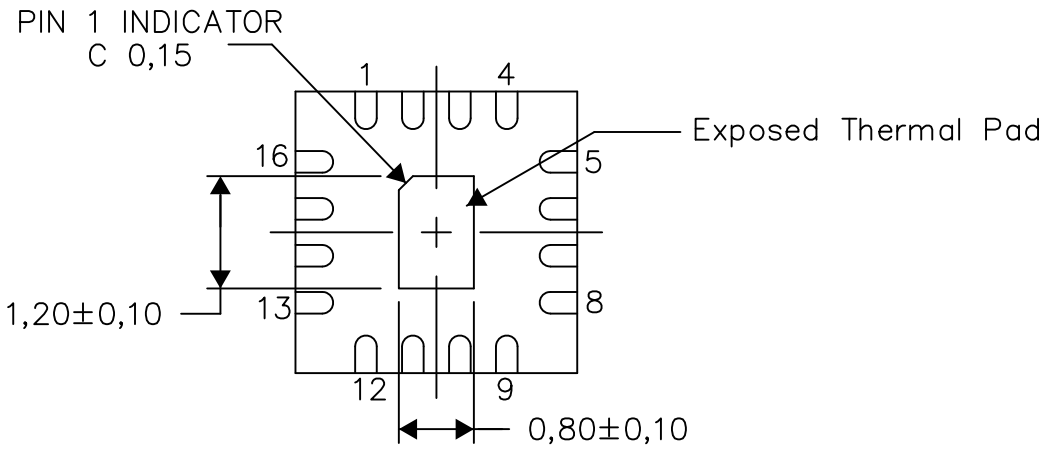
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



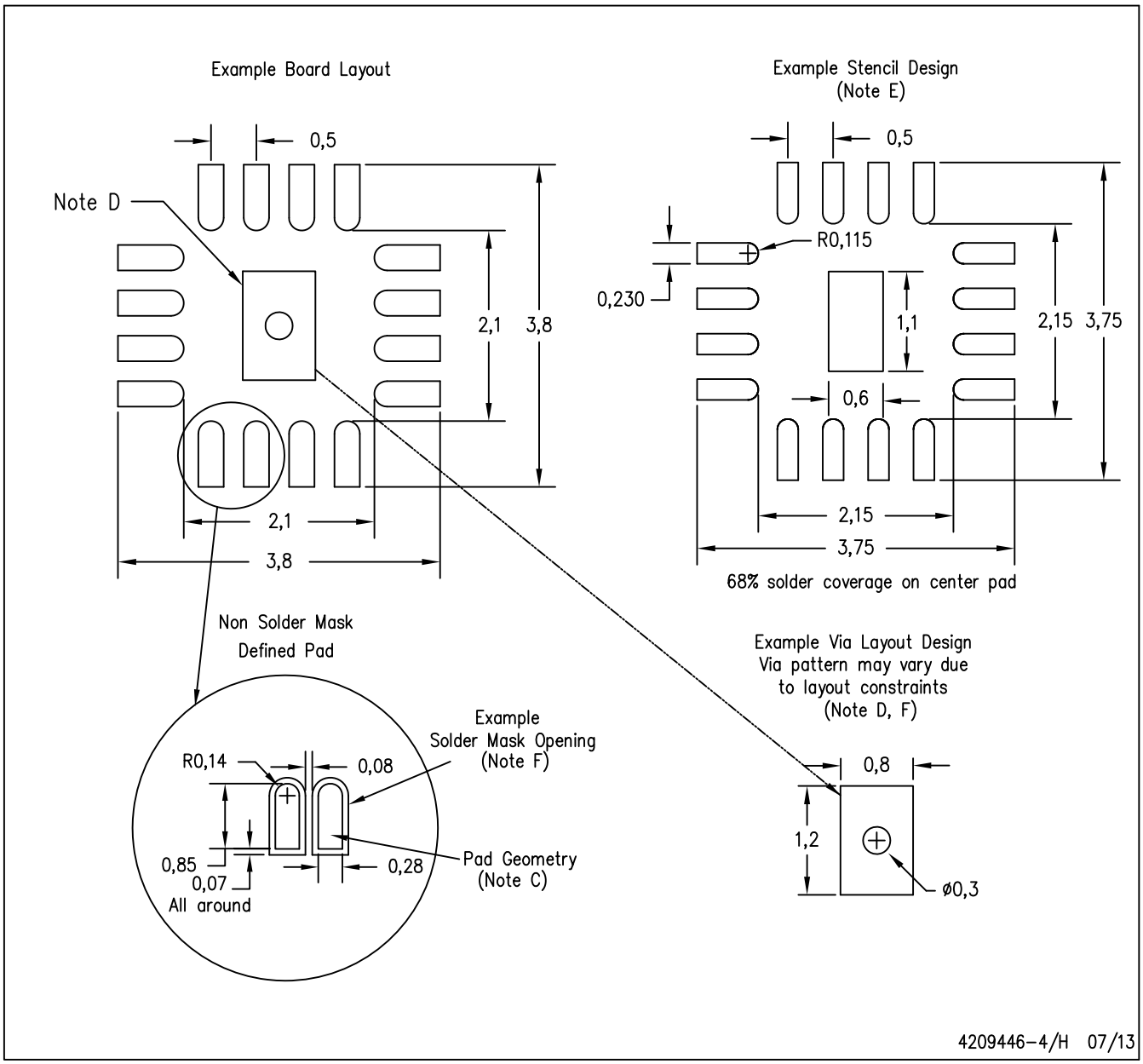
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/N 07/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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