TPS3813-Q1 Processor Supervisory Circuits With Window-Watchdog

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C4B
- Window-Watchdog With Programmable Delay and Window Ratio
- 6-Pin SOT-23 Package
- Supply Current of 9 µA (Typ)
- Power-On Reset Generator With a Fixed Delay Time of 25 ms
- Precision Supply-Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Open-Drain Reset Output

2 Applications

- Applications Using DSPs, Microcontrollers, or Microprocessors
- Safety-Critical Systems
- Automotive Systems
- Heating Systems

3 Description

The TPS3813-Q1 supervisory circuits provide circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power on, the $\overline{\text{RESET}}$ pin is asserted when the supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ pin active as long as V_{DD} remains below the threshold voltage (V_{IT}).

An internal timer delays the return of the output to the inactive (high) state to ensure proper system reset. The delay time, t_d = 25 ms typical, begins after V_{DD} has risen above the threshold voltage (V_{IT}). When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

For safety-critical applications, the TPS3813-Q1 family of devices incorporate a window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting the WDT pin to GND or V_{DD}, or by using an external capacitor. The lower limit, and thus the window ratio, is set by connecting the WDR pin to GND or V_{DD}. The $\overline{\text{RESET}}$ pin will assert a reset to the microcontroller if the watchdog is incorrectly serviced.

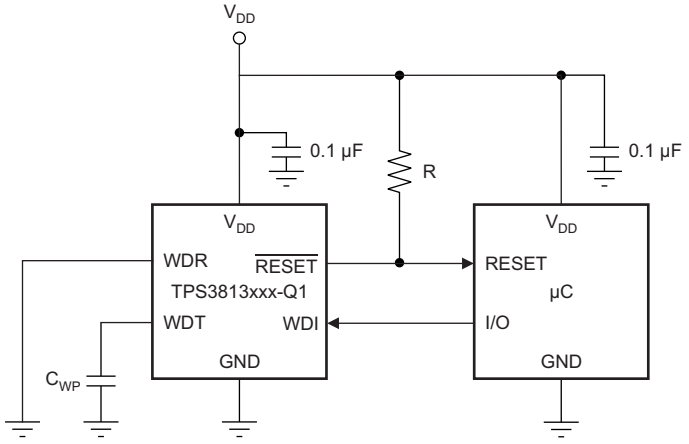
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The devices are available in a 6-pin SOT-23 package. The devices are characterized for operation over a temperature range of –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3813K33-Q1	SOT-23 (6)	2.90 mm × 1.60 mm
TPS3813I50-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2013) to Revision D — **Page**

- Deleted the TPS38131J25-Q1 and TPS3813L30-Q1 devices from the data sheet ... 1
- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted the *Dissipation Ratings* table ... 4
- Changed the voltage on the V_{DD} pin from 0.6 V to 1.1 V in the *Timing Diagram* figure ... 9

Changes from Revision B (May 2012) to Revision C — **Page**

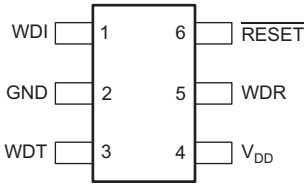
- Deleted banner stating that TPS3813K33-Q1 is *Not Recommended for New Designs* ... 6

Changes from Revision A (November 2008) to Revision B — **Page**

- Changed value from 47 pF to 155 pF. ... 11

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	I	Ground
$\overline{\text{RESET}}$	6	O	Open-drain reset output
V_{DD}	4	I	Supply voltage and supervising input
WDI	1	I	Watchdog timer input
WDR	5	I	Selectable watchdog window ratio input
WDT	3	I	Programmable watchdog delay input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)	V_{DD}		7	V
		$\overline{\text{RESET}}$	–0.3	V_{DD} + 0.3	
		All other pins(2)	–0.3	7	
I_{OL}	Maximum low output current			5	mA
I_{OH}	Maximum high output current			–5	mA
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})			±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})			±20	mA
	Continuous total power dissipation		See *Thermal Information*		
T_A	Operating free-air temperature		–40	125	°C
	Soldering temperature			260°C	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 3, 4, and 6)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

at specified temperature range

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}		V
V_{IL}	Low-level input voltage		0.3 × V_{DD}	V
Δt/ΔV	Input transition rise and fall rate		100	ns/V
t_w	Pulse width of WDI trigger pulse	50		ns
T_A	Operating free-air temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS3813-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	44.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power up reset voltage (1)		V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.2	V
V_{IT}	Negative-going input threshold voltage (2)	TPS3813-Q1J25		2.2	2.25	2.3	V
		TPS3813-Q1L30		2.58	2.64	2.7	
		TPS3813-Q1K33		2.87	2.93	3	
		TPS3813-Q1I50		4.45	4.55	4.65	
V_{hys}	Hysteresis	TPS3813-Q1J25			30		mV
		TPS3813-Q1L30			35		
		TPS3813-Q1K33			40		
		TPS3813-Q1I50			60		
I_{IH}	High-level input current	WDI, WDR	WDI = V_{DD} = 6 V, WDR = V_{DD} = 6 V	–125		125	nA
		WDT	WDT = V_{DD} = 6 V, V_{DD} > V_{IT}, $\overline{\text{RESET}}$ = High	–125		125	
I_{IL}	Low-level input current	WDI, WDR	WDI = 0 V, WDR = 0 V, V_{DD} = 6 V	–125		125	
		WDT	WDT = 0 V, V_{DD} > V_{IT}, $\overline{\text{RESET}}$ = High	–125		125	
I_{OH}	High-level output current		V_{DD} = V_{IT} + 0.2 V, V_{OH} = V_{DD}			25	nA
I_{DD}	Supply current		V_{DD} = 2 V output unconnected		9	13	µA
			V_{DD} = 5 V output unconnected		20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.

6.6 Timing Requirements

R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 125°C

			MIN	MAX	UNIT
t_w	Pulse width at V_{DD}	$V_{DD} = V_{IT-} + 0.2$ V, $V_{DD} = V_{IT-} – 0.2$ V	3		µs

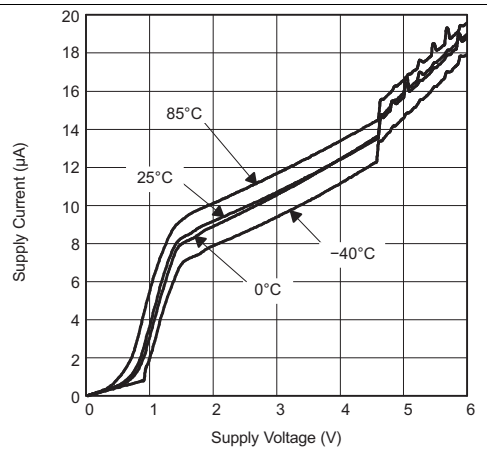
6.7 Switching Characteristics

R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT} + 0.2$ V (see Figure 7)	20	25	30	ms
$t_{t(out)}$	Watchdog time-out	Upper limit	WDT = 0 V	0.2	0.25	0.3	s
			WDT = V_{DD}	2	2.5	3	
			WDT = programmable (1)		See (2)		ms
	Watchdog window ratio		WDR = 0 V, WDT = 0 V		1:31.8		
			WDR = 0 V, WDT = V_{DD}		1:32		
			WDR = 0 V, WDT = programmable		1:25.8		
			WDR = V_{DD}, WDT = 0 V		1:124.9		
			WDR = V_{DD}, WDT = V_{DD}		1:127.7		
			WDR = V_{DD}, WDT = programmable		1:64.5		
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{\text{RESET}}$ delay	$V_{IL} = V_{IT} – 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V		30	50	µs

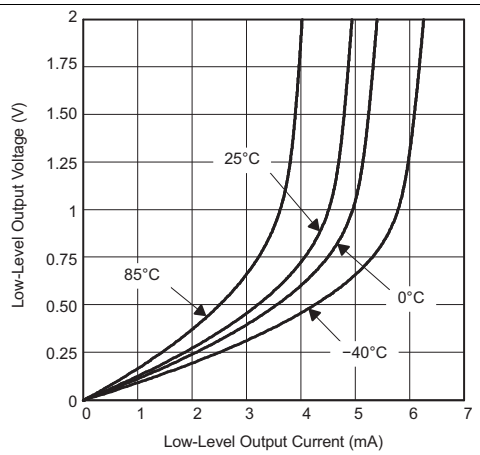
(1) 155 pF < $C_{(ext)}$ < 63 nF
(2) ($C_{(ext)}$ / 15.55 pF + 1) × 6.25 ms

6.8 Typical Characteristics



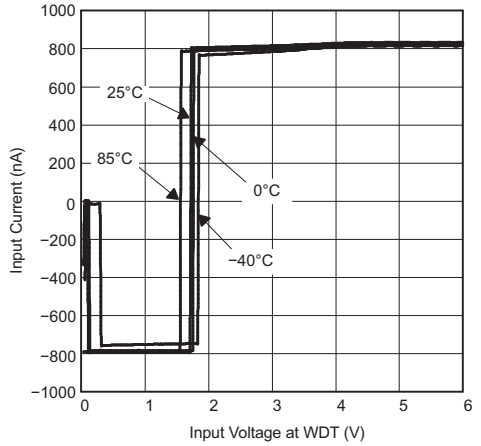
WDI = GND WDT = GND WDR = GND

Figure 1. Supply Current vs Supply Voltage



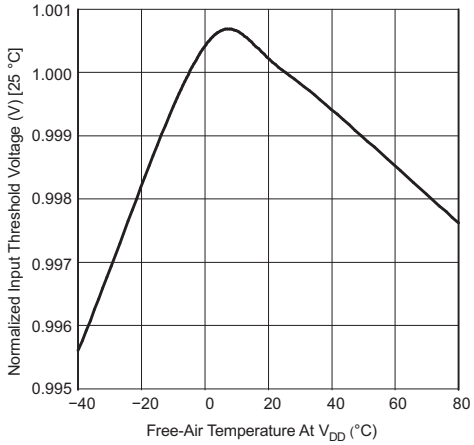
WDI = GND WDT = GND WDR = GND
V_{DD} = 2 V

Figure 2. Low-Level Output Voltage vs Low-Level Output Current



WDI = GND WDR = GND V_{DD} = 6 V

Figure 3. Input Current vs Input Voltage at WDT



WDI = Triggered WDT = GND WDR = GND

Figure 4. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

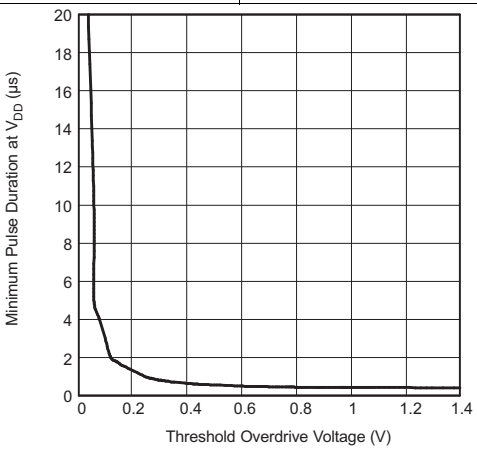


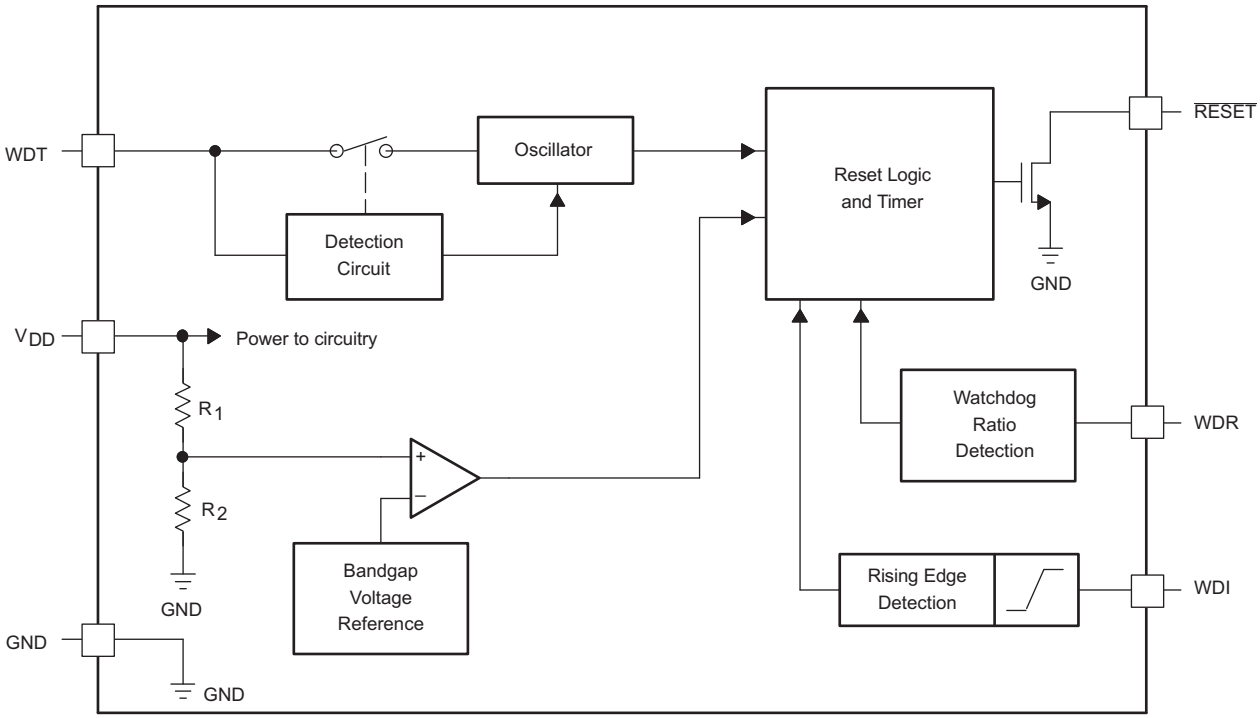
Figure 5. Minimum Pulse Duration At V_{DD} vs V_{DD} Threshold Overdrive Voltage

7 Detailed Description

7.1 Overview

The TPS3813-Q1 devices (TPS3813K33-Q1 and TPS3813I50-Q1) are a family of supervisory circuits with watchdog functionality. The TPS3813-Q1 family of devices is designed to assert a reset on the $\overline{\text{RESET}}$ pin when the supply (V_{DD}) drops below the threshold voltage (V_{IT}) which varies depending on which device is used. When the V_{DD} supply rises above 1.1 V, the $\overline{\text{RESET}}$ pin is set high, and remains active until a reset condition occurs. The watchdog window can be programmed using the WDT and WDR pins with several different configurations, all of which are explained in the following sections.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Implemented Window-Watchdog Settings

The watchdog window can be set up in two different ways. The first way is to use the implemented timing, which is a default setting. The other way is to activate the default settings by wiring the WDT and WDR pin to V_{DD} or GND. Four different timings available with these settings which are listed in Table 1.

Table 1. Window-Watchdog Configuration Settings

SELECTED OPERATION MODE		WINDOW FRAME	LOWER WINDOW FRAME
WDT = 0 V	WDR = 0 V	Max = 0.3 s	Max = 9.46 ms
		Typ = 0.25 s	Typ = 7.86 ms
		Min = 0.2 s	Min = 6.27 ms
	WDR = V_{DD}	Max = 0.3 s	Max = 2.43 ms
		Typ = 0.25 s	Typ = 2 ms
		Min = 0.2 s	Min = 1.58 ms
WDT = V_{DD}	WDR = 0 V	Max = 3 s	Max = 93.8 ms
		Typ = 2.5 s	Typ = 78.2 ms
		Min = 2 s	Min = 62.5 ms
	WDR = V_{DD}	Max = 3 s	Max = 23.5 ms
		Typ = 2.5 s	Typ = 19.6 ms
		Min = 2 s	Min = 15.6 ms

See Figure 6 to visualize the values named in the table. Table 1 describes the upper and lower boundary settings. For an application, the important boundaries are the $t_{boundary,max}$ and $t_{window,min}$. Within these values, the watchdog timer should be retriggered to avoid a timeout condition or a boundary violation in the event of a trigger pulse in the lower boundary. The values in Table 1 are typical and worst case conditions. These values are valid over the whole temperature range of –40°C to 125°C.

The shaded area shown in Figure 6 cannot be predicted if the device detects a violation or not and releases a reset. This case is also true for the area between the boundary tolerance of $t_{boundary,min}$ and $t_{boundary,max}$ as well as between $t_{window,min}$ and $t_{window,max}$. Setting up the trigger pulses accordingly to avoid violations in these areas is important.

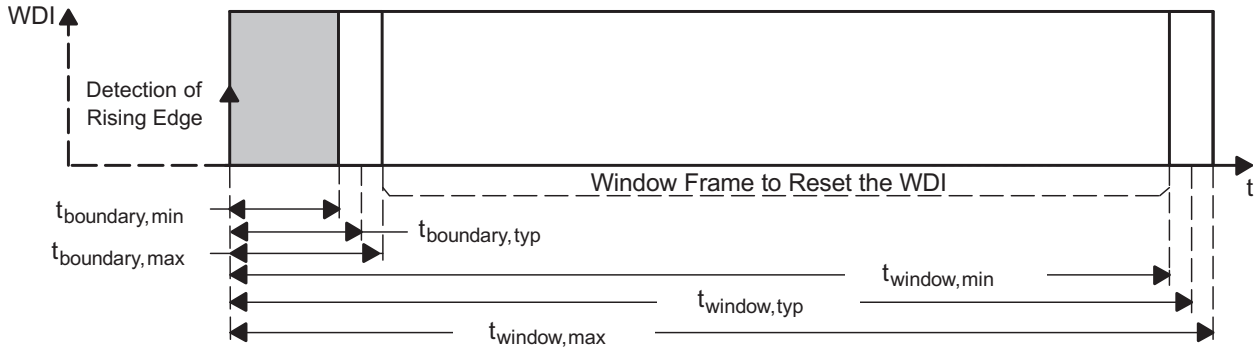


Figure 6. Upper and Lower Boundary Visualization

7.3.1.1 Timing Rules of Window-Watchdog

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses must fit into the configured window frame.

The lower boundary of the watchdog window begins with the rising edge of the WDI trigger pulse. At the same time, all internal timers are reset. If an external capacitor is used, the lower boundary is impacted because of the different oscillator frequency. See the *Programming Window-Watchdog Using an External Capacitor* section for additional details. Figure 7, especially the shaded boundary area, was prepared in a nonreal ratio scale to better visualize the description.

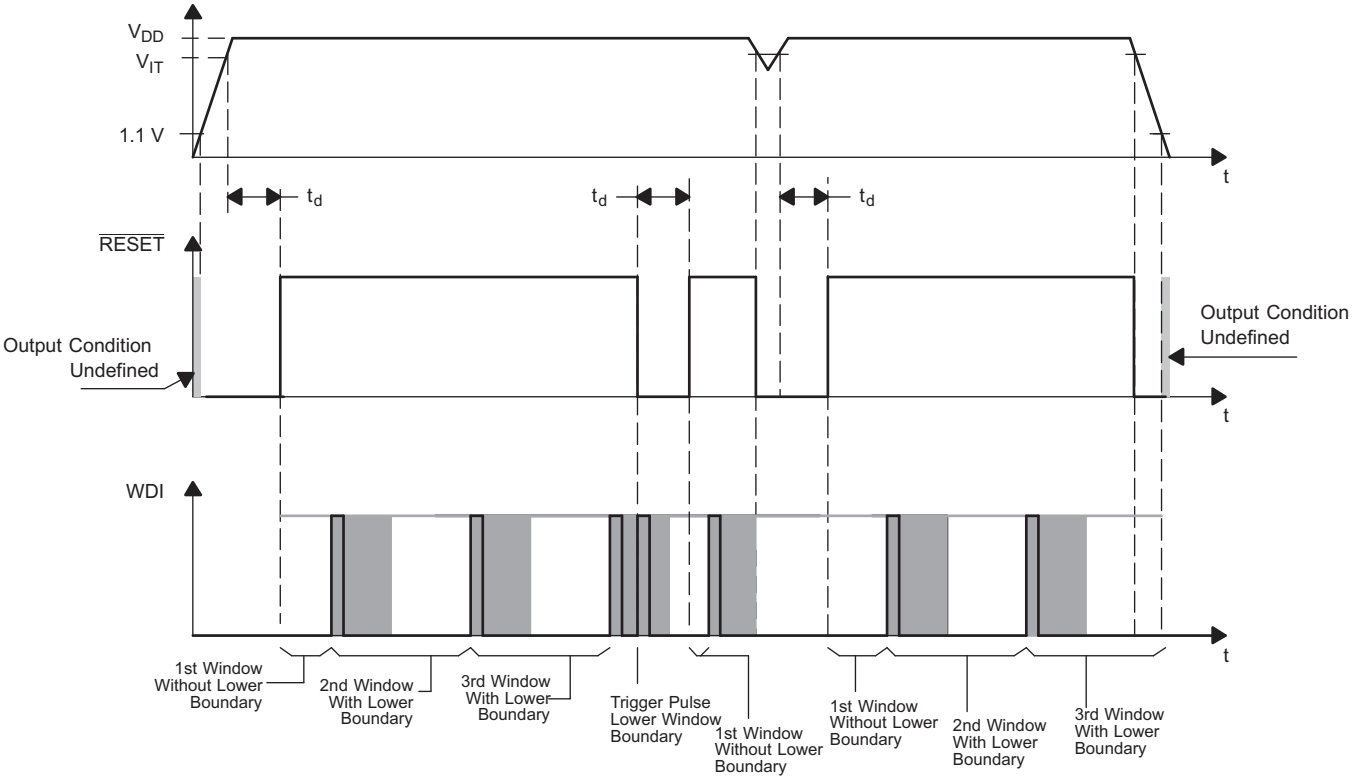


Figure 7. Timing Diagram

7.3.2 Watchdog Software Considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, TI recommends that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses should be set to different timings inside the window frame to release a defined reset if the program should hang in any subroutine. This setting allows the window watchdog to detect timeouts of the trigger pulse as well as pulses that distort the lower boundary.

7.4 Device Functional Modes

The functional mode for the TPS3813-Q1 family family of devices is either on or reset. Table 2 lists the device truth table.

Table 2. Device States

CONDITION	STATE	$\overline{\text{RESET}}$
$V_{DD} > V_{IT}$	On	H
$V_{DD} < V_{IT}$	Reset	L
Watchdog fault		

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Lower-Boundary Calculation

The lower boundary can be calculated based on the values listed in the *Switching Characteristics* table. Additionally, facts must be taken into account to verify that the lower boundary is where it is expected. Because the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin is taken into account at the next internal clock cycle. Accounting for any rising edge at the WDI pin occurs regardless of the external source. Because the shift between internal and external clock is not known, consider the worst-case condition when calculating this value.

Table 3. Watchdog Lower-Boundary Calculation

SELECTED OPERATION MODE		LOWER BOUNDARY OF FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V	$t_{boundary,max} = t_{window,max} / 23.5$
		$t_{boundary,typ} = t_{window,typ} / 25.8$
		$t_{boundary,min} = t_{window,min} / 28.7$
	WDR = V_{DD}	$t_{boundary,max} = t_{window,max} / 51.6$
		$t_{boundary,typ} = t_{window,typ} / 64.5$
		$t_{boundary,min} = t_{window,min} / 92.7$

8.2 Typical Application

A typical application example (see Figure 8) is used to describe the function of the watchdog in more detail.

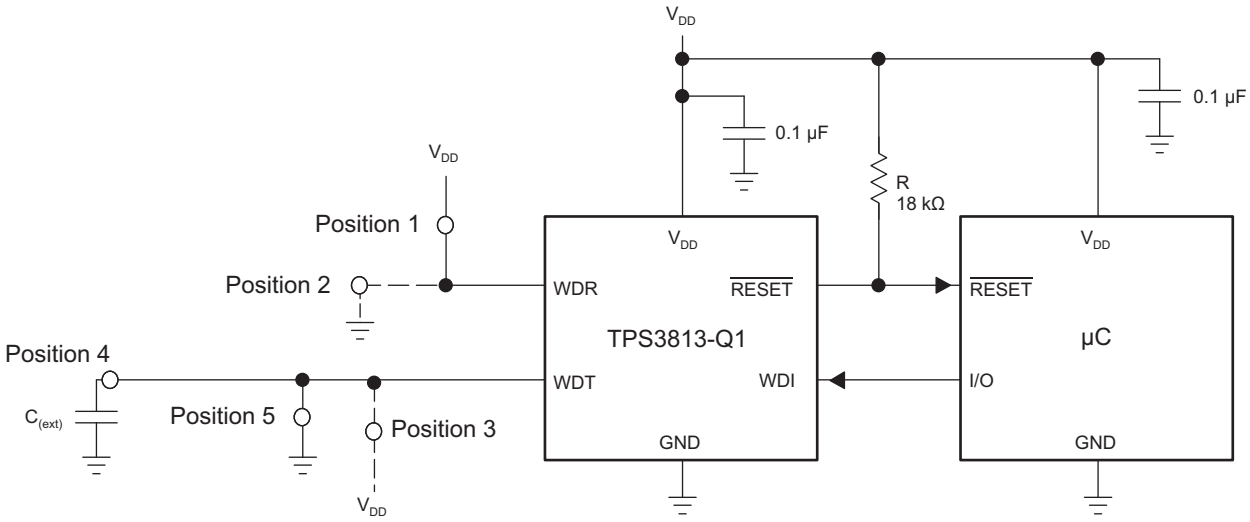


Figure 8. Application Example

Typical Application (continued)

8.2.1 Design Requirements

Design requirements include any design parameters that are solely based on the watchdog timing desired by the user. The *Implemented Window-Watchdog Settings* and *Detailed Design Procedure* sections describe these timings. Select the TPS3813-Q1 device option based on desired threshold voltage of either 2.5 V, 3 V, 3.3 V, or 5 V.

8.2.2 Detailed Design Procedure

To configure the window watchdog function, two pins are provided by the TPS3813-Q1 family of devices. These pins set the window timeout and ratio.

The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. This ratio can be configured in two different frame sizes.

If the window watchdog ratio pin (WDR) is set to V_{DD} (Position 1 in Figure 8) then the lower window frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:124.9, for WDT connected to V_{DD}, the value is a ratio of 1:127.7, and for an external capacitor connected to WDT, the value is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND (Position 2) the lower window frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:31.8, for WDT connected to V_{DD} the value is a ratio 1:32, and for an external capacitor connected to WDT the value is a ratio of 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 s and 2.5 s for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

For example, if the watchdog timeout pin (WDT) is connected to V_{DD}, the timeout is 2.5 s. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD}, the lower boundary is 19.6 ms.

8.2.2.1 Programming Window-Watchdog Using an External Capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. The capacitors that are used should have low ESR and low tolerances because the tolerances must be considered to perform the calculations. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{boundary,max}$ and $t_{window,min}$. The trigger pulse must fit into this window frame.

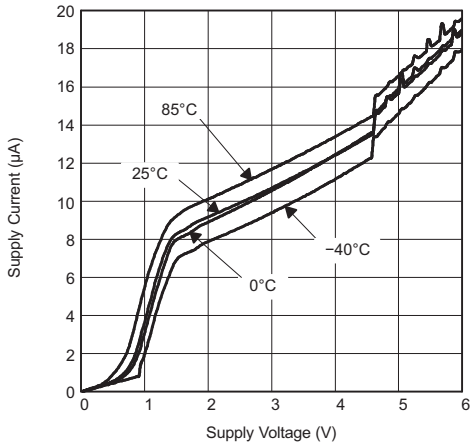
The external capacitor should have a value between a minimum of 155 pF and a maximum of 63 nF.

$$t_{window,typ} = \left(\frac{C_{(ext)}}{15.55\ pF} \right) \times 6.25\ ms \quad (1)$$

Table 4. Watchdog Upper-Boundary Capacitor Programming

SELECTED OPERATION MODE		WINDOW FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V and WDR = V_{DD}	$t_{window,max} = 1.25 \times t_{window,typ}$
		$t_{window,min} = 0.75 \times t_{window,typ}$

8.2.3 Application Curve



WDI = GND WDT = GND WDR = GND

Figure 9. Supply Current vs Supply Voltage

9 Power Supply Recommendations

TPS3813-Q1 family of devices are designed to operate from an input supply with a voltage range from 2 V to 6 V. Although not required, placing a 0.1-µF ceramic capacitor close to the V_{DD} pin is good analog design practice.

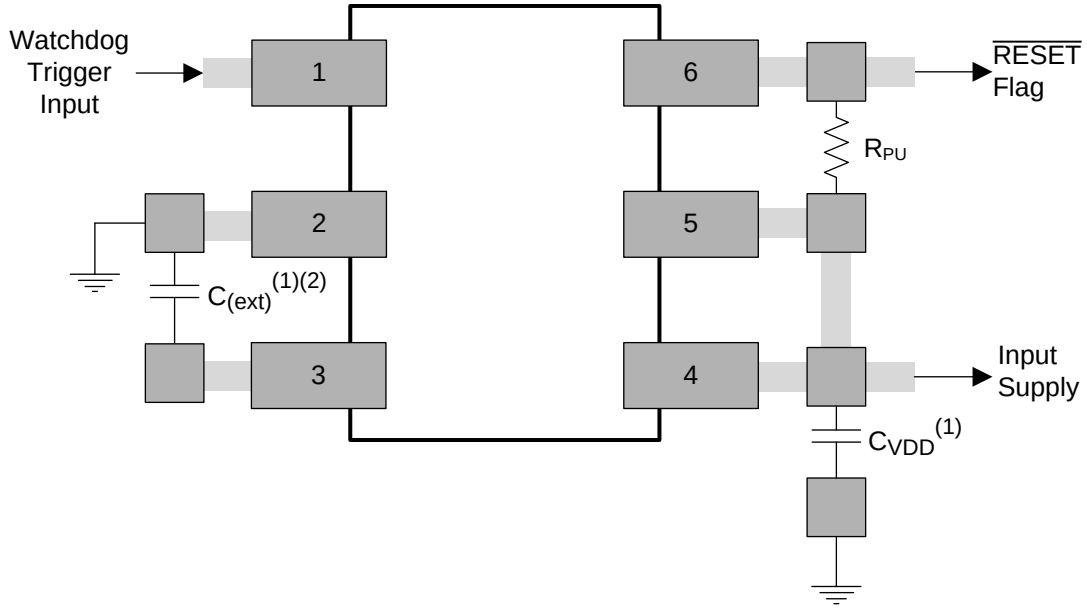
10 Layout

10.1 Layout Guidelines

Use the following guidelines for proper layout design of the device:

- Place the V_{DD} decoupling capacitor as close to the device as possible.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor, along with the parasitic inductance from the supply to the capacitor, can cause ringing if the traces are excessive.
- If using a capacitor between the WDT pin and GND pin to program the upper boundary of the window-watchdog, the capacitor must be placed as close to the device as possible.
- Traces for WDR and WDT pins must be short and tight to avoid building up excessive parasitics.

10.2 Layout Example



(1) In this layout example, the WDR pin is tied to V_{DD} and the WDT pin is tied to GND through an external capacitor.

(2) The overall window timeout in this configuration is based on the external capacitor connected to the WDT pin. The formula used to calculate this value can be found in the *Detailed Design Procedure* section.

NOTE: In this configuration, the ratio of the frame lower boundary is 1:64.5 (typical) of the overall window timeout size. The maximum and minimum ratios are 1:51.6 and 1:92.7 of the overall window timeout size, respectively.

Figure 10. Device Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 11 shows a legend for reading the complete device name for and DRV5013 device.

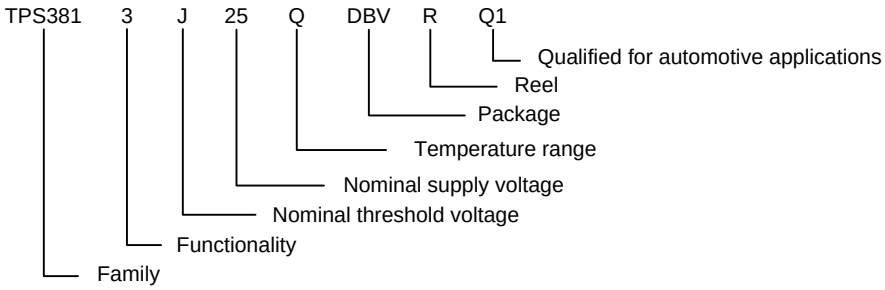


Figure 11. Device Nomenclature

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *All Window–Watchdog Supervisors*, SLVA365
- *Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs*, SLVA485
- *Disabling the Watchdog Timer for TI's Family of Supervisors*, SLVA145

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3813K33-Q1	Click here	Click here	Click here	Click here	Click here
TPS3813I50-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3813I50QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBI	Samples
TPS3813K33QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3813I50-Q1, TPS3813K33-Q1 :

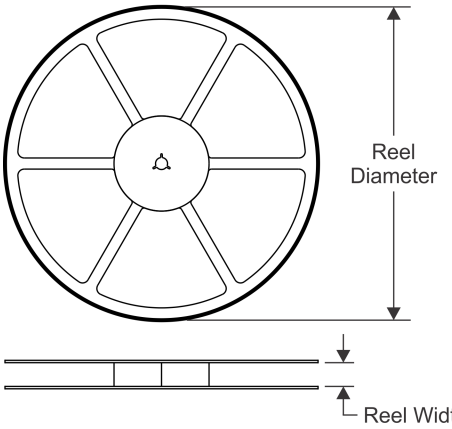
- Catalog: TPS3813I50, TPS3813K33
- Enhanced Product: TPS3813K33-EP

NOTE: Qualified Version Definitions:

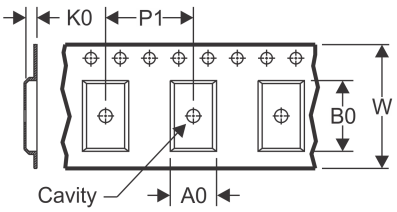
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

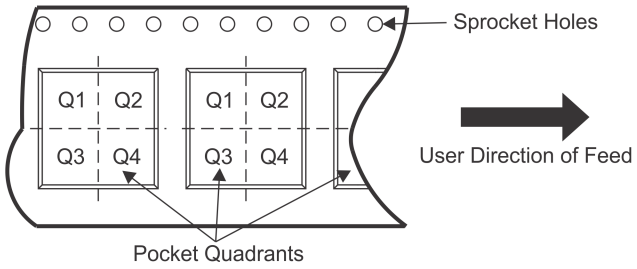


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

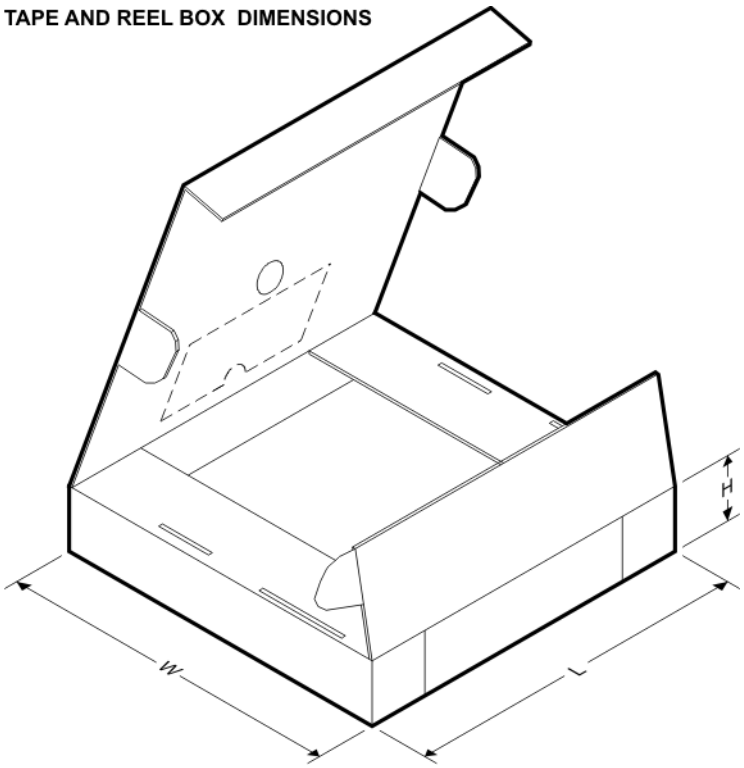
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

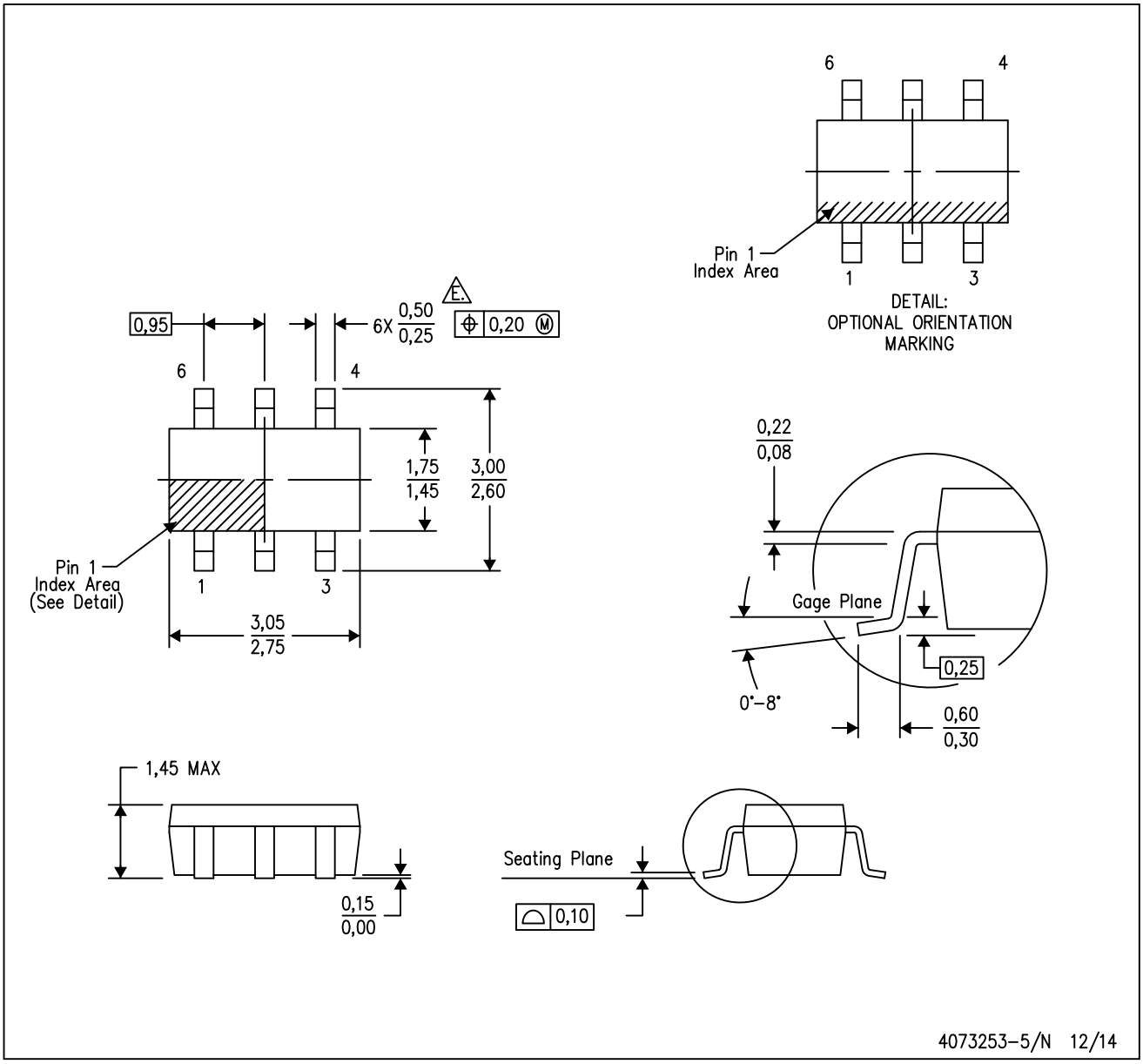
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

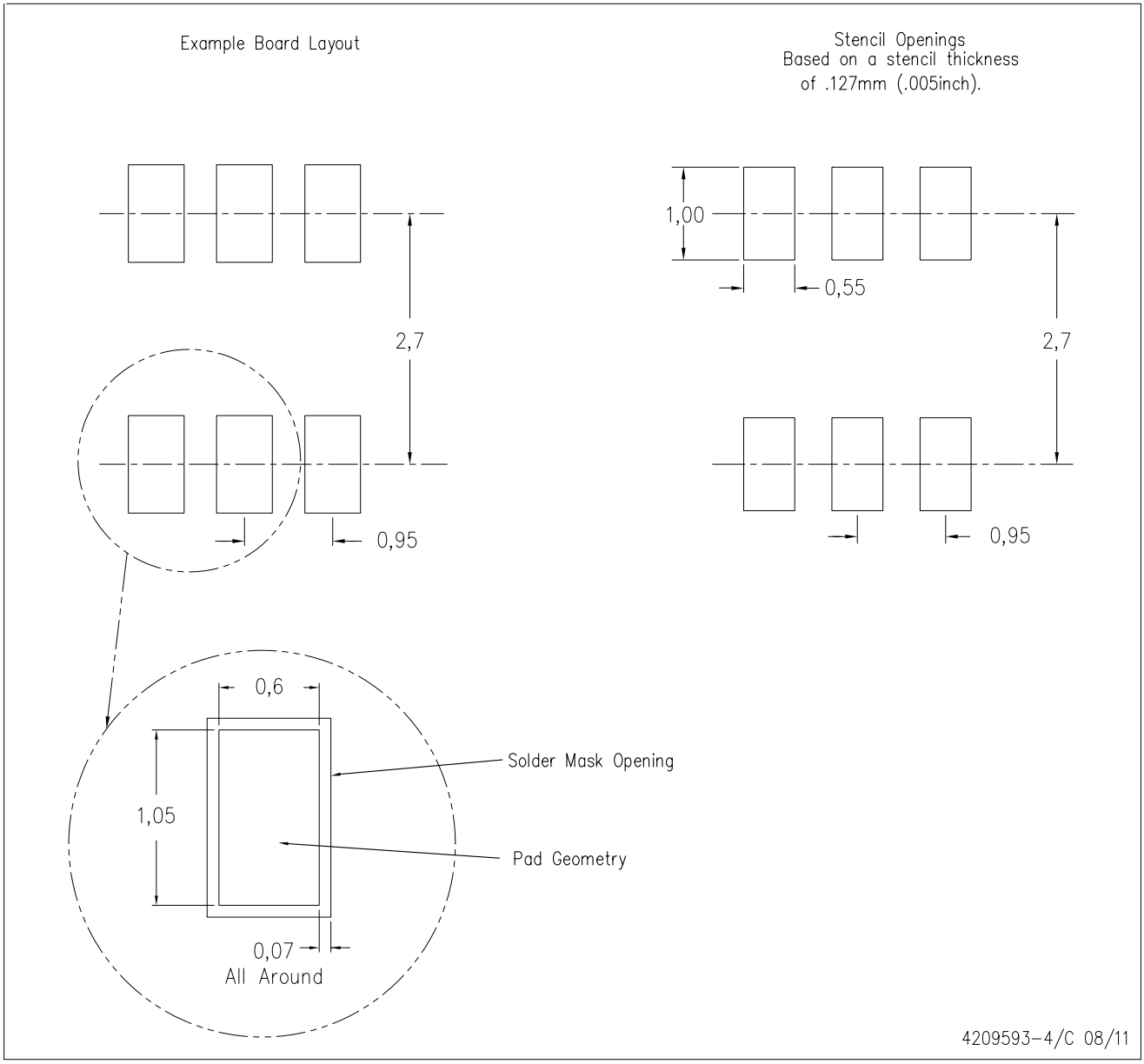
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	182.0	182.0	20.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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