High-Frequency 4-A Sink Synchronous MOSFET Driver

FEATURES

- **Drives Two N-Channel MOSFETs with 14-ns Adaptive Dead Time**
- **Wide Gate Drive Voltage: 4.5V Up to 8.8V With Best Efficiency at 7V to 8V**
- **Wide Power System Train Input Voltage: 3V Up to 27V**
- **Wide Input PWM Signals: 2.0V up to 13.2-V Amplitude**
- **Capable Drive MOSFETs with ≥40-A Current per Phase**
- **High Frequency Operation: 14ns Propagation Delay and 10ns Rise/Fall Time Allow Fsw - 2MHz**
- **Capable Propagate <30-ns Input PWM Pulses**
- **Low-Side Driver Sink On-Resistance (0.4Ω) Prevents dV/dT Related Shoot-Through Current**
- **3-State PWM Input for Power Stage Shutdown**
- **Space Saving Enable (input) and Power Good (output) Signals on Same Pin**
- **Thermal Shutdown**
- **UVLO Protection**
- **Internal Bootstrap Diode**
- **Economical SOIC-8 and Thermally Enhanced 3-mm x 3-mm DFN-8 Packages**
- **High Performance Replacement for Popular 3-State Input Drivers**

APPLICATIONS

- **Multi-Phase DC-to-DC Converters with Analog or Digital Control**
- **Desktop and Server VRMs and EVRDs**
- **Portable/Notebook Regulators**
- **Synchronous Rectification for Isolated Power Supplies**

DESCRIPTION

The TPS28225 is a high-speed driver for N-channel complimentary driven power MOSFETs with adaptive dead-time control. This driver is optimized for use in variety of high-current one and multi-phase dc-to-dc converters. The TPS28225 is a solution that provides highly efficient, small size low EMI emmissions.

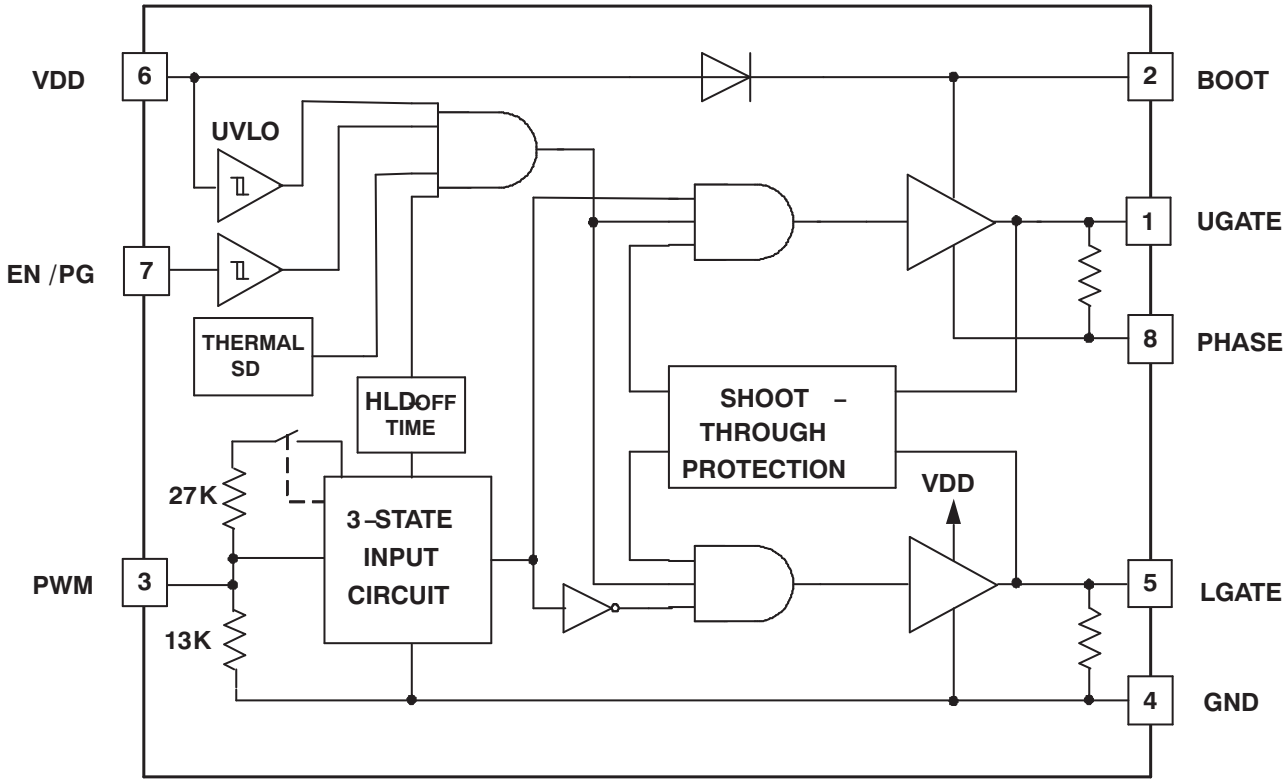
The performance is achieved by up to 8.8-V gate drive voltage, 14-ns adaptive dead-time control, 14-ns propagation delays and high-current 2-A source and 4-A sink drive capability. The 0.4-Ω impedance for the lower gate driver holds the gate of power MOSFET below its threshold and ensures no shoot-through current at high dV/dt phase node transitions. The bootstrap capacitor charged by an internal diode allows use of N-channel MOSFETs in half-bridge configuration.

The TPS28225 features a 3-state PWM input compatible with all multi-phase controllers employing 3-state output feature. As long as the input stays within 3-state window for the 250-ns hold-off time, the driver switches both outputs low. This shutdown mode prevents a load from the reversed-output-voltage.

The other features include under voltage lockout, thermal shutdown and two-way enable/power good signal. Systems without 3-state featured controllers can use enable/power good input/output to hold both outputs low during shutting down.

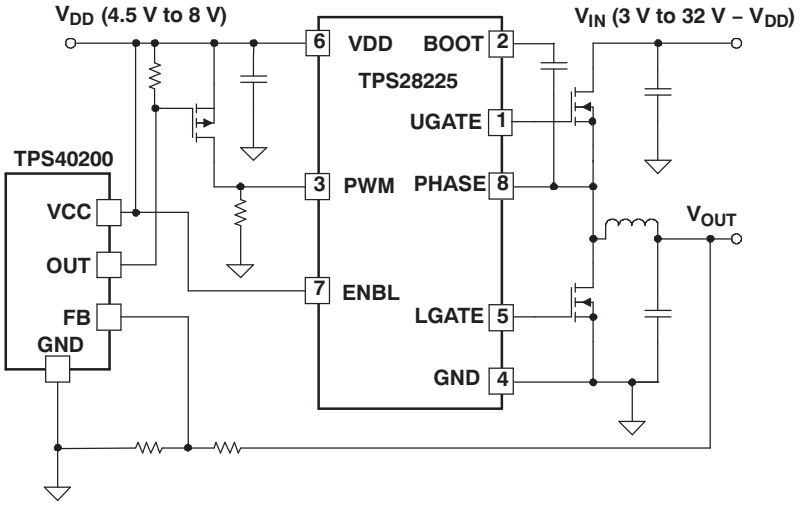
The TPS28225 is offered in an economical SOIC-8 and thermally enhanced low-size Dual Flat No-Lead (DFN-8) packages. The driver is specified in the extended temperature range of –40°C to 125°C with the absolute maximum junction temperature 150°C.

FUNCTIONAL BLOCK DIAGRAM



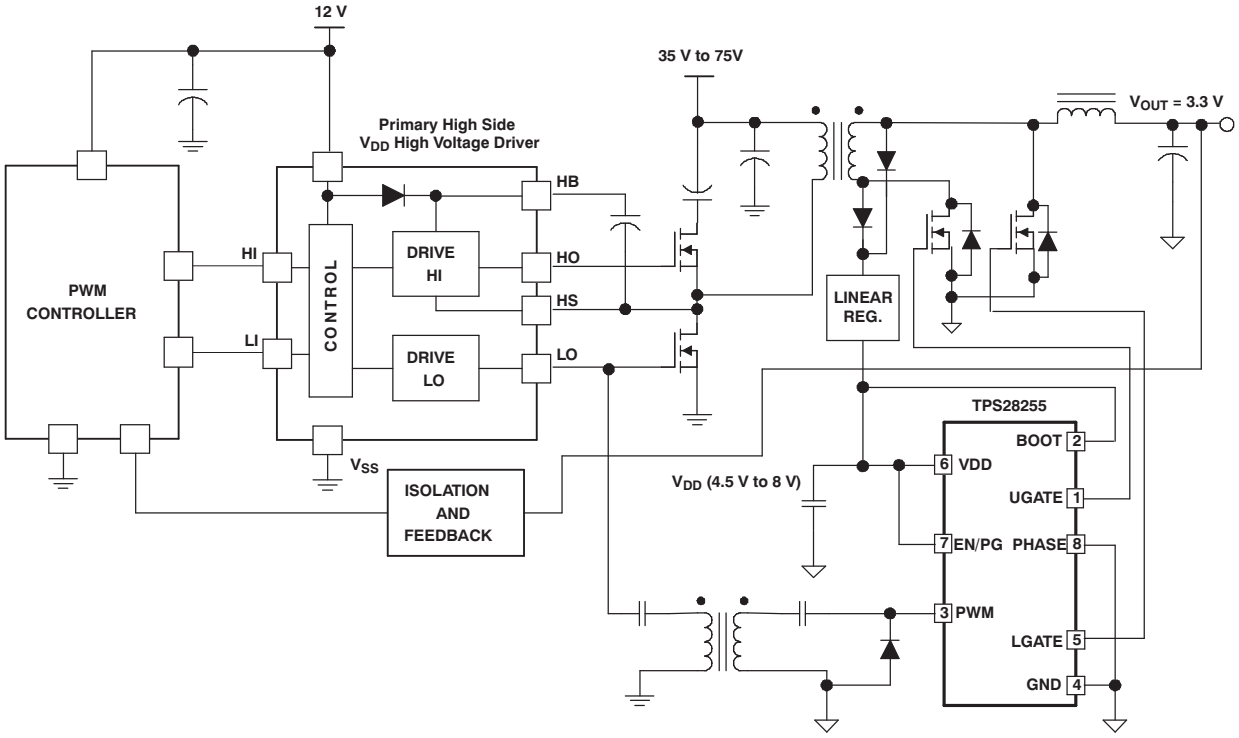
TYPICAL APPLICATIONS

One-Phase POL Regulator



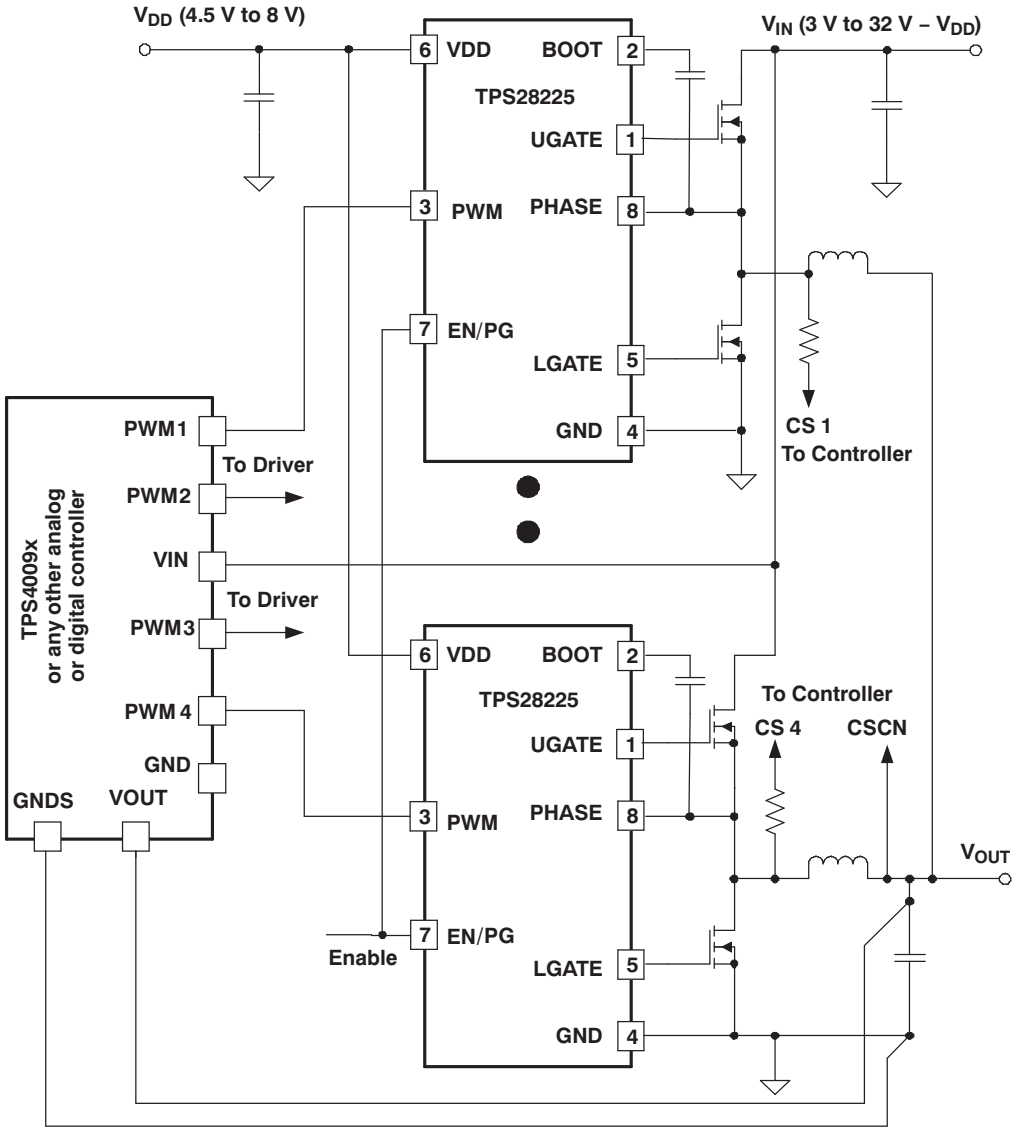
TYPICAL APPLICATIONS (continued)

Driver for Synchronous Rectification with Complementary Driven MOSFETs



TYPICAL APPLICATIONS (continued)

Multi-Phase Synchronous Buck Converter



ORDERING INFORMATION (1)(2)(3)

TEMPERATURE RANGE, $T_A = T_J$	PACKAGE	TAPE AND REEL QTY.	PART NUMBER
-40°C to 125°C	Plastic 8-pin SOIC (D)	250	TPS28225DT
	Plastic 8-pin SOIC (D)	2500	TPS28225DR
	Plastic 8-pin DFN (DRB)	250	TPS28225DRBT
	Plastic 8-pin DFN (DRB)	3000	TPS28225DRBR

(1) SOIC-8 (D) and DFN-8 (DRB) packages are available taped and reeled. Add T suffix to device type (e.g. TPS28225DT) to order taped devices and suffix R to device type to order reeled devices.
(2) The SOIC-8 (D) and DFN-8 (DRB) package uses in Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(3) In the DFN package, the pad underneath the center of the device is a thermal substrate. The PCB “thermal land” design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the DFN to achieve its full thermal potential. This pad should be either grounded for best noise immunity, and it should not be connected to other nodes.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

TPS28225		VALUE	UNIT
Input supply voltage range, V_{DD} (3)		–0.3 to 8.8	V
Boot voltage, V_{BOOT}		–0.3 to 33	
Phase voltage, V_{PHASE}	DC	–2 to 32 or V_{BOOT} + 0.3 – V_{DD} whichever is less	
	Pulse < 400 ns, E = 20 µJ	–7 to 33.1 or V_{BOOT} + 0.3 – V_{DD} whichever is less	
Input voltage range, V_{PWM}, $V_{EN/PG}$		–0.3 to 13.2	
Output voltage range, V_{UGATE}		V_{PHASE}– 0.3 to V_{BOOT} + 0.3, (V_{BOOT}– V_{PHASE} < 8.8)	
	Pulse < 100 ns, E = 2 µJ	V_{PHASE}– 2 to V_{BOOT} + 0.3, (V_{BOOT}– V_{PHASE} < 8.8)	
Output voltage range, V_{LGATE}		–0.3 to V_{DD} + 0.3	
	Pulse < 100 ns, E = 2 µJ	–2 to V_{DD} + 0.3	
ESD rating, HBM		2 k	
ESD rating, HBM ESD rating, CDM		500	
Continuous total power dissipation		See Dissipation Rating Table	
Operating virtual junction temperature range, T_J		–40 to 150	°C
Operating ambient temperature range, T_A		–40 to 125	
Storage temperature, T_{stg}		–65 to 150	
Lead temperature (soldering, 10 sec.)		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.

DISSIPATION RATINGS(1)

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C POWER RATING	T_A =70°C POWER RATING	T_A = 85°C POWER RATING
High-K(2)	D	39.4°C/W	100°C/W	10 mW/°C	1.25 W	0.8 W	0.65 W
High-K(3)	DRB	1.4°C/W	48.5°C/W	20.6 mW/°C	2.58 W	1.65 W	1.34 W

(1) These thermal data are taken at standard JEDEC test conditions and are useful for the thermal performance comparison of different packages. The cooling condition and thermal impedance $R_{\theta JA}$ of practical design is specific.
(2) The JEDEC test board JESD51-7, 3-inch x 3-inch, 4-layer with 1-oz internal power and ground planes and 2-oz top and bottom trace layers.
(3) The JEDEC test board JESD51-5 with direct thermal pad attach, 3-inch x 3-inch, 4-layer with 1-oz internal power and ground planes and 2-oz top and bottom trace layers.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Input supply voltage	4.5	7.2	8	V
V_{IN}	Power input voltage	3		32 $V_{–VDD}$	
T_J	Operating junction temperature range	–40		125	°C

ELECTRICAL CHARACTERISTICS(1)

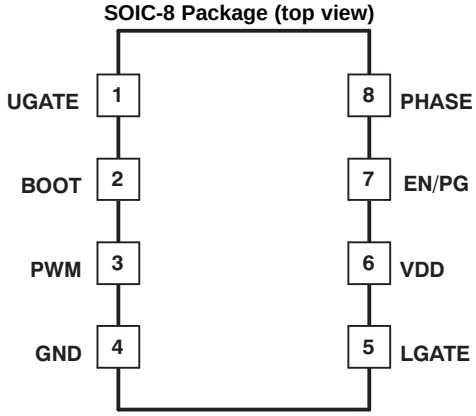
V_{DD} = 7.2 V, EN/PG pulled up to V_{DD} by 100-kΩ resistor, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCKOUT						
	Rising threshold	V_{PWM} = 0 V	3.2	3.5	3.8	V
	Falling threshold	V_{PWM} = 0 V	2.7	3.0		
	Hysteresis			0.5		
BIAS CURRENTS						
$I_{DD(off)}$	Bias supply current	$V_{EN/PG}$ = low, PWM pin floating		350		µA
I_{DD}	Bias supply current	$V_{EN/PG}$ = high, PWM pin floating		500		
INPUT (PWM)						
I_{PWM}	Input current	V_{PWM} = 5 V		185		µA
		V_{PWM} = 0 V		–200		
	PWM 3-state rising threshold(2)			1.0		V
	PWM 3-state falling threshold	V_{PWM} PEAK = 5 V	3.4	3.8	4.0	
t_{HLD_R}	3-state shutdown Hold-off time			250		ns
T_{MIN}	PWM minimum pulse to force U_{GATE} pulse	C_L = 3 nF at U_{GATE} , V_{PWM} = 5 V		30		
ENABLE/POWER GOOD (EN/PG)						
	Enable high rising threshold	PG FET OFF		1.7	2.1	V
	Enable low falling threshold	PG FET OFF	0.8	1.0		
	Hysteresis		0.35	0.70		
	Power good output	V_{DD} = 2.5 V			0.2	
UPPER GATE DRIVER OUTPUT (UGATE)						
	Source resistance	500 mA source current		1.0	2.0	Ω
	Source current (2)	$V_{UGATE-PHASE}$ = 2.5 V		2.0		A
t_{RU}	Rise time	C_L = 3 nF		10		ns
	Sink resistance	500 mA sink current		1.0	2.0	Ω
	Sink current (2)	$V_{UGATE-PHASE}$ = 2.5 V		2.0		A
t_{FU}	Fall time	C_L = 3 nF		10		ns
LOWER GATE DRIVER OUTPUT (LGATE)						
	Source resistance	500 mA source current		1.0	2.0	Ω
	Source current(2)	V_{LGATE} = 2.5 V		2.0		A
t_{RL}	Rise time(2)	C_L = 3 nF		10		ns
	Sink resistance	500 mA sink current		0.4	1.0	Ω
	Sink current(2)	V_{LGATE} = 2.5 V		4.0		A
	Fall time(2)	C_L = 3 nF		5		ns
SWITCHING TIME						
t_{DLU}	UGATE turn-off propagation Delay	C_L = 3 nF		14		ns
t_{DLL}	LGATE turn-off propagation Delay	C_L = 3 nF		14		
t_{DTU}	Dead time LGATE turn-off to UGATE turn-on	C_L = 3 nF		14		
t_{DTL}	Dead time UGATE turn-off to LGATE turn-on	C_L = 3 nF		14		
BOOTSTRAP DIODE						
V_F	Forward voltage	Forward bias current 100 mA		1.0		V
THERMAL SHUTDOWN						
	Rising threshold(2)		150	160	170	°C
	Falling threshold(2)		130	140	150	
	Hysteresis			20		

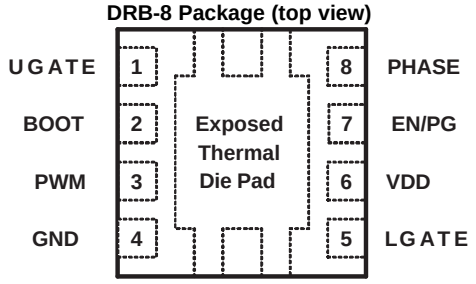
(1) Typical values for T_A = 25°C
(2) Not tested in production

DEVICE INFORMATION

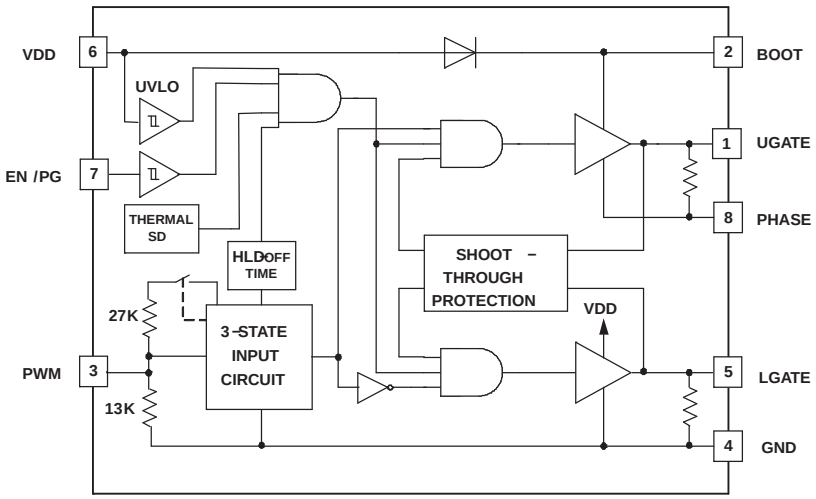
SOIC-8 Package (top view)



DRB-8 Package (top view)



FUNCTIONAL BLOCK DIAGRAM

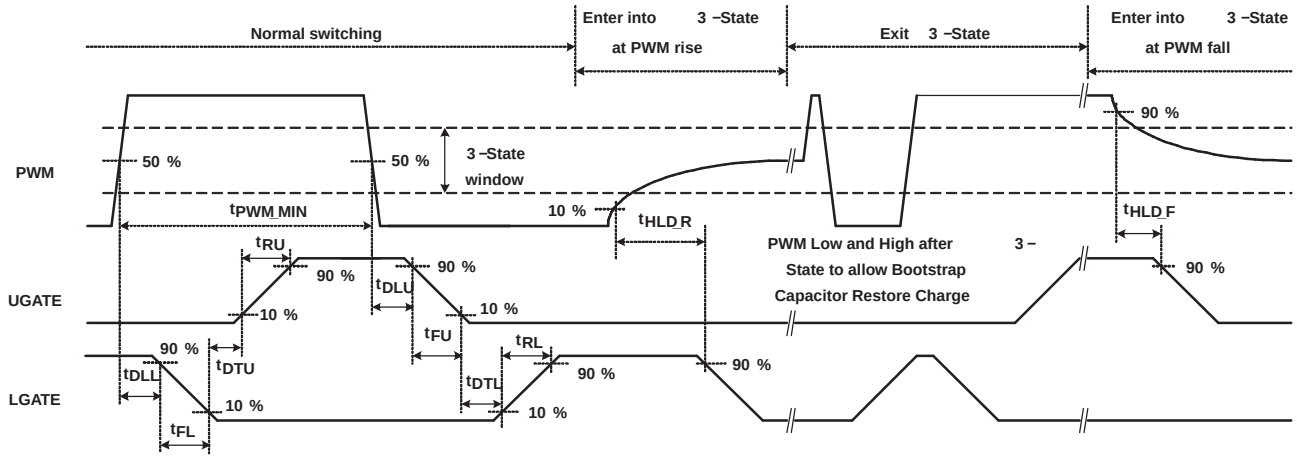


A. For the TPS28224DRB device the thermal PAD on the bottom side of package must be soldered and connected to the GND pin and to the GND plane of the PCB in the shortest possible way. See Recommended Land Pattern in the Application section.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
SOIC-8	DRB-8	NAME		
1	1	UGATE	O	Upper gate drive sink/source output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	I/O	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
3	3	PWM	I	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the 3-state PWM Input section under DETAILED DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
4	4	GND	—	Ground pin. All signals are referenced to this node.
	Exposed die pad	Thermal pad	—	Connect directly to the GND for better thermal performance and EMI
5	5	LGATE	O	Lower gate drive sink/source output. Connect to the gate of the low-side power N-Channel MOSFET.
6	6	VDD	I	Connect this pin to a 5-V bias supply. Place a high quality bypass capacitor from this pin to GND.
7	7	EN/PG	I/O	Enable/Power Good input/output pin with 1MΩ impedance. Connect this pin to HIGH to enable and LOW to disable the IC. When disabled, the device draws less than 350µA bias current. If the V_{DD} is below UVLO threshold or over temperature shutdown occurs, this pin is internally pulled low.
8	8	PHASE	I	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

TIMING DIAGRAM



TRUTH TABLE

PIN	V_{DD} RISING < 3.5 V OR T_J > 160°C	V_{DD} FALLING > 3 V AND T_J < 150°C			
		EN/PG RISING < 1.7 V	EN/PG FALLING > 1.0 V		
			PWM < 1 V	PWM > 1.5 V AND T_{RISE}/T_{FALL} < 200 ns	PWM SIGNAL SOURCE IMPEDANCE >40 kΩ FOR > 250ns (3-State)(1)
LGATE	Low	Low	High	Low	Low
UGATE	Low	Low	Low	High	Low
EN/PG	Low				

(1) To exit the 3-state condition, the PWM signal should go low. One Low PWM input signal followed by one High PWM input signal is required before re-entering the 3-state condition.

TYPICAL CHARACTERISTICS

BIAS SUPPLY CURRENT vs TEMPERATURE ($V_{EN/PG}$ = Low, PWM Input Floating, V_{DD} = 7.2V)

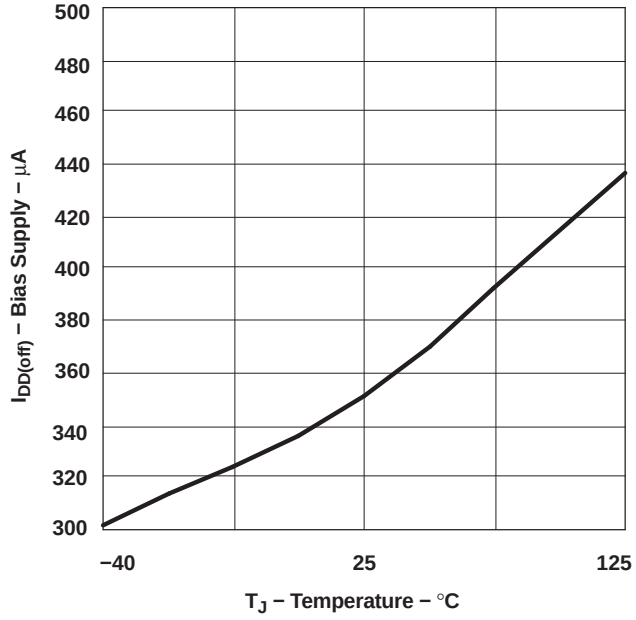


Figure 1.

UNDER VOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

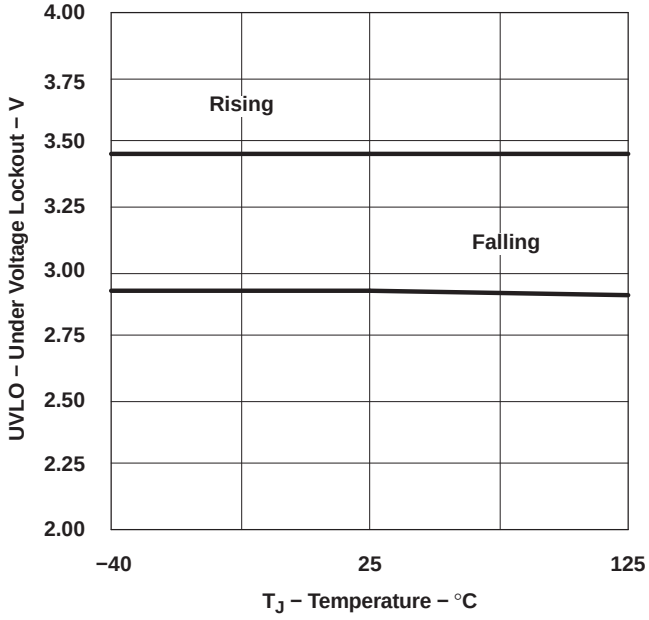


Figure 2.

ENABLE/POWER GOOD THRESHOLD vs TEMPERATURE (V_{DD} = 7.2 V)

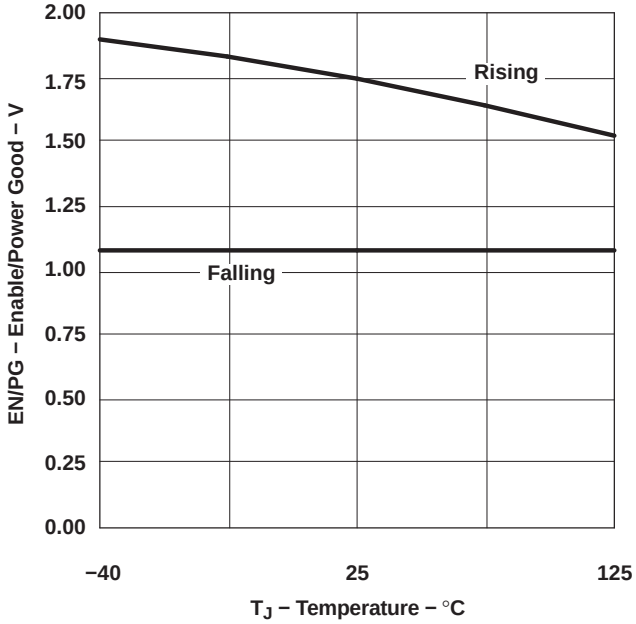


Figure 3.

PWM 3-STATE THRESHOLDS, (5-V Input Pulses) vs TEMPERATURE, (V_{DD} = 7.2 V)

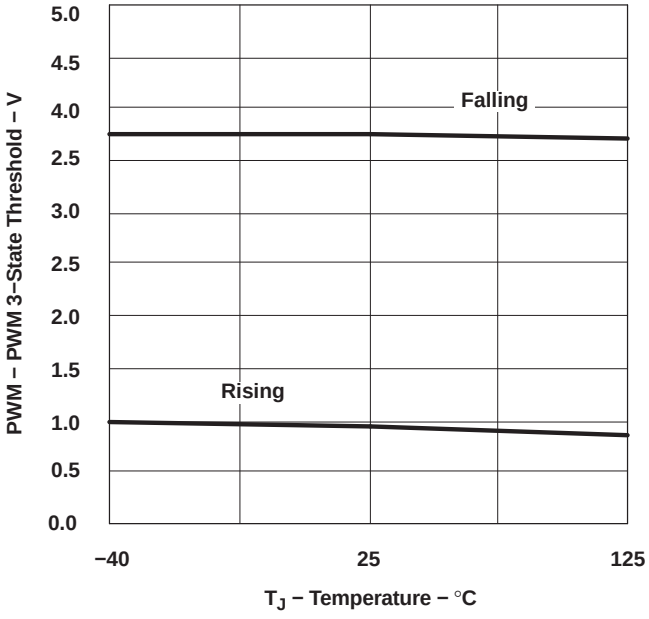


Figure 4.

TYPICAL CHARACTERISTICS (continued)

UGATE DC OUTPUT IMPEDANCE
vs
TEMPERATURE, (V_{DD} = 7.2 V)

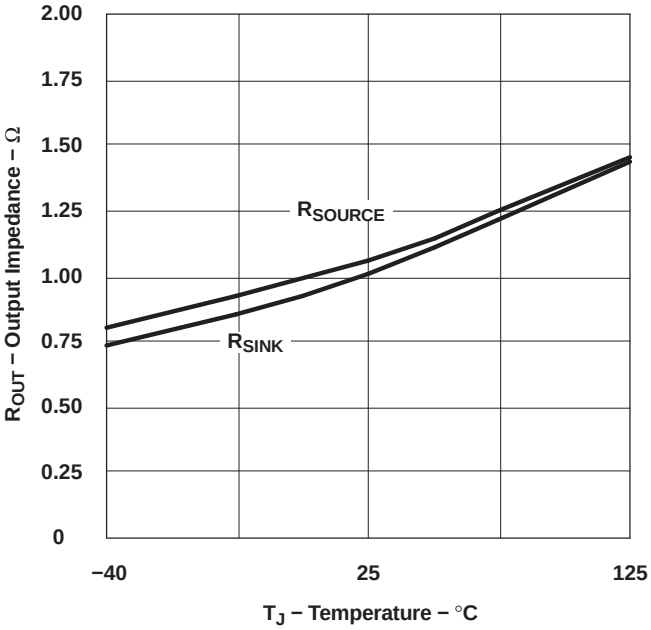


Figure 5.

LGATE DC OUTPUT IMPEDANCE
vs
TEMPERATURE (V_{DD} = 7.2 V)

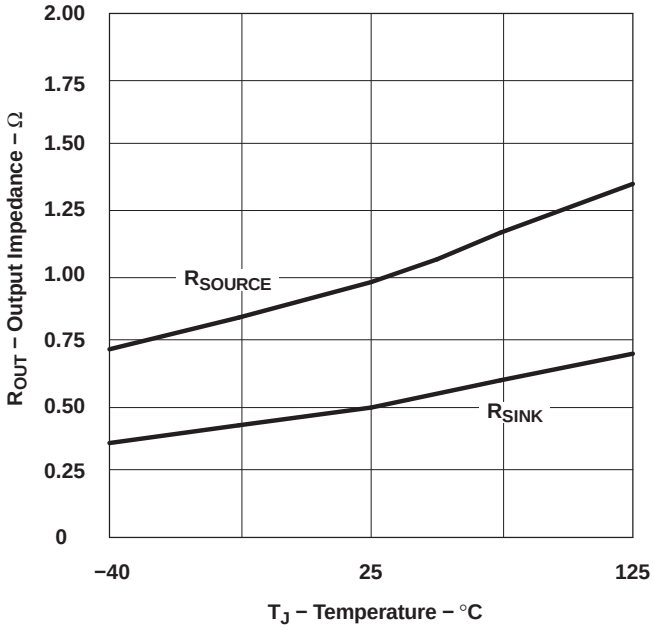


Figure 6.

UGATE RISE AND FALL TIME
vs
TEMPERATURE (V_{DD} = 7.2 V, C_{LOAD} = 3 nF)

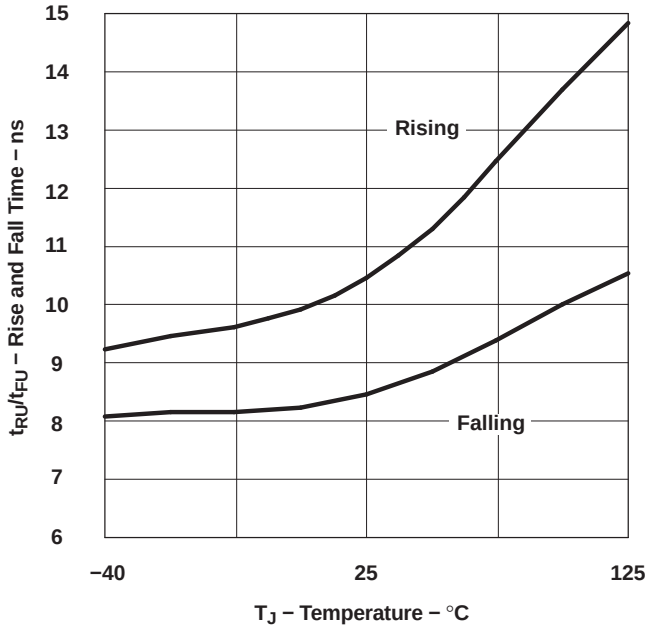


Figure 7.

LGATE RISE AND FALL TIME
vs
TEMPERATURE (V_{DD} = 7.2 V, C_{LOAD} = 3 nF)

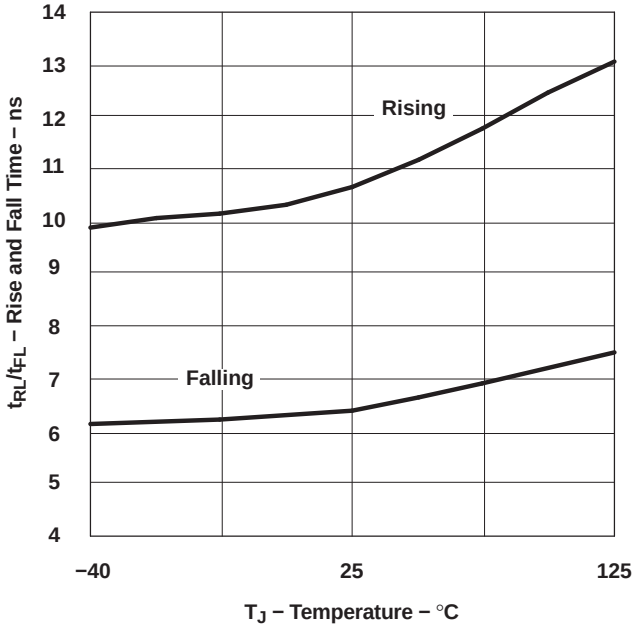


Figure 8.

TYPICAL CHARACTERISTICS (continued)

UGATE AND LGATE (Turning OFF Propagation Delays) vs TEMPERTURE (V_{DD} = 7.2 V, C_{LOAD} = 3 nF)

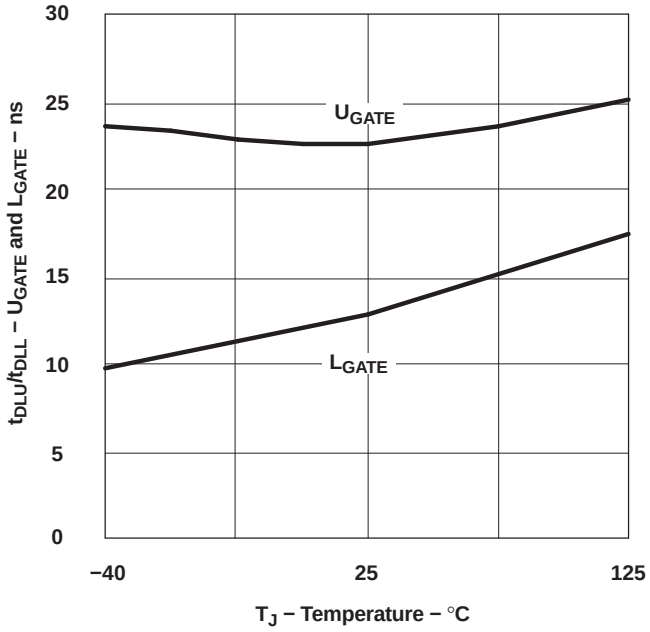


Figure 9.

UGATE AND LGATE (Dead Time) vs TEMPERTURE (V_{DD} = 7.2 V, C_{LOAD} = 3 nF)

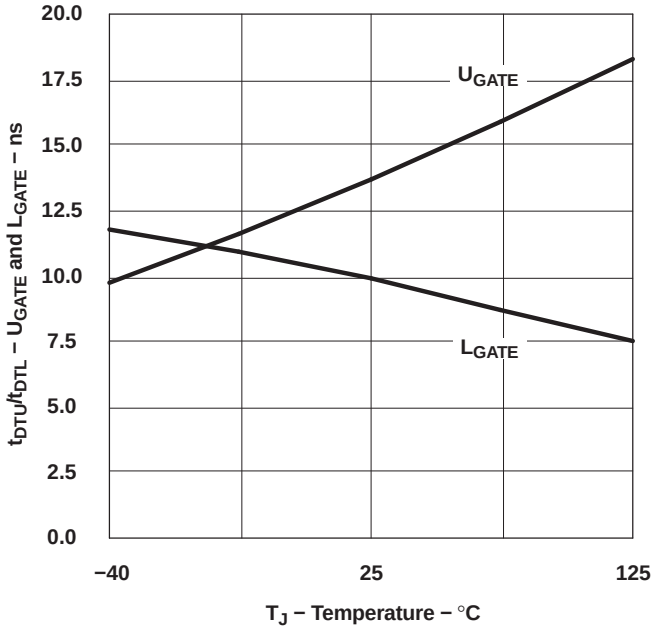


Figure 10.

UGATE MINIMUM SHORT PULSE vs TEMPERATURE (V_{DD} = 7.2 V, C_{LOAD} = 3 nF)

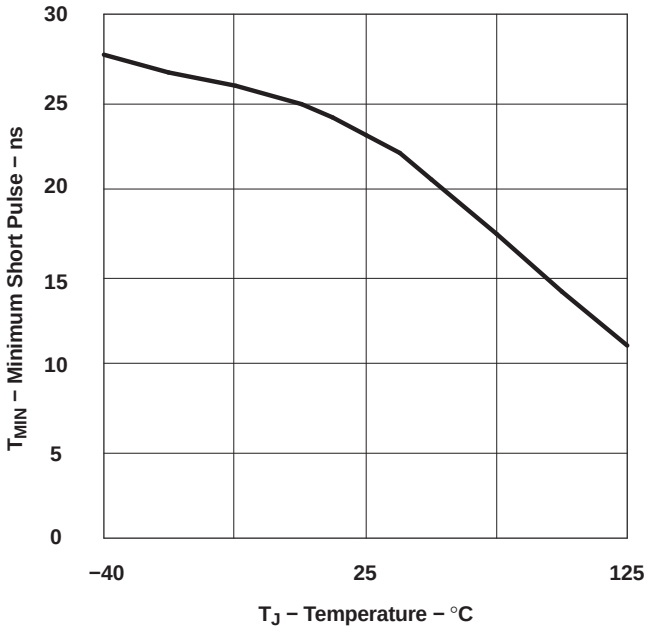


Figure 11.

BOOTSTRAP DIODE FORWARD VOLTAGE vs TEMPERATURE (V_{DD} = 7.2 V, I_F = 100 mA)

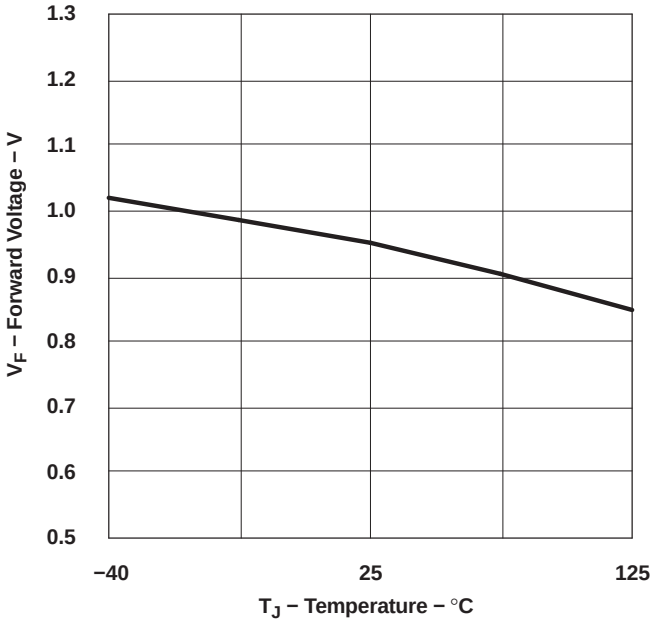


Figure 12.

TYPICAL CHARACTERISTICS (continued)

BIAS SUPPLY CURRENT vs SWITCHING FREQUENCY (V_{DD} = 7.2 V, No Load, T_J = 25°C)

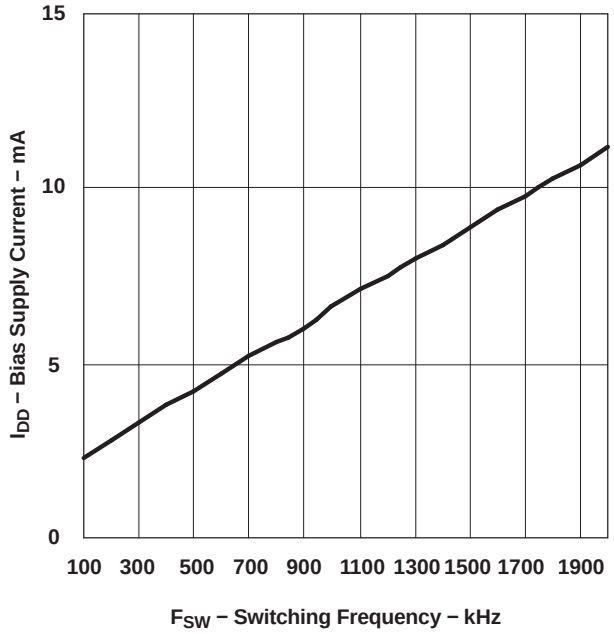


Figure 13.

DRIVER DISSIPATED POWER vs SWITCHING FREQUENCY (Different Load Charge, V_{DD} = 7.2 V, T_J = 25°C)

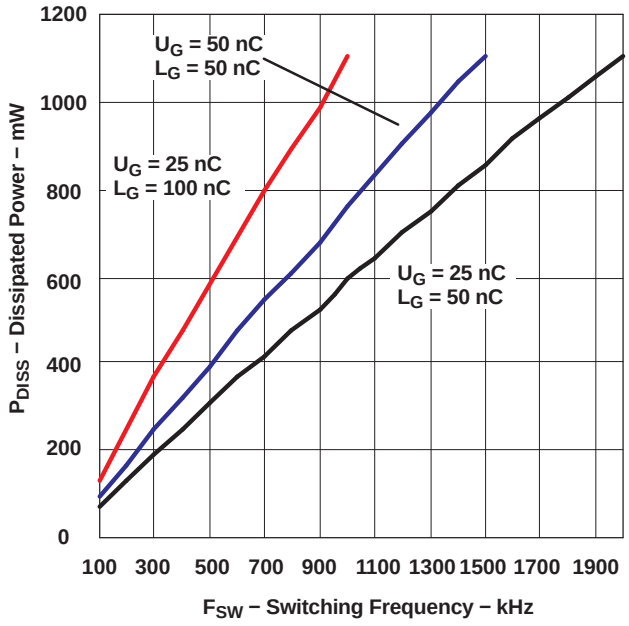


Figure 14.

PWM INPUT RISING SWITCHING WAVEFORMS

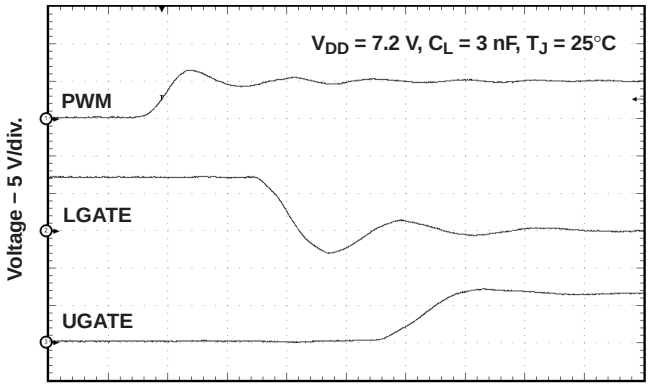


Figure 15.

PWM INPUT FALLING SWITCHING WAVEFORMS

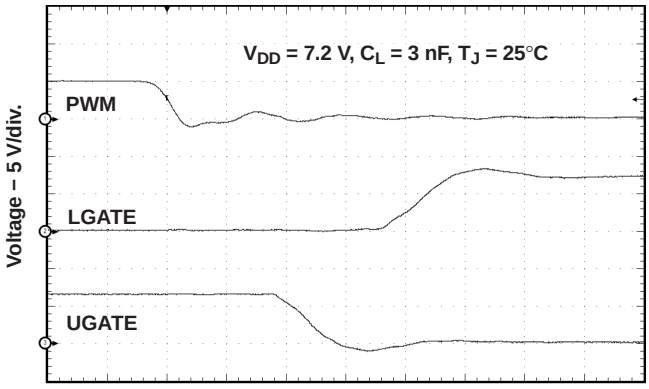
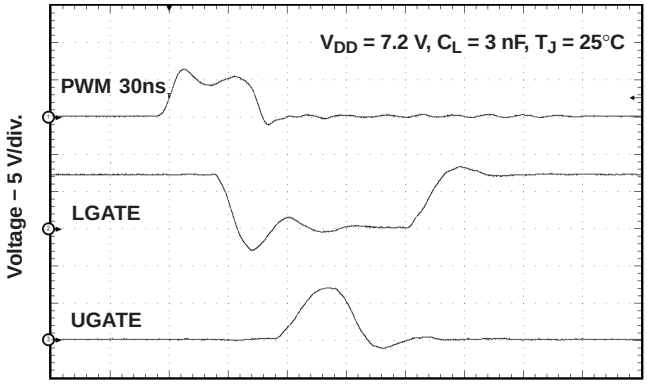


Figure 16.

TYPICAL CHARACTERISTICS (continued)

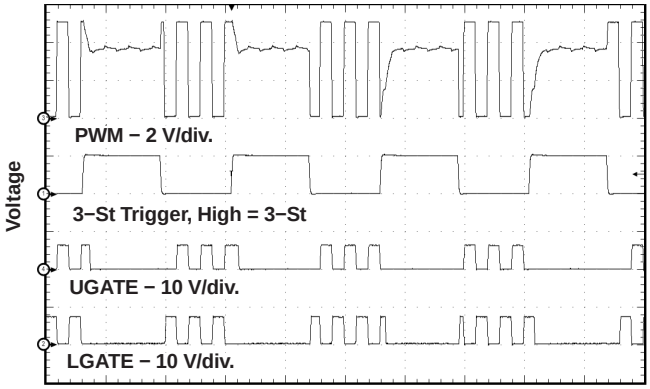
MINIMUM UGATE PULSE SWITCHING WAVEFORMS



t – Time – 20 ns/div.

Figure 17.

NORMAL AND 3-STATE OPERATION ENTER/EXIT CONDITIONS



t – Time – 5 μs/div.

Figure 18.

DETAILED DESCRIPTION

UNDER VOLTAGE LOCKOUT (UVLO)

The TPS28225 incorporates an under voltage lockout circuit that keeps the driver disabled and external power FETs in an OFF state when the input supply voltage V_{DD} is insufficient to drive external power FETs reliably. During power up, both gate drive outputs remain low until voltage V_{DD} reaches UVLO threshold, typically 3.5V. Once the UVLO threshold is reached, the condition of gate drive outputs is defined by the input PWM and EN/PG signals. During power down the UVLO threshold is set lower, typically 3.0V. The 0.5-V hysteresis is selected to prevent the driver from turning ON and OFF while the input voltage crosses UVLO thresholds, especially with low slew rate. The TPS28225 has the ability to send a signal back to the system controller that the input supply voltage V_{DD} is insufficient by internally pulling down the EN/PG pin. The TPS28225 releases EN/PG pin immediately after the V_{DD} has risen above the UVLO threshold.

OUTPUT ACTIVE LOW

The output active low circuit effectively keeps the gate outputs low even if the driver is not powered up. This prevents open gate conditions on the external power FETs and accidental turn ON when the main power stage supply voltage is applied before the driver is powered up. For the simplicity, the output active low circuit is shown in a block diagram as the resistor connected between LGATE and GND pins with another one connected between UGATE and PHASE pins.

ENABLE/POWER GOOD

The Enable/Power Good circuit allows the TPS28225 to follow the PWM input signal when the voltage at EN/PG pin is above 2.1 V maximum. This circuit has a unique two-way communication capability. This is illustrated by Figure 19.

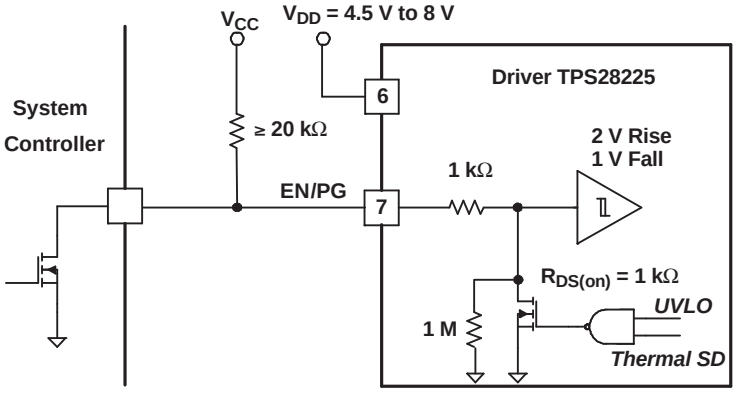


Figure 19. Enable/Power Good Circuit

The EN/PG pin has approximately 1-kΩ internal series resistor. Pulling EN/PG high by an external ≥ 20-kΩ resistor allows two-way communication between controller and driver. If the input voltage V_{DD} is below UVLO threshold or thermal shut down occurs, the internal MOSFET pulls EN/PG pin to GND through 1-kΩ resistor. The voltage across the EN/PG pin is now defined by the resistor divider comprised by the external pull up resistor, 1-kΩ internal resistor and the internal FET having 1kΩ $R_{DS(on)}$. Even if the system controller allows the driver to start by setting its own enable output transistor OFF, the driver keeps the voltage at EN/PG low. Low EN/PG signal indicates that the driver is not ready yet because the supply voltage V_{DD} is low or that the driver is in thermal shutdown mode. The system controller can arrange the delay of PWM input signals coming to the driver until the driver releases EN/PG pin. If the input voltage V_{DD} is back to normal, or the driver is cooled down below its lower thermal shutdown threshold, then the internal MOSFET releases the EN/PG pin and normal operation resumes under the external Enable signal applied to EN/PG input. Another feature includes an internal 1MΩ resistor that pulls EN/PG pin low and disables the driver in case the system controller accidentally loses connection with the driver. This could happen if, for example, the system controller is located on a separate PCB daughter board.

DETAILED DESCRIPTION (continued)

The EN/PG pin can serve as the second pulse input of the driver additionally to PWM input. The delay between EN/PG and the UGATE going high, provided that PWM input is also high, is only about 30ns. If the PWM input pulses are synchronized with EN/PG input, then when PWM and EN/PG are high, the UGATE is high and LGATE is low. If both PWM and EN/PG are low, then UGATE and LGATE are both low as well. This means the driver allows operation of a synchronous buck regulator as a convertional buck regulator using the body diode of the low side power MOSFET as the freewheeling diode. This feature can be useful in some specific applications to allow startup with a pre-biased output or, to improve the efficiency of buck regulator when in power saving mode with low output current.

3-STATE INPUT

As soon as the EN/PG pin is set high and input PWM pulses are initiated (see 1 below(1)). The dead-time control circuit ensures that there is no overlapping between UGATE and LGATE drive outputs to eliminate shoot through current through the external power FETs. Additionally to operate under periodical pulse sequencing, the TPS28225 has a self-adjustable PWM 3-state input circuit. The 3-state circuit sets both gate drive outputs low, and thus turns the external power FETs OFF if the input signal is in a high impedance state for at least 250 ns typical. At this condition, the PWM input voltage level is defined by the internal 27kΩ to 13kΩ resistor divider shown in the block diagram. This resistor divider forces the input voltage to move into the 3-state window. Initially the 3-state window is set between 1.0-V and 2.0-V thresholds. The lower threshold of the 3-state window is always fixed at about 1.0 V. The higher threshold is adjusted to about 75% of the input signal amplitude. The self-adjustable upper threshold allows shorter delay if the input signal enters the 3-state window while the input signal was high, thus keeping the high-side power FET in ON state just slightly longer then 250 ns time constant set by an internal 3-state timer. Both modes of operation, PWM input pulse sequencing and at the 3-state condition, are illustrated in the timing diagrams shown in Figure 18. The self-adjustable upper threshold allows operation in wide range amplitude of input PWM pulse signals. The waveforms in Figure 20 and Figure 21 illustrate operation at normal and 3-state mode with the input pulse amplitudes 6 V and 2.5 V accordingly. After entering into the 3-state window and staying within the window for the hold-off time, the PWM input signal level is defined by the internal resistor divider and, depending on the input pulse amplitude, can be pulled up above the normal PWM pulse amplitude (Figure 21) or down below the normal input PWM pulse (Figure 20). To exit from the 3-state operation mode, the input signal should go low and then high at least once. This is necessary to restore the voltage across the bootstrap capacitor that could be discharged during the 3-state mode if the 3-state condition lasts long enough.

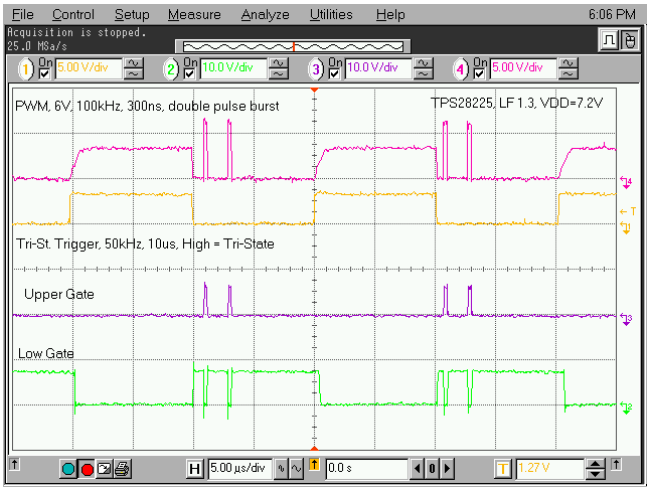


Figure 20. 6-V Amplitude PWM Pulse

Figure 21. 2.5-V Amplitude PWM Pulse

(1) The driver sets UGATE low and LGATE high when PWM is low. When the PWM goes high, UGATE goes high and LGATE goes low.

DETAILED DESCRIPTION (continued)

IMPORTANT NOTE: Any external resistor between PWM input and GND with the value lower than 40kΩ can interfere with the 3-state thresholds. If the driver is intended to operate in the 3-state mode, any resistor below 40kΩ at the PWM and GND should be avoided. A resistor lower than 3.5kΩ connected between the PWM and GND completely disables the 3-state function. In such case, the 3-state window shrinks to zero and the lower 3-state threshold becomes the boundary between the UGATE staying low and LGATE being high and vice versa depending on the PWM input signal applied. It is not necessary to use a resistor <3.5kΩ to avoid the 3-state condition while using a controller that is 3-state capable. If the rise and fall time of the input PWM signal is shorter than 250ns, then the driver never enter into the 3-state mode.

In the case where the low-side MOSFET of a buck converter stays on during shutdown, the 3-state feature can be fused to avoid negative resonent voltage across the output capacitor. This feature also can be used during start up with a pre-biased output in the case where pulling the output low during the startup is not allowed due to system requirements. If the system controller does not have the 3-state feature and never goes into the high-impedance state, then setting the EN/PG signal low will keep both gate drive outputs low and turn both low- and high-side MOSFETs OFF during the shut down and start up with the pre-biased output.

The self-adjustable input circuit accepts wide range of input pulse amplitudes (2V up to 13.2V) allowing use of a variety of controllers with different outputs including logic level. The wide PWM input voltage allows some flexibility if the driver is used in secondary side synchronous rectifier circuit. The operation of the TPS28225 with a 12-V input PWM pulse amplitude, and with V_{DD} = 7.2V and V_{DD} = 5V respectively is shown in Figure 22 and Figure 23.

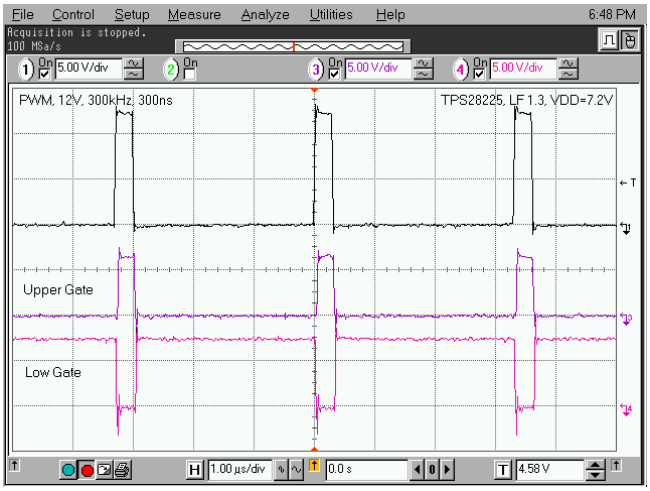


Figure 22. 12-V PWM Pulse at V_{DD} = 7.2 V

Figure 23. 12-V PWM Pulse at V_{DD} = 5 V

DETAILED DESCRIPTION (continued)

BOOTSTRAP DIODE

The bootstrap diode provides the supply voltage for the UGATE driver by charging the bootstrap capacitor connected between BOOT and PHASE pins from the input voltage VDD when the low-side FET is in ON state. At the very initial stage when both power FETs are OFF, the bootstrap capacitor is pre-charged through this path including the PHASE pin, output inductor and large output capacitor down to GND. The forward voltage drop across the diode is only 1.0V at bias current 100 mA. This allows quick charge restore of the bootstrap capacitor during the high-frequency operation.

UPPER AND LOWER GATE DRIVERS

The upper and lower gate drivers charge and discharge the input capacitance of the power MOSFETs to allow operation at switching frequencies up to 2 MHz. The output stage consists of a P-channel MOSFET providing source output current and an N-channel MOSFET providing sink current through the output stage. The ON state resistances of these MOSFETs are optimized for the synchronous buck converter configuration working with low duty cycle at the nominal steady state condition. The UGATE output driver is capable of propagating PWM input puses of less than 30-ns while still maintaining proper dead time to avoid any shoot through current conditions. The waveforms related to the narrow input PWM pulse operation are shown in Figure 17.

DEAD TIME CONTROL

The dead-time control circuit is critical for highest efficiency and no shoot through current operation througout the whole duty cycle range with the different power MOSFETs. By sensing the output of driver going low, this circuit does not allow the gate drive output of another driver to go high until the first driver output falls below the specified threshold. This approach to control the dead time is called adaptive. The overall dead time also includes the fixed portion to ensure that overlapping never exists. The typical dead time is around 14 ns, although it varies over the driver internal tolerances, layout and external MOSFET parasitic inductances. The proper dead time is maintained whenever the current through the output inductor of the power stage flows in the forward or reverse direction. Reverse current could happen in a buck configuration during the transients or while dynamically changing the output voltage on the fly, as some microprocessors require. Because the dead time does not depend on inductor current direction, this driver can be used both in buck and boost regulators or in any bridge configuration where the power MOSFETs are switching in a complementary manner. Keeping the dead time at short optimal level boosts efficiency by 1% to 2% depending on the switching frequency. Measured switching waveforms in one of the practical designs show 10-ns dead time for the rising edge of PHASE node and 22 ns for the falling edge (Figure 29 and Figure 30 in the Application Section of the data sheet).

Large non-optimal dead time can cause duty cycle modulation of the dc-to-dc converter during the operation point where the output inductor current changes its direction right before the turn ON of the high-side MOSFET. This modulation can interfere with the controller operation and it impacts the power stage frequency response transfer function. As the result, some output ripple increase can be observed. The TPS28225 driver is designed with the short adaptive dead time having fixed delay portion that eliminates risk of the effective duty cycle modulation at the described boundary condition.

THERMAL SHUTDOWN

If the junction temperature exceeds 160°C, the thermal shutdown circuit will pull both gate driver outputs low and thus turning both, low-side and high-side power FETs OFF. When the driver cools down below 140°C after a thermal shutdown, then it resumes its normal operation and follows the PWM input and EN/PG signals from the external control circuit. While in thermal shutdown state, the internal MOSFET pulls the EN/PG pin low, thus setting a flag indicating the driver is not ready to continue normal operation. Normally the driver is located close to the MOSFETs, and this is usually the hottest spots on the PCB. Thus, the thermal shutdown feature of TPS28225 can be used as an additional protection for the whole system from overheating.

APPLICATION INFORMATION

SWITCHING THE MOSFETs

Driving the MOSFETs efficiently at high switching frequencies requires special attention to layout and the reduction of parasitic inductances. Efforts need to be done both at the driver's die and package level and at the PCB layout level to keep the parasitic inductances as low as possible. Figure 24 shows the main parasitic inductances and current flow during turning ON and OFF of the MOSFET by charging its C_{GS} gate capacitance.

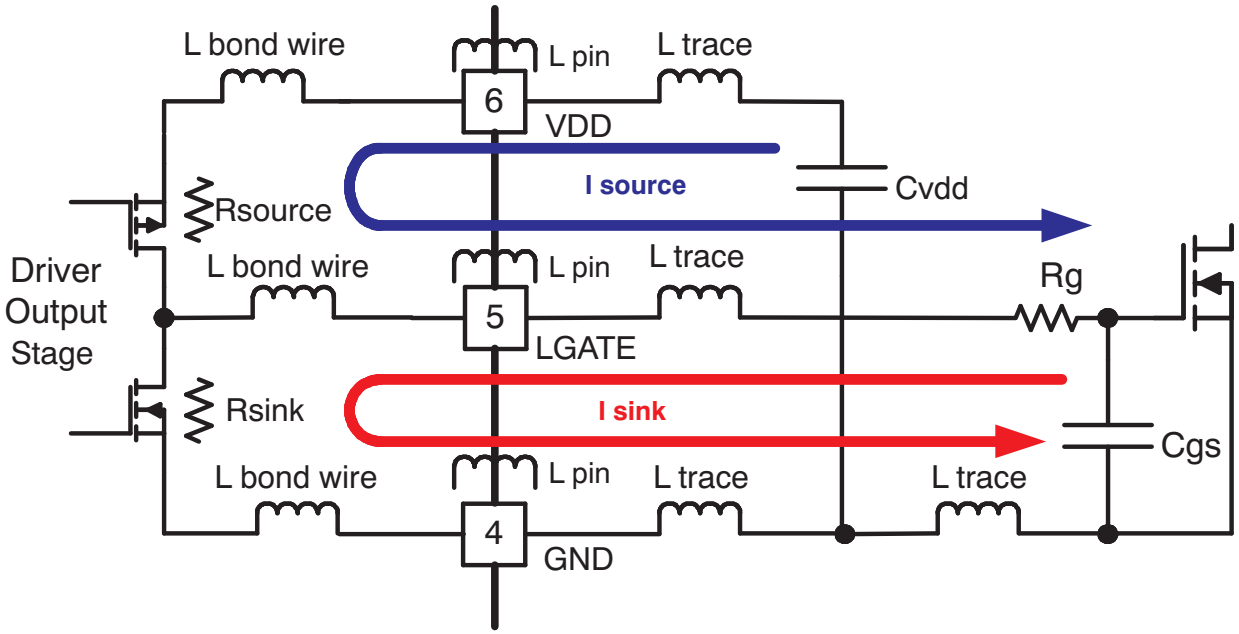


Figure 24. MOSFET Drive Paths and Main Circuit Parasitics

APPLICATION INFORMATION (continued)

The I_{SOURCE} current charges the gate capacitor and the I_{SINK} current discharges it. The rise and fall time of voltage across the gate defines how quickly the MOSFET can be switched. The timing parameters specified in datasheet for both upper and lower driver are shown in Figure 15 and Figure 16 where 3-nF load capacitor has been used for the characterization data. Based on these actual measurements, the analytical curves in Figure 25 and Figure 26 show the output voltage and current of upper and low side drivers during the discharging of load capacitor. The left waveforms show the voltage and current as a function of time, while the right waveforms show the relation between the voltage and current during fast switching. These waveforms show the actual switching process and its limitations because of parasitic inductances. The static V_{OUT}/ I_{OUT} curves shown in many datasheets and specifications for the MOSFET drivers do not replicate actual switching condition and provide limited information for the user.

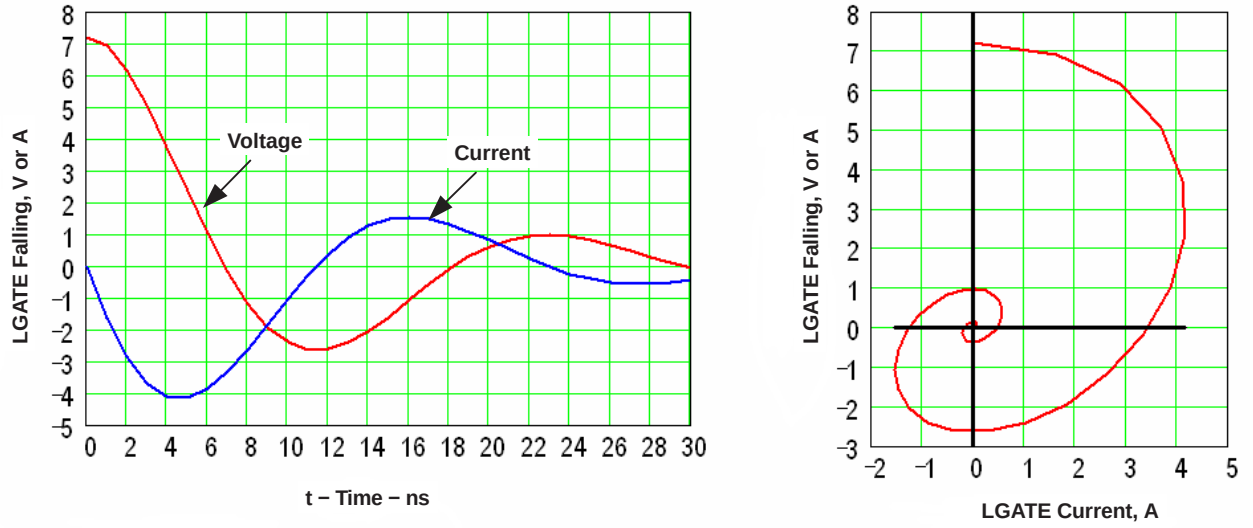


Figure 25. LGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right))

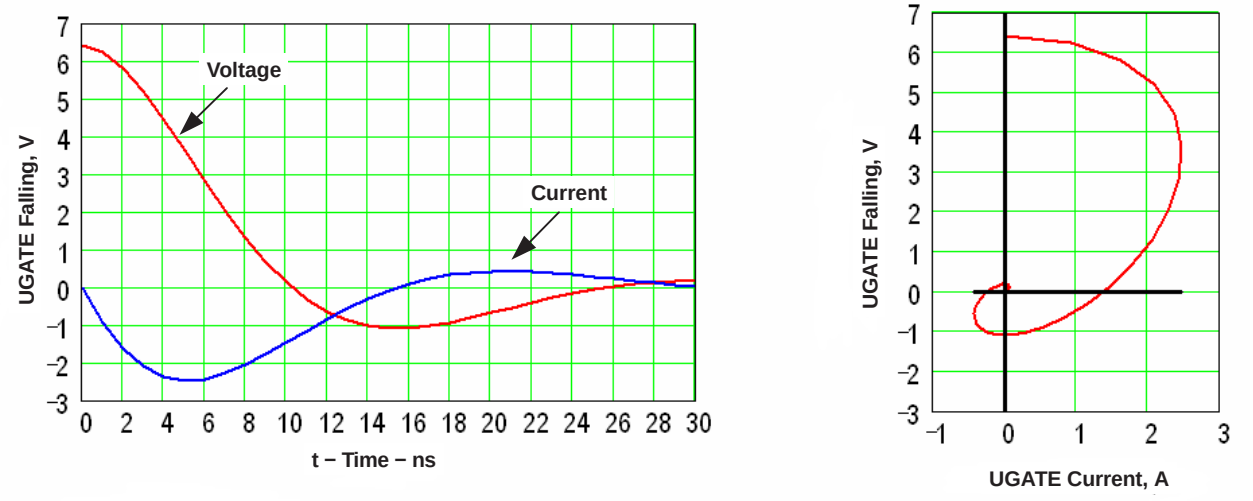


Figure 26. UGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right)_

APPLICATION INFORMATION (continued)

Turning Off of the MOSFET needs to be done as fast as possible to reduce switching losses. For this reason the TPS28225 driver has very low output impedance specified as 0.4Ω typ for lower driver and 1Ω typ for upper driver at dc current. Assuming 8-V drive voltage and no parasitic inductances, one can expect an initial sink current amplitude of 20A and 8A respectively for the lower and upper drivers. With pure R-C discharge circuit for the gate capacitor, the voltage and current waveforms are expected to be exponential. However, because of parasitic inductances, the actual waveforms have some ringing and the peak current for the lower driver is about 4A and about 2.5A for the upper driver (Figure 25 and Figure 26). The overall parasitic inductance for the lower drive path is estimated as 4nH and for the upper drive path as 6nH. The internal parasitic inductance of the driver, which includes inductances of bonded wires and package leads, can be estimated for SOIC-8 package as 2nH for lower gate and 4nH for the upper gate. Use of DFN-8 package reduces the internal parasitic inductances by approximately 50%.

Layout Recommendations

To improve the switching characteristicsand efficiency of a design, the following layout rules need to be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the DFN-8 package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the PHASE node as for the GND.
- Use wide traces for UGATE and LGATE closely following the related PHASE and GND traces. Eighty to 100 mils width is preferable where possible.
- Use at least 2 or more vias if the MOSFET driving trace needs to be routed from one layer to another. For the GND the number of vias are determined not only by the parasitic inductance but also by the requirements for the thermal pad.
- Avoid PWM and enable traces going close to the PHASE node and pad where high dV/dT voltage can induce significant noise into the relatively high impedance leads.

It should be taken into account that poor layout can cause 3% to 5% less efficiency versus a good layout design and can even decrease the reliability of the whole system.

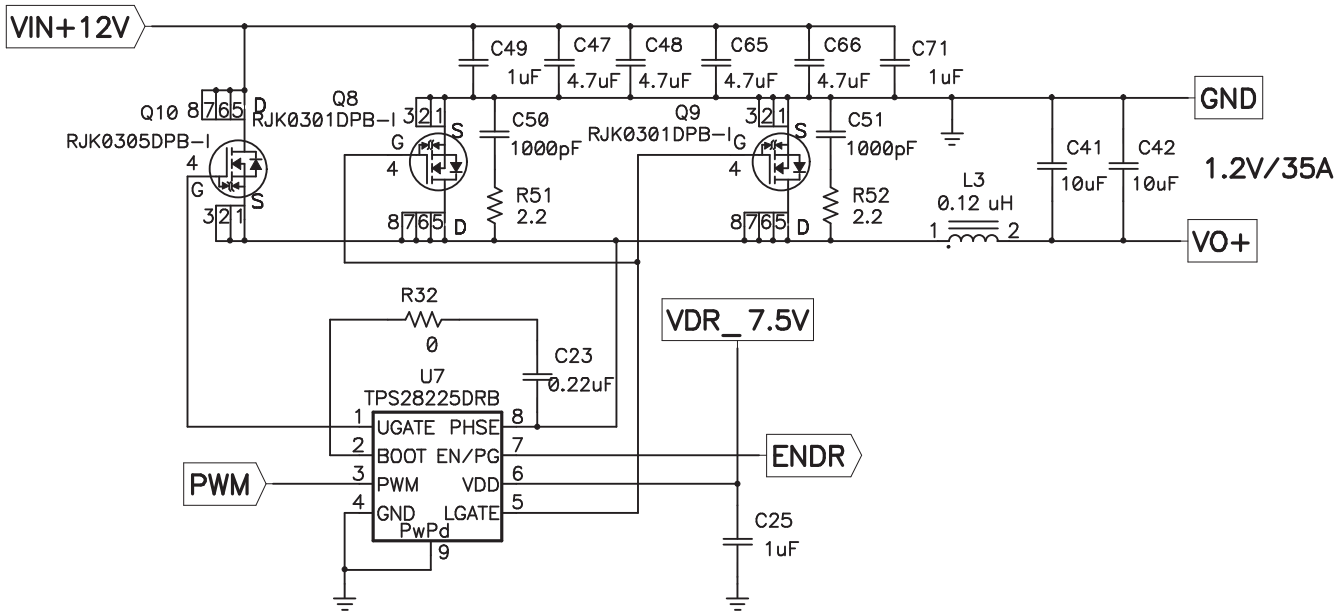


Figure 27. One of Phases Driven by TPS28225 Driver in 4-phase VRM Reference Design

APPLICATION INFORMATION (continued)

The schematic of one of the phases in a multi-phase synchronous buck regulator and the related layout are shown in Figure 27 and Figure 28. These help to illustrate good design practices. The power stage includes one high-side MOSFET Q10 and two low-side MOSFETS (Q8 and Q9). The driver (U7) is located on bottom side of PCB close to the power MOSFETs. The related switching waveforms during turning ON and OFF of upper FET are shown in Figure 29 and Figure 30. The dead time during turning ON is only 10ns (Figure 29) and 22ns during turning OFF (Figure 30).

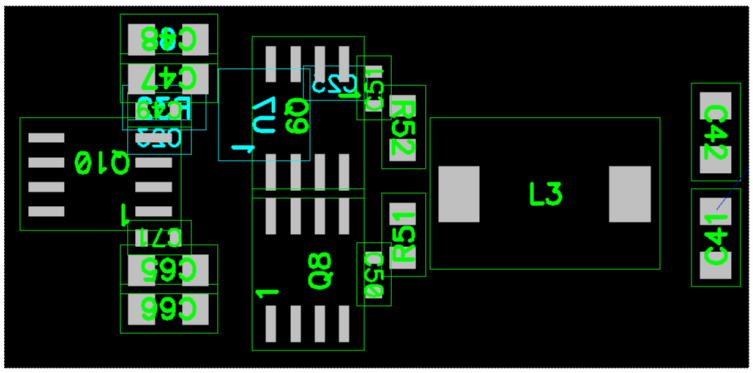


Figure 28. Component Placement Based on Schematic in Figure 27

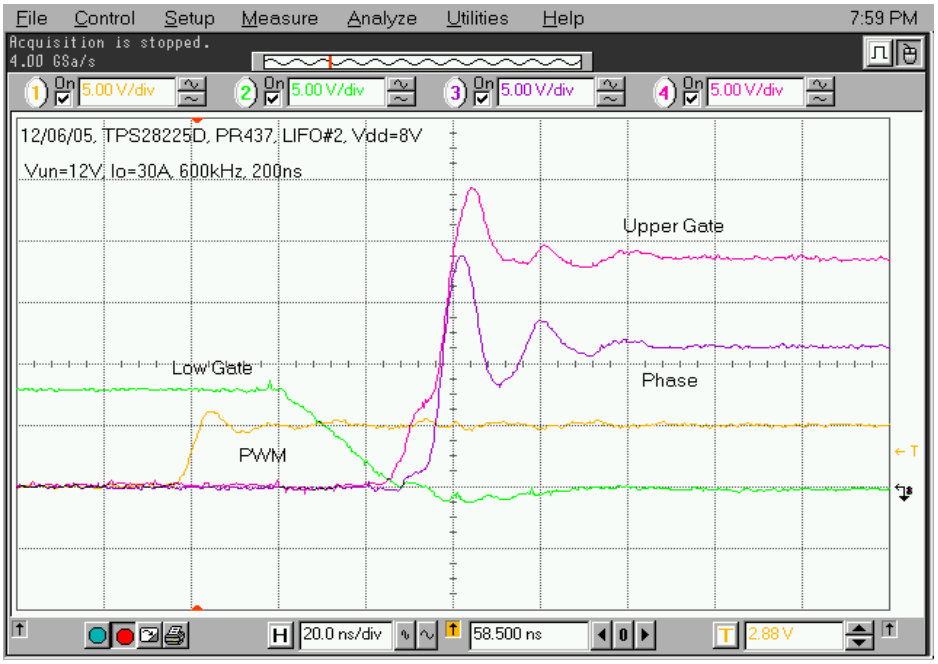


Figure 29. Phase Rising Edge Switching Waveforms (20ns/div) of the Power Stage in Figure 27

APPLICATION INFORMATION (continued)

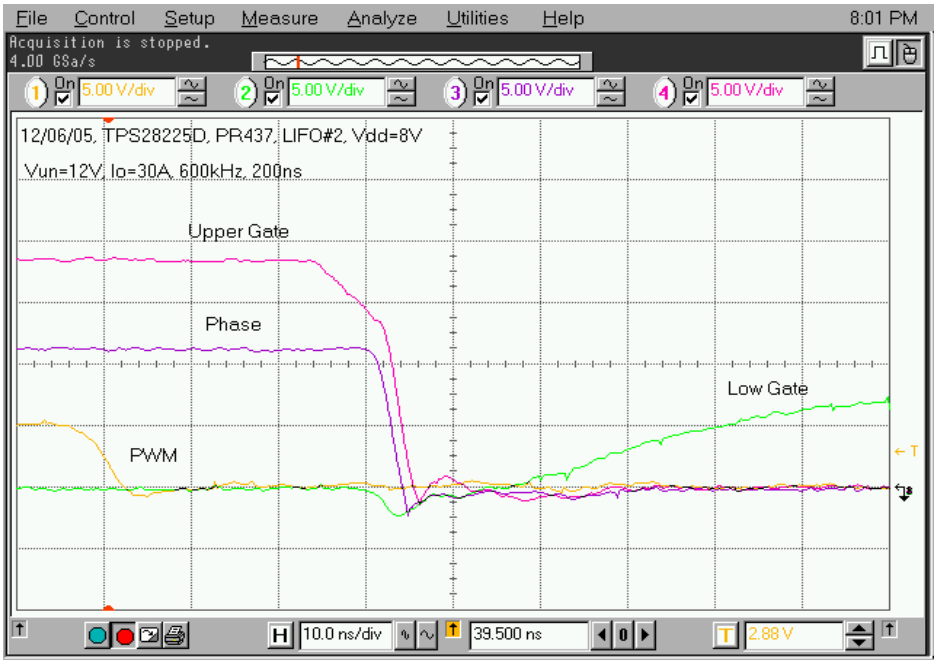


Figure 30. Phase Falling Edge Switching Waveforms (10ns/div) of the Power State in Figure 27

LIST OF MATERIALS

The list of materials for this specific example is provided in the table. The component vendors are not limited to those shown in the table below. It should be notd that, in this example, the power MOSFET packages were chosen with drains on top. The decoupling capacitors C47, C48, C65, and C66 were chosen to have low profiles. This allows the designer to meet good layout rules and place a heatsink on top of the FETs using an electrically isolated and thermally conductive pad.

List of Materials

REF DES	COUNT	DESCRIPTION	MANUFACTURE	PART NUMBER
C47, C48, C65, C66	4	Capacitor, ceramic, 4.7 µF, 16 V, X5R 10%, low profile 0.95 mm, 1206	TDK	C3216X5R1C475K
C41, C42	2	Capacitor, ceramic, 10 µF, 16 V, X7R 10%, 1206	TDK	C3216X7R1C106K
C50, C51	2	Capacitor, ceramic, 1000 pF, 50 V, X7R, 10%, 0603	Std	Std
C23	1	Capacitor, ceramic, 0.22 µF, 16 V, X7R, 10%, 0603	Std	Std
C25, C49, C71	3	Capacitor, ceramic, 1 µF, 16 V, X7R, 10%, '0603	Std	Std
L3	1	Inductor, SMT, 0.12 µH, 31 A, 0.36 mΩ, 0.400 x 0.276	Pulse	PA0511-101
Q8, Q9	2	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 2.4 mΩ, I_D 45 A, LFPAK-i	Renesas	RJK0301DPB-I
Q10	1	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 6.2 mΩ, I_D 30 A, LFPAK-i	Renesas	RJK0305DPB-I
R32	1	Resistor, chip, 0 Ω, 1/10 W, 1%, '0805	Std	Std
R51, R52	2	Resistor, chip, 2.2 Ω, 1/10 W, 1%, '0805	Std	Std
U7	1	Device, High Frequency 4-A Sink Synchronous Buck MOSFET Driver, DFN-8	Texas Instruments	TPS28225DRB

EFFICIENCY OF POWER STAGE vs LOAD CURRENT AT DIFFERENT SWITCHING FREQUENCIES

Efficiency achieved using TPS28225 driver with 8-V drive at different switching frequencies a similar industry 5-V driver using the power stage in Figure 27 is shown in Figure 33, Figure 35, Figure 34, Figure 31 and Figure 32.

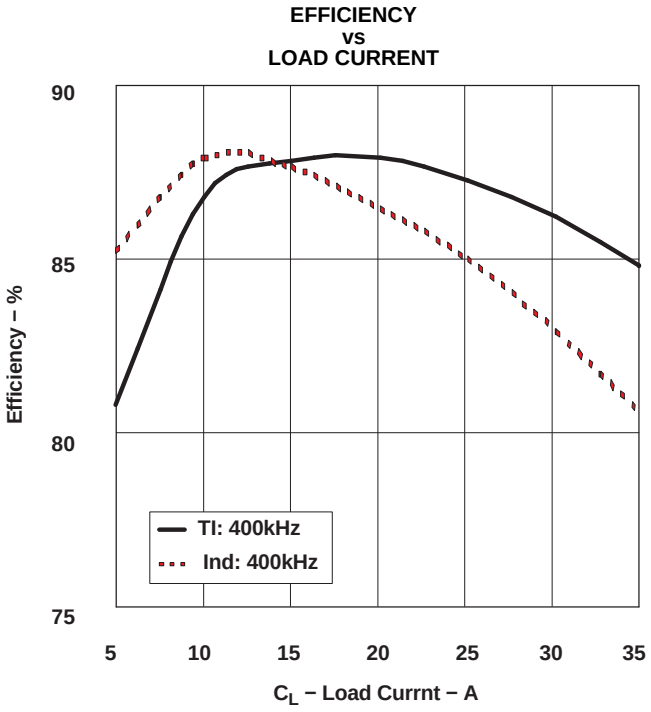


Figure 31.

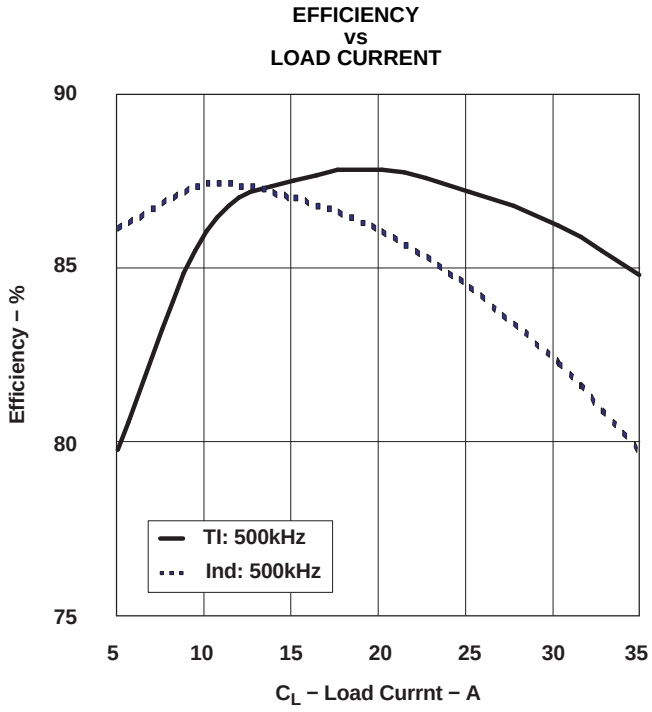


Figure 32.

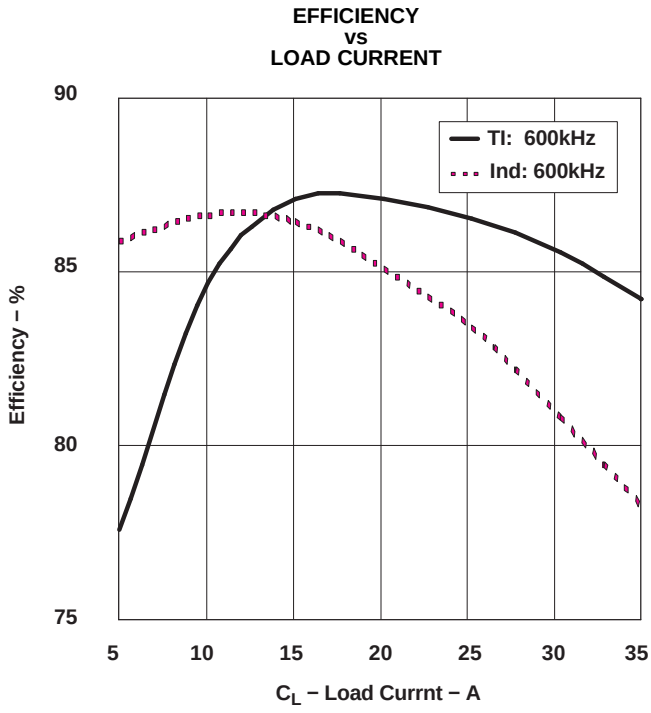


Figure 33.

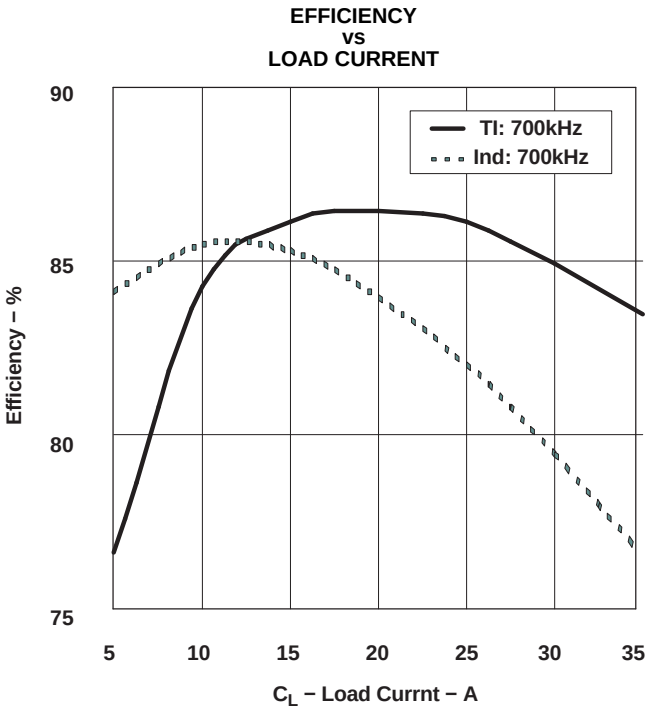


Figure 34.

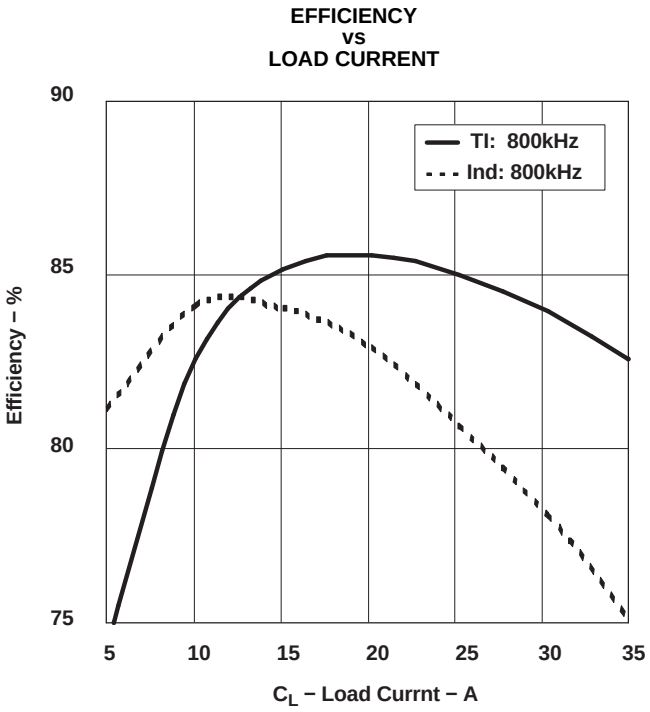


Figure 35.

When using the same power stage, the driver with the optimal drive voltage and optimal dead time can boost efficiency up to 5%. The optimal 8-V drive voltage versus 5-V drive contributes 2% to 3% efficiency increase and the remaining 1% to 2% can be attributed to the reduced dead time. The 7-V to 8-V drive voltage is optimal for operation at switching frequency range above 400kHz and can be illustrated by observing typical $R_{DS(on)}$ curves of modern FETs as a function of their gate drive voltage. This is shown in Figure 36.

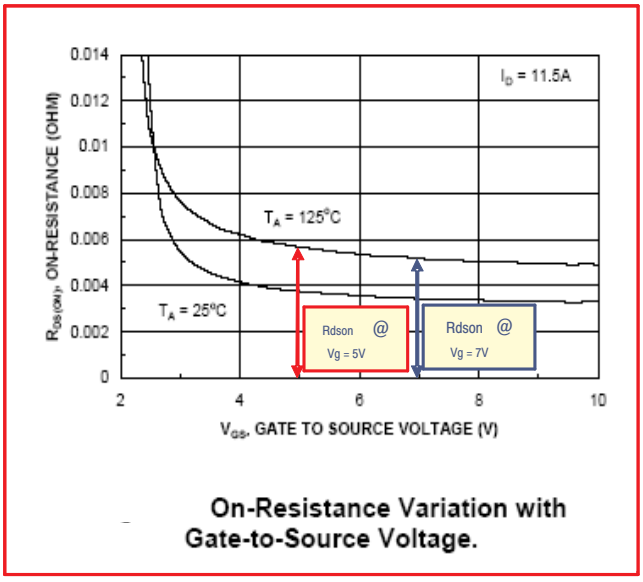


Figure 36. $R_{DS(on)}$ of MOSFET as Function of V_{GS}

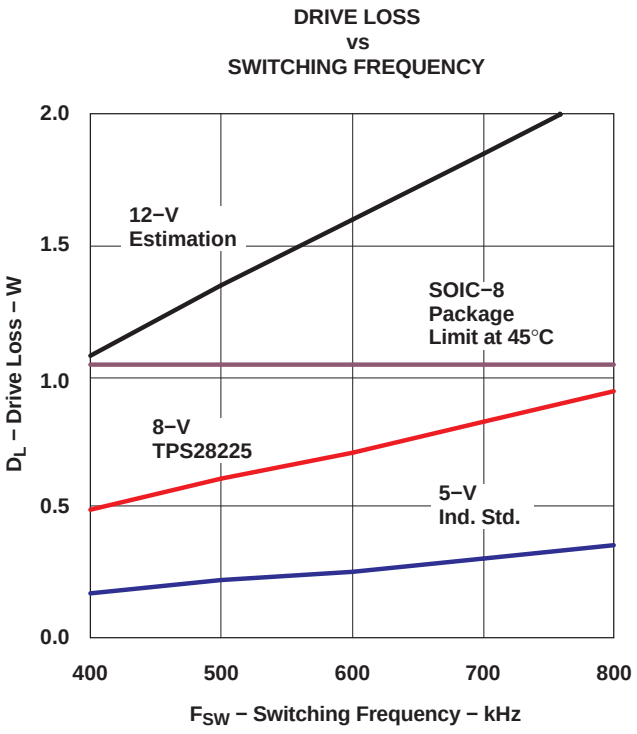


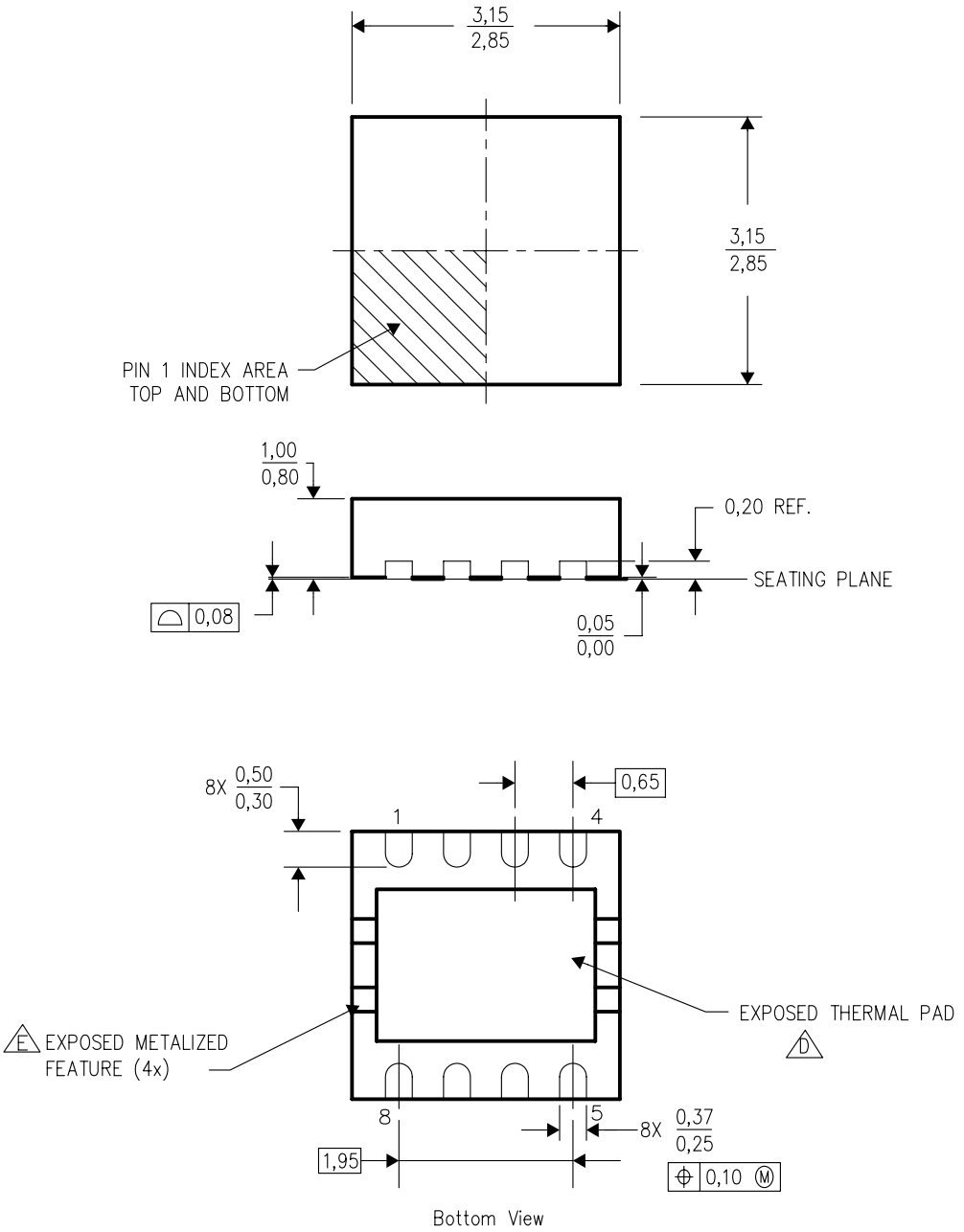
Figure 37. Drive Power as Function of V_{GS} and F_{SW}

The plots show that the $R_{DS(on)}$ at 5-V drive is substantially larger than at 7 V and above that the $R_{DS(on)}$ curve is almost flat. This means that moving from 5-V drive to an 8-V drive boosts the efficiency because of lower $R_{DS(on)}$ of the MOSFETs at 8 V. Further increase of drive voltage from 8 V to 12 V only slightly decreases the conduction losses but the power dissipated inside the driver increases dramatically (by 125%). The power dissipated by the driver with 5V, 8V and 12V drive as a function of switching frequency from 400kHz to 800kHz. It should be noted that the 12-V driver exceeds the maximum dissipated power allowed for an SOIC-8 package even at 400-kHz switching frequency.

RELATED PRODUCTS

- TPS40090, 2/3/4-Phase Multi-Phase Controller
- TPS40091, 2/3/4-Phase Multi-Phase Controller

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

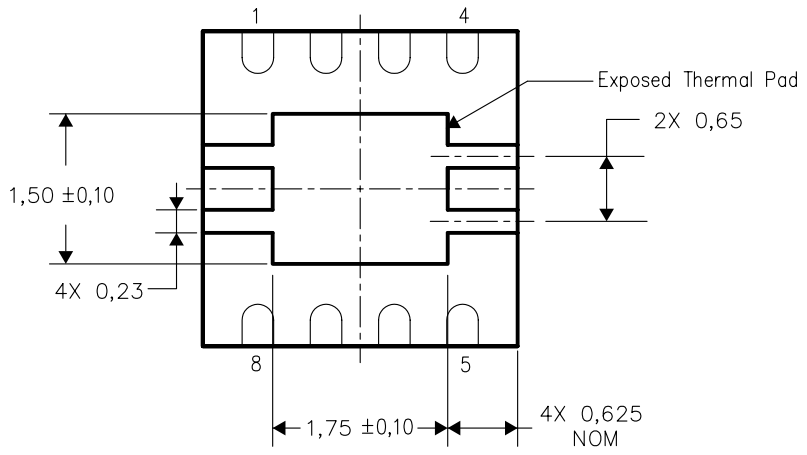
DRB (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

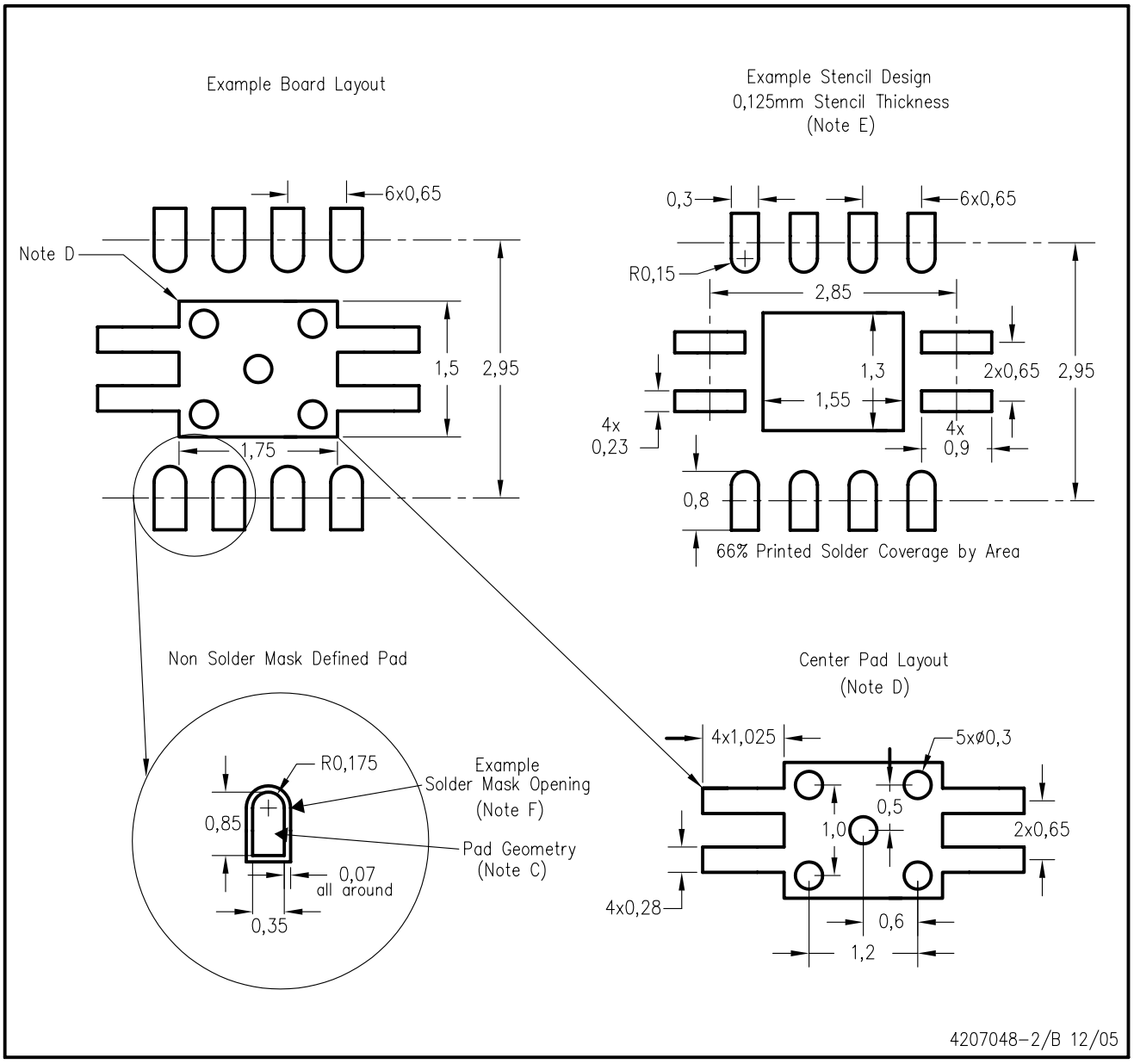


Bottom View

NOTE: All linear dimensions are in millimeters

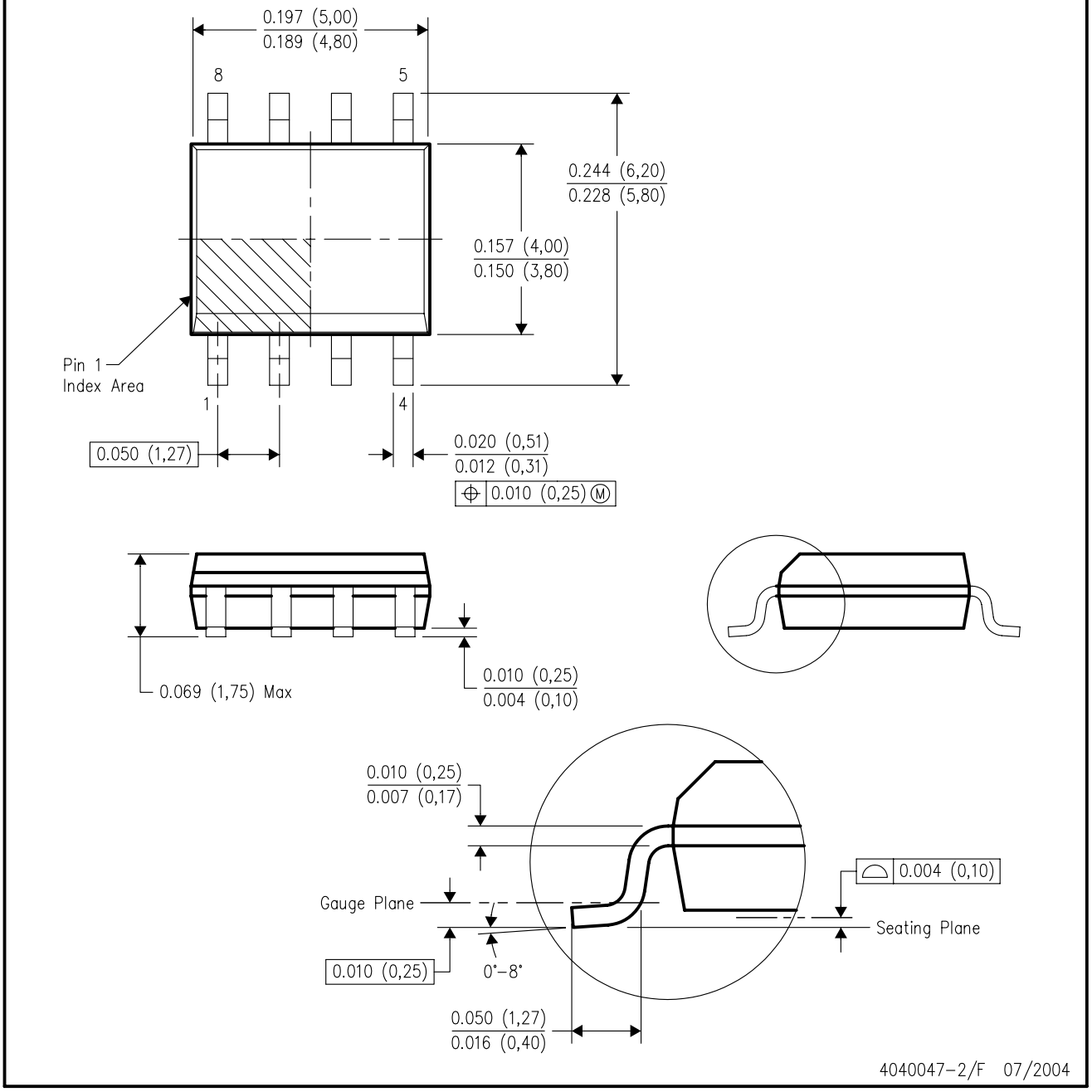
Exposed Thermal Pad Dimensions

DRB (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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