TPS25980: 2.7- 24 V, 8 A, 3 mΩ Smart eFuse - Integrated Hot-swap Protection With Adjustable Transient Fault Management

1 Features

- Wide input voltage range: 2.7 V to 24 V
  - 30-V Absolute maximum
- Low On-Resistance: R_{ON} = 3-mΩ typical
- Circuit Breaker Response
- Adjustable current limit threshold
  - Range: 2 A to 8 A
  - Accuracy: ± 8% (typical for I_{LIM} > 5 A)
- Adjustable over-current blanking timer
  - Handles load transients without tripping
- Accurate current monitor output
  - ± 3% (typical at 25 °C for I_{OUT} > 3 A)
- User configurable fault response
  - Latch-off or auto-retry
  - Number of retries (Finite or indefinite)
  - Delay between retries
- Robust short-circuit protection
  - Fast-trip response time < 400-ns typical
  - Tested against 1 million power-into-short events
  - Immune to line transients - no nuisance tripping
- Adjustable output slew rate (dVdt) control
- Adjustable undervoltage lockout
- Overvoltage lockout (Fixed 3.7-V, 7.6-V, 16.9-V and no-OVLO options)
- Integrated overtemperature protection
- Power good indication
- Adjustable load detect and handshake timer
- UL 2367 Recognition
  - File no. E339631
  - R_{ILIM} ≥ 182 Ω
- IEC 62368 CB Certification
- Small footprint: 4-mm × 4-mm QFN package

2 Applications

- Hot-Swap, hot-plug
- Server standby rail, PCIe riser, add-on card and fan module protection
- Routers and switches optical module protection
- Industrial PC
- Digital TV

3 Description

The TPS25980x family of eFuses is a highly integrated circuit protection and power management solution in a small package. The devices are operational over a wide input voltage range. A single part caters to low-voltage systems needing minimal I*R voltage drop as well as higher voltage, high current systems needing low power dissipation. They are a robust defense against overloads, short-circuits, voltage surges and excessive inrush current.

Overvoltage events are limited by internal cutoff circuits, with multiple device options to choose the overvoltage threshold.

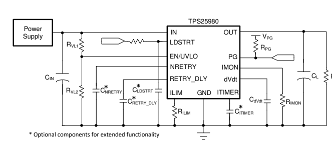
The device provides a circuit-breaker response to overcurrent conditions. The overcurrent limit (circuit-breaker threshold) and fast-trip (short-circuit) threshold can be set with a single external resistor. The devices intelligently manage the overcurrent response by distinguishing between transient events and actual faults, thereby allowing the system to function uninterrupted during line and load transients without compromising on the robustness of the protection against faults. The device can be configured to stay latched off or retry automatically after a fault shutdown. The number of auto-retries as well as the retry delay are configurable with capacitors. This enables remote systems to automatically recover from temporary faults while ensuring that power supplies are not stressed indefinitely due to a persistent fault.

The TPS25980x devices are available in a small 4 mm × 4 mm QFN package. The devices are characterized for operation over a junction temperature range of –40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25980x	QFN (24)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2020	*	Initial release.

5 Device Comparison Table

PART NUMBER	OVERVOLTAGE LOCKOUT THRESHOLD	OVERCURRENT RESPONSE
	TYPICAL (V)	
TPS259802ONRGE	3.7	Circuit Breaker
TPS259803ONRGE	7.6	Circuit Breaker
TPS259804ONRGE	16.9	Circuit Breaker
TPS259807ONRGE	No OVLO	Circuit Breaker

6 Pin Configuration and Functions

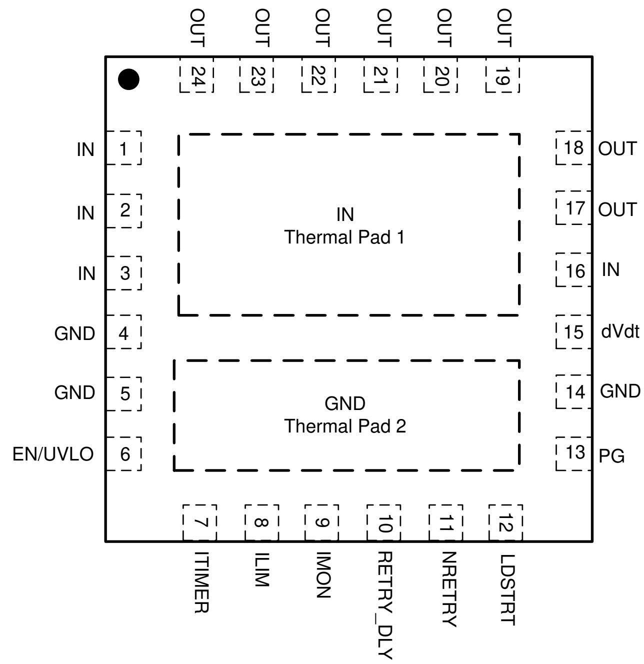


Figure 6-1. RGE 24-Pin QFN Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT	17, 18, 19, 20, 21, 22, 23, 24	Power	Power Output.
IN	1, 2, 3, 16, Pad 1	Thermal / Power	Power Input. The exposed pad must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
GND	4, 5, 14, Pad 2	Ground	Connect to System Ground.
EN/UVLO	6	Analog Input	Active High Enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. **Do not leave floating.**
ITIMER	7	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to *ITIMER Functional Mode Summary* for more details.
ILIM	8	Analog Output	An external resistor from this pin to GND sets the output current limit threshold and fast trip threshold. **Do not leave floating.**
IMON	9	Analog Output	Analog output load current monitor. This pin sources a current proportional to the load current. This can be converted to a voltage signal by connecting an appropriate resistor from this pin to GND.
RETRY_DLY	10	Analog Output	A capacitor from this pin to GND sets the time period that has to elapse after a fault shutdown before the device attempts to restart automatically. Connect this pin to GND for latch-off operation (no auto-retries) after a fault. Refer to *Fault Response* section for more details.
NRETRY	11	Analog Output	A capacitor from this pin to GND sets the number of times the part attempts to restart automatically after shutdown due to fault. Connect this pin to GND if the part should retry indefinitely. Refer to *Fault Response* section for more details.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
LDSTRT	12	Analog Input	Load Detect/Handshake Signal. A capacitor from this pin to GND sets the time period after PG assertion within which the pin has to be pulled low for the device to remain ON. Connect to GND if the load detect/handshake feature is not used. Refer to *Load Detect/Handshake (LDSTRT)* section for more details. **Do not leave floating.**
PG	13	Digital Output	Active High Power Good Indication. This pin is asserted when the FET is fully enhanced and output has reached maximum voltage. It is an open drain output that requires an external pull-up resistor to an external supply. This pin remains logic low when $V_{IN} < V_{UVP}$.
dVdt	15	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest slew rate during start up.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	IN	–0.3	30	V
V_{OUT}	Maximum Output Voltage Range	OUT	–0.8	min (30V, V_{IN} + 0.3)	V
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	7	V
V_{LDSTRT}	Maximum LDSTRT Pin Voltage Range	LDSTRT		7	V
V_{dVdt}	Maximum dVdt Pin Voltage Range	dVdt	Internally Limited		V
V_{PG}	Maximum PG Pin Voltage Range	PG	–0.3	7	V
V_{ITIMER}	Maximum ITIMER Pin Voltage Range	ITIMER	Internally Limited		V
V_{NRETRY}	Maximum NRETRY Pin Voltage Range	NRETRY	Internally Limited		V
V_{RETRY_DLY}	Maximum RETRY_DLY Pin Voltage Range	RETRY_DLY	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Soldering Temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	± 2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins[2]	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	24	V
V_{OUT}	Output Voltage Range	OUT		V_{IN} + 0.3	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		6[(1)]	V
V_{LDSTRT}	LDSTRT Pin Capacitor Voltage Rating	LDSTRT	4		V
V_{dVdT}	dVdT Pin Capacitor Voltage Rating	dVdt	V_{IN} + 4		V
V_{PG}	PG Pin Voltage Range	PG		6[(2)]	V
V_{ITIMER}	ITIMER Pin Capacitor Voltage Rating	ITIMER	4		V
V_{NRETRY}	NRETRY Pin Capacitor Voltage Rating	NRETRY	4		V
V_{RETRY_DLY}	RETRY_DLY Pin Capacitor Voltage Rating	RETRY_DLY	4		V
R_{ILIM}	ILIM Pin Resistor	ILIM	182	1650	Ω
I_{MAX}	Continuous Switch Current	IN to OUT		8	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 6V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 6V, it is recommended to use an appropriate resistor divider between IN, EN and GND to ensure the voltage at the EN pin is within the specified limits.
(2) For supply voltages below 6V, it is okay to pull up the PG pin to IN/OUT through a resistor. For supply voltages greater than 6V, it is recommended to use a stepped down power supply to ensure the voltage at the PG pin is within the specified limits.

7.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		TPS25980X	UNIT
		RGE (QFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with minimum recommended pad size (2 oz Cu) and 3x2 via array.

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS259804x/7x, 5 V for TPS259803x, 3.3 V for TPS259802x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 1650 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (IN)						
V_{IN}	Input Voltage Range		2.7		24	V
I_Q	IN Quiescent Current	V_{EN} ≥ $V_{UVLO(R)}$		800	1200	µA
I_{SD}	IN Shutdown Current	V_{SD} < V_{EN} < V_{UVLO}		204	300	µA
		V_{EN} < V_{SD}		3.67	20	µA
V_{UVP}	IN Undervoltage Protection Threshold	V_{IN} Rising	2.46	2.53	2.6	V
		V_{IN} Falling	2.35	2.42	2.49	V
OVERVOLTAGE PROTECTION (IN)						
$V_{OVP(R)}$	Overvoltage Protection Threshold	TPS259802x, V_{IN} Rising	3.62	3.7	3.76	V
		TPS259803x, V_{IN} Rising	7.39	7.6	7.76	V
		TPS259804x, V_{IN} Rising	16.32	16.9	17.31	V
$V_{OVP(F)}$		TPS259802x, V_{IN} Falling	3.52	3.6	3.66	V
		TPS259803x, V_{IN} Falling	7.22	7.4	7.55	V
		TPS259804x, V_{IN} Falling	15.80	16.4	16.81	V
OUTPUT CURRENT MONITOR (IMON)						
G_{IMON}	Current Monitor Gain (I_{IMON}:I_{OUT})	3 A ≤ I_{OUT} ≤ min(8 A, I_{LIM})	228.78	246	263.22	µA/A
OUTPUT CURRENT LIMIT (ILIM)						
I_{LIM}	I_{OUT} Current Limit Threshold	R_{ILIM} = 773 Ω, T_J = 25 °C	1.76	2	2.17	A
		R_{ILIM} = 773 Ω, T_J = -40 to 125 °C	1.53	2	2.43	A
		R_{ILIM} = 300 Ω, T_J = 25 °C	4.75	4.98	5.23	A
		R_{ILIM} = 300 Ω, T_J = -40 to 125 °C	4.36	4.98	5.66	A
		R_{ILIM} = 182 Ω, T_J = 25 °C	7.77	8.13	8.54	A
		R_{ILIM} = 182 Ω, T_J = -40 to 125 °C	7.23	8.13	9.07	A
		R_{ILIM} = Open		0		A
I_{CB}	I_{OUT} Circuit Breaker Threshold During ILIM pin Short to GND Condition (Single point failure)	R_{ILIM} = Short to GND, T_J = 25 °C			20	A
I_{SC}	Short-circuit Fast Trip Threshold			210		% I_{LIM}
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON State Resistance	T_J = 25 °C, I_{OUT} = 2 A		3		mΩ
		T_J = -40 to 125 °C, I_{OUT} = 2 A			5	mΩ
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO Pin Voltage Threshold	V_{EN} Rising	1.18	1.2	1.23	V
$V_{UVLO(F)}$		V_{EN} Falling	1.08	1.1	1.13	V
V_{SD}	EN/UVLO Pin Voltage Threshold for Lowest Shutdown Current	V_{EN} Falling	0.59	0.8		V
I_{ENLKG}	EN/UVLO Pin Leakage Current				0.1	µA
POWER GOOD INDICATION (PG)						
V_{PGD}	PG Pin Low Voltage (PG de-asserted)	V_{IN} < V_{UVP}, V_{EN} < V_{SD}, I_{PG} = 26 µA		651	786	mV
		V_{IN} = 3.3V, I_{PG} ≤ 5 mA		320		mV
		V_{IN} ≥ 5V, I_{PG} ≤ 5 mA		100		mV
I_{PGLKG}	PG Pin Leakage Current (PG asserted)	PG pulled up to 5 V through 10 kΩ			1.7	µA
$R_{ON(PGA)}$	R_{ON} When PG is asserted			4.2		mΩ

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS259804x/7x, 5 V for TPS259803x, 3.3 V for TPS259802x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 1650 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PGTHD}	V_{IN} - V_{OUT} Threshold when PG is de-asserted		0.224	0.326	0.450	V
AUTO-RETRY DELAY INTERVAL (RETRY_DLY)						
$V_{RETRY\_DLY(R)}$	RETRY_DLY Oscillator Comparator Threshold			1.1		V
$V_{RETRY\_DLY(F)}$				0.35		V
$V_{RETRY\_DLY\_HYS}$	RETRY_DLY Oscillator Hysteresis		0.65	0.75	0.85	V
I_{RETRY_DLY}	RETRY_DLY Pin Bias Current		1.7	2.05	2.5	µA
NUMBER OF AUTO-RETRIES (NRETRY)						
$V_{NRETRY(R)}$	NRETRY Oscillator Comparator Threshold			1.1		V
$V_{NRETRY(F)}$				0.35		V
V_{NRETRY_HYS}	NRETRY Oscillator Hysteresis		0.65	0.75	0.85	V
I_{NRETRY}	NRETRY Pin Bias Current		1.7	2.05	2.5	µA
CURRENT FAULT TIMER (ITIMER)						
I_{ITIMER}	ITIMER Discharge Current	I_{SC} > I_{OUT} > I_{LIM}	1.4	2.1	2.8	µA
R_{ITIMER}	ITIMER Internal Pull-up Resistance	I_{OUT} < I_{LIM}		23		kΩ
V_{INT}	ITIMER Pin Default Voltage	I_{OUT} < I_{LIM}		2.5		V
V_{ITIMER}	ITIMER Comparator Falling Threshold	I_{SC} > I_{OUT} > $I_{LIM,}$ ITIMER Voltage Rising		1.53		V
ΔV_{ITIMER}	ITIMER Comparator Voltage Threshold Delta	I_{SC} > I_{OUT} > $I_{LIM,}$ ITIMER Voltage Falling	0.7	0.98	1.3	V
LDSTRT						
V_{LDSTRT}	LDSTRT Rising Threshold	LDSTRT voltage rising	1.1	1.21	1.3	V
I_{LDSTRT}	LDSTRT Charging Current	PG asserted	1.7	2.05	2.4	µA
R_{LDSTRT}	LDSTRT Internal Pull-down Resistance			31		Ω
RQOD	QOD effective resistance	IN connected to EN, OUT connected to QOD, EN! to 1V		73.2		mA
OVERTEMPERATURE PROTECTION						
TSD	Thermal Shutdown Threshold	T_J Rising		150		°C
TSDHys	Thermal Shutdown Hysteresis	T_J Falling		10		°C
dVdt						
I_{dVdt}	dVdt Pin Charging Current		2	4.6	6.33	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage Protection Response Time (1)	V_{IN} > $V_{OVLO(R)}$ to V_{OUT}↓, TPS259802x		1.5		µs
		V_{IN} > $V_{OVLO(R)}$ to V_{OUT}↓, TPS259803x		5		µs
		V_{IN} > $V_{OVLO(R)}$ to V_{OUT}↓, TPS259804x		5		µs
t_{SC}	Short Circuit Response Time	I_{OUT} > 3 x I_{LIM} to V_{OUT} turned OFF		400		ns
t_{PGD}	PG Assertion/De-assertion De-glitch (2)	V_G > (V_{IN} + 3.6V) to PG↑ or (V_{IN} - V_{OUT})> V_{PGTHD} to PG↓		120		µs

(1) Please refer to Fig. 8-2
(2) Please refer to Fig. 8-5

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 3.6 Ω, C_{OUT} = 1 mF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 3300pF	C_{dVdt} = 6800pF	UNIT
SR_{ON}	Output Rising slew rate	2.7 V	6.26	1.39	0.68	V/ms
		12 V	7.35	1.4	0.68	
		24 V	7.4	1.4	0.68	
$t_{D,ON}$	Turn on delay	2.7 V	1.3	1.49	1.7	ms
		12 V	1.24	2.1	3.01	
		24 V	1.2	2.91	4.74	
t_R	Rise time	2.7 V	0.67	1.63	3.35	ms
		12 V	1.35	6.99	14.41	
		24 V	2.66	13.77	28.41	
t_{ON}	Turn on time	2.7 V	1.97	3.12	5.05	ms
		12 V	2.59	9.09	17.42	
		24 V	3.86	16.68	33.15	
$t_{D,OFF}$	Turn off delay	2.7 V	151	152	152	µs
		12 V	212	212	212	
		24 V	262	262	262	

7.8 Typical Characteristics

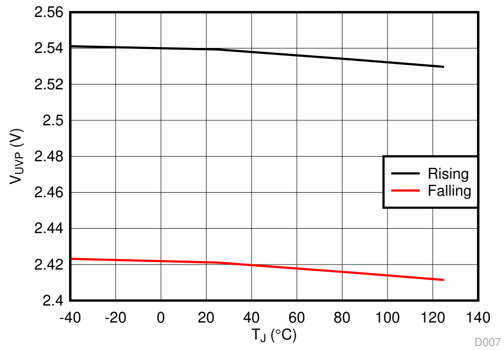
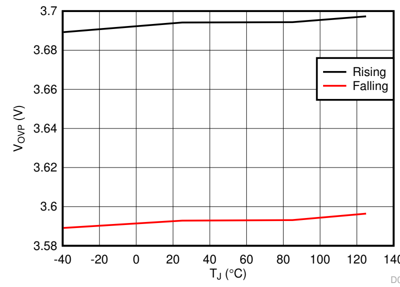
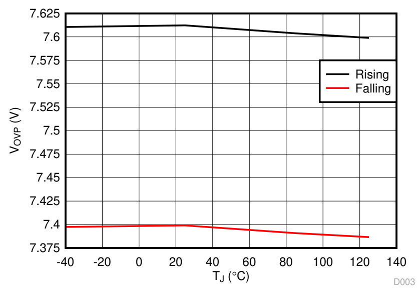


Figure 7-1. Supply UVP Threshold vs Temperature



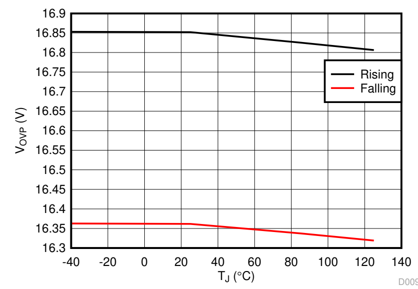
TPS259802x Variants

Figure 7-2. Supply OVP Threshold vs Temperature



TPS259803x Variants

Figure 7-3. Supply OVP Threshold vs Temperature



TPS259804x Variants

Figure 7-4. Supply OVP Threshold vs Temperature

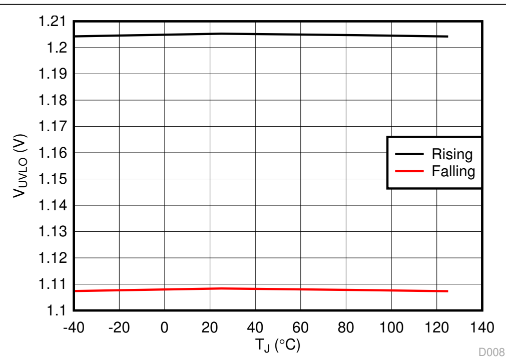
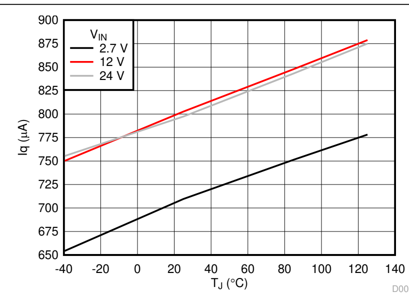


Figure 7-5. EN/UVLO Threshold vs Temperature



V_{ENUVLO} = 2 V, OUT = Open

Figure 7-6. Quiescent Current vs Temperature

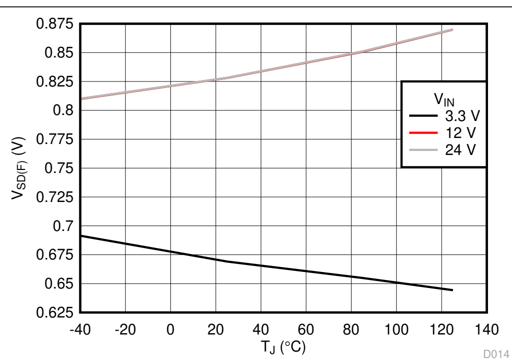
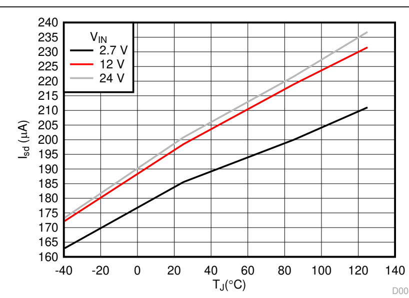
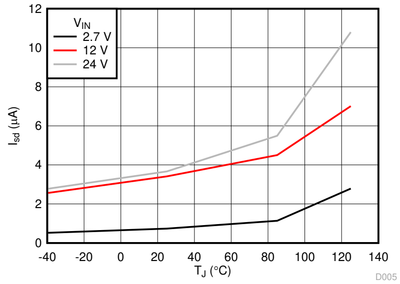


Figure 7-7. EN/UVLO Falling Threshold for Lowest Current Consumption



V_{ENUVLO} = 1 V, OUT = Open

Figure 7-8. Shut-Down Current vs Temperature



V_{ENUVLO} = 0 V, OUT = Open

Figure 7-9. Deep Shut-Down Current vs Temperature

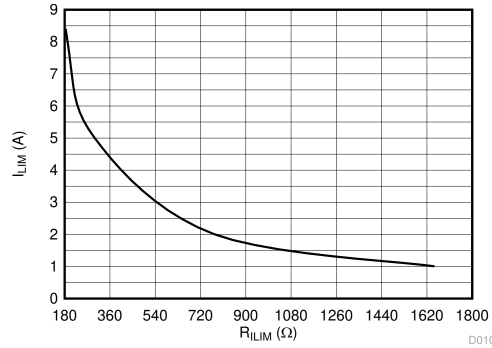
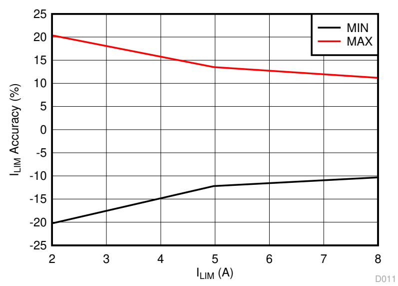
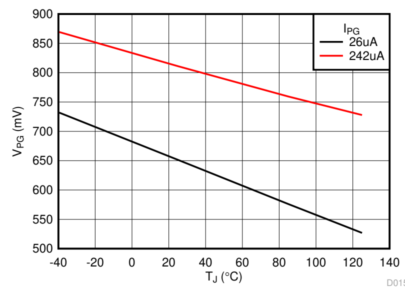


Figure 7-10. Output Current Limit (I_{LIM}) vs R_{ILIM}



Across Process, Voltage, Temperature Corners

Figure 7-11. Output Current Limit (I_{LIM}) Accuracy



V_{IN} = 0 V

Figure 7-12. Power Good Output Voltage (De-asserted State) vs Temperature

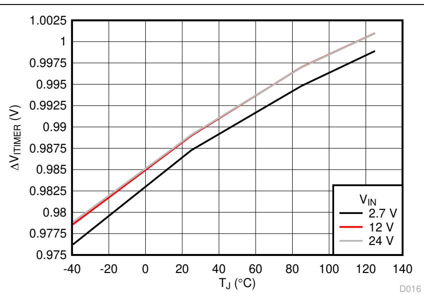


Figure 7-13. ITIMER Voltage Threshold Delta vs Temperature

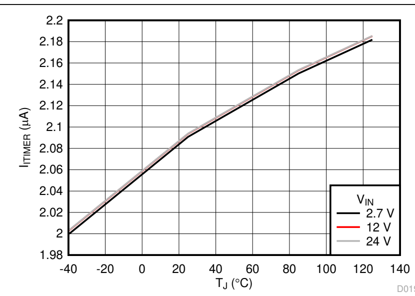


Figure 7-14. ITIMER Discharge Current vs Temperature

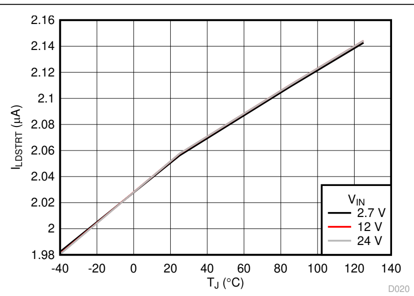


Figure 7-15. LDSTRT Charging Current vs Temperature

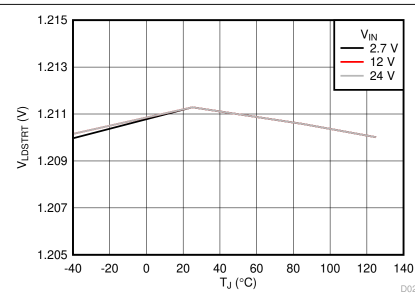


Figure 7-16. LDSTRT Threshold Voltage vs Temperature

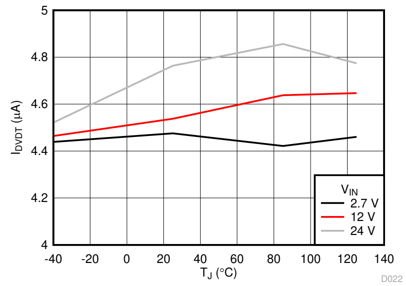


Figure 7-17. DVDT Charging Current vs Temperature

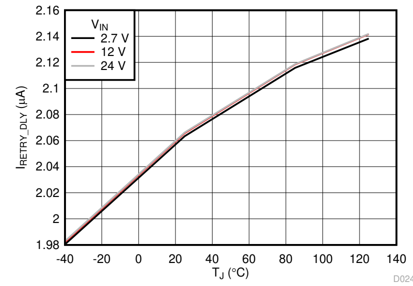


Figure 7-18. RETRY_DLY Bias Current vs Temperature

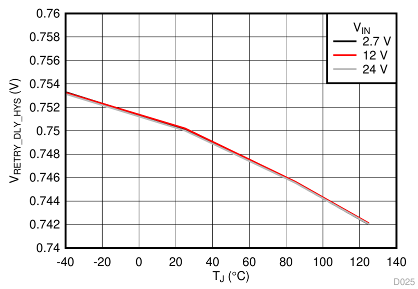


Figure 7-19. RETRY_DLY Oscillator Hysteresis vs Temperature

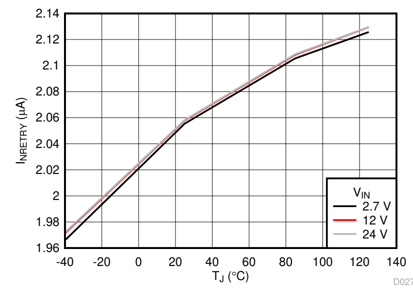


Figure 7-20. NRETRY Bias Current vs Temperature

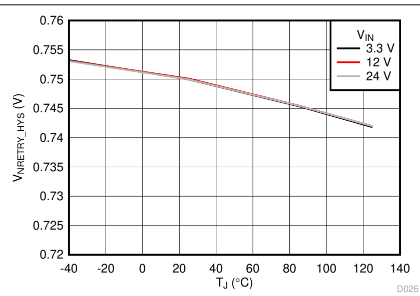


Figure 7-21. NRETRY Oscillator Hysteresis vs Temperature

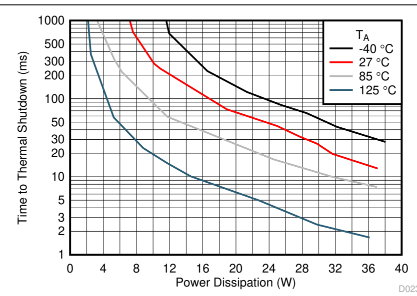


Figure 7-22. Thermal Shutdown Plot - Steady State

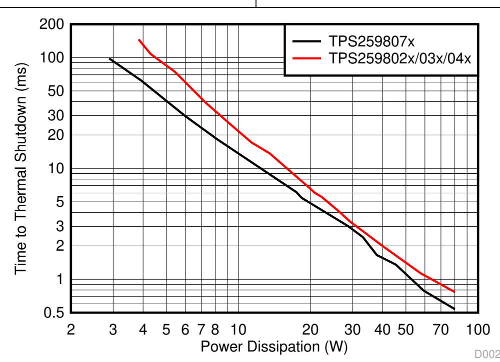
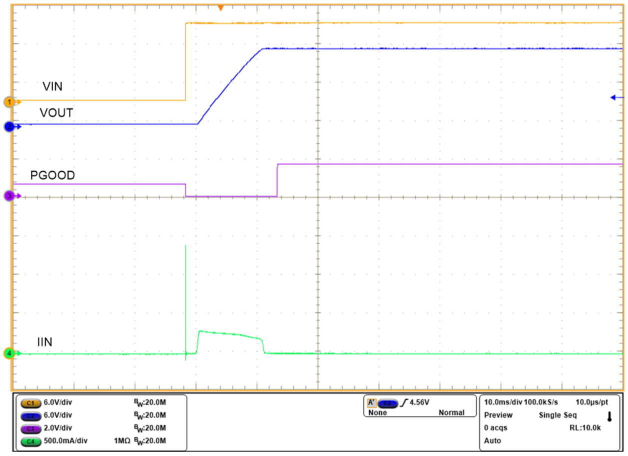
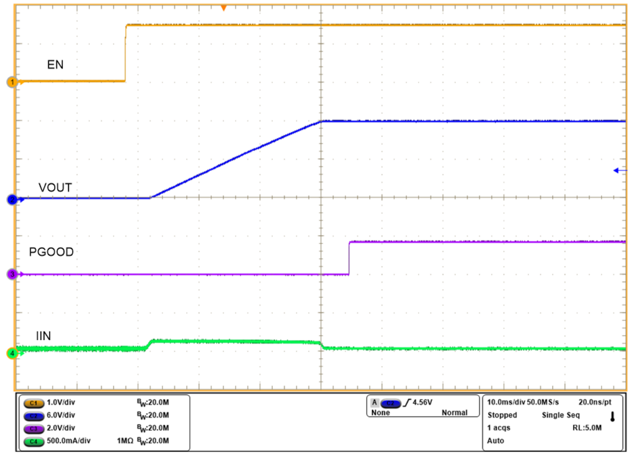


Figure 7-23. Thermal Shutdown Plot - Inrush/Overload



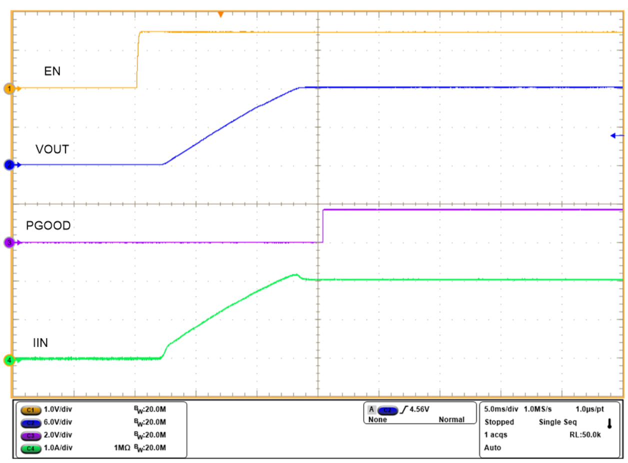
C_{IN} = 1 µF C_{OUT} = 220 µF C_{dVdt} = 3.3 nF

Figure 7-24. Hotplug



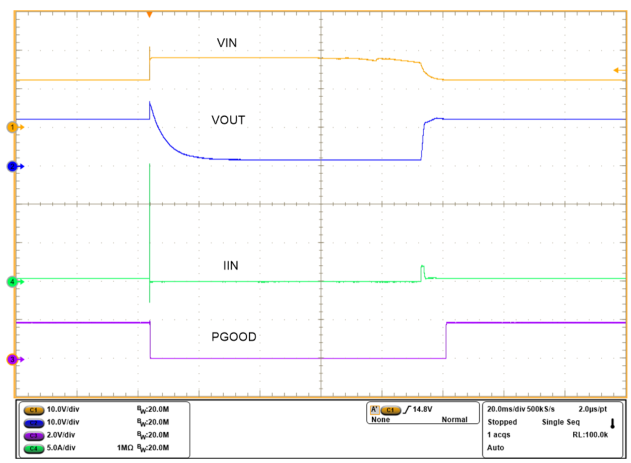
C_{OUT} = 220 µF C_{dVdt} = 10 nF R_{OUT} = Open

Figure 7-25. Startup With EN - dVdt Limited



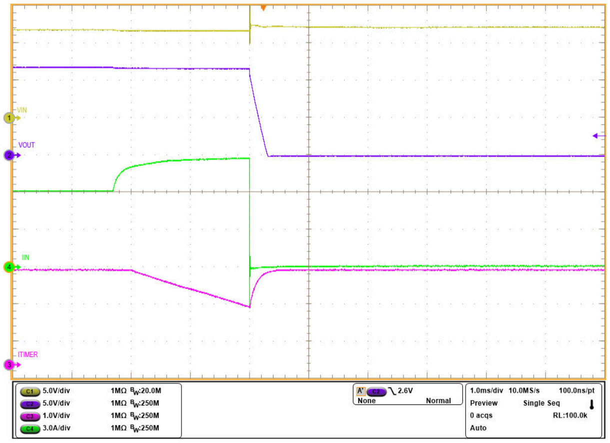
C_{OUT} = 220 µF C_{dVdt} = 3.3 nF R_{OUT} = 6 Ω

Figure 7-26. Startup With EN Into Resistive Load - dVdt Limited



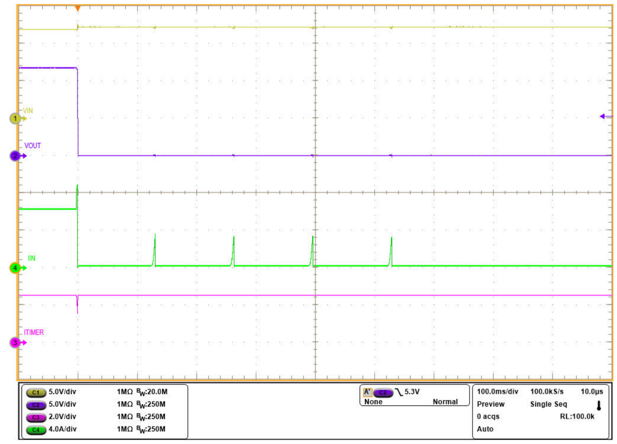
TPS259804x (16.7-V OVP variant)

Figure 7-27. Overvoltage Protection



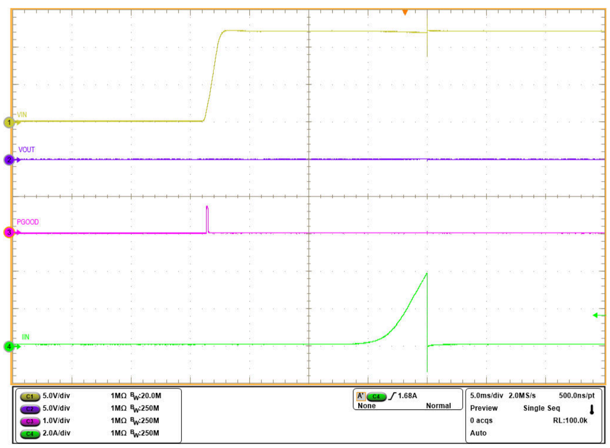
R_{ILIM} = 182 Ω C_{ITIMER} = 4.7 nF

Figure 7-28. Circuit Breaker With Transient Overcurrent Blanking



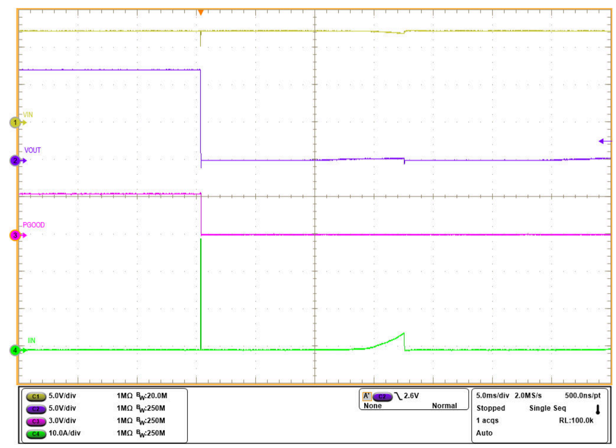
A. R_{ILIM} = 182 Ω C_{ITIMER} = 4.7 nF C_{RETRY_DLY} = 2.2 nF, C_{NRETRY} = 2.2 nF

Figure 7-29. Circuit Breaker - Auto-Retry



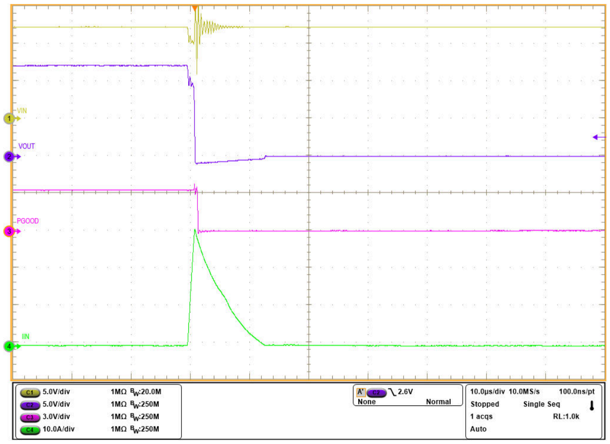
R_{ILIM} = 182 Ω

Figure 7-30. Power Up Into Output Short-Circuit



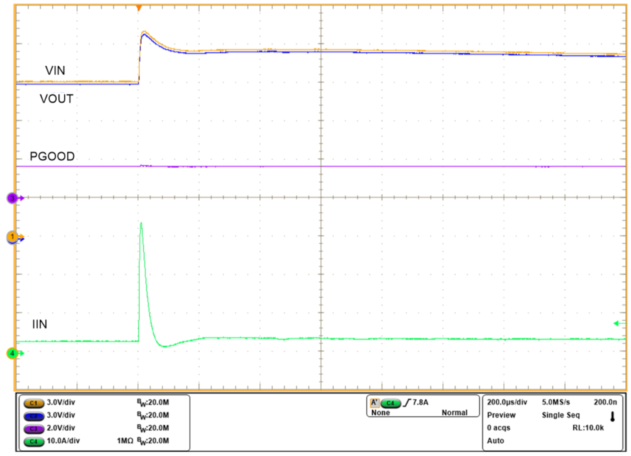
R_{ILIM} = 182 Ω

Figure 7-31. Output Hard Short-Circuit While ON



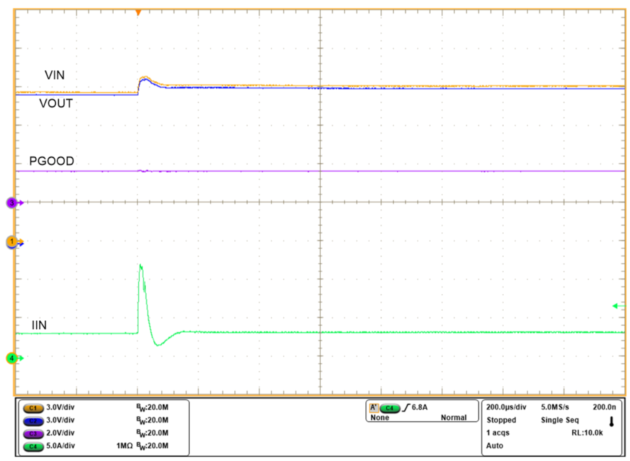
R_{ILIM} = 182 Ω

Figure 7-32. Output Hard Short-Circuit While ON (Zoomed In)



R_{ILIM} = 332 Ω

Figure 7-33. Supply Line Transient Immunity - Input Voltage Step



R_{ILIM} = 511 Ω

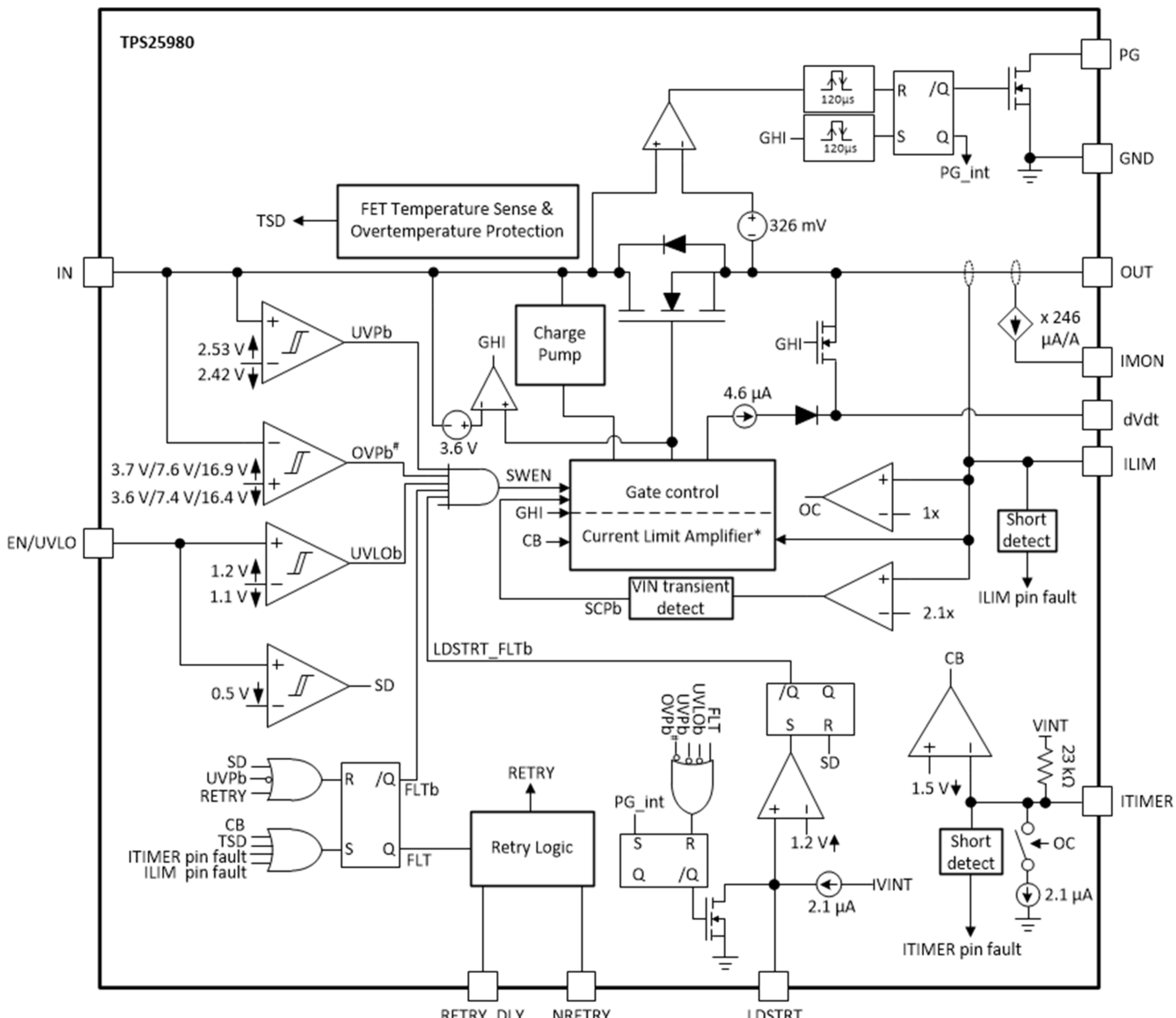
Figure 7-34. Supply Line Transient Immunity - Adjacent Load Hot Unplug

8 Detailed Description

8.1 Overview

The TPS25980x device is a smart eFuse with integrated power switch that is used to manage load voltage and load current. The device starts its operation by monitoring the IN bus. When V_{IN} is above the Undervoltage Protection threshold (V_{UVP}) and below the Overvoltage Protection threshold (V_{OVP}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low, the internal MOSFET is turned off. After a successful start-up sequence, the device now actively monitors its load current, input voltage and protects the load from harmful overcurrent and overvoltage conditions. The device also relies on a built-in thermal sense circuit to shut down and protect itself in case the device internal temperature (T_J) exceeds the safe operating conditions.

8.2 Functional Block Diagram



Not applicable for TPS259807x (no-OVP variant)

8.3 Feature Description

The TPS25980x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Protection (UVLO and UVP)

The TPS25980x implements Undervoltage Protection on IN to turn off the output in case the applied voltage becomes too low for the downstream load or the device to operate correctly. The Undervoltage Protection has a default internal threshold of V_{UVP}. If needed, it is also possible to set a user defined Undervoltage Protection threshold higher than V_{UVP} using the UVLO comparator on the EN/UVLO pin. Figure 8-1 and Equation 1 show how a resistor divider from supply to GND can be used to set the UVLO set point for a given voltage supply level.

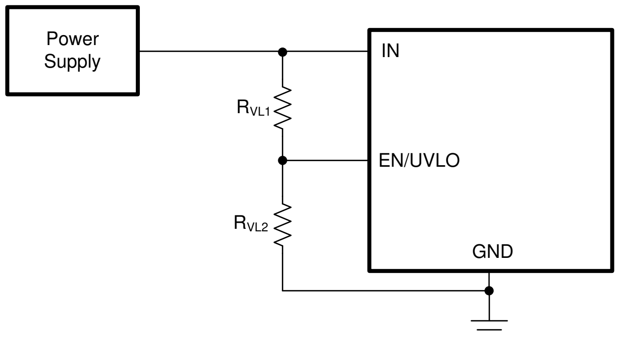


Figure 8-1. Adjustable Supply UVLO Threshold

$$VIN_{UVLO} = \frac{V_{UVLO(R)} \times (R_{VL1} + R_{VL2})}{R_{VL2}} \quad (1)$$

The resistors must be sized large enough to minimize the constant leakage from supply to ground through the resistor divider network. At the same time, keep the current through the resistor network sufficiently larger (20x) than the leakage current on the EN/UVLO pin to minimize the error in the resistor divider ratio.

8.3.2 Overvoltage Protection (OVP)

The TPS25980x implements Overvoltage Lock-Out (OVLO) on IN to protect the output load in the event of input overvoltage. When the input exceeds the Overvoltage Protection threshold ($V_{OVP(R)}$) the device turns off the output within t_{OVP}. As long as an overvoltage condition is present on the input, the device stays disabled and the output will be turned off. Once the input voltage returns to the normal operating range, the device attempts to start up normally.

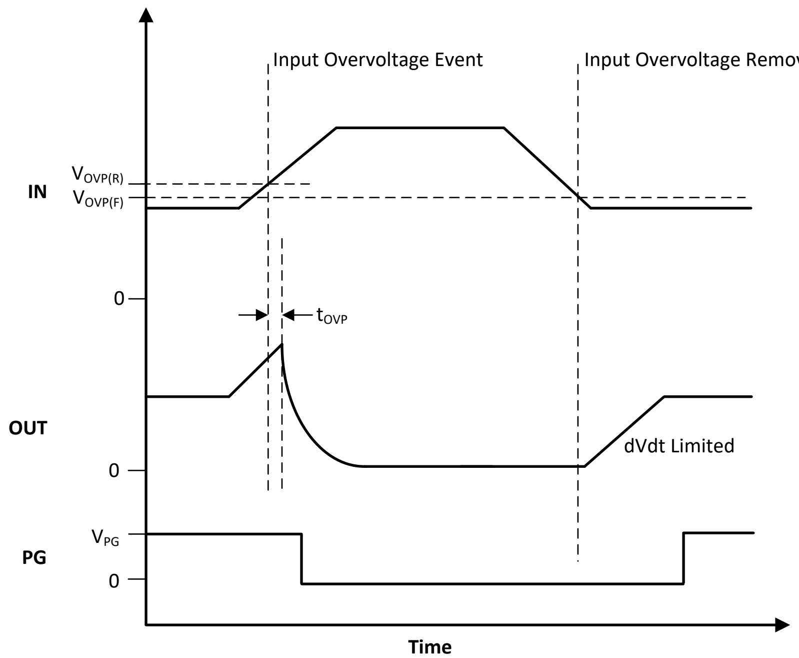


Figure 8-2. Overvoltage Response

There are multiple device options with different fixed overvoltage thresholds to choose from, including one without internal overvoltage protection. See the *Device Comparison Table* for a list of available options.

8.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25980x devices incorporate three levels of protection against overcurrent:

- Adjustable slew rate (dVdt) for inrush current control
- Adjustable overcurrent protection (with adjustable blanking timer) - Circuit Breaker to protect against soft overload conditions
- Adjustable fast-trip response to quickly protect against severe overcurrent (short-circuit) faults

8.3.3.1 Slew Rate and Inrush Current Control (dVdt)

During hot-plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not controlled, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The TPS25980x provides integrated output slew rate (dVdt) control to manage the inrush current during start-up. The inrush current is directly proportional to the load capacitance and rising slew rate. The following equation can be used to calculate the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR(V/ms) = \frac{I_{INRUSH}(mA)}{C_{OUT}(\mu F)} \tag{2}$$

An external capacitance can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the following formula:

$$C_{dVdt}(pF) = \frac{4600}{SR(V/ms)} \tag{3}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

8.3.3.2 Circuit Breaker

The TPS25980x responds to output overcurrent conditions by turning off the output after a user adjustable transient fault blanking interval. When the load current exceeds the programmed current limit threshold (I_{LIM} set by the ILIM pin resistor R_{ILIM}), but lower than the fast-trip threshold (2.1 x I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal pull-down current (I_{ITIMER}). If the load current drops below the current limit threshold before the ITIMER capacitor drops by ΔV_{ITIMER}, the circuit breaker action is not engaged and the ITIMER is reset by pulling it up to V_{INT} internally. This allows short transient overcurrent pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor continues to discharge and once it falls by ΔV_{ITIMER}, the circuit breaker action turns off the FET immediately. The following equation can be used to calculate the R_{ILIM} value for a desired current limit threshold.

$$R_{ILIM}(\Omega) = \frac{1460}{I_{LIM}(A) - 0.11} \quad (4)$$

Note

Leaving the ILIM pin Open sets the current limit to zero and causes the FET to shut off as soon as any load current is detected. Shorting the ILIM pin to ground at any point during normal operation is detected as a fault and the part shuts down. The ILIM pin Short to GND fault detection circuit requires a minimum amount of load current (I_{CB}) to flow through the device. This ensures robust eFuse behavior even under single point failure conditions. Refer to the *Fault Response* section for details on the device behavior after a fault.

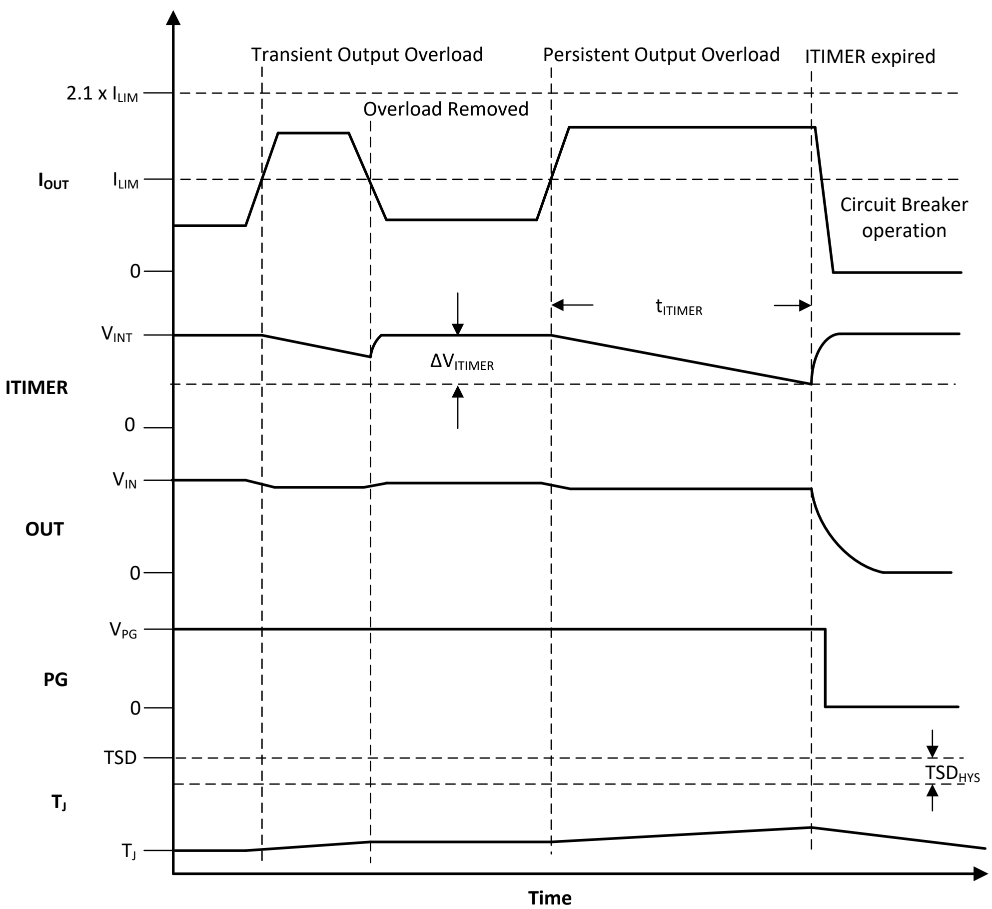


Figure 8-3. Circuit Breaker Response

The duration for which load transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculated using Equation 5.

$$t_{ITIMER}\,(ms) = \frac{C_{ITIMER}\,(nF) \times \Delta V_{ITIMER}\,(V)}{I_{ITIMER}\,(\mu A)} \quad (5)$$

Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.

Table 8-1. Device ITIMER Functional Mode Summary

ITIMER Pin Connection	Timer Delay before Overcurrent response
OPEN	0 s
Capacitor to ground	As per Equation 5
Short to GND	ITIMER Pin Fault - Part Shuts Off

Note

1. Shorting the ITIMER pin to ground is detected as a fault and the part shuts down. This ensures robust eFuse behavior even in case of single point failure conditions. Refer to the *Fault Response* section for details on the device behavior after a fault.

2. Larger ITIMER capacitors take longer to charge during start-up and may lead to incorrect fault assertion if the ITIMER voltage is still below the pin short detection threshold after the device has reached steady state. To avoid this, it is recommended to limit the maximum ITIMER capacitor to the value suggested by the equation below.

$$C_{ITIMER} < \frac{t_{GHI}}{53000}$$

$$t_{GHI} = t_{D,ON} + C_{dvdt} \times \left(\frac{V_{IN} + 3.6V}{I_{dvdt}}\right)$$

Where

- t_{GHI} is the time taken by the device to reach steady state
- $t_{D,ON}$ is the device turn-on delay
- C_{dvdt} is the dVdt capacitance
- I_{dvdt} is the dVdt charging current

It is possible to avoid incorrect ITIMER pin fault assertion and achieve higher ITIMER intervals if needed by increasing the dVdt capacitor value accordingly, but at the expense of higher start-up time.

Once the part shuts down due to a Circuit Breaker fault, it can be configured to either stay latched off or restart automatically. Refer to the *Fault Response* section for details.

8.3.3.3 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator turns off the output within the t_{SC}. The comparator employs a scalable threshold which is equal to 2.1 × I_{LIM}. This enables the user to adjust the fast-trip threshold as per system needs rather than using a fixed threshold which may not be suitable for all systems. After a fast trip event, the device restarts in a current limited mode to try and restore power to the load quickly in case the fast trip was triggered by a transient event. However, if the fault is persistent, the device will stay in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See *Overtemperature Protection (OTP)* section for details on the device response to overtemperature.

In some of the systems, for example servers or telecom equipment which house multiple hot-pluggable cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which could be potentially large enough to inadvertently trigger the fast-trip comparator of the eFuse. The TPS25980x uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating un-interrupted system operation.

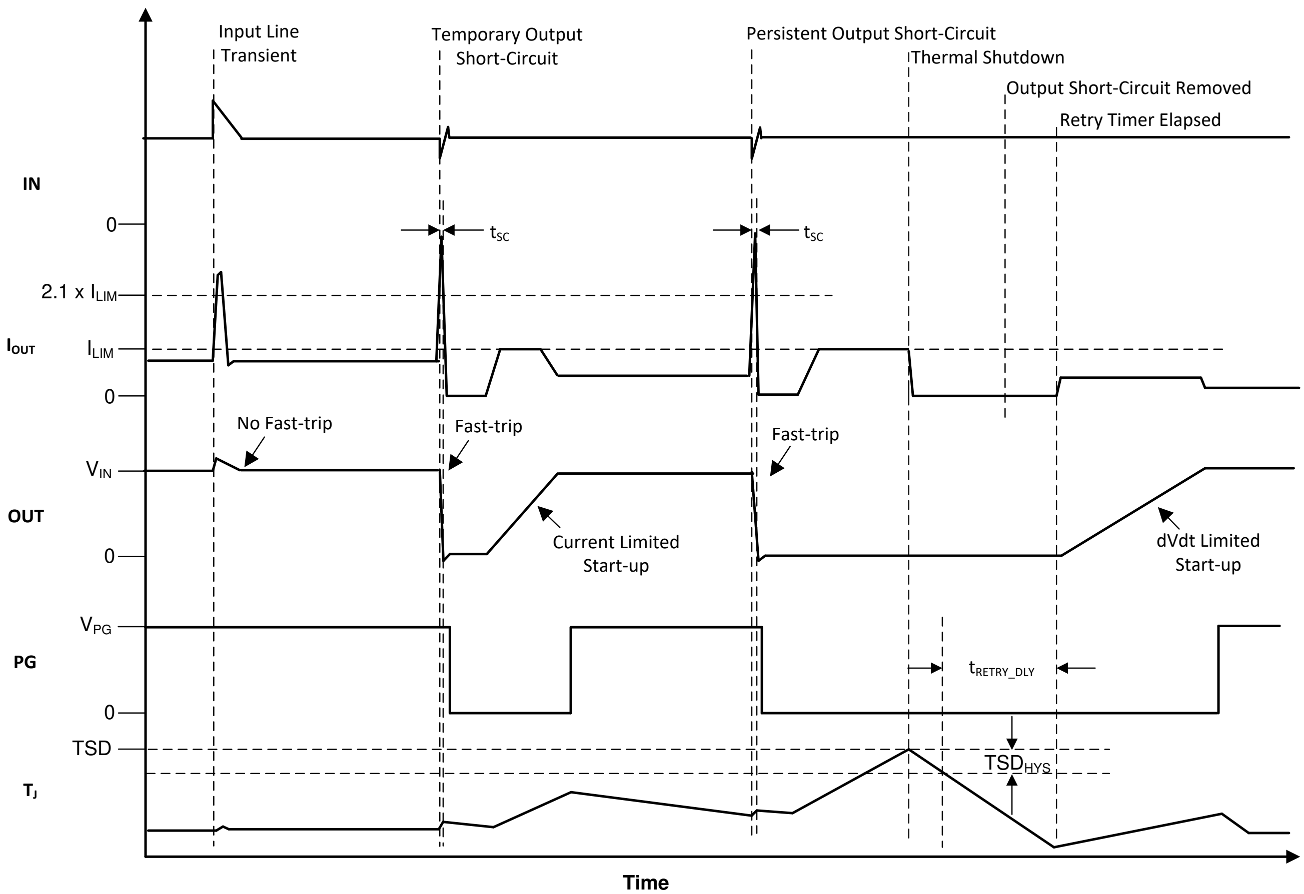


Figure 8-4. Input Line Transient and Output Short-Circuit Response

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Note

To prevent the circuit breaker loop from interfering with the input line transient detection logic, TI recommends to set the ITIMER interval higher than 100 µs. Refer to *Table 8-1* for more details on ITIMER.

8.3.4 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device will not turn back on until the die cools down sufficiently, that is the die temperature falls below (TSD - TSDHys). Thereafter, the part can be configured to either remain latched off or restart automatically. Refer to the *Fault Response* section for details.

8.3.5 Analog Load Current Monitor (IMON)

The device allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The user can connect a resistor from IMON to ground to convert this signal to a voltage which can be fed to the input of an Analog-to-Digital Converter. The internal amplifier on the IMON employs chopper based offset cancellation techniques to provide accurate measurement even at lower currents over time and temperature.

$$V_{IMON}(V) = G_{IMON}(\mu A / A) \times I_{OUT}(A) \times R_{IMON}(\Omega) \quad (6)$$

It is recommended to limit the maximum IMON voltage to the values mentioned in *VIMON(Max) Recommended Values* . This is to ensure the IMON pin internal amplifier has sufficient headroom to operate linearly.

Table 8-2. $V_{IMON(MAX)}$ Recommended Values

V_{IN}	Recommended $V_{IMON(MAX)}$
2.7 V	1 V
3.3 V	1.8 V
> 5 V	3.3 V

It is recommended to add a RC low pass filter on the IMON output to filter out any glitches and get a smooth average current measurement. TI recommends a series resistance of 10 kΩ or higher.

8.3.6 Power Good (PG)

PG is an active high open drain output which indicates whether the FET is fully turned ON and the output voltage has reached the maximum value. After power-up, PG is pulled low initially. The gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches (V_{IN} + 3.6V), PG is asserted after a de-glitch time (t_{PGD}). During normal operation, if at any time V_{OUT} falls below (V_{IN} - V_{PGTHD}), PG is de-asserted after a de-glitch time (t_{PGD}).

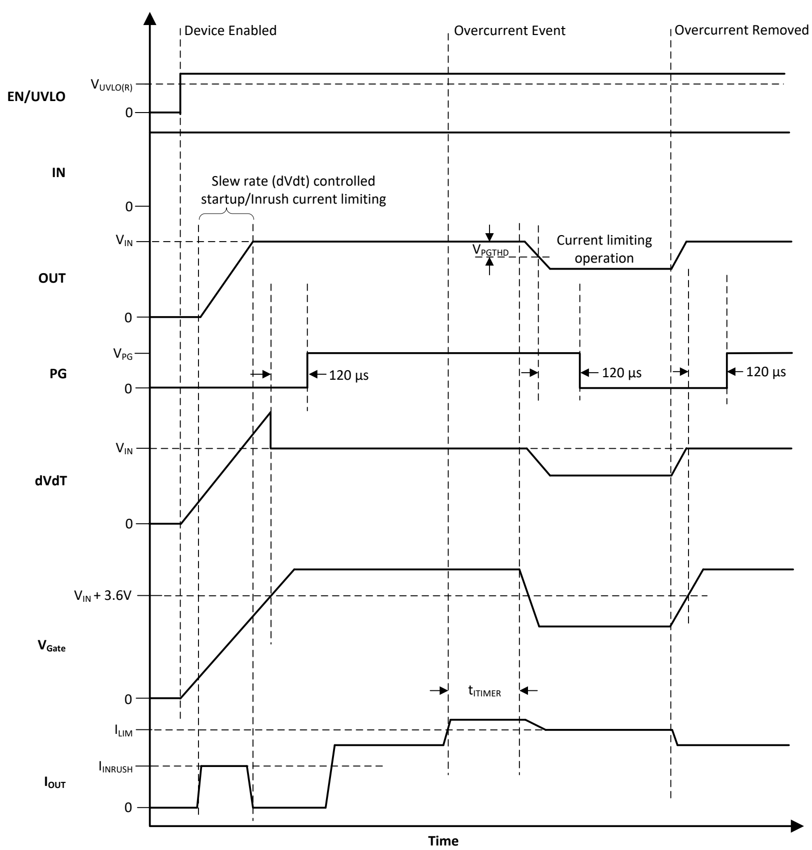


Figure 8-5. Power Good Assertion and De-assertion

Note

1. When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the TPS25980x is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which in turn is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

2. The PG pin provides a mechanism to detect a possible failed MOSFET condition during start-up. If the PG does not get asserted for an extended period of time after the device is powered up and enabled, it might be an indication of internal MOSFET failure.

8.3.7 Load Detect/Handshake (LDSTRT)

The LDSTRT pin provides a mechanism for the downstream load circuit to indicate to the TPS25980x that the load is present and has powered up successfully. This allows the system to have additional control over the conditions in which power is presented to the load and disconnect the power when the load is not present or unable to provide a valid handshake signal after an expected boot-up time.

Once the TPS25980x completes the startup sequence and the output reaches the full voltage, it asserts the PG signal. At the same time, it also starts charging the capacitor on the LDSTRT pin (C_{LDSTRT}) with an internal current source (I_{LDSTRT}). If the LDSTRT pin voltage rises above V_{LDSTRT} before the load circuit pulls it low, the TPS25980x detects the condition as a LDSTRT fault and turns off the FET to power down the load. The time to trigger the LDSTRT fault can be calculated from the following equation:

$$t_{LDSTRT}\,(ms) = \frac{C_{LDSTRT}\,(nF) \times V_{LDSTRT}\,(V)}{I_{LDSTRT}\,(\mu A)} \tag{7}$$

During normal operation, if at any time the load circuit releases the active pull-down on the LDSTRT pin, the capacitor C_{LDSTRT} would start charging up again and eventually trigger a shutdown due to LDSTRT fault once the capacitor charges up to V_{LDSTRT}.

Once the TPS25980x turns off due to LDSTRT fault, it can be turned ON again in 3 ways:

- LDSTRT pin is driven low
- Input supply voltage is driven low (< $V_{UVP(F)}$) and then driven high (> $V_{UVP(R)}$)
- EN/UVLO voltage is driven low (< V_{SD}) and then driven high (> $V_{UVLO(R)}$)

Tie the LDSTRT pin to ground if this functionality is not needed.

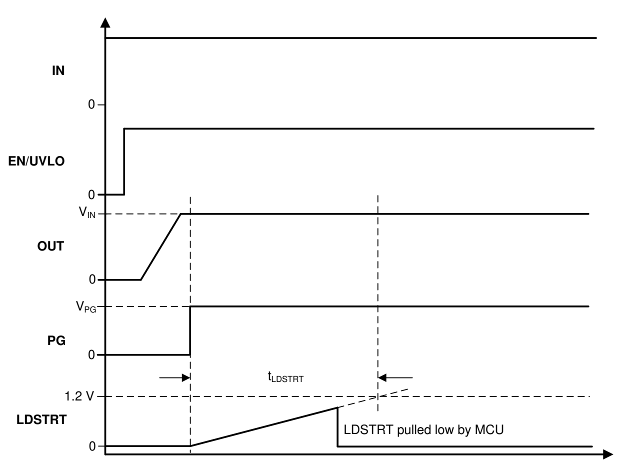


Figure 8-6. Successful LDSTRT Handshake

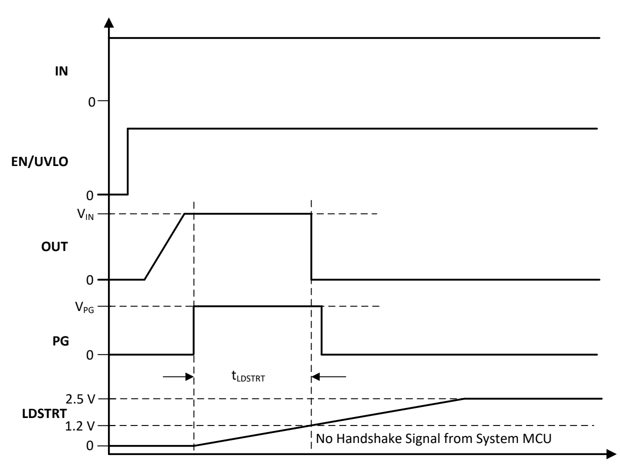


Figure 8-7. Unsuccessful LDSTRT Handshake

The LDSTRT pin can also be used to implement a load or module detect function wherein the output power is presented only when the load or module is plugged in. A typical use case for this function is on optical module power supply rails in Switches/Routers or similar networking end equipment. The LDSTRT pin should be tied to a corresponding pin on the module connector which gets pulled low by the module when it is plugged in. An example of such a signal is ModPrsL on QSFP-DD modules.

In this scheme, initially when the TPS25980x is powered up or enabled, the output charges up and PG is asserted. If the module is not plugged in, there is no external pull-down on the LDSTRT pin and the pin voltage starts rising due to internal pull-up . Once the LDSTRT pin voltage exceeds V_{LDSTRT}, the TPS25980x turns off the output power. If the module is plugged in later, the LDSTRT pin is pulled low by the module and the TPS25980x turns on the output power.

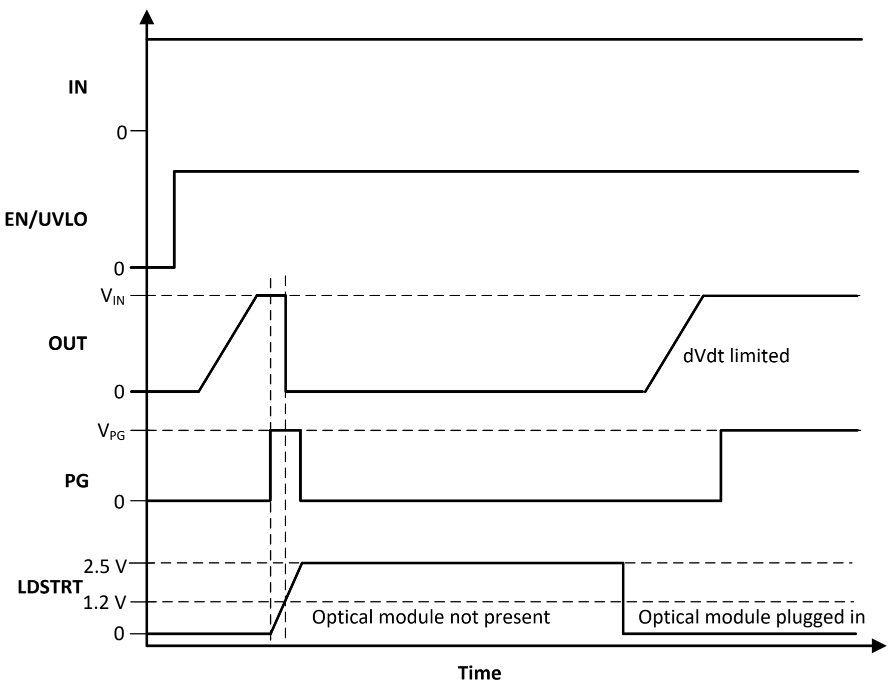


Figure 8-8. Optical Module Plug-In Detection Using LDSTRT

8.4 Fault Response

The following events trigger an internal fault which causes the device to shut down:

- Overtemperature Protection
- Circuit Breaker Operation
- ITIMER pin Short to GND
- ILIM pin Short to GND

Once the device shuts down due to a fault, even if the associated external fault is subsequently cleared, the fault stays latched internally and the output cannot turn on again until the latch is reset. The fault latch can be externally reset by one of the following methods:

- Input supply voltage is driven low (< $V_{UVP(F)}$)
- EN/UVLO voltage is driven low (< V_{SD})

The fault latch can also be reset by an internal auto-retry logic. The user can either disable the auto-retry behavior completely (latch-off behavior) or configure the device to auto-retry indefinitely or for a limited number of times before latching off. The auto-retry behavior is controlled by the connections on the RETRY_DLY and NRETRY pins.

Table 8-3. Pin Configurable Fault Response

EN/UVLO	RETRY_DLY	NRETRY	DEVICE STATE
L	X	X	Disabled
H	Short to GND	X	No auto-retry (Latch-off)
H	Open	Open	Auto-retry 4 times with minimum delay between retries and then latch-off
H	Open	Short to GND	Auto-retry indefinitely with minimum delay between retries
H	Capacitor to GND	Capacitor to GND	Auto-retry delay and count as per Equation 8 and Equation 9
H	Capacitor to GND	Open	Auto-retry 4 times with finite delay between retries as per Equation 8 and then latch-off
H	Capacitor to GND	Short to GND	Auto-retry indefinitely with finite delay between retries as per Equation 8

To configure the part for a finite number of auto-retries with a finite auto-retry delay, first choose the capacitor value on RETRY_DLY pin using the following equation.

$$t_{RETRY\_DLY}\,(\mu s) = \frac{128 \times \left(C_{RETRY\_DLY}\,(pF) + 4\ pF\right) \times V_{RETRY\_DLY\_HYS}\,(V)}{I_{RETRY\_DLY}\,(\mu A)} \tag{8}$$

Next, choose the capacitor value on the NRETRY pin using the following equation.

$$N_{RETRY} = \frac{4 \times I_{RETRY\_DLY}\,(\mu A) \times C_{NRETRY}\,(pF)}{I_{NRETRY}\,(\mu A) \times \left(C_{RETRY\_DLY}\,(pF) + 4\ pF\right)} \tag{9}$$

The number of auto-retries is quantized to certain discrete levels as shown in Table 8-4 .

Table 8-4. NRETRY Quantization Levels

NRETRY Calculated From Equation 9	NRETRY Actual
0 < N < 4	4
4 < N < 16	16
16 < N < 64	64
64 < N < 256	256
256 < N < 1024	1024

Table 8-5. NRETRY and RETRY_DLY Combination Examples

Auto Retry Delay	915 ms	416 ms	91.7 ms	9.3 ms	3 ms
RETRY_DLY Capacitor	22 nF	10 nF	2.2 nF	220 pF	68 pF
No. of Auto Retries	**NRETRY Capacitor**				
4	Open				
16	47 nF	22 nF	4.7 nF	1 nF	220 pF
64	0.22 µF	0.1 µF	22 nF	2.2 nF	1 nF
256	1 µF	0.47 µF	0.1 µF	10 nF	4.7 nF
1024	3.3 µF	1.5 µF	0.47 µF	33 nF	10 nF
Infinite	Short to GND				

A spreadsheet design tool *TPS25980xx Design Calculator* is also available for simplified calculations.

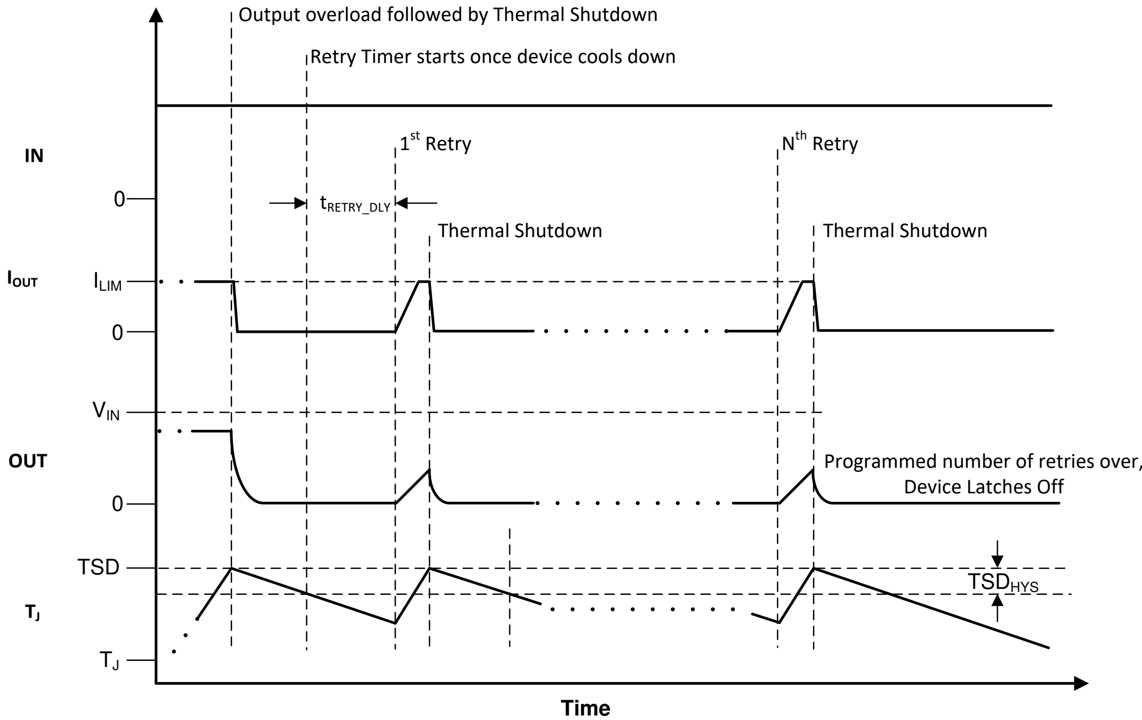


Figure 8-9. Auto-Retry After Fault

The auto-retry logic has a mechanism to reset the count to zero if two consecutive faults occur far apart in time. This ensures that the auto-retry response to any later fault is handled as a fresh sequence and not as a continuation of the previous fault. If the fault which triggered the shutdown and subsequent auto-retry cycle is cleared eventually and does not occur again for a duration equal to 7 retry delay timer periods starting from the last fault, the auto-retry logic resets the internal auto-retry count to zero.

8.5 Device Functional Modes

The TPS25980x can be pin strapped to support various configurable functional modes.

Table 8-6. LDSTRT Handshake Functional Modes

EN/UVLO	LDSTRT	DEVICE STATE
L	X	Disabled
H	L	ON
H	H	OFF

Refer to *Load Detect/Handshake (LDSTRT)* section for more details.

Table 8-7. Fault Response Functional Modes

EN/UVLO	RETRY_DLY	NRETRY	DEVICE STATE
L	X	X	Disabled
H	Short to GND	X	No auto-retry (Latch-off)
H	Open	Open	Auto-retry 4 times with minimum delay between retries and then latch-off
H	Open	Short to GND	Auto-retry indefinitely with minimum delay between retries
H	Capacitor to GND	Capacitor to GND	Auto-retry delay and count as per Equation 8 and Equation 9
H	Capacitor to GND	Open	Auto-retry 4 times with finite delay between retries as per Equation 8 and then latch-off
H	Capacitor to GND	Short to GND	Auto-retry indefinitely with finite delay between retries as per Equation 8

Refer to *Fault Response* section for more details.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS25980x device is an integrated 8-A eFuse that is typically used for hot-swap and power rail protection applications. It operates from 2.7 V to 24 V with adjustable overcurrent and undervoltage protection. It also provides optional overvoltage with various fixed internal thresholds. The device aids in controlling the inrush current and has the flexibility to configure the number of auto-retries and retry delay. The adjustable overcurrent blanking timer provides the functionality to allow transient overcurrent pulses without limiting or tripping. These devices protect source, load and internal MOSFET from potentially damaging events in systems such as PCIe cards, SSDs, HDDs, Optical Modules, Routers, Switches, Industrial PCs, Retail ePOS (Point-of-sale) terminals and Patient Monitoring Systems.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool *TPS25980xx Design Calculator* is available in the web product folder.

9.2 Typical Application: Patient Monitoring System in Medical Applications

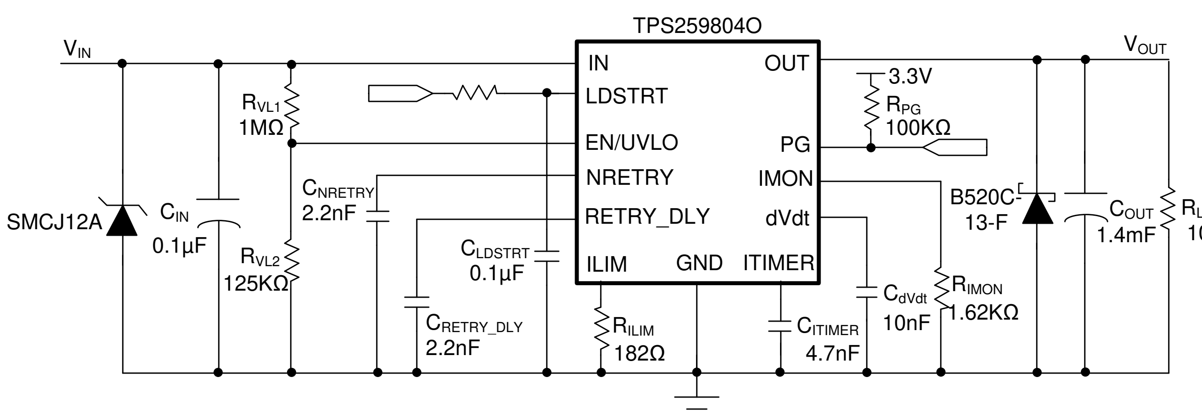


Figure 9-1. Typical Application Schematic - Input Protection for Patient Monitoring System

9.2.1 Design Requirements

Table 9-1 shows the design parameters for this application example.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	10.8 V
Maximum load current, I_{OUT}	6.5 A
Current limit, I_{LIM}	8 A
Transient overcurrent blanking interval (t_{ITIMER})	2 ms
Load capacitance, C_{OUT}	1.4 mF
Load at start-up, $R_{L(SU)}$	10 Ω
Output voltage ramp time, T_{dVdt}	20 ms
Maximum ambient temperature, T_A	70 °C

Table 9-1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Retry delay, t_{RETRY_DLY}	100 ms
No. of retries, N_{RETRY}	4

9.2.2 Detailed Design Procedure

9.2.2.1 Device Selection

This design example considers a 12-V system operating voltage with a tolerance of ±10 %. The rated load current is 6.5 A. If the current exceeds 8 A, then the device must allow overload current for 2-ms interval before breaking the circuit and then restart. Accordingly, the TPS259804O variant is chosen. (Refer to *Device Comparison Table* for device options.) Ambient temperatures may range from 20 °C to 70 °C. The load has a minimum input capacitance of 1.4 mF and start-up resistive load of 10 Ω. The downstream load is turned on only after the PG signal is asserted.

9.2.2.2 Setting the Current Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the overload current limit, whose value can be calculated using Equation 10.

$$R_{ILIM}(\Omega) = \frac{1460}{I_{LIM}(A) - 0.11} \tag{10}$$

For I_{LIM} = 8 A, R_{ILIM} value is calculated to be 185.04 Ω. Choose the closest available standard value: 182 Ω, 1%. Refering to the Electrical Characteristics table, it can be verified that the minimum current limit across temperature for R_{ILIM} value of 182 Ω is 7.23 A, which is higher than the nominal rated load current (6.5 A), thereby ensuring stable operation under normal conditions.

9.2.2.3 Setting the Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_{VL1} and R_{VL2} connected between IN, EN/UVLO and GND pins of the device. The resistor values required for setting the undervoltage are calculated using Equation 11.

$$VIN_{UVLO} = \frac{V_{UVLO(R)} \text{ x } (R_{VL1} + R_{VL2})}{R_{VL2}} \tag{11}$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_{VL1} and R_{VL2}. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{RVL12} must be 20 times greater than the leakage current (I_{ENLKG}).

From the device electrical specifications, UVLO rising threshold $V_{UVLO(R)}$ = 1.2 V. From design requirements, VIN_{UVLO} = 10.8 V. First choose the value of R_{VL1} = 1 MΩ and use Equation 11 to calculate R_{VL2} = 125 kΩ.

Use the closest standard 1% resistor values: R_{VL1} = 1 MΩ, and R_{VL2} = 125 kΩ

9.2.2.4 Choosing the Current Monitoring Resistor: R_{IMON}

Voltage at IMON pin V_{IMON} is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the maximum IMON pin voltage at full-scale load current. The maximum IMON pin voltage must be selected based on the input voltage range of the ADC used or the value suggested in *VIMON(Max) Recommended Values*, whichever is lower. R_{IMON} is set using Equation 12.

$$R_{IMON}(\Omega) = \frac{V_{IMONmax}(V)}{I_{OUTmax}(A) \times 246 \times 10^{-6}} \quad (12)$$

For I_{LIM} = 8 A and considering the operating range of ADC to be 0 V to 3.3 V, R_{IMON} can be calculated as

$$R_{IMON} = \frac{3.3}{8 \times 243 \times 10^{-6}} = 1697\ \Omega \quad (13)$$

Selecting R_{IMON} value less than shown in Equation 13 ensures that ADC limits are not exceeded for maximum value of load current. Choose closest available standard value: 1620 Ω, 1 %.

9.2.2.5 Setting the Output Voltage Ramp Time (T_{dVdt})

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The required ramp-up capacitor C_{dVdt} is calculated considering the two possible cases (see *Case 1: Start-Up Without Load: Only Output Capacitance C_{OUT} Draws Current* and *Case 2: Start-Up With Load:Output Capacitance C_{OUT} and Load Draw Current*)

9.2.2.5.1 Case 1: Start-Up Without Load: Only Output Capacitance C_{OUT} Draws Current

During start-up, as the output capacitor charges, the voltage drop as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using equation 14

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (14)$$

Where I_{INRUSH} is the inrush current and is determined by Equation 15

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{dVdt}} \quad (15)$$

Equation 14 assumes that the load does not draw any current (apart from the capacitor charging current) until the output voltage has reached its final value.

9.2.2.5.2 Case 2: Start-Up With Load: Output Capacitance C_{OUT} and Load Draw Current

When the load draws current during the turn-on sequence, there is additional power dissipated. Considering a resistive load during start-up $R_{L(SU)}$, load current ramps up proportionally with increase in output voltage during T_{dVdt} time. Equation 16 shows the average power dissipation in the internal FET during charging time due to resistive load.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{IN}^2}{R_{L(SU)}} \quad (16)$$

Equation 17 gives the total power dissipated in the device during start-up

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (17)$$

The power dissipation, with and without load, for selected start-up time must not exceed the start-up thermal shutdown limits as shown in *Thermal Shutdown Plot During Start-up*

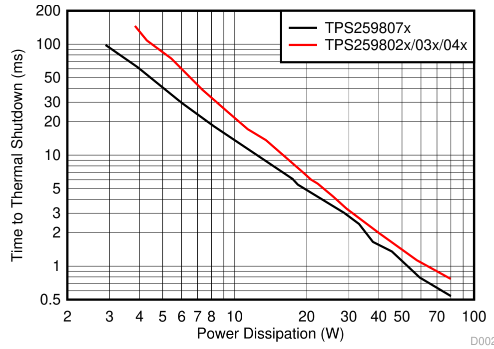


Figure 9-2. Thermal Shutdown Plot During Start-up

For the design example under discussion, the output voltage has to be ramped up in 20 ms, which mandates a slew-rate of 0.6 V/ms for a 12 V rail.

The required C_{dVdt} capacitance on dVdt pin to set 0.6 V/ms slew rate can be calculated using Equation 18

$$C_{dVdt}(pF) = \frac{4600}{SR(V/ms)} = 7666\ pF \tag{18}$$

The dVdt capacitor is subjected to typically V_{IN}+ 4 V during startup. The high voltage bias leads to a drop in the effective capacitor value. So, it is suggested to choose 20% higher than the calculated value, which gives 9.2 nF. Choose closest 10% standard value: 10 nF

The 10 nF C_{dVdt} capacitance sets a slew-rate of 0.46 V/ms and output ramp time T_{dVdt} of 26 ms.

The inrush current drawn by the load capacitance C_{OUT} during ramp-up can be calculated using Equation 19

$$I_{INRUSH} = 1.4\ mF \times \frac{12\ V}{26\ ms} = 0.65\ A \tag{19}$$

The inrush power dissipation can be calculated using Equation 20

$$P_{D(INRUSH)} = 0.5 \times 12 \times 0.65 = 3.9\ W \tag{20}$$

For 3.9 W of power loss, the thermal shutdown time of the device must be greater than the ramp-up time T_{dVdt} to ensure a successful start-up. *Figure 9-2* shows the start-up thermal shutdown limit. For 3.9 W of power, the shutdown time is approximately 100 ms. So it is safe to use 26 ms as the start-up time without any load on the output.

The additional power dissipation when a 10-Ω load is present during start-up is calculated using Equation 21

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{12^2}{10} = 2.4W \tag{21}$$

The total device power dissipation during start-up can be calculated using Equation 22

$$P_{D(STARTUP)} = 3.9 + 2.4 = 6.3\ W \tag{22}$$

From *Thermal Shutdown Plot During Start-up*, the thermal shutdown time for 6.3 W is approximately 40 ms. It is safe to have 30% margin to allow for variation of system parameters such as load, component tolerance, and input voltage. So it is well within acceptable limits to use the 10 nF for C_{dVdt} capacitor with start-up load of 10 Ω.

When C_{OUT} is large, there is a need to decrease the power dissipation during start-up. This can be done by increasing the value of the C_{dVdt} capacitor. A spreadsheet tool *TPS25980xx Design Calculator* available on the web can be used for iterative calculations.

9.2.2.6 Setting the Load Handshake (LDSTRT) Delay

To indicate a successful start-up, the load circuit must provide a handshake signal to TPS25980x by pulling down the LDSTRT pin within the time set by the capacitor C_{LDSTRT} on the LDSTRT pin. Once the PG asserts, the device sources 2-µA current into C_{LDSTRT}. For a successful handshake, the load circuit must pull-down the LDSTRT pin before C_{LDSTRT} charges up to 1.2 V.

For the design requirement of 60-ms handshake delay, use Equation 23 to calculate C_{LDSTRT}

$$C_{LDSTRT} = I_{LDSTRT} \times \frac{t_{LDSTRT}}{V_{LDSTRT}} = 2\mu A \times \frac{60ms}{1.2V} = 0.1\mu F \tag{23}$$

Choose closest available standard value: 0.1 µF, 10 %.

9.2.2.7 Setting the Transient Overcurrent Blanking Interval (t_{ITIMER})

For the design example under discussion, overcurrent transients are allowed for 2-ms duration. This blanking interval can be set by selecting appropriate capacitor C_{ITIMER} from ITIMER pin to ground. The value of C_{ITIMER} to set 2 ms for t_{ITIMER} can be calculated using Equation 24.

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms)}{0.47} = 4.255\ nF \tag{24}$$

Choose closest available standard value: 4.7 nF, 10 %.

9.2.2.8 Setting the Auto-Retry Delay and Number of Retries

The time delay between retries can be programmed by selecting capacitor C_{RETRY_DLY} on RETRY_DLY pin. The value of C_{RETRY_DLY} to set a 100-ms auto-retry delay can be calculated using Equation 25.

$$C_{RETRY\_DLY}\,(pF) = \frac{t_{RETRY\_DLY}\,(\mu s)}{46.83} - 4\ pF = 2131.38\ pF \tag{25}$$

Choose closest available standard value: 2.2 nF, 10 %.

The number of auto-retry attempts can be set by a capacitor C_{NRETRY} on the NRETRY pin using Equation 26

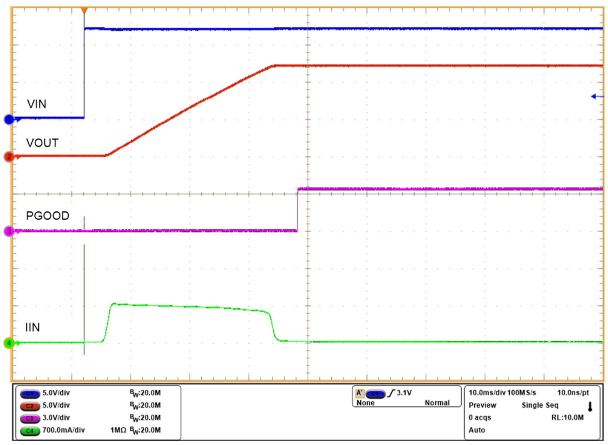
$$N_{RETRY} = \frac{4 \times C_{NRETRY}\,(pF)}{C_{RETRY\_DLY}\,(pF) + 4\ pF} \tag{26}$$

For this design example, the requirement is to retry 4 times after the device shuts down due to a fault. Since, the number of auto-retries can be adjusted in discrete steps as explained in *Fault Response*, choose C_{NRETRY} such that N_{RETRY} is less than 4. Use Equation 27 to calculate C_{NRETRY}.

$$C_{NRETRY}\,(pF) < \frac{N_{RETRY} \times \left(C_{RETRY\_DLY}\,(pF) + 4\ pF\right)}{4} < 2204\ pF \tag{27}$$

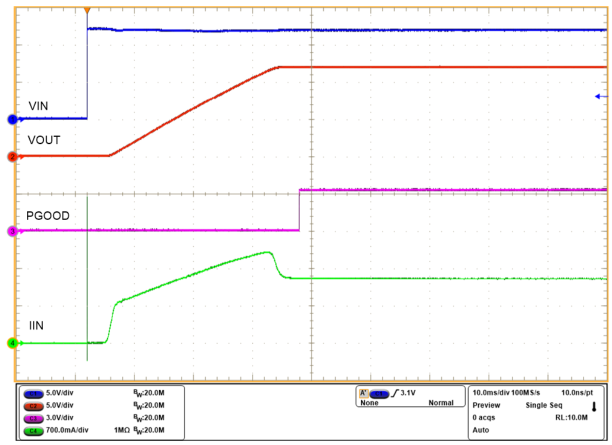
Choose closest available standard value: 2.2 nF, 10 %.

9.2.3 Application Curves



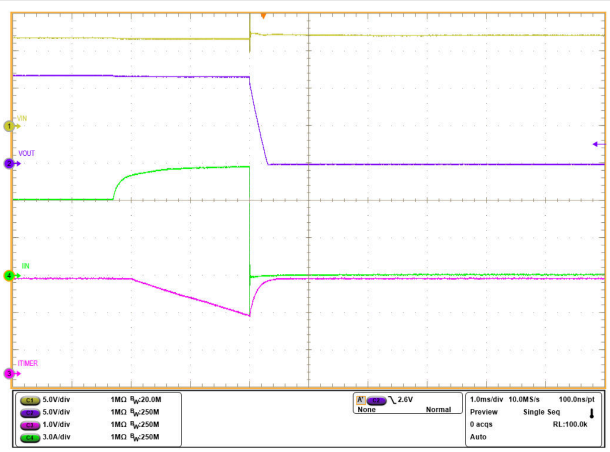
A. C_{OUT} = 1.4 mF C_{dVdt} = 10 nF $R_{L(SU)}$ = Open

Figure 9-3. Hot-Plug Start-Up Without Load on Output - dVdt Limited



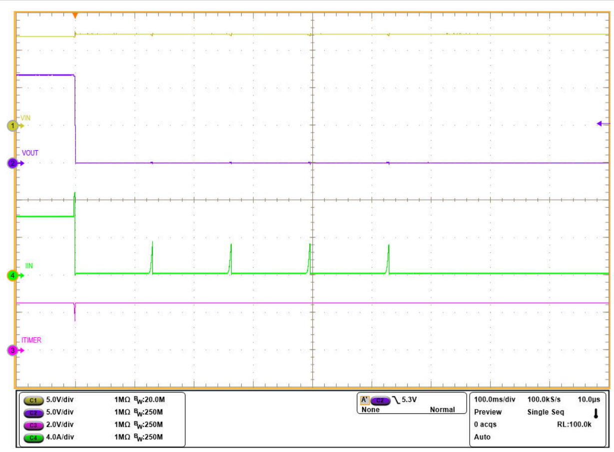
A. C_{OUT} = 1.4 mF C_{dVdt} = 10 nF $R_{L(SU)}$ = 10 Ω

Figure 9-4. Hot-Plug Start-Up With Load on Output - dVdt Limited



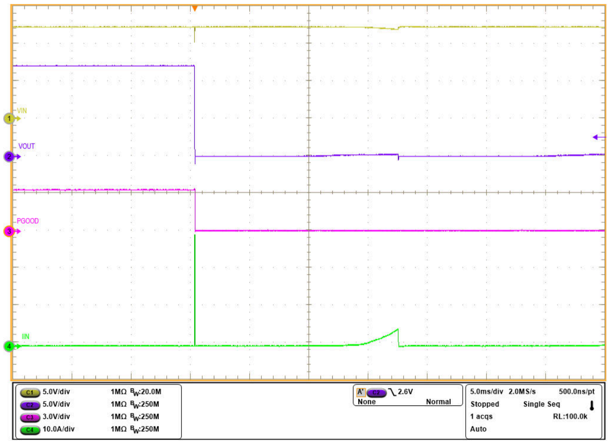
A. R_{ILIM} = 182 Ω C_{ITIMER} = 4.7 nF

Figure 9-5. Circuit Breaker With Transient Overcurrent Blanking Interval of 2 ms



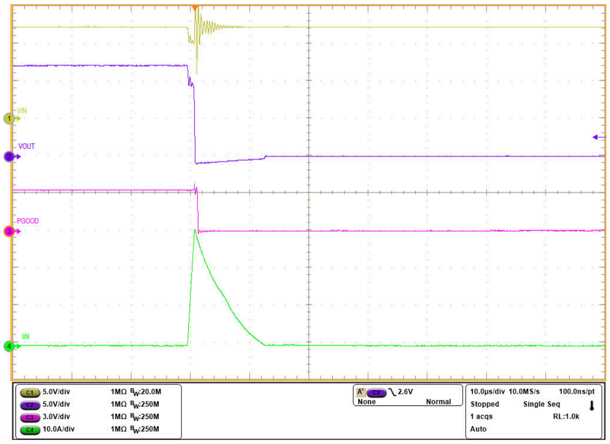
A. R_{ILIM} = TBD Ω C_{ITIMER} = 4.7 nF C_{RETRY_DLY} = 2.2 nF, C_{NRETRY} = 2.2 nF

Figure 9-6. Circuit Breaker - Auto-Retry 4 Times With Retry Delay of 100 ms



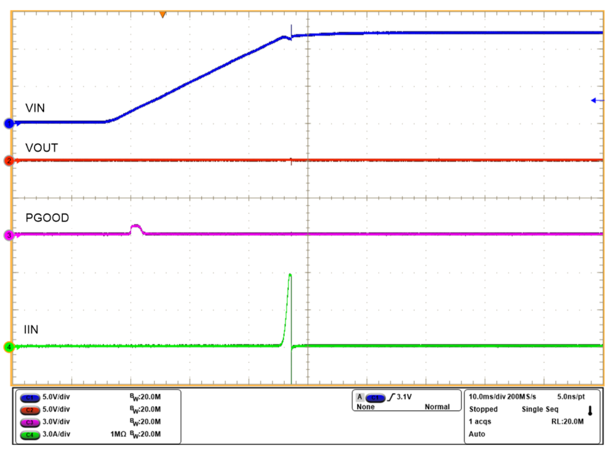
A. R_{ILIM} = 182 Ω

Figure 9-7. Output Hard Short-Circuit While ON



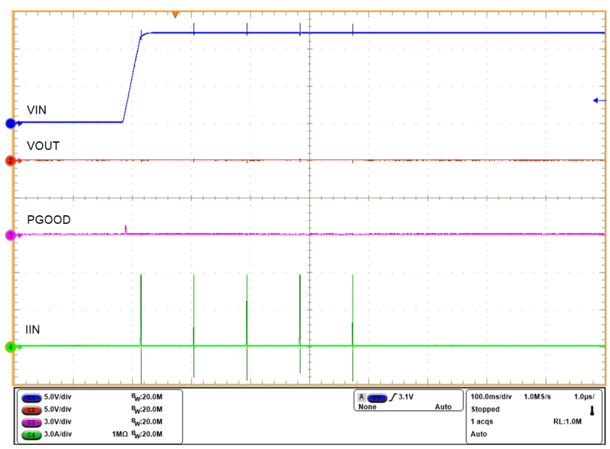
A. R_{ILIM} = 182 Ω

Figure 9-8. Output Hard Short-Circuit While ON (Zoomed In)



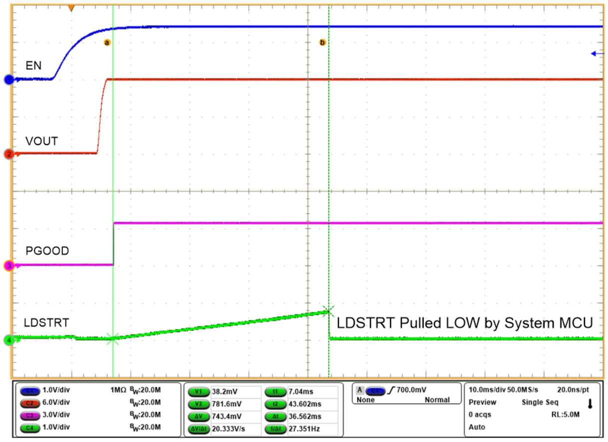
A. R_{ILIM} = 182 Ω

Figure 9-9. Power-Up With Short-Circuit on Output



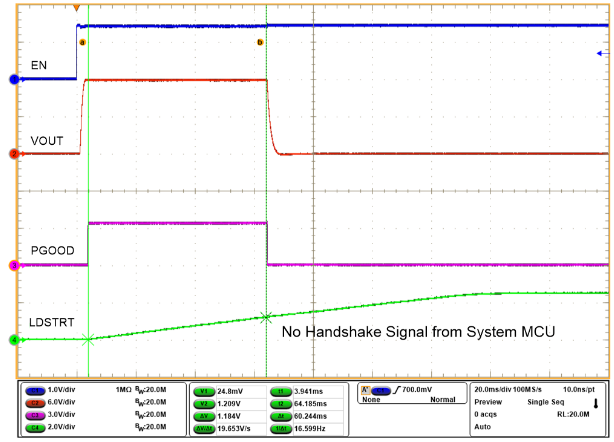
A. R_{ILIM} = 182 Ω

Figure 9-10. Power-Up With Short-Circuit on Output - Auto-Retry 4 Times With Retry Delay of 100 ms



A. C_{LDSTRT} = 0.1 µF

Figure 9-11. Successful Load Handshake (LDSTRT)



A. C_{LDSTRT} = 0.1 µF

Figure 9-12. Unsuccessful Load Handshake (LDSTRT)

9.3 System Examples

9.3.1 Optical Module Power Rail Path Protection

Optical modules are commonly used in high-bandwidth data communication systems such as Optical Networking equipment, Enterprise/Data-Center Switches and Routers. Several variants of optical modules are available in the market, which differ in the form-factor and the data speed support (Gbit/s). Of these, the popular variant Double Dense Quad Small Form-factor Pluggable (QSFP-DD) module supports speeds up to 400 Gbit/s. In addition to the system protection during hot-plug events, the other key requirement for optical module is the tight voltage regulation. The optical module uses 3.3 V supply and requires voltage regulation within ±5 % for proper operation.

A typical power tree of such system is shown in Figure 9-13. The optical line card consists of DC-DC converter, protection device (eFuse) and power supply filters. The DC-DC converter steps-down the 12 V to 3.3 V and maintains the 3.3 V rail within ±2 %. The power supply filtering network uses ‘LC’ components to reduce high frequency noise injection into the optical module. The DC resistance of the inductor ‘L’ causes voltage drop of around 1.5 % which leaves us with a voltage drop budget of just 1.5 % (3.3 V * 1.5% = 50 mV) across the protection device. Considering a maximum load current of 5.5 A per module, the maximum ON-resistance of the protection device should be less than 9 mΩ. TPS25980x eFuse offers ultra-low ON-resistance of 2.7 mΩ (typical) and 4.5 mΩ (maximum, across temperature), thereby meeting the target specification with additional margin to spare and simplifying the overall system design.

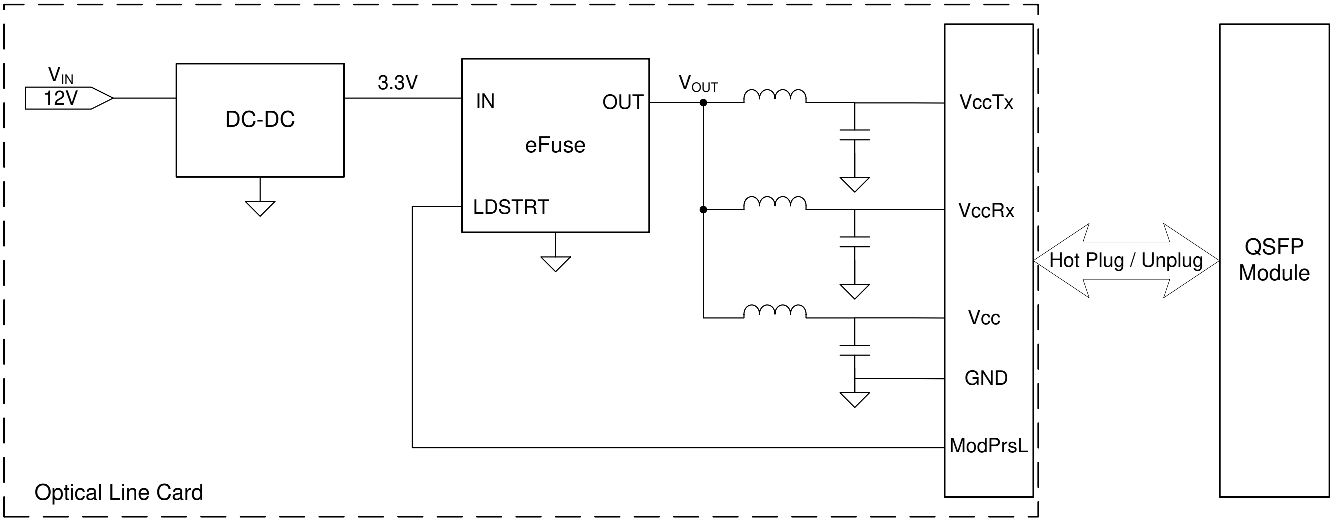


Figure 9-13. Power Tree Block Diagram of a Typical Optical Line Card

As shown in *Figure 9-13*, ModPrsL signal acts as a handshake signal between the line card and the optical module. ModPrsL is always pulled to ground inside the module. When the module is hot-plugged into the host “Optical Line Card” connector, the ModPrsL signal pulls down the LDSTRT pin and enables the TPS25980x eFuse to power the module. This ensures that power is applied on the port only when a module is plugged in and disconnected when there is no module present.

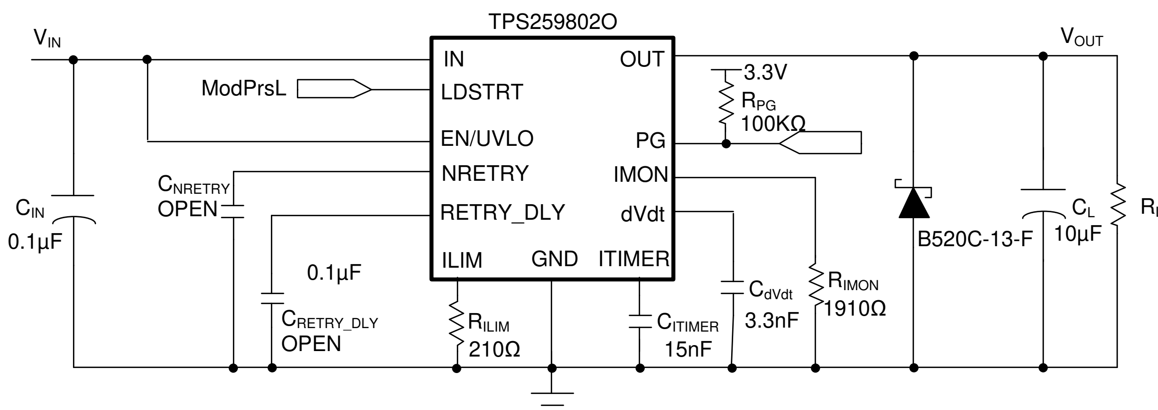


Figure 9-14. TPS259802O Configured for a 3.3-V Power Rail Path Protection in Optical Module

9.3.1.1 Design Requirements

Table 9-2 shows the design parameters for this example.

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_{IN}	3.3 V
Overvoltage lockout, V_{OVP}	3.7 V
Maximum voltage drop in the path	± 5 %
Maximum load current, I_{OUT}	5.5 A
Current limit, I_{LIM}	7 A
Transient overcurrent blanking interval (t_{ITIMER})	6 ms
Load capacitance, C_{OUT}	10 µF
Maximum ambient temperature, T_A	85 °C
Module present detection, ModPrsL	Yes

Table 9-2. Design Parameters (continued)

Retry delay, t_{RETRY_DLY}	200 µs
No. of retries, N_{RETRY}	4

9.3.1.2 Device Selection

Optical modules are very sensitive to supply voltage variations and thus require input overvoltage protection. TPS259802O variant from TPS25980x family is selected to set overvoltage protection at 3.7 V. TPS259802O allows overcurrents for a user specified blanking interval t_{ITIMER} before breaking the circuit path. In this use case, t_{ITIMER} is set for 6 ms interval.

9.3.1.3 External Component Settings

By following similar design procedure as outlined in *Detailed Design Procedure*, the external component values are calculated as below

- R_{ILIM} = 210 Ω to set 7-A current limit
- C_{ITIMER} = 15 nF to set fault blanking time of 6 ms
- R_{IMON} = 1910 Ω to set maximum IMON pin voltage V_{IMON} within ADC range of 3.3 V
- C_{dVdt} capacitance is chosen as 3.3 nF
- Leave RETRY_DLY and NRETRY pins OPEN to set minimum auto-retry delay of 200 µs and number of retries to 4

9.3.1.4 Voltage Drop

Table 9-3 shows the power path voltage drop (%) due to the eFuse in QSFP modules of different power classes.

Table 9-3. Voltage Drop across TPS25980x on QSFP Module Power Rail

POWER CLASS	MAXIMUM POWER CONSUMPTION PER MODULE (W)	MAXIMUM LOAD CURRENT (A)	TYPICAL VOLTAGE DROP (%)
1	1.5	0.454	0.037
2	3.5	1.06	0.087
3	7	2.12	0.174
4	8	2.42	0.2
5	10	3.03	0.248
6	12	3.63	0.3
7	14	4.24	0.347
8	18	5.45	0.446

9.3.1.5 Application Curves

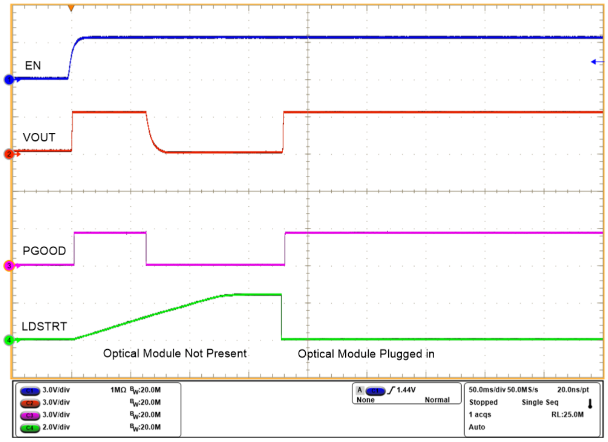


Figure 9-15. Output Voltage Profile When Optical Module is Inserted

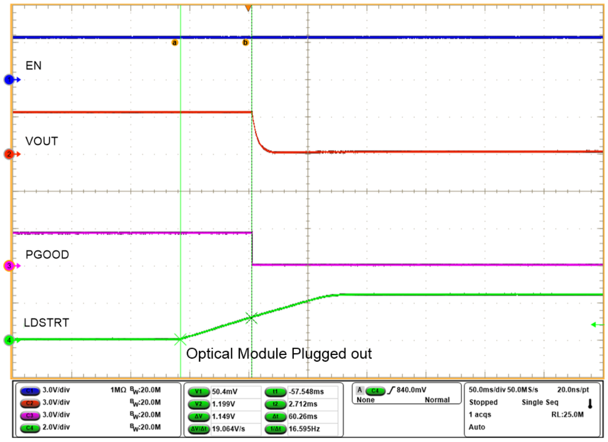


Figure 9-16. Output Voltage Profile When Optical Module is Plugged Out

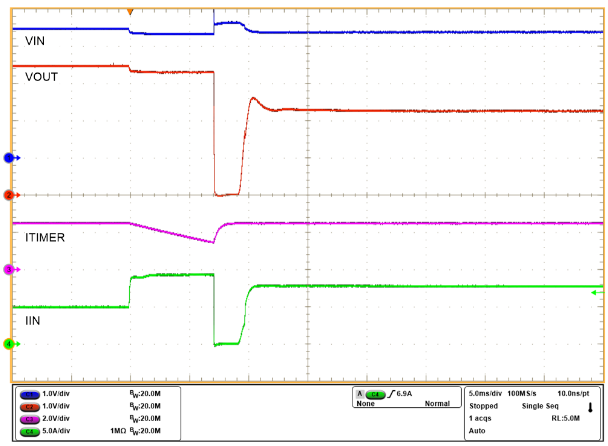


Figure 9-17. Circuit Breaker With Transient Overcurrent Blanking Interval of 6 ms; Device Restarts in Current Limit Mode

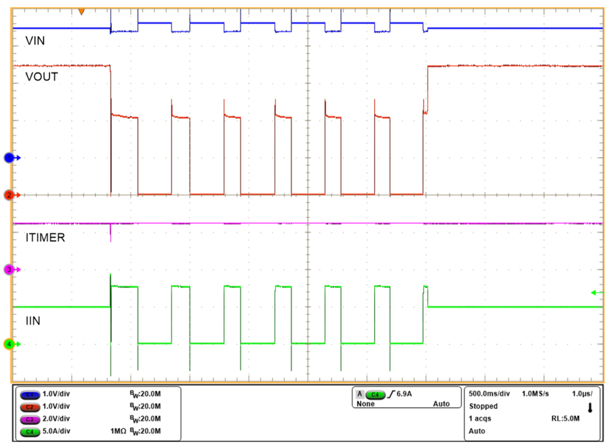


Figure 9-18. Overload Response and Recovery

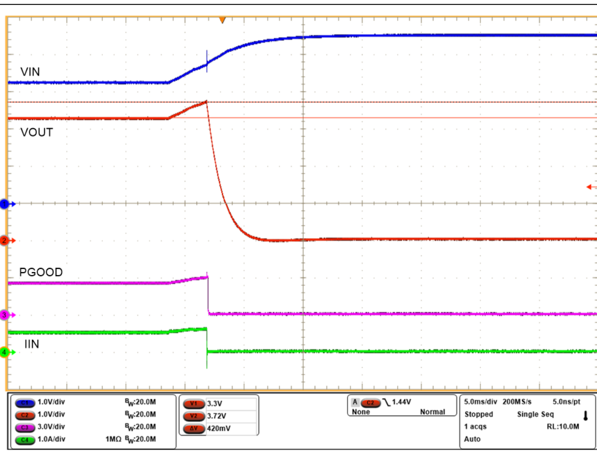


Figure 9-19. Overvoltage Cut-off at 3.7 V with TPS259802O Device

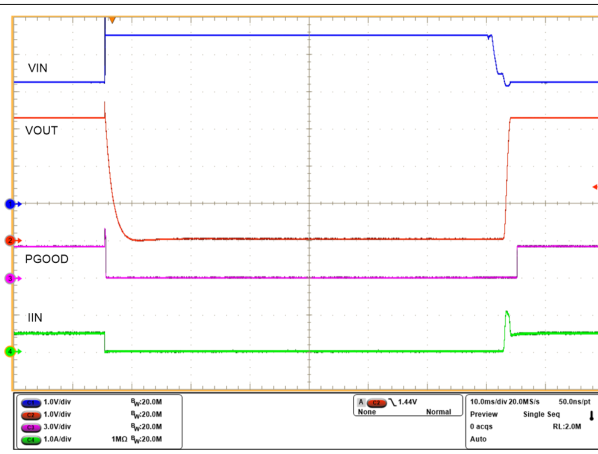


Figure 9-20. Overvoltage Protection Response and Recovery with TPS259802O Device

9.3.2 Input Protection for 12-V Rail Applications: PCIe Cards, Storage Interfaces and DC Fans

TPS25980x eFuse provides inrush current management and also protects the system from most common faults such as undervoltage, overvoltage and overcurrents. The combination of high current support along with low ON-resistance makes TPS25980x eFuse an ideal protection solution for PCIe cards, Storage Interfaces and DC Fan loads. The external component values can be calculated by following the design procedure outlined in *Detailed Design Procedure*. Alternatively, a spreadsheet design tool *TPS25980xx Design Calculator* is available for simplified design efforts.

10 Power Supply Recommendations

The TPS25980x devices are designed for a supply voltage range of 2.7 V ≤ VIN ≤ 24 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low value ceramic capacitor C_{IN} = 0.001 µF to 0.1 µF to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated using Equation 28.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (28)$$

where

- V_{IN} is the nominal supply voltage
- I_{LOAD} is the load current
- L_{IN} equals the effective inductance seen looking into the source
- C_{IN} is the capacitance present at the input

Some of the applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. A typical circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in Figure 10-1.

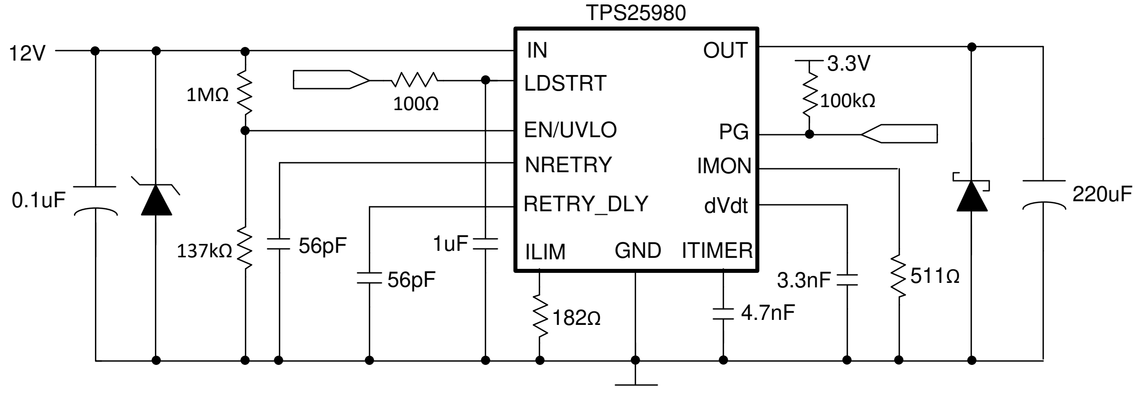


Figure 10-1. Typical Circuit Implementation With Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Board layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results.

Note

Do not expect to see waveforms exactly like the waveforms in this data sheet because every setup is different.

---

11 Layout

11.1 Layout Guidelines

- The IN Exposed Thermal Pad is used for Heat Dissipation. Connect to as much copper area as possible using an array of thermal vias. The via array also helps to minimize the voltage gradient across the VIN pad and facilitates uniform current distribution through the internal FET, which improves the current sensing and monitoring accuracy.
- For all applications, TI recommends a ceramic decoupling capacitor of 0.01 µF or greater between IN and GND terminals. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current. It is recommended to use a minimum trace width of 50 mil for the OUT power connection.
- The GND terminal is the reference for all internal signals and must be isolated from any bounce due to large switching currents in the system power ground plane. It is recommended to connect the device GND to a signal ground island on the board, which in turn is connected to the system power GND plane at one point.
- Locate the support components for the following signals close to their respective connection pins - ILIM, IMON, ITIMER, RETRY_DLY, NRETRY and dVdT with the shortest possible trace routing to reduce parasitic effects on the respective associated functions. These traces must not have any coupling to switching signals on the board.
- The ILIM pin is highly sensitive to capacitance and TI recommends to pay special attention to the layout to maintain the parasitic capacitance below 30 pF for stable operation.
- Use short traces on the RETRY_DLY and NRETRY pins to ensure the auto-retry timer delay and number of auto-retries is not altered by the additional parasitic capacitance on these pins.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Use proper layout and thermal management techniques to ensure there is no significant steady state thermal gradient between the two thermal pads on the IC. This is necessary for proper functioning of the device overtemperature protection mechanism and successful startup under all conditions.
- Obtaining acceptable performance with alternate layout schemes is possible; the *Layout Example* is intended as a guideline and shown to produce good results from electrical and thermal standpoint.

11.2 Layout Example

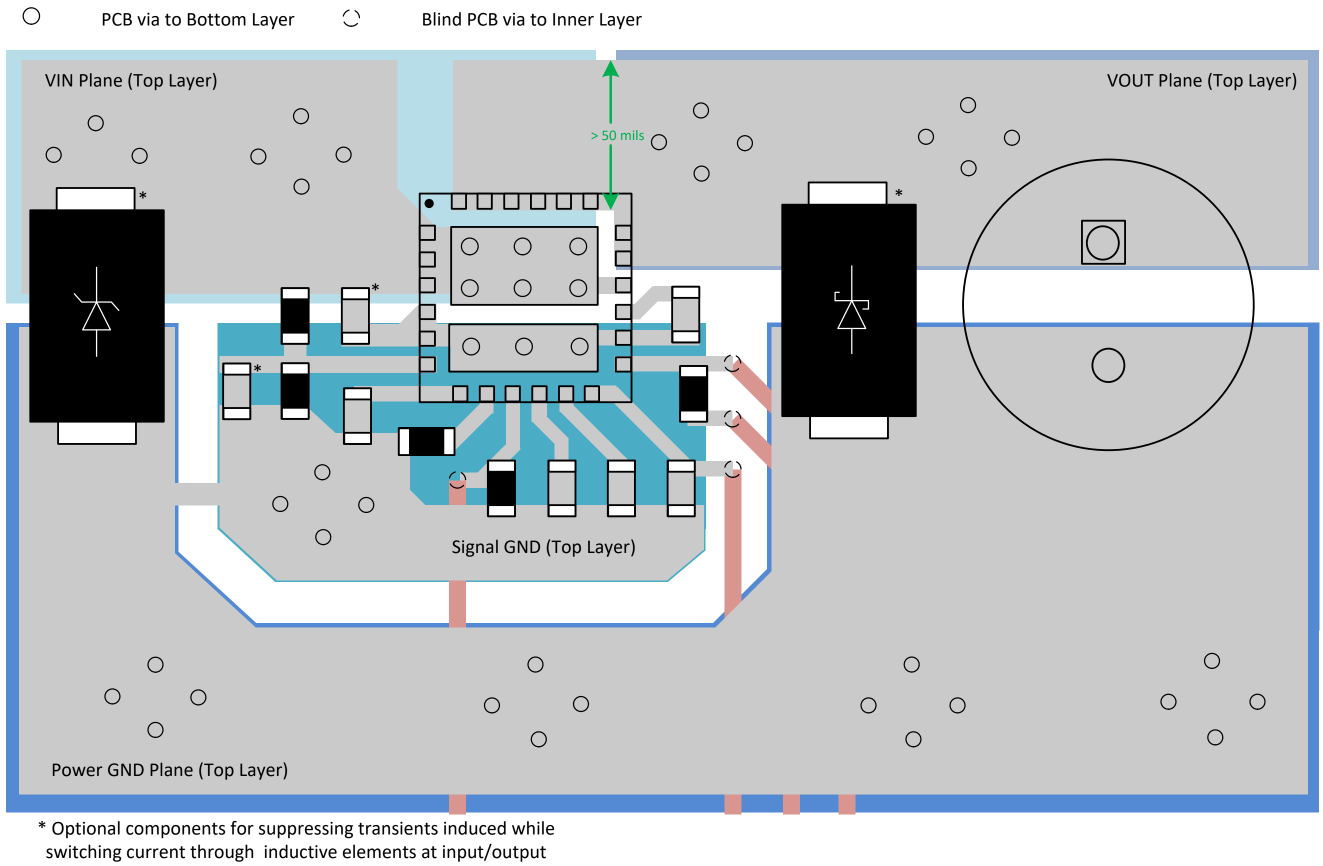


Figure 11-1. TPS25980 Example PCB Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *TPS259804OEVM eFuse Evaluation Board*
- *TPS25980xx Design Calculator*

12.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS259802O	Click here	Click here	Click here	Click here	Click here
TPS259803O	Click here	Click here	Click here	Click here	Click here
TPS259804O	Click here	Click here	Click here	Click here	Click here
TPS259807O	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259802ONRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TP2598 02ON	Samples
TPS259803ONRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TP2598 03ON	Samples
TPS259804ONRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TP2598 04ON	Samples
TPS259807ONRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TP2598 07ON	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

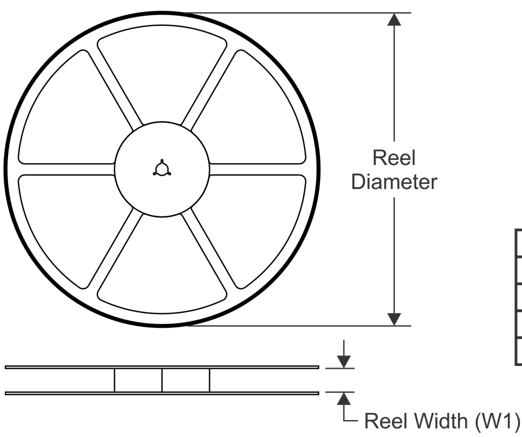
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

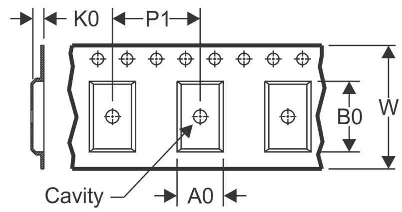
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

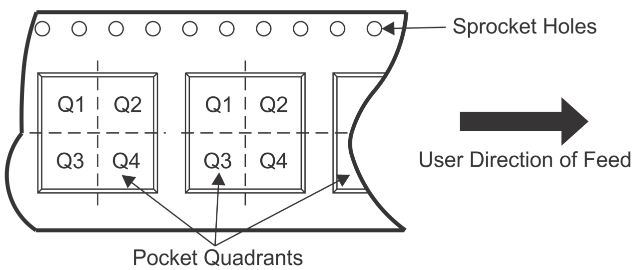


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

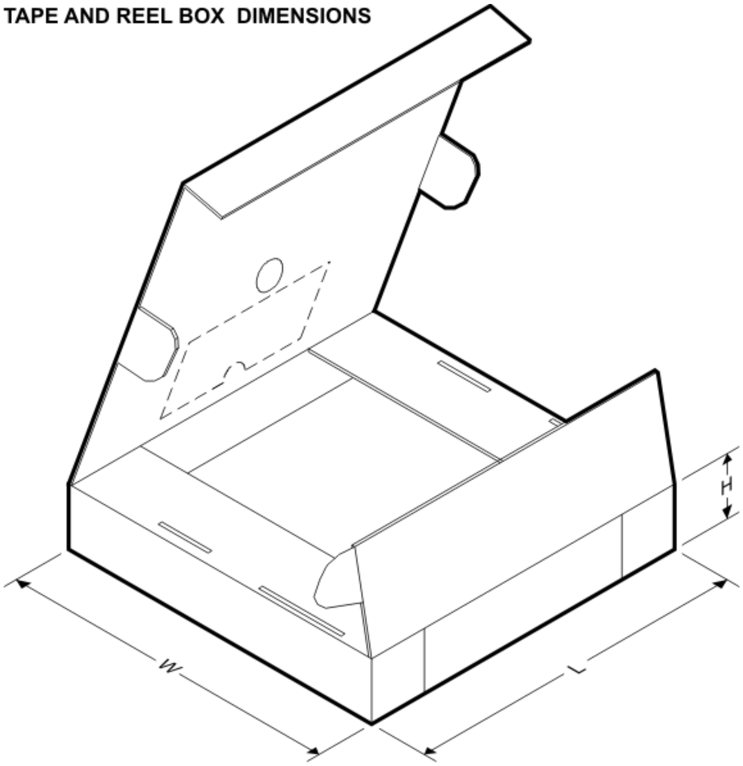
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259802ONRGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS259803ONRGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS259804ONRGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS259807ONRGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

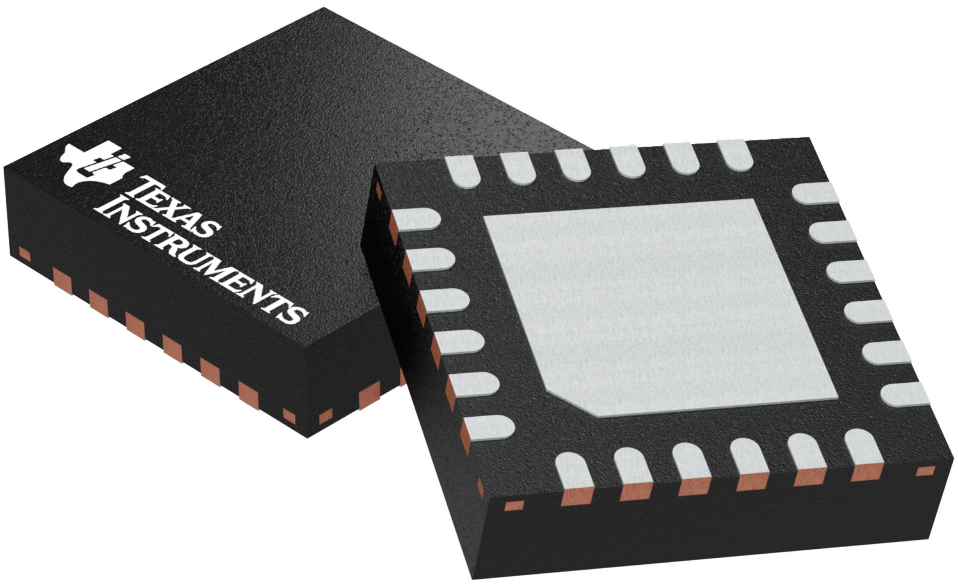


*All dimensions are nominal

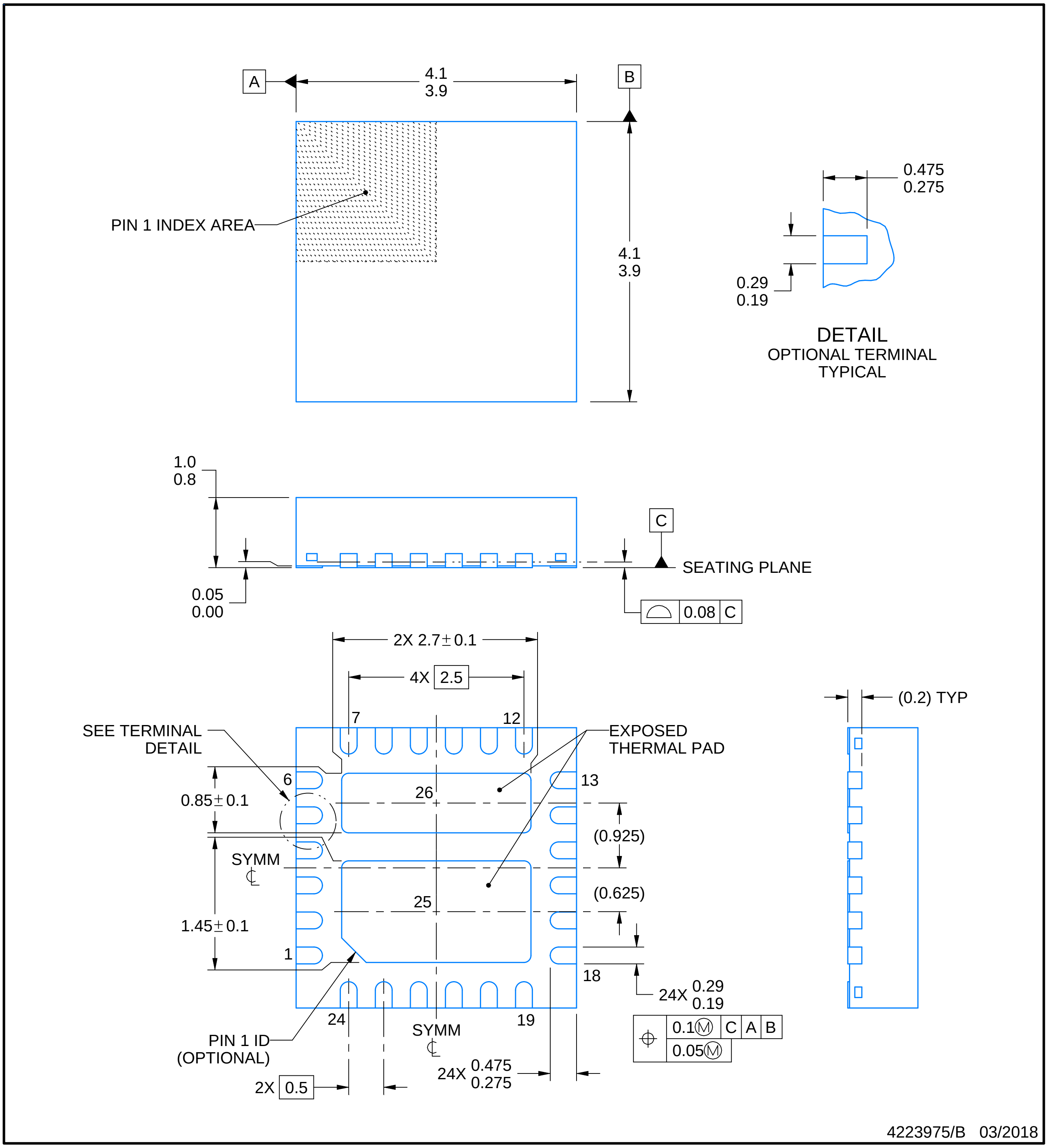
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259802ONRGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS259803ONRGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS259804ONRGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS259807ONRGER	VQFN	RGE	24	3000	338.0	355.0	50.0

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

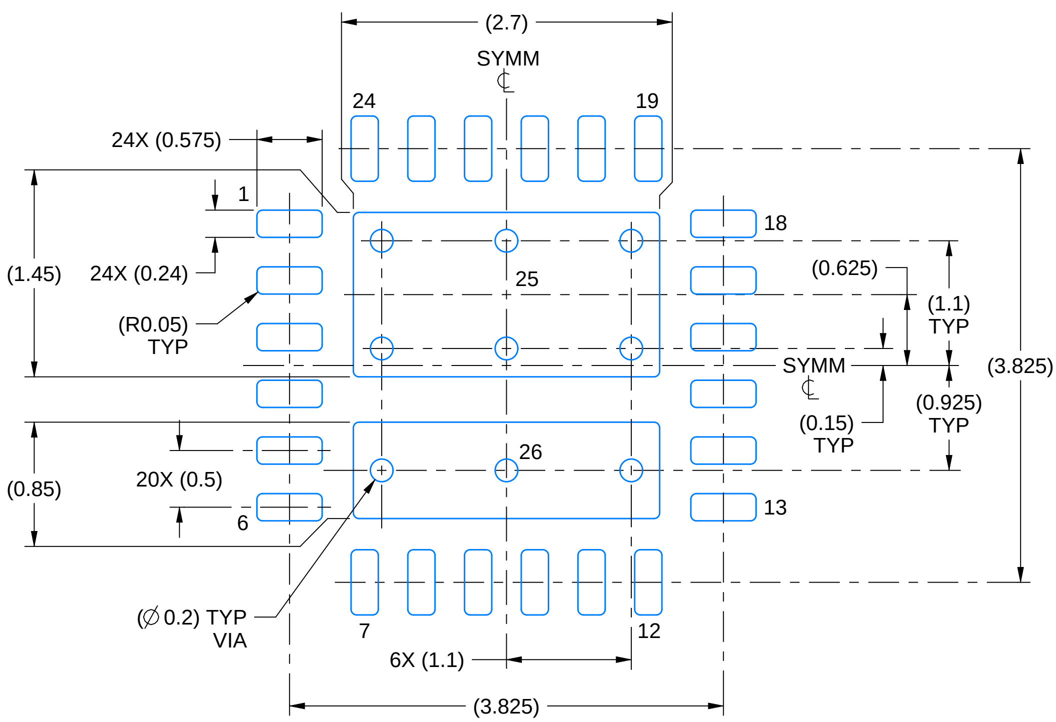


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

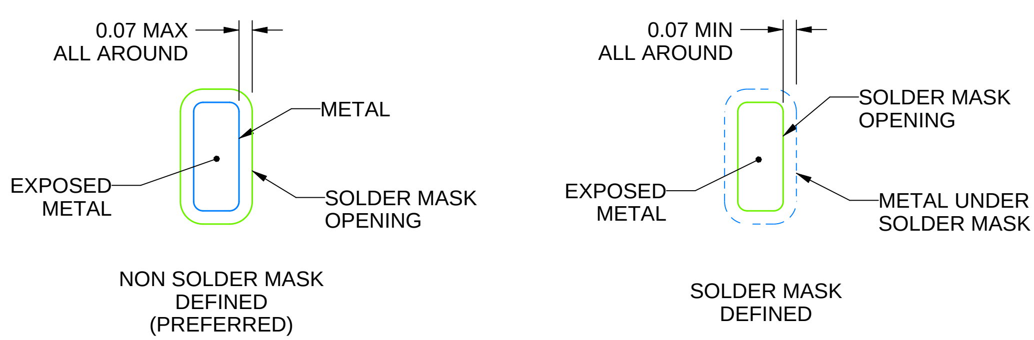


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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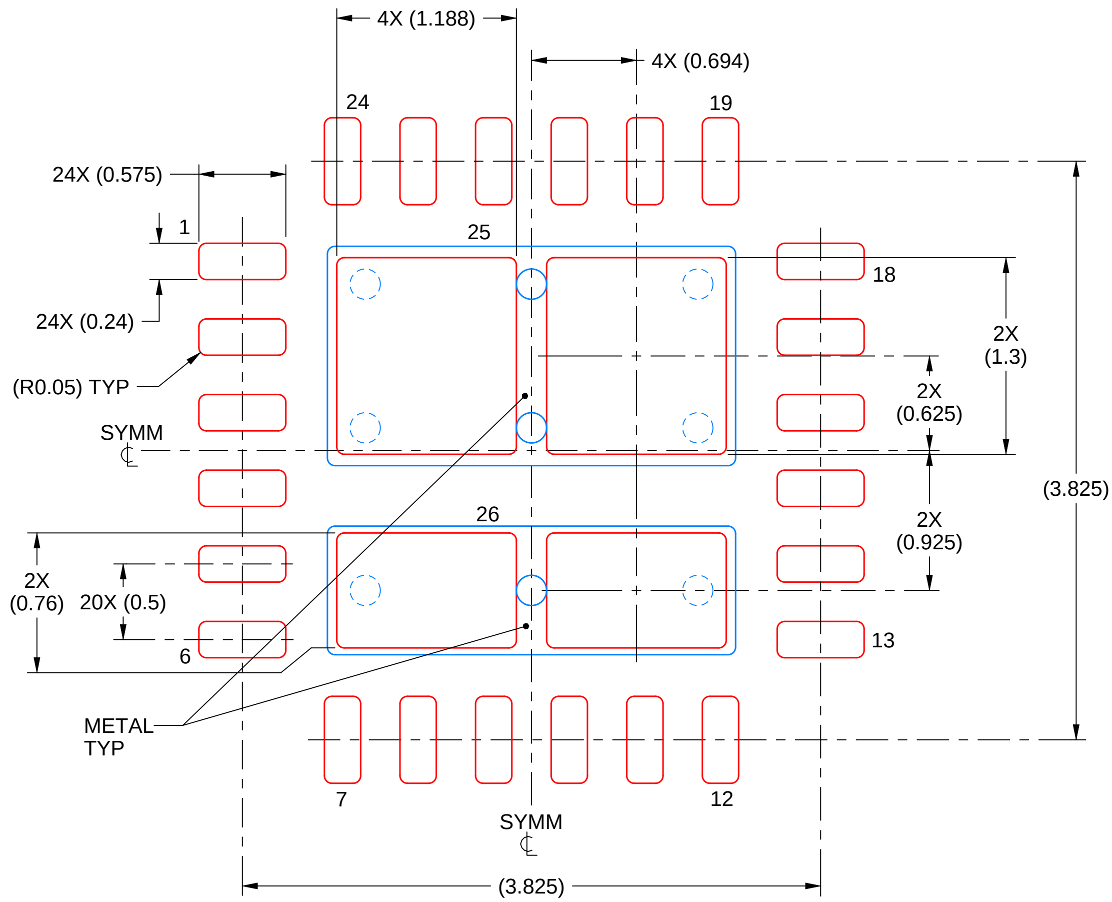
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.