TPS2521xx, 2.7 - 5.7 V, 4 A, 31-mΩ True Reverse Current Blocking eFuse with Input Reverse Polarity Protection

1 Features

- Wide operating input voltage range: 2.7 V to 5.7 V
- 28-V absolute maximum
- Withstands negative voltages up to – 15 V
- Integrated back-to-back FETs with low On-Resistance: R_{ON} = 31 mΩ (typ)
- Ideal diode operation with true reverse current blocking
- Fast overvoltage clamp (OVC) with pin-selectable threshold (3.8 V, 5.7 V) with 5-µs (typ) response time
- Overcurrent protection with load current monitor output (ILM)
  - Active current limit response
  - Adjustable threshold (I_{LIM}) 0.5 A - 4.44 A
    - ±10% accuracy for I_{LIM} > 1 A
  - Adjustable transient blanking timer (ITIMER) to allow peak currents up to 2 x I_{LIM}
  - Output load current monitor accuracy: ±6% (I_{OUT} ≥ 1 A)
- Fast-trip response for short-circuit protection
  - 500-ns (typ) response time
  - Adjustable (2 x I_{LIM}) and fixed thresholds
- Active High Enable input with adjustable undervoltage lockout threshold (UVLO)
- Adjustable output slew rate control (dVdt)
- Overtemperature protection
- Power Good indication (PG) with adjustable threshold (PGTH)
- IEC 62368 CB certification (pending)
- UL 2367 recognition (pending)
- Small footprint: QFN 2 mm × 2 mm, 0.45-mm pitch

2 Applications

- Adapter input protection
- Enterprise storage - RAID/HBA/SAN/eSSD
- USB PD port protection
- Server/PC motherboard/add-on cards
- Monitors/docks

3 Description

The TPS2521x family of eFuses is a highly integrated circuit protection and power management solution in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short-circuits, voltage surges, reverse polarity and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the device well suited for systems which need load side energy hold up storage in case input power supply fails.

Output current limit level can be set with a single external resistor. It is also possible to get an accurate sense of the output load current by measuring the voltage drop across the current limit resistor.

Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Loads are protected from input overvoltage conditions by clamping the output to a safe fixed maximum voltage (pin selectable).

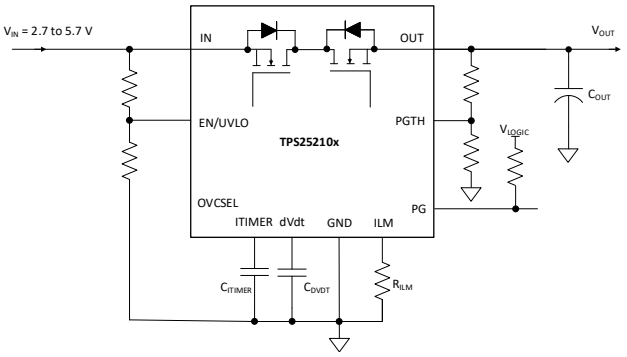
The devices are available in a 2-mm × 2-mm, 10-pin HotRod QFN package for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS2521xxRPW	QFN (10)	2 mm × 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2021	*	Initial Release

5 Device Comparison Table

Part Number	Overvoltage Response	Overcurrent Response	Response to Fault
TPS25210A	Pin Selectable OVC (3.8 V/5.7 V)	Active Current Limit	Auto-Retry
TPS25210L			Latch-Off

6 Pin Configuration and Functions

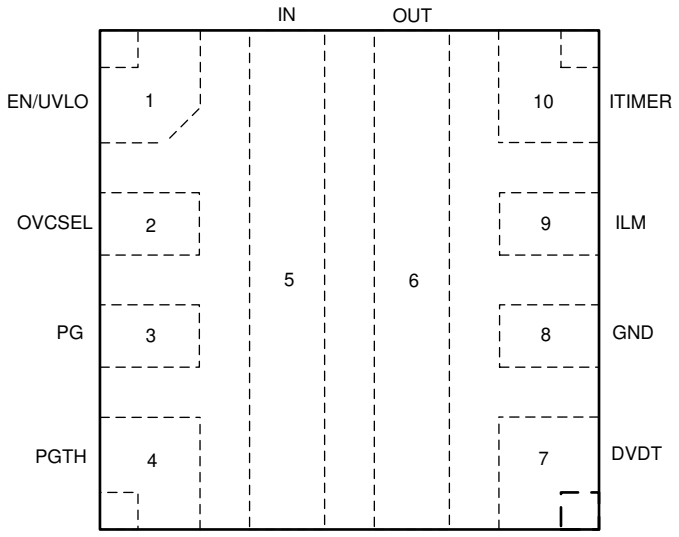


Figure 6-1. TPS2521x RPW Package 10-Pin QFN Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active High Enable for the device. A Resistor Divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. **Do not leave floating.** Refer to Section 8.3.2 for details.
OVCSEL	2	Analog Input	Overvoltage Clamp Threshold Select Pin. Refer to Section 8.3.3 for details.
PG	3	Digital Output	Power Good indication. This is an Open Drain signal which is asserted High when the internal powerpath is fully turned ON and PGTH input exceeds a certain threshold. Refer to Section 8.3.9 for more details.
PGTH	4	Analog Input	Power Good Threshold. Refer to Section 8.3.9 for more details.
IN	5	Power	Power Input.
OUT	6	Power	Power Output.
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to Section 8.3.4.1 for details.
GND	8	Ground	This is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog Output	This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. **Do not leave floating.** Refer to Section 8.3.4.2 for more details.
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to Section 8.3.4.2 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range, -40 °C ≤ T_J ≤ 125 °C	IN	max(-15, V_{OUT} - 21)	28	V
	Maximum Input Voltage Range, -10 °C ≤ T_J ≤ 125 °C		max(-15, V_{OUT} - 22)	28	V
V_{OUT}	Maximum Output Voltage Range, -40 °C ≤ T_J ≤ 125 °C	OUT	–0.3	min (28, V_{IN} + 21)	
	Maximum Output Voltage Range, -10 °C ≤ T_J ≤ 125 °C		–0.3	min (28, V_{IN} + 22)	
$V_{OUT,PLS}$	Minimum Output Voltage Pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range (2)	EN/UVLO	–0.3	6.5	V
V_{OVCSEL}	Maximum OVCSEL Pin Voltage Range	OVCSEL	Internally Limited		V
V_{dVdT}	Maximum dVdT Pin Voltage Range	dVdt	Internally Limited		V
V_{ITIMER}	Maximum ITIMER Pin Voltage Range	ITIMER	Internally Limited		V
V_{PGTH}	Maximum PGTH Pin Voltage Range (2)	PGTH	–0.3	6.5	V
V_{PG}	Maximum PG Pin Voltage Range	PG	–0.3	6.5	V
V_{ILM}	Maximum ILM Pin Voltage Range	ILM	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Lead Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) If this pin has a pull-up up to V_{IN}, it is recommended to use a resistance of 350 kΩ or higher to limit the current under conditions where IN can be exposed to reverse polarity.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	5.7 (1)	V
V_{OUT}	Output Voltage Range	OUT		min (23, V_{IN} + 20)	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5 (2)	V
V_{dVdT}	dVdT Capacitor Voltage Rating	dVdt	V_{IN} + 5 V		V
V_{PGTH}	PGTH Pin Voltage Range	PGTH		5 (3)	V
V_{PG}	PG Pin Voltage Range	PG		5 (3)	V
V_{ITIMER}	ITIMER Pin Capacitor Voltage Rating	ITIMER	4		V
R_{ILM}	ILM Pin Resistance	ILM	750	6650	Ω
I_{MAX}	Continuous Switch Current, T_J ≤ 125 °C	IN to OUT		4	A
T_J	Junction temperature		–40	125	°C

(1) The input operating voltage should be limited to the selected Output Voltage Clamp threshold as listed in the Electrical Characteristics section

(2) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V or systems which can be exposed to reverse polarity on input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ.

(3) For systems which can be exposed to reverse polarity on input supply, if this pin is referred to input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ to limit the current through the pin.

7.4 Thermal Information

THERMAL METRIC (1)		TPS2521xx	UNIT
		RPW (QFN)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.7 (2)	°C/W
		74.5 (3)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20 (2)	°C/W
		27.6 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device

(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 5 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, OVCSEL = Open, R_{ILM} = 750 Ω , dVdT = Open, ITIMER = Open, PGTH = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$V_{UVP(R)}$	IN Supply UVP Rising Threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN Supply UVP Falling Threshold	2.35	2.42	2.55	V
$I_{Q(ON)}$	IN Supply Quiescent Current		411	593	µA
$I_{Q(ON)}$	IN Supply Current during OVC		426	620	µA
$I_{Q(ON)}$	IN Supply Quiescent Current during RCB, V_{OUT} = V_{IN} + 1 V		186		µA
$I_{Q(OFF)}$	IN Supply OFF State Current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		67	130	µA
I_{SD}	IN Supply Shutdown Current (V_{EN} < $V_{SD(F)}$)		1.62	28.7	µA
$I_{INLKG(IRPP)}$	IN Supply Leakage Current (V_{IN} = -14 V, V_{OUT} = 0 V)		-3.7		µA
ON RESISTANCE (IN - OUT)					
R_{ON}	V_{IN} = 5 V, I_{OUT} = 3 A, T_J = 25 ℃		31		mΩ
	2.7 ≤ V_{IN} ≤ 5.7 V, –40 ℃ ≤ T_J ≤ 125 ℃			50.2	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO Rising Threshold	1.183	1.2	1.223	V
$V_{UVLO(F)}$	EN/UVLO Falling Threshold	1.076	1.1	1.116	V
$V_{SD(F)}$	EN/UVLO Falling Threshold for lowest shutdown current	0.45	0.73		V
I_{ENLKG}	EN/UVLO Leakage Current	-0.1		0.1	µA
OUTPUT VOLTAGE CLAMP (OUT)					
V_{OVC}	Overvoltage Clamp Threshold, OVCSEL = Shorted to GND	3.65	3.88	4.1	V
	Overvoltage Clamp Threshold, OVCSEL = Open	5.25	5.74	6.2	V
V_{CLAMP}	Output Voltage During Clamping, OVCSEL = Shorted to GND, I_{OUT} = 10 mA	3.2	3.82	4.2	V
	Output Voltage During Clamping, OVCSEL = Open, I_{OUT} = 10 mA	5	5.58	6.1	V
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Current Limit Threshold, R_{ILM} = 6.65 kΩ	0.425	0.5	0.575	A
	Current Limit Threshold, R_{ILM} = 3.32 kΩ	0.85	1.0	1.15	A
	Current Limit Threshold, R_{ILM} = 1.65 kΩ	1.8	2.02	2.2	A
	Current Limit Threshold, R_{ILM} = 750 Ω	3.96	4.44	4.84	A
I_{FLT}	Circuit Breaker Threshold, ILM Pin Open (Single point failure)		0.1		A
	Circuit Breaker Threshold, ILM Pin Short to GND (Single point failure)		1.1	2.1	A
I_{SCGain}	Scalable Fast Trip Threshold (I_{SC}) : I_{LIM} Ratio		201		%
I_{FT}	Fixed Fast-trip Current Threshold		22		A
V_{FB}	V_{OUT} threshold to exit Current Limit Foldback		1.9		V
V_{INT}	ITIMER pin internal pull-up voltage	2.3	2.52	2.72	V
OVERCURRENT FAULT TIMER (ITIMER)					
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.2	1.81	2.5	µA
R_{ITIMER}	ITIMER pin internal pull-up resistance		15		kΩ
ΔV_{ITIMER}	ITIMER discharge voltage	1.28	1.51	1.74	V
OUTPUT LOAD CURRENT MONITOR (ILM)					

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 5 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, OVCSEL = Open, R_{ILM} = 750 Ω , dVdT = Open, ITIMER = Open, PGTH = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
G_{IMON}	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 0.5 A to 1 A, I_{OUT} < I_{LIM}	165	182	200	µA/A
	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 1 A to 4 A, I_{OUT} < I_{LIM}	165	182	200	µA/A
REVERSE CURRENT BLOCKING (IN - OUT)					
V_{FWD}	V_{IN} - V_{OUT} Forward regulation voltage, I_{OUT} = 10 mA	5	17.4		mV
V_{REVTH}	V_{IN} - V_{OUT} threshold for fast BFET turn off (enter reverse current blocking)	-36.5	-29.1	-22.3	mV
V_{FWDTH}	V_{IN} - V_{OUT} threshold for fast BFET turn on (exit reverse current blocking)	83	102.2	125	mV
$I_{OUTLKG(RCB)}$	OUT Leakage Current during ON state with RCB, V_{OUT} = V_{IN} + 1 V		270		µA
$I_{REVLKG(OFF)}$	Reverse Leakage Current during unpowered condition, V_{OUT} = 12 V, V_{IN} = 0 V		4.8		µA
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pull-up (I_{PG} = 26 µA)		0.67	1	V
	PG pin voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pull-up (I_{PG} = 242 µA)		0.78	1	V
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0		V
I_{PGLKG}	PG Pin Leakage Current, PG asserted		0.9	3	µA
POWERGOOD THRESHOLD (PGTH)					
$V_{PGTH(R)}$	PGTH Rising Threshold	1.183	1.2	1.223	V
$V_{PGTH(F)}$	PGTH Falling Threshold	1.076	1.09	1.116	V
$I_{PGTHLKG}$	PGTH Leakage Current	-0.1		0.3	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown Rising Threshold, T_J↑		154		°C
TSD_{HYS}	Thermal Shutdown Hysteresis, T_J↓		10		°C
DVDT					
I_{dVdt}	dVdt Pin Charging Current	0.78	1.97	3.3	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVC}	Overvoltage clamp response time	V_{IN} > V_{OVC} to V_{OUT}↓		5		µs
t_{LIM}	Current limit response time	I_{OUT} > 1.2 x I_{LIM} & ITIMER expired to I_{OUT} settling to within 5 % of I_{LIM}		400		µs
t_{SC}	Scalable fast-trip response time	I_{OUT} > 3 x I_{LIM} to I_{OUT}↓		500		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT}↓		500		ns
t_{RST}	Auto-Retry Interval after fault (TPS25210A)			110		ms
t_{SWRCB}	Reverse Current Blocking recovery time	(V_{IN} - V_{OUT}) > V_{FWDTH} to V_{OUT} ↑		50		µs
t_{RCB}	Reverse Current Blocking comparator response time	(V_{OUT} - V_{IN}) > 1.3 x V_{REVTH} to BFET OFF		1		µs
t_{PGA}	PG Assertion de-glitch			12		µs
t_{PGD}	PG De-assertion de-glitch			12		µs

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. V_{IN} = 2.7 V, R_L = 100 Ω, C_{OUT} = 1 µF

PARAMETER		C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNIT
SR_{ON}	Output Rising slew rate	12.14	0.87	0.5	V/ms
$t_{D,ON}$	Turn on delay	0.09	0.6	0.97	ms
t_R	Rise time	0.17	2.51	4.33	ms
t_{ON}	Turn on time	0.27	3.11	5.31	ms
$t_{D,OFF}$	Turn off delay	64.44	64.44	64.44	µs

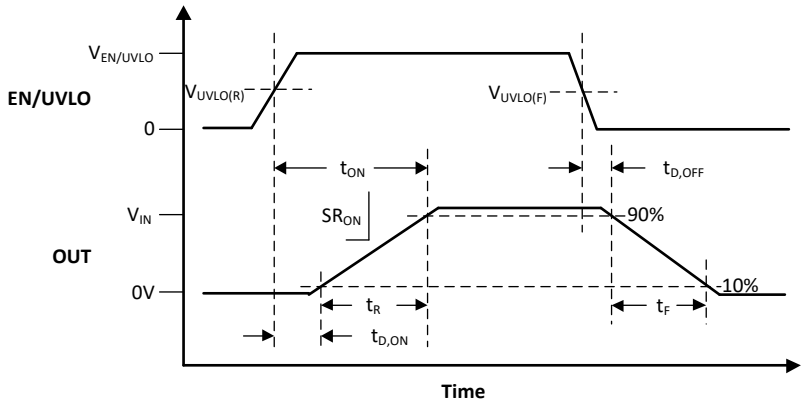


Figure 7-1. TPS2521xx Switching Times

7.8 Typical Characteristics

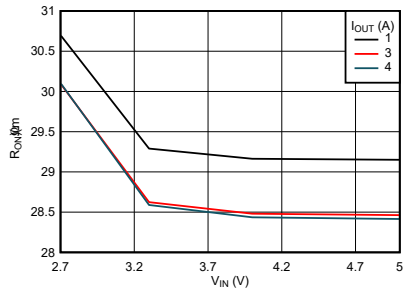


Figure 7-2. ON-Resistance vs Supply Voltage

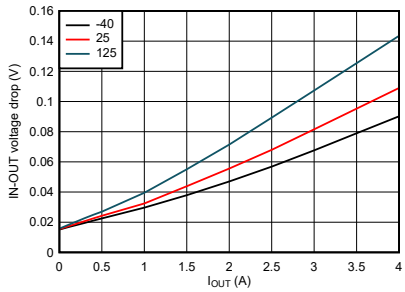


Figure 7-3. Forward Voltage Drop vs Load Current

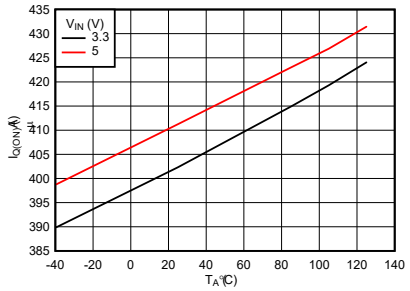


Figure 7-4. IN Quiescent Current vs Temperature

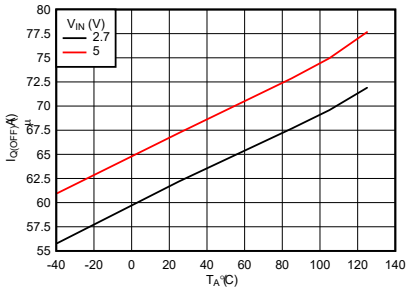


Figure 7-5. IN OFF state (UVLO) Current vs Temperature

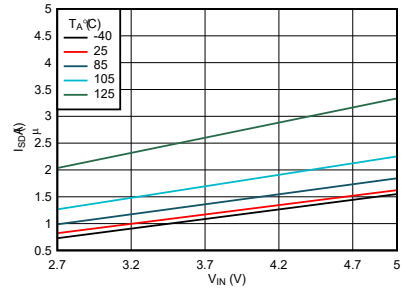


Figure 7-6. IN Shutdown Current vs Supply Voltage

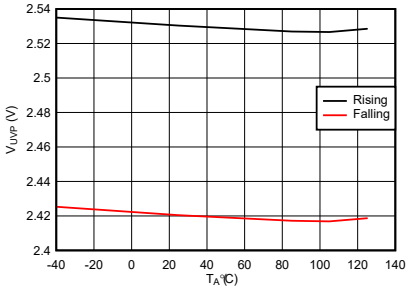


Figure 7-7. IN Undervoltage Threshold vs Temperature

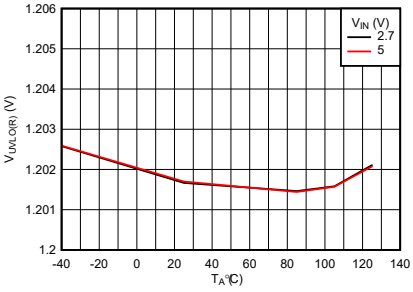


Figure 7-8. EN/UVLO Rising Threshold vs Temperature

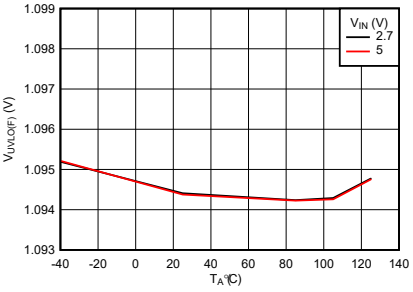


Figure 7-9. EN/UVLO Falling Threshold vs Temperature

7.8 Typical Characteristics (continued)

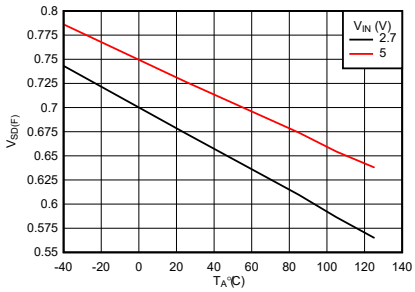


Figure 7-10. EN/UVLO Shutdown Falling Threshold vs Temperature

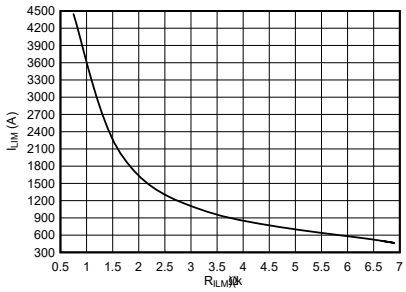


Figure 7-11. Overcurrent Protection Threshold vs ILM resistor

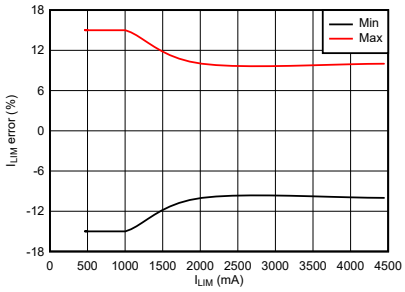


Figure 7-12. Overcurrent Protection Threshold Accuracy (Across Process, Voltage & Temperature)

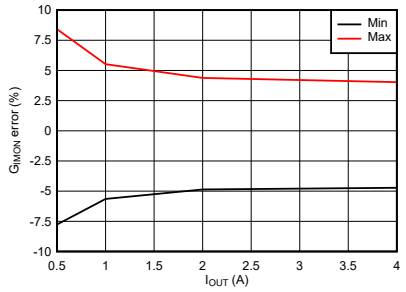


Figure 7-13. Analog Current Monitor Gain Accuracy

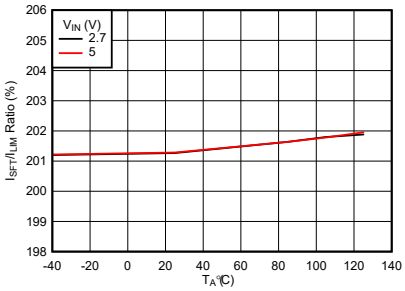


Figure 7-14. Scalable Fast-Trip Threshold:Current Limit Threshold (I_{LIM}) Ratio vs Temperature

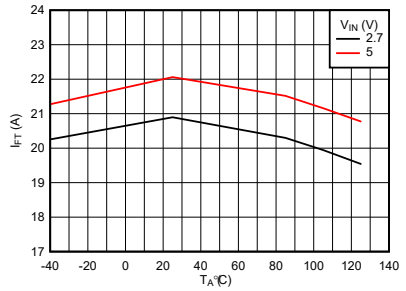


Figure 7-15. Steady State Fixed Fast-Trip Current Threshold vs Temperature

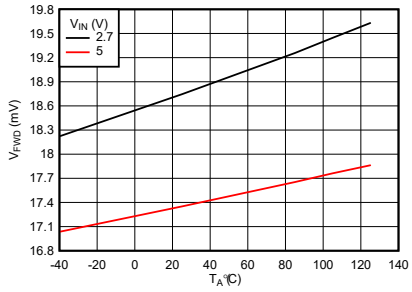


Figure 7-16. RCB - Forward Regulation Voltage vs Temperature

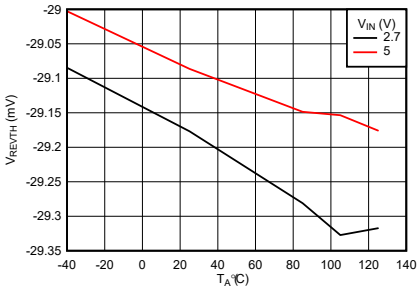


Figure 7-17. RCB - Reverse Comparator Threshold vs Temperature

7.8 Typical Characteristics (continued)

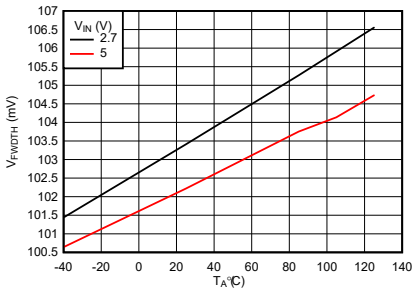


Figure 7-18. RCB - Forward Comparator Threshold vs Temperature

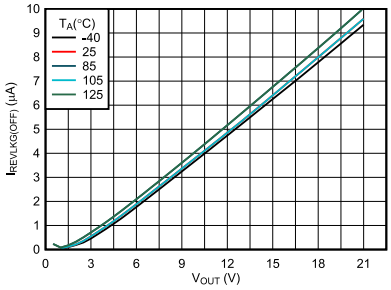


Figure 7-19. Reverse Leakage Current During OFF-State

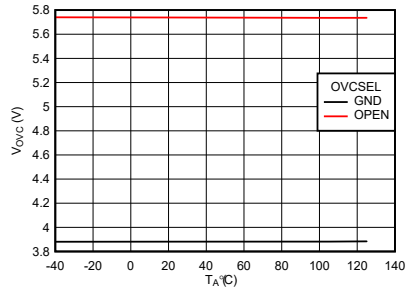


Figure 7-20. OVC Threshold vs Temperature

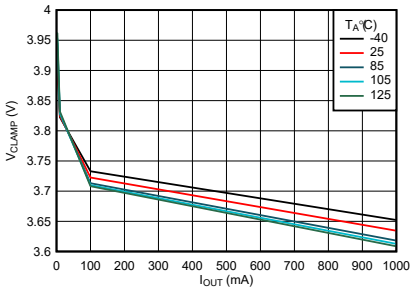


Figure 7-21. OVC Clamping Voltage (OVCSEL = GND) vs Load current

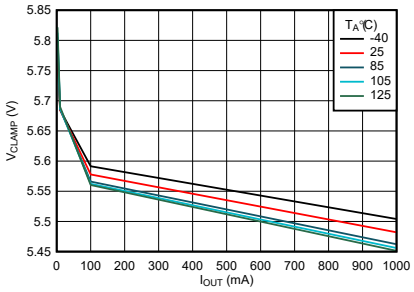


Figure 7-22. OVC Clamping Voltage (OVCSEL = Open) vs Load current

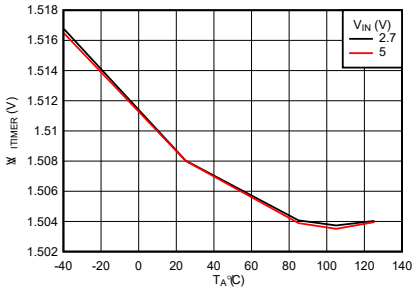


Figure 7-23. ITIMER discharge differential voltage threshold vs Temperature

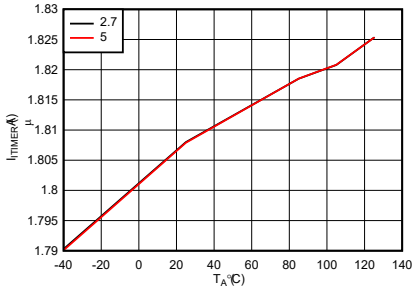


Figure 7-24. ITIMER discharge current vs Temperature

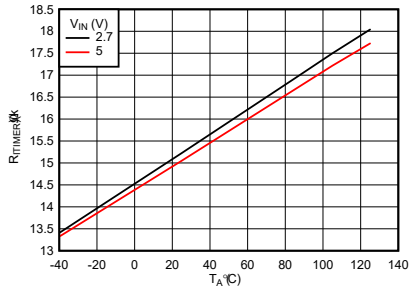


Figure 7-25. ITIMER internal pull-up resistance vs Temperature

7.8 Typical Characteristics (continued)

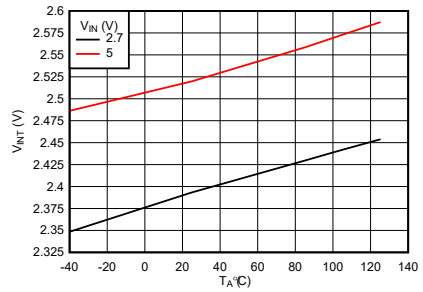


Figure 7-26. ITIMER internal pull-up voltage vs Temperature

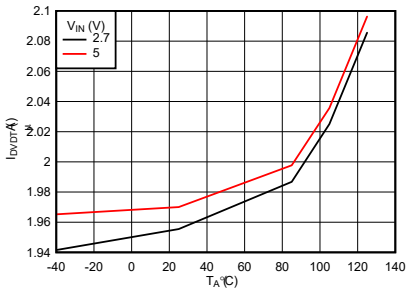


Figure 7-27. DVDT Charging Current vs Temperature

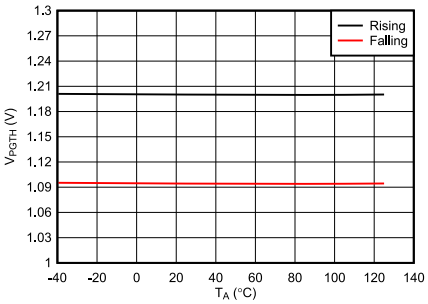


Figure 7-28. PGTH Threshold vs Temperature

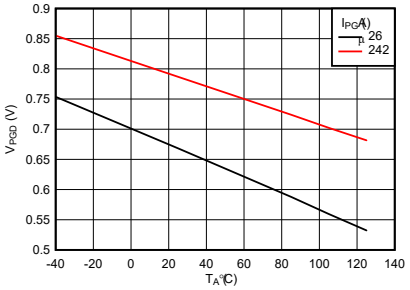


Figure 7-29. PG low voltage without input supply vs Temperature

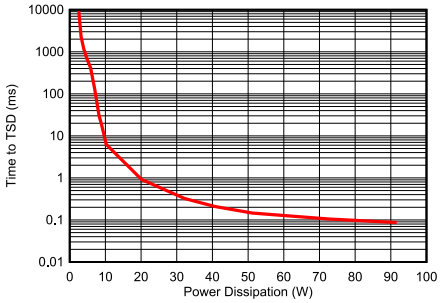


Figure 7-30. Time to Thermal Shut-Down During Inrush State

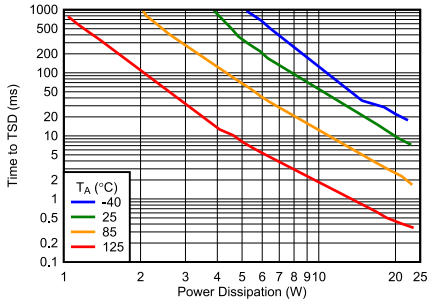
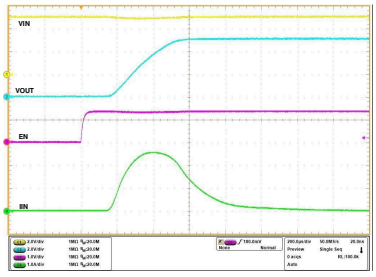
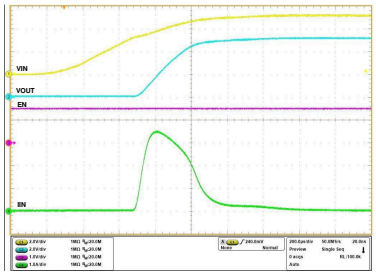


Figure 7-31. Time to thermal Shut-Down During Steady State



V_{IN} = 5 V, C_{OUT} = 220 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 1.4 V

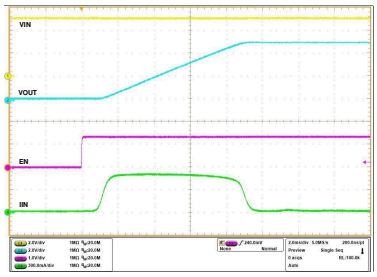
Figure 7-32. Start Up with Enable



$V_{EN/UVLO}$ = 1.5 V, C_{OUT} = 220 µF, C_{dVdt} = Open, V_{IN} ramped up to 5 V

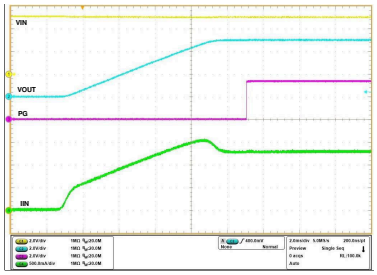
Figure 7-33. Start Up with Supply

7.8 Typical Characteristics (continued)



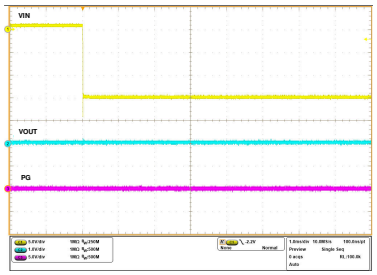
V_{IN} = 5 V, C_{OUT} = 690 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-34. Inrush Current with Capacitive Load



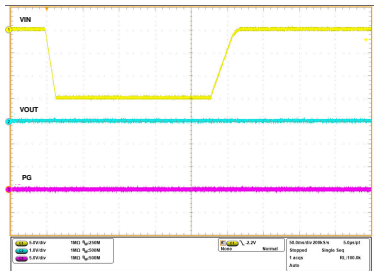
V_{IN} = 5 V, C_{OUT} = 690 µF, R_{OUT} = 4 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-35. Inrush Current with Resistive and Capacitive Load



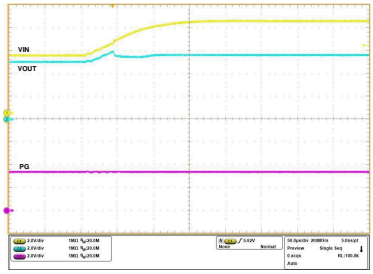
C_{OUT} = 220 µF, PG pulled up to 3 V, - 15 V hot-plugged to IN

Figure 7-36. Input Reverse Polarity Protection - Fast Ramp



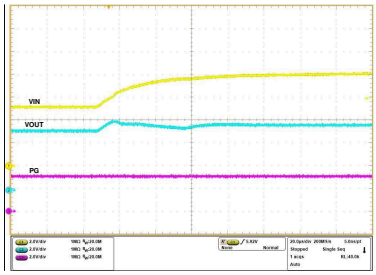
C_{OUT} = 220 µF, PG pulled up to 3 V, V_{IN} ramped down from 0 V to - 15 V and then ramped up to 0 V

Figure 7-37. Input Reverse Polarity Protection - Slow Ramp



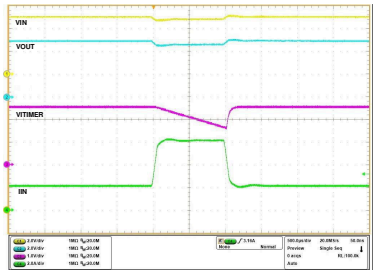
R_{OVCSEL} = GND, C_{OUT} = 220 µF, I_{OUT} = 120 mA, V_{IN} ramped up from 3.3 V to 6 V

Figure 7-38. Overvoltage Clamp Response



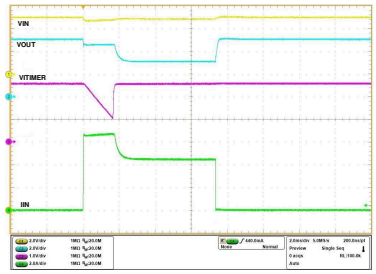
R_{OVCSEL} = Open, C_{OUT} = 220 µF, I_{OUT} = 150 mA, V_{IN} ramped up from 5 V to 8 V

Figure 7-39. Overvoltage Clamp Response



V_{IN} = 5 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 750 Ω, I_{OUT} stepped from 2 A → 6 A → 2 A within 1 ms

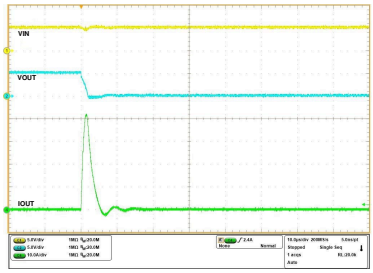
Figure 7-40. Transient Overcurrent Blanking Timer Response



V_{IN} = 5 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 750 Ω, I_{OUT} stepped from 0 A → 6.7 A

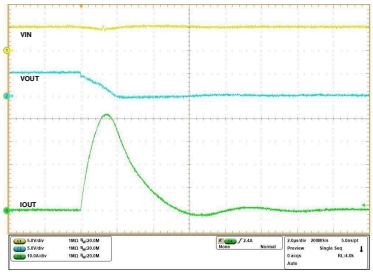
Figure 7-41. Active Current Limit Response

7.8 Typical Characteristics (continued)



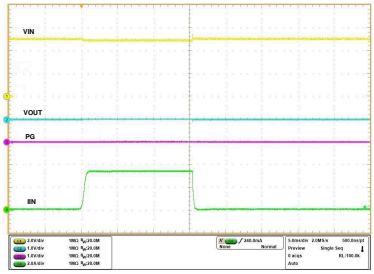
V_{IN} = 5 V, R_{ILM} = 750 Ω, $V_{EN/UVLO}$ = 1.4 V, OUT stepped from Open → Short-circuit to GND

Figure 7-42. Output Short-Circuit During Steady State



V_{IN} = 5 V, R_{ILM} = 750 Ω, $V_{EN/UVLO}$ = 1.4 V, OUT stepped from Open → Short-circuit to GND

Figure 7-43. Output Short-Circuit During Steady State (zoomed in)



V_{IN} = 5 V, C_{OUT} = Open, OUT short-circuit to GND, R_{ILM} = 750 Ω, $V_{EN/UVLO}$ stepped from 0 V to 1.4 V

Figure 7-44. Power Up into Short-Circuit

8 Detailed Description

8.1 Overview

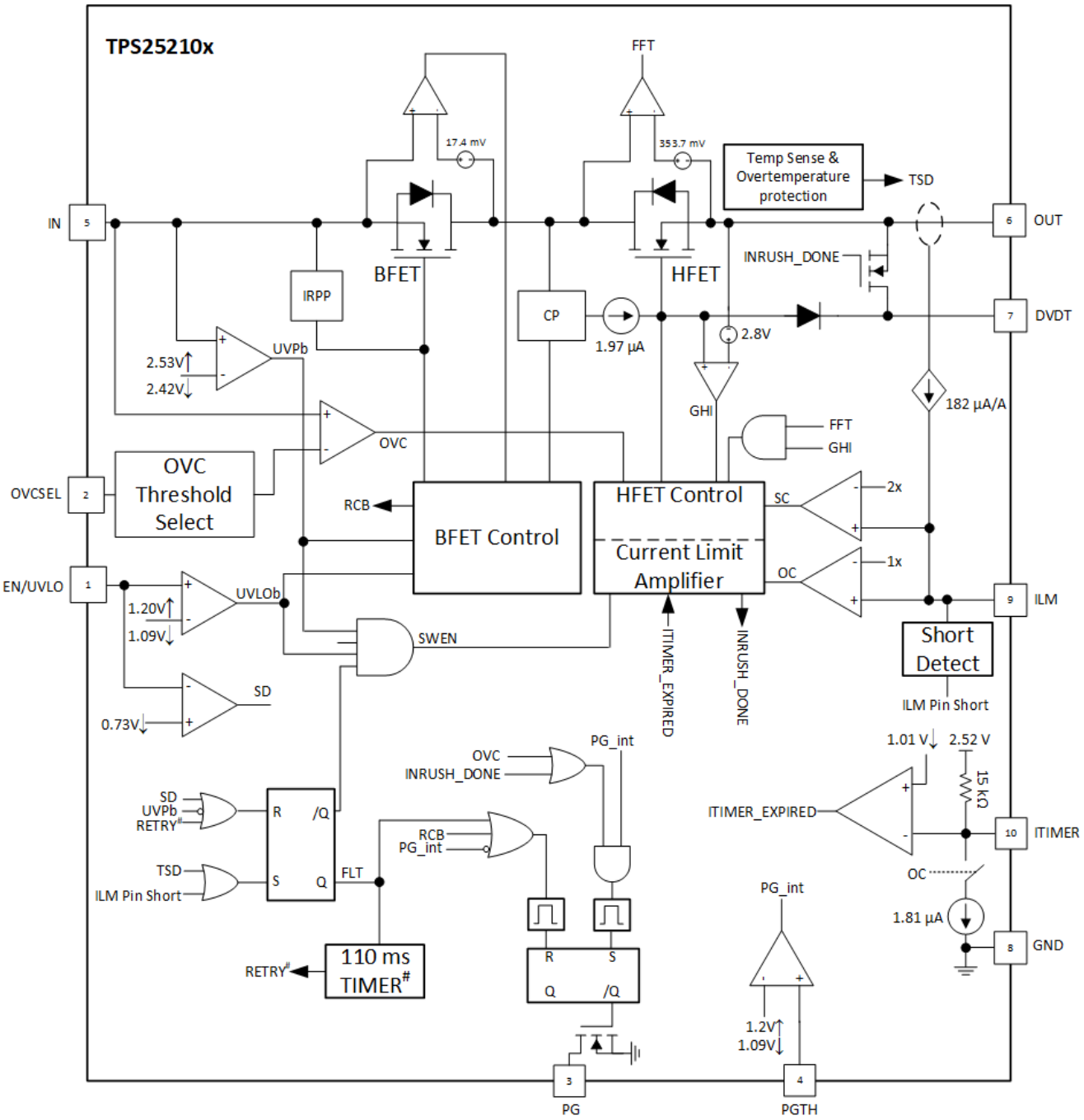
The TPS2521xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the Undervoltage Protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off. In case of reverse voltages appearing at the input, the power path remains OFF thereby protecting the output load.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are either safely clamped to the selected threshold voltage (V_{OVC}). The device also provides fast protection against severe overcurrent during short-circuit events. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (V_{FWD}) in forward conduction mode and turned off completely to block reverse current if output voltage exceeds the input voltage.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

8.2 Functional Block Diagram



Not applicable to Latch-off variant (TPS25210L)

8.3 Feature Description

The TPS2521xx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Input Reverse Polarity Protection

The TPS2521xx device is internally protected against steady state negative voltages applied at the input supply pin. The device blocks the negative voltage from appearing at the output, thereby protecting the load circuits. There's no reverse current flowing from output to the input in this condition. The lowest negative voltage the device can handle at the input is limited to -15 V or VOUT – 21 V, whichever is higher. It's also recommended that all signal pins (e.g. EN/UVLO, PGTH) which are connected to input supply should have a sufficiently large pull-up resistor to limit the current flowing out of these pins during reverse polarity conditions.

8.3.2 Undervoltage Lockout (UVLO & UVP)

The TPS2521x implements Undervoltage Protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage Protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The Figure 8-1 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

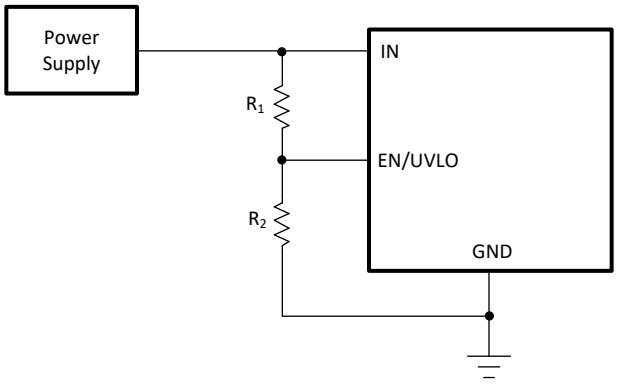


Figure 8-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \text{ x } (R1 + R2)}{R2} \quad (1)$$

8.3.3 Overvoltage Clamp (OVC)

The TPS2521xx implements a voltage clamp on the output to protect the system in the event of input overvoltage. When the device detects the input has exceeded the Overvoltage Clamp Threshold (V_{OVC}), it quickly responds within t_{OVC} and stops the output from rising further and then regulates the HFET linearly to clamp the output voltage below V_{CLAMP} as long as an overvoltage condition is present on the input.

If the part stays in clamping state for an extended period of time, there will be higher power dissipation inside the part which may eventually lead to thermal shut-down (TSD). Once the part shuts down due to TSD fault, it would either stay latched off (TPS2521xL variant) or restart automatically after a fixed delay (TPS2521xA variant). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

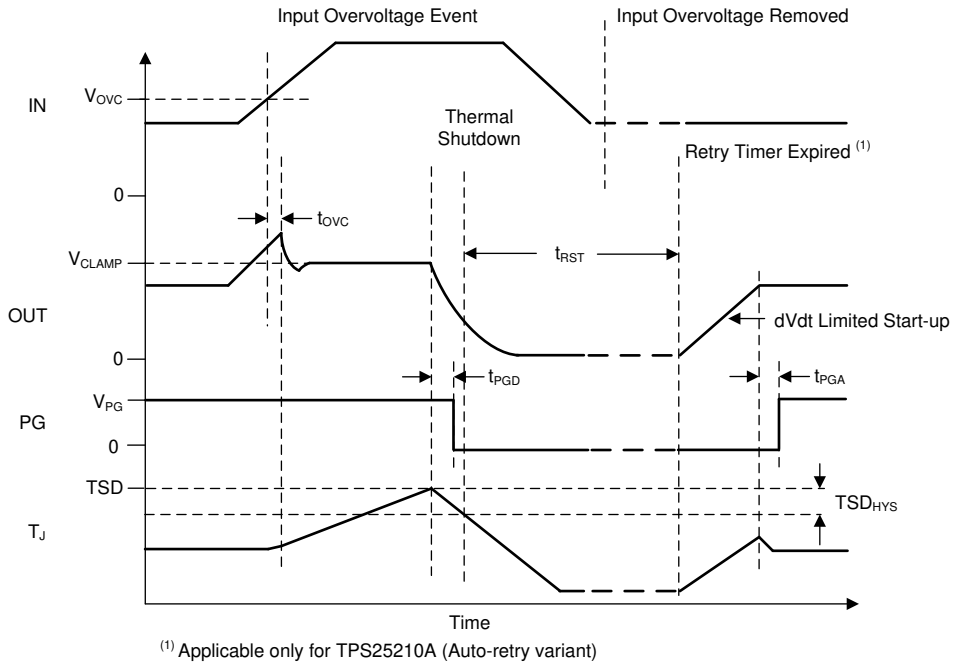


Figure 8-2. TPS2521xA Overvoltage Response (Auto-Retry)

There are 2 available overvoltage clamp threshold options which can be configured using the OVCSEL pin.

Table 8-1. TPS2521xx Overvoltage Clamp Threshold Selection

OVCSEL Pin Connection	Overvoltage Clamp Threshold
Shorted to GND	3.8 V
Open	5.7 V

8.3.4 Inrush Current, Overcurrent, and Short Circuit Protection

TPS2521xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state

8.3.4.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\,(V/ms) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \quad (2)$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using Equation 3.

$$C_{dVdt}\,(pF) = \frac{2000}{SR\,(V/ms)} \quad (3)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

For C_{dVdt} > 10 nF, it's recommended to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

8.3.4.2 Active Current Limiting

The TPS2521xx responds to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 x I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 1.8-µA pull-down current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This allows short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and once it discharges by ΔV_{ITIMER}, the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. Equation 4 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} \tag{4}$$

Note

1. Leaving the ILM pin Open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
3. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There's a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using Equation 5 below.

$$t_{ITIMER}\,(ms) = \frac{\Delta V_{ITIMER}\,(V)\ x\ C_{ITIMER}\,(nF)}{I_{ITIMER}\,(\mu A)} \tag{5}$$

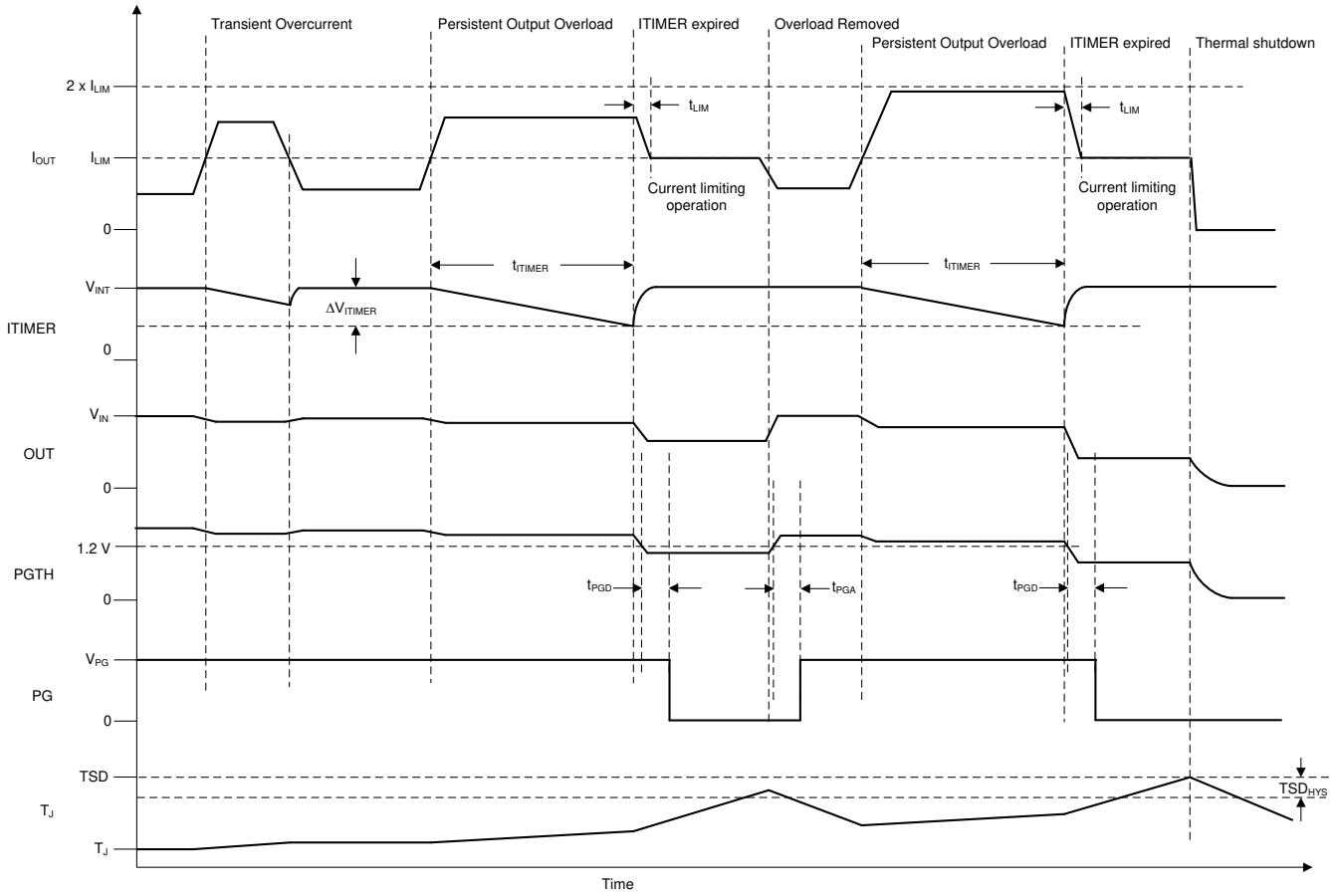


Figure 8-3. TPS2521xx Active Current Limit Response

Note

1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
3. Active current limiting based on R_{ILM} is active during startup. In case the startup current exceeds I_{LIM}, the device regulates the current to the set limit. However, during startup the current limit is engaged without waiting for the ITIMER delay.
4. During overvoltage clamp condition, if an overcurrent event occurs, the current limit is engaged without waiting for the ITIMER delay.
5. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it will take lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage will drop resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. Once the part shuts down due to TSD fault, it would either stay latched off (TPS252x1L variant) or restart automatically after a fixed delay (TPS2521xA variant). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

8.3.4.3 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level.

The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. Once the current exceeds I_{SC} or I_{FT}, the HFET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the HFET back ON after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device will stay in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See *Overtemperature Protection (OTP)* section for details on the device response to overtemperature.

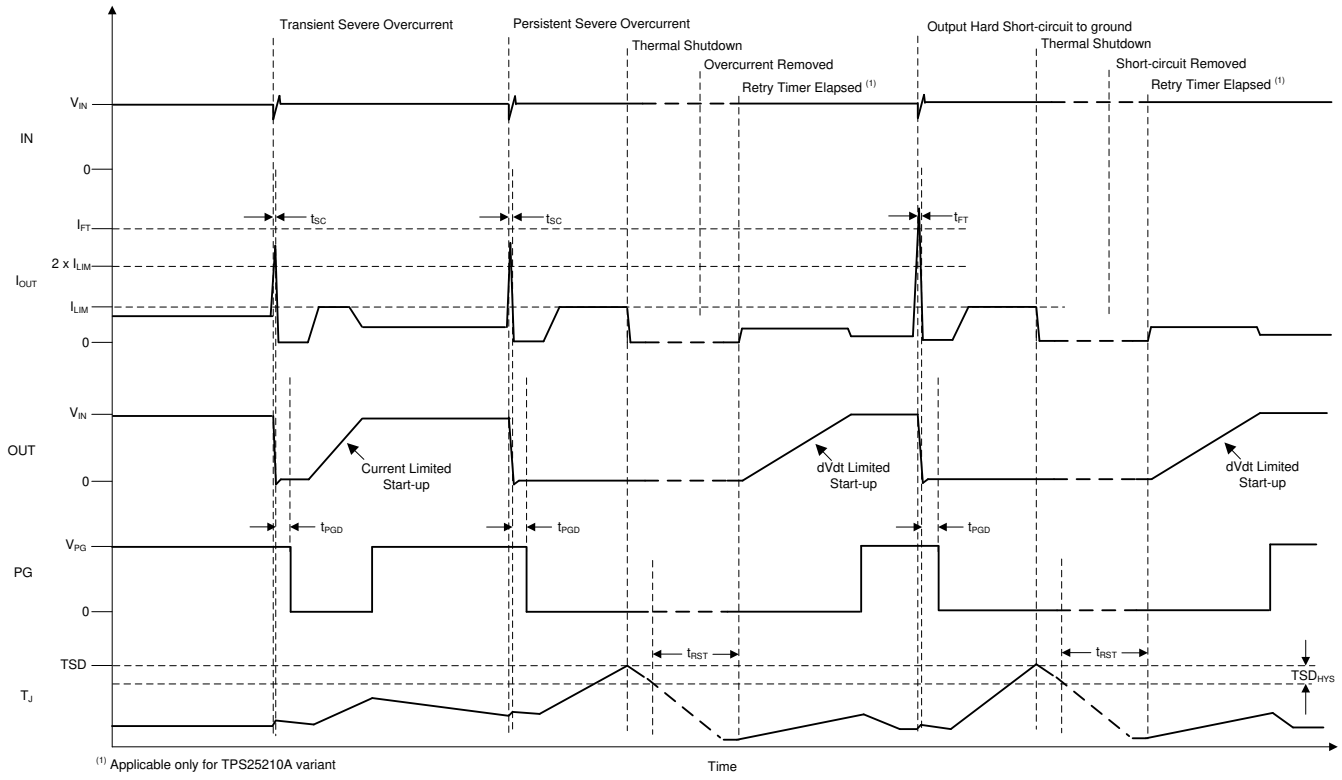


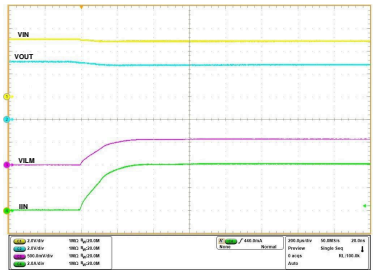
Figure 8-4. TPS2521xx Short-Circuit Response

8.3.5 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{OUT}\,(A) = \frac{V_{ILM}\,(\mu V)}{R_{ILM}\,(\Omega)\ x\ G_{IMON}\,(\mu A/A)} \tag{6}$$

The waveform below shows the ILM signal response to a load step at the output.



V_{IN} = 5 V, C_{OUT} = 220 µF, R_{ILM} = 750 Ω, I_{OUT} stepped up from 0 A to 4 A

Figure 8-5. Analog Load Current Monitor Response

Note

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

8.3.6 Reverse Current Protection

The device functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at V_{FWD}. This closed loop regulation scheme (linear ORing control) enables graceful turn off of the MOSFET during a reverse current event and ensures there's no DC reverse current flow.

The device also uses a conventional comparator (V_{REVTH}) based reverse blocking mechanism to provide fast response (t_{RCB}) to transient reverse currents.Once the device enters reverse current blocking condition, it waits for the (V_{IN} - V_{OUT}) forward drop to exceed the V_{FWDTH} before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysterisis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (t_{SWRCB}). This ensures minimum supply droop which is helpful in applications such as supply MUXing/ORing and USB Fast Role Swap (FRS).

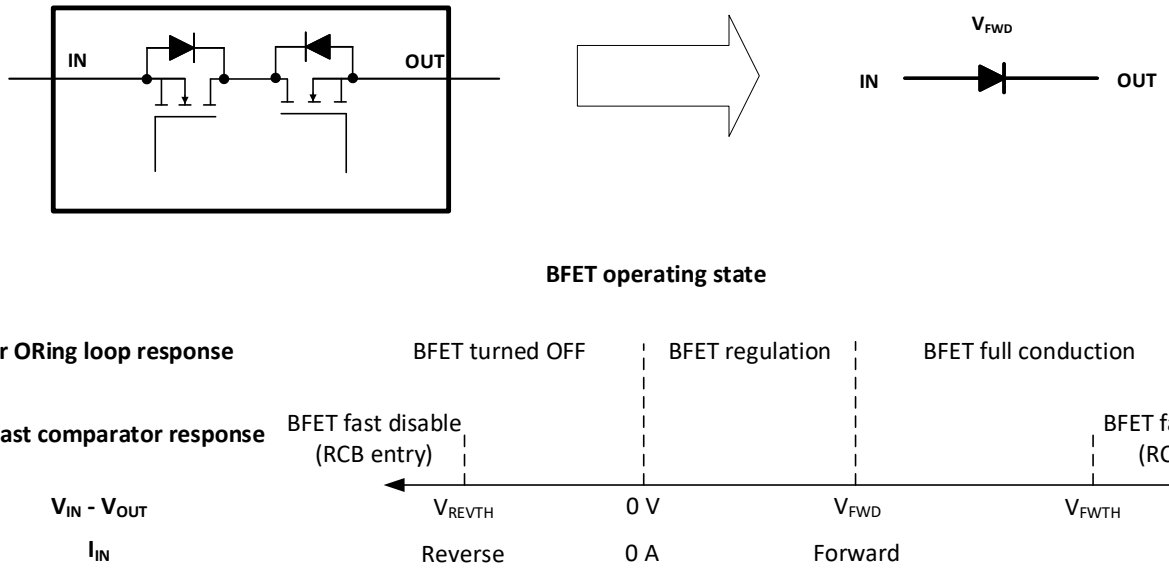


Figure 8-6. Reverse Current Blocking Response

The waveforms below illustrate the reverse current blocking performance in various scenarios.

During fast voltage step at output (e.g. hot-plug), the fast comparator based reverse blocking mechanism ensures minimum jump/glitch on the input rail.

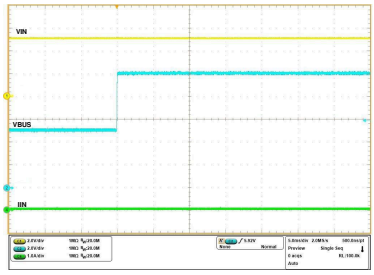


Figure 8-7. Reverse Current Blocking Performance During Fast Voltage Step at Output

During slow voltage ramp at output, the linear ORing based reverse blocking mechanism ensures there's no DC current flow from OUT to IN, thereby avoiding input rail from getting slowly charged up to output voltage.

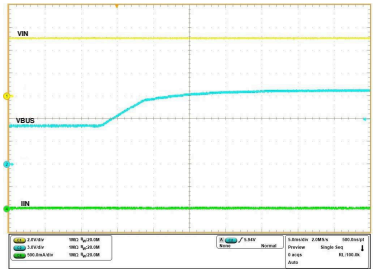


Figure 8-8. Reverse Current Blocking Performance During Slow Voltage Ramp at Output

When the input supply droops or gets disconnected while the output storage element (capacitor bank or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum hold-up time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

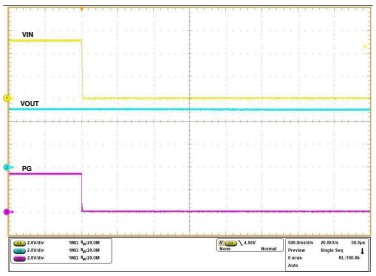


Figure 8-9. Reverse Current Blocking Performance During Input Supply Failure

8.3.7 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device will not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD - TSD_{HYS}).

When the TPS2521xL (latch-off variant) detects thermal overload, it will be shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS2521xA (auto-retry variant) detects thermal overload, it will remain off until it has cooled down by TSD_{HYS}. Thereafter, it will remain off for an additional delay of t_{RST} after which it will automatically retry to turn on if it is still enabled.

Table 8-2. Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS2521xL (Latch-Off)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
TPS2521xA (Auto-Retry)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$ OR t_{RST} timer expired

8.3.8 Fault Response

The following table summarizes the device response to various fault conditions.

Table 8-3. Fault Summary

Event	Protection Response	Fault Latched Internally
Overtemperature	Shutdown	Y
Undervoltage (UVP or UVLO)	Shutdown	N
Input Reverse Polarity	Shutdown	N
Input Overvoltage	Voltage Clamp	N
Transient Overcurrent ($I_{LIM} < I_{OUT} < 2 \times I_{LIM}$)	None	N
Persistent Overcurrent	Current Limit	N
Output Short-Circuit to GND	Fast trip followed by Current Limit	N
ILM Pin Open (During Steady State)	Shutdown	N
ILM Pin Shorted to GND	Shutdown	Y
Reverse Current ($(V_{OUT} - V_{IN}) > V_{REVTH}$)	Reverse Current Blocking	N

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This also resets the t_{RST} timer for the TPS2521xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This is true for both TPS2521xL (latch-off) & TPS2521xA (auto-retry) variants.

For TPS2521xA (auto-retry) variant, on expiry of the t_{RST}timer after a fault, the device restarts automatically.

8.3.9 Power Good Indication (PG)

The TPS2521xx provides an active high digital output (PG) which serves as a power good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and needs to be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.

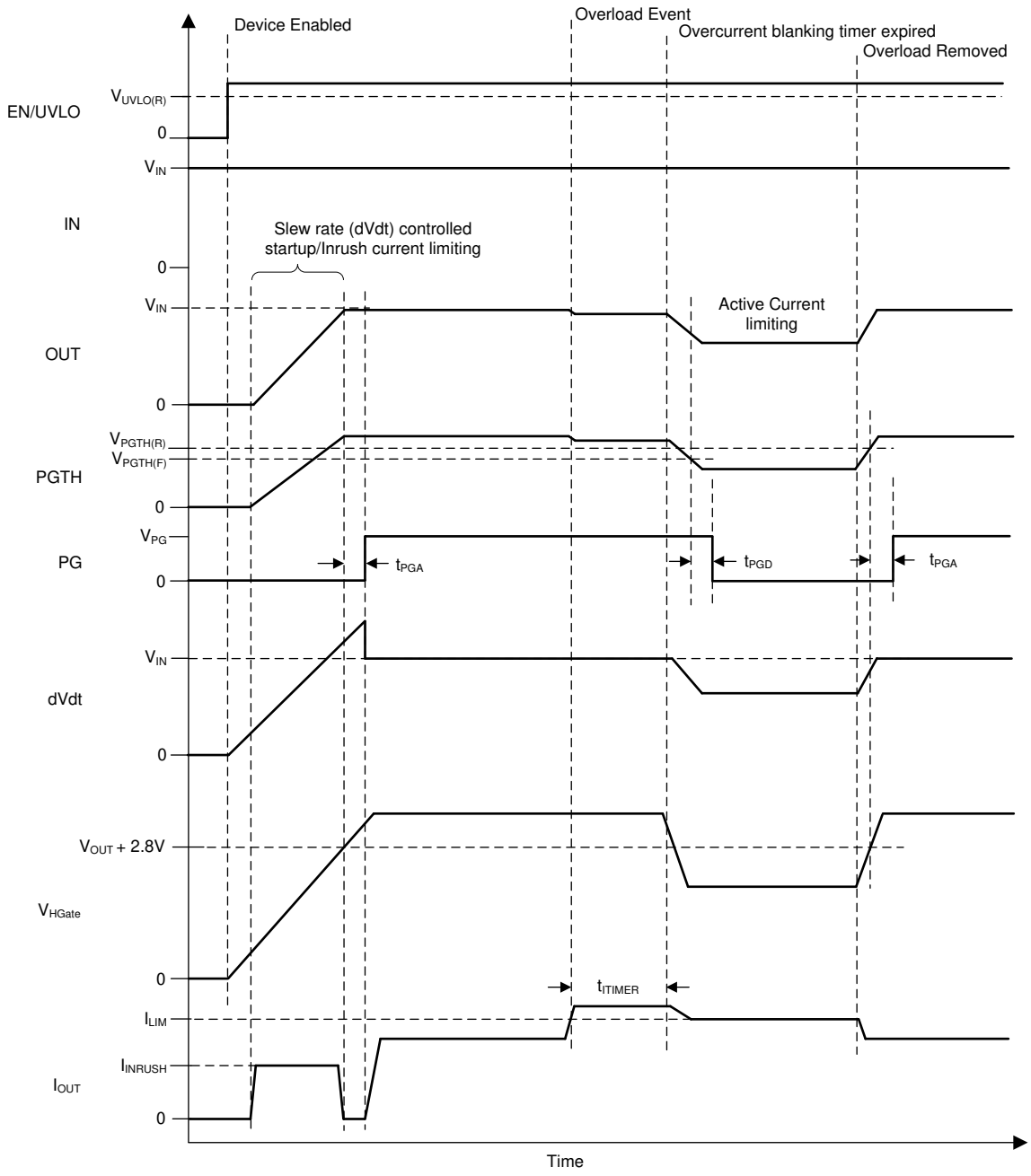


Figure 8-10. TPS2521xx PG Timing Diagram

Table 8-4. TPS2521xx PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Input Reverse Polarity	Shutdown	L	
Overvoltage (OVC)	Clamp	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}

Table 8-4. TPS2521xx PG Indication Summary (continued)

Event	Protection Response	PG Pin	PG Delay
Steady State	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Transient overcurrent	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload	Current Limiting	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Output Short-Circuit to GND	Fast trip followed by Current Limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
ILM Pin Open	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
ILM Pin Shorted to GND	Shutdown	L (If PGTH < $V_{PGTH(F)}$)	t_{PGD}
Reverse current ((V_{OUT} - V_{IN}) > V_{REVTH})	Reverse current blocking	L	t_{PGD}
Overtemperature	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.4 Device Functional Modes

Table 8-5. TPS2521xx Overvoltage Clamp Threshold Selection

OVCSEL Pin Connection	Overvoltage Clamp Threshold
Shorted to GND	3.8 V
Open	5.7 V

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS2521xx is a 2.7 V to 5.7 V, 4-A eFuse that is typically used for power rail protection applications. It can withstand maximum input voltage of 28 V with adjustable undervoltage lockout and fast overvoltage clamp protection. It provides ability to control inrush current and protection against input reverse polarity as well as reverse current conditions. It can be used in a variety of systems such as Adapter Input Protection, Storage – eSSD/cSSD, e-Meters, Smart Speakers, Headphones, USB power accessories. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool TPS2521x Design Calculator is available in the web product folder.

9.2 Single Device, Self-Controlled

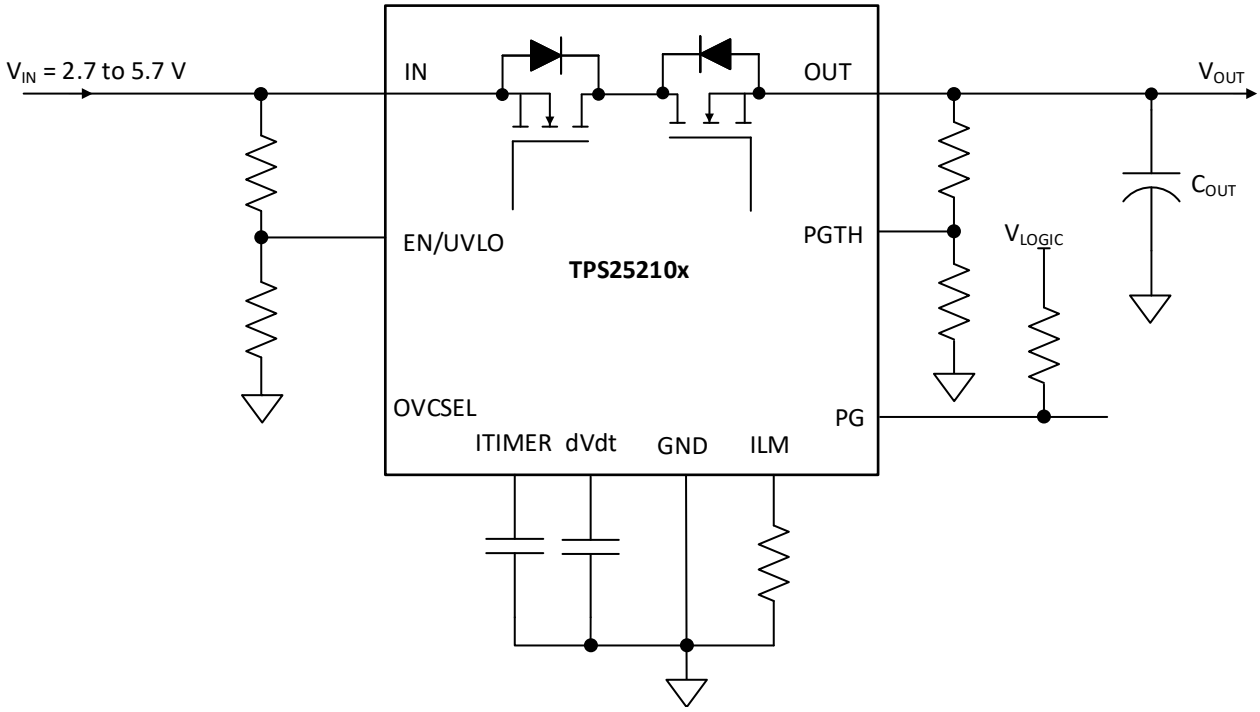


Figure 9-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVCSEL can also be driven from the host GPIO to control/ configure the device operation.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

Note

It's recommended to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation.

Either V_{IN} or V_{OUT} can be used to drive the PGTH resistor divider depending on which supply needs to be monitored for power good indication.

9.3 Typical Application

End equipments like PC, Notebooks, Docking Stations, Monitors etc.. have USB PD ports which can be configured as DFP (Source), UFP (Sink) or DRP (Source+Sink). TPS2521xx can be used independently or in conjunction with LM73100 to handle the power path protection requirements of USB PD ports as shown in Figure 9-2 below.

TPS2521xx provides Overcurrent & Short-Circuit protection in the source path, while blocking any reverse current from the port to the internal source power rail. The fast recovery (t_{SWRCB}) from reverse current blocking ensures minimum supply droop during Fast Role Swap (FRS) events.

The LM73100 provides overvoltage protection on the sink path, while blocking reverse current from internal sink rail to the port.

The linear ORing mechanism in TPS2521xx & LM73100 ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

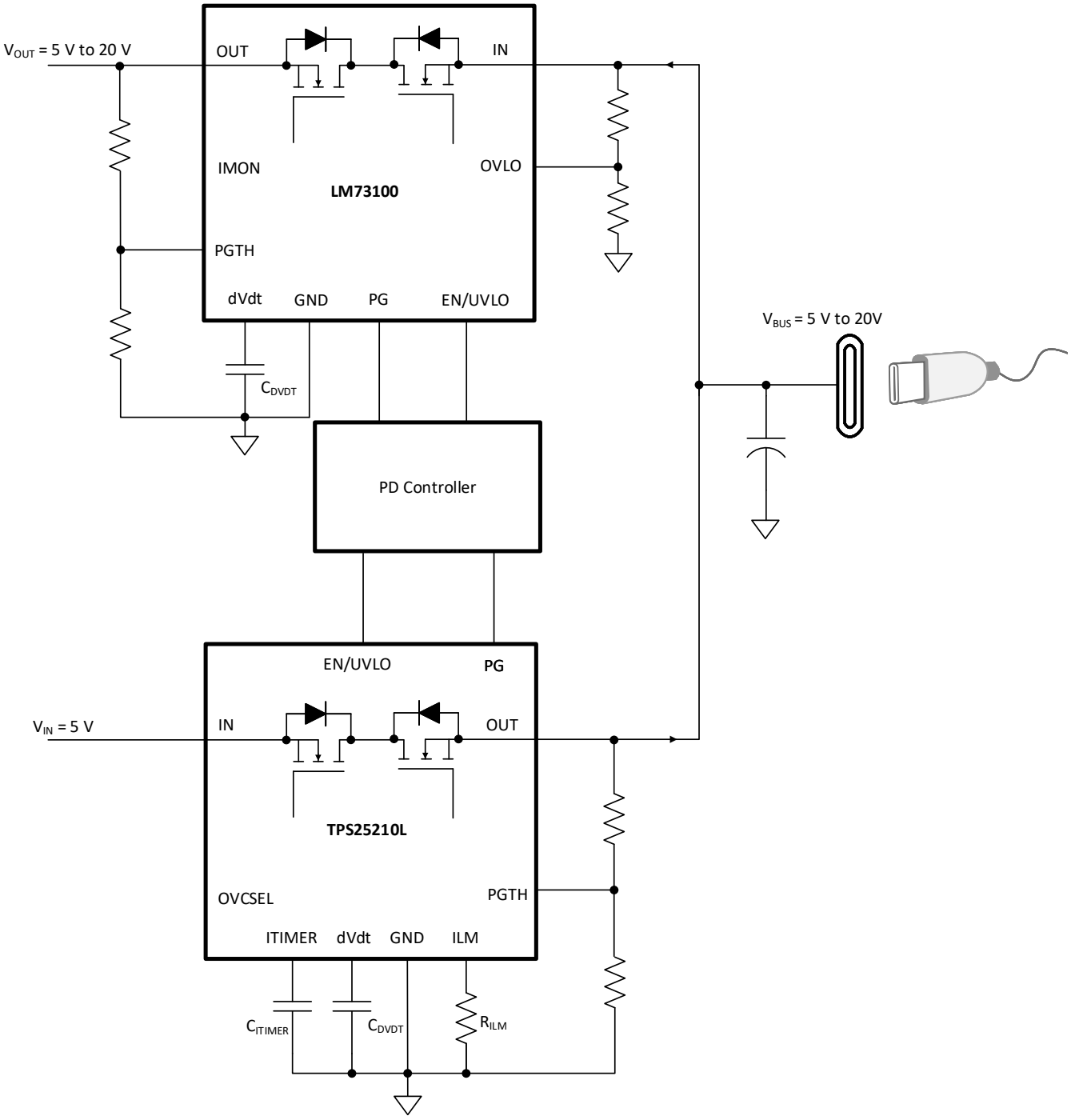


Figure 9-2. USB PD Port Protection

9.3.1 Application

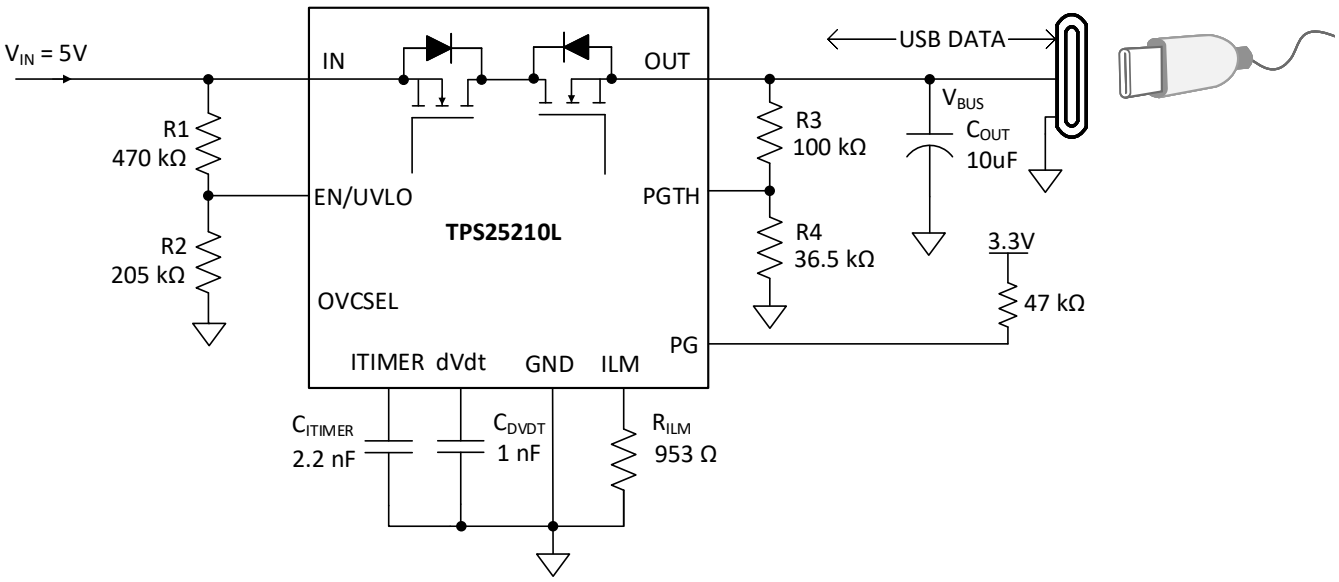


Figure 9-3. TPS2521xx Application Circuit for USB PD Source Path Protection

9.3.2 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	5 V
Undervoltage threshold ($V_{IN(UV)}$)	4 V
Overvoltage Clamp ($V_{IN(OVC)}$)	5.7 V
Output power good threshold (V_{PG})	4.5 V
Output capacitance (C_{OUT})	10 µF
Output Slew Rate (SR)	2 V/ms
Max continuous current	3 A
Overcurrent response	Current Limit
Current Limit Threshold (I_{LIM})	3.5 A
Load transient blanking interval (t_{ITIMER})	2 ms
Fault response	Latch-off

9.3.3 Detailed Design Procedure

9.3.3.1 Device Selection

Since the application requires current limit response to overcurrent with latch-off response after a fault, the TPS25210L variant is selected after refering to the *Device Comparison Table*.

9.3.3.2 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage threshold is set using the resistors R1 , R2 and can be calculated using Equation 7:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \times (R1 + R2)}{R2} \quad (7)$$

$V_{UVLO(R)}$ is the UVLO rising threshold. Because R1 & R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1 and R2 from the power supply is IR12 = V_{IN} / (R1 + R2). However, leakage currents due to external active

components connected to the resistor string can add error to these calculations. So, the resistor string current, IR12 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO pin.

From the device electrical specifications, the EN/UVLO leakage current is 0.1 µA (max), and $V_{UVLO(R)}$ = 1.2 V. From design requirements,$V_{IN(UV)}$ = 4 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equation to solve for R2 = 201.4 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ and R2 = 205 kΩ.

Refer to Table 8-5 to set overvoltage clamp. OVCSEL pin is left open to select overvoltage clamp as 5.7 V.

9.3.3.3 Setting Output Voltage Rise Time (t_R)

The slew rate (SR) needed to meet the target specification is:

$$\mathrm{SR\,(V/ms)} = 2\ \mathrm{V/ms} \tag{8}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$\mathrm{C_{dVdt}\,(pF)} = \frac{2000}{\mathrm{SR\ (V/ms)}} = \frac{2000}{2} = 1000\ \mathrm{pF} \tag{9}$$

Choose the nearest standard capacitor value as 1 nF.

For this slew rate, the inrush current can be calculated as:

$$\mathrm{I_{INRUSH}\,(mA)} = \mathrm{SR\,(V/ms)\ x\ C_{OUT}\,(\mu F)} = 2\ \mathrm{x}\ 10 = 20\ \mathrm{mA} \tag{10}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\mathrm{PD_{INRUSH}\,(W)} = \frac{\mathrm{I_{INRUSH}\ (A)\ x\ V_{IN}\ (V)}}{2} = \frac{0.02\ \mathrm{x}\ 5}{2} = 0.05\ \mathrm{W} \tag{11}$$

The power dissipation is below the allowed limit for a successful start-up without hitting thermal shut-down within the target rise time as shown in Figure 9-4.

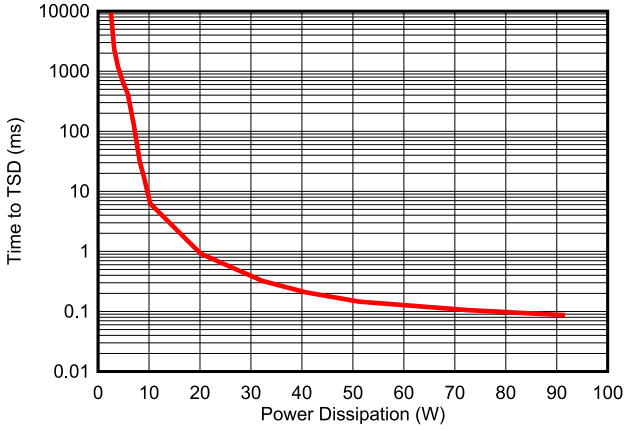


Figure 9-4. Thermal Shut-Down Plot During Inrush

9.3.3.4 Setting Power Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R3 & R4 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \text{ x } (R3 + R4)}{R4} \quad (12)$$

Because R3 and R4 leak the current from the output rail V_{OUT}, these resistors must be selected to minimize the leakage current. The current drawn by R3and R4 from the power supply is IR34 = V_{OUT} / (R3+ R4). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR34 must be chosen to be 20 times greater than the PGTH leakage current expected.

From the device electrical specifications, PGTH leakage current is 1 µA (max), $V_{PGTH(R)}$ = 1.2 V and from design requirements, V_{PG} = 4.5 V. To solve the equation, first choose the value of R3 = 100 kΩ and calculate R4 = 36.4 kΩ. Choose nearest 1% standard resistor value as R4 = 36.5 kΩ.

9.3.3.5 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (Current limit) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} = \frac{3334}{3.5\text{ A}} = 952.57\ \Omega \quad (13)$$

Choose nearest 1% standard resistor value as 953 Ω.

9.3.3.6 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \text{ x } I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} = \frac{2 \text{ x } 1.8}{1.5} = 2.4\text{ nF} \quad (14)$$

Choose nearest standard capacitor value as 2.2 nF.

9.3.4 Application Curves

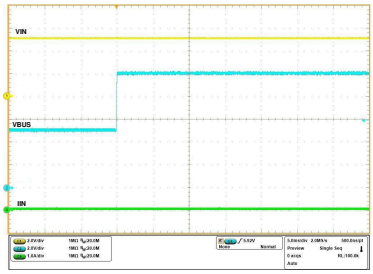


Figure 9-5. VBUS 20-V Hot-Plug

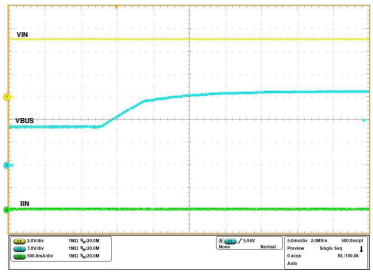
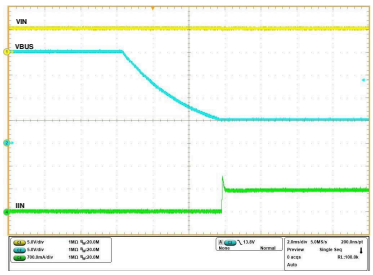


Figure 9-6. VBUS 20-V Slow Ramp Up



V_{IN} = 5 V, C_{OUT} = 10 µF, R_{OUT} = 8 Ω, V_{BUS} = 20 V initially and then disconnected

Figure 9-7. Fast Role Swap

10 Power Supply Recommendations

The TPS2521xx devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 5.7 V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

The lowest negative voltage the device can handle at the input is limited to -15 V or V_{OUT} – 21 V, whichever is higher. Any low voltage signals (e.g. EN/UVLO, PGTH) derived from the input supply must have a sufficiently large pull-up resistor to limit the current through those pins to < 10 µA during reverse polarity conditions. Please refer to *Absolute Maximum Ratings* table for more details.

10.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Connect a low ESR capacitor of value greater than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating should be atleast twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 15:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

where

- V_{IN} is the nominal supply voltage.
- I_{LOAD} is the load current.
- L_{IN} equals the effective inductance seen looking into the source.
- C_{IN} is the capacitance present at the input.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

Note

If there's a likelihood of input reverse polarity in the system, it's recommended to use a bi-directional TVS, or a reverse blocking diode in series with the TVS.

For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there could be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. It's recommended to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in Figure 10-1.

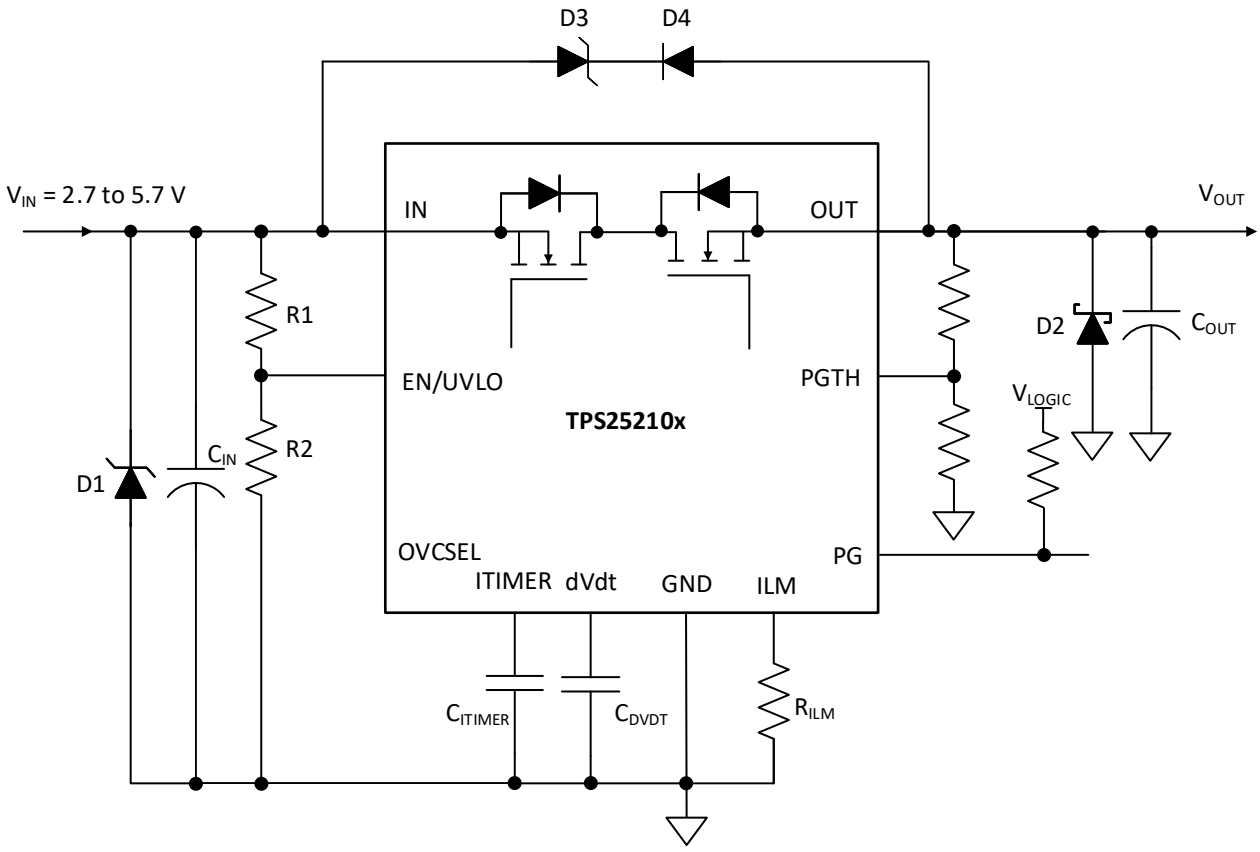


Figure 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. It's recommended to have a separate ground plane island for the eFuse. This plane doesn't carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane should be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible. Adding thermal vias on the under the device further helps to minimize the voltage gradient accross the IN and OUT pads and distribute current unformly through the device, which improves the on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, OVCSEL and PGTH pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. It's recommended to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Since the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads. It's also recommended to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

11.2 Layout Example

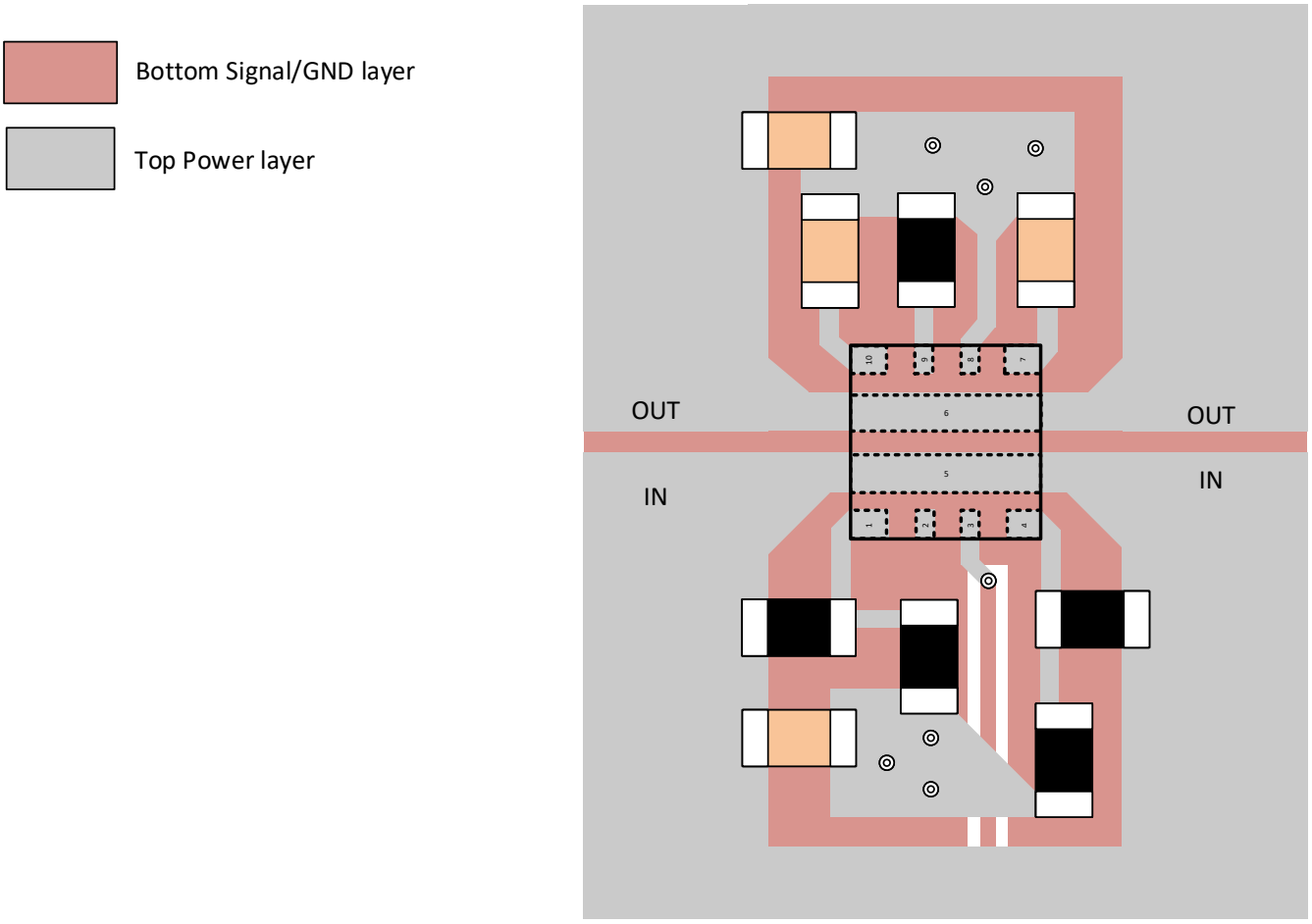


Figure 11-1. Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *TPS25210EVM eFuse Evaluation Board*
- *TPS2521x Design Calculator*
- *Application brief - eFuses for USB Type-C protection*
- *Application brief - eFuses in smart e-meters*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25210ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2AJH	Samples
TPS25210LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2AIH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

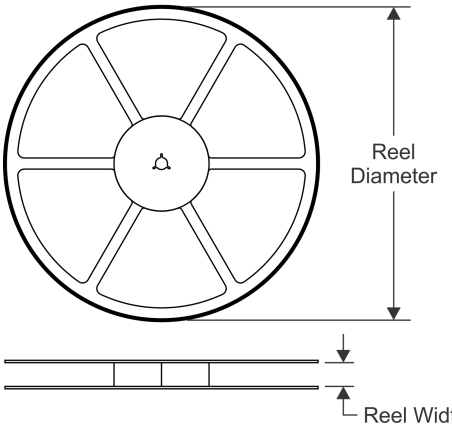
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

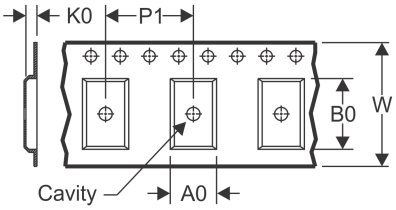
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

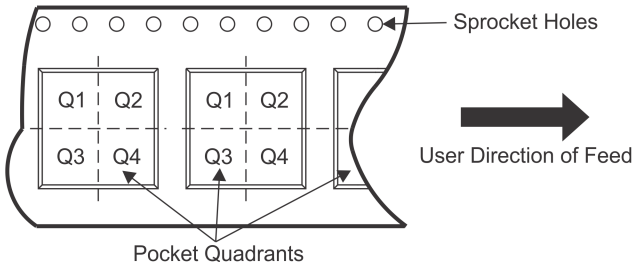


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

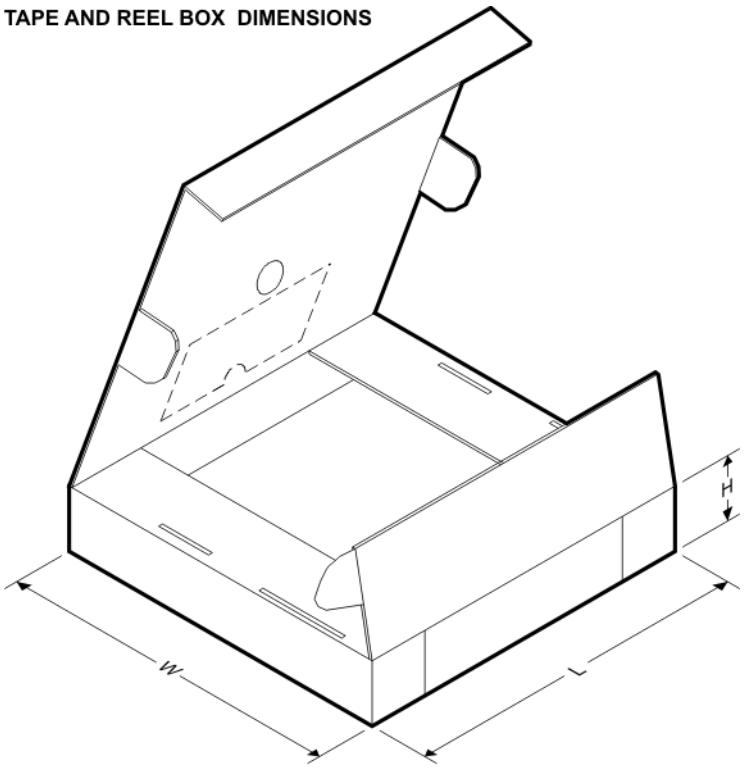
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25210ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25210LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

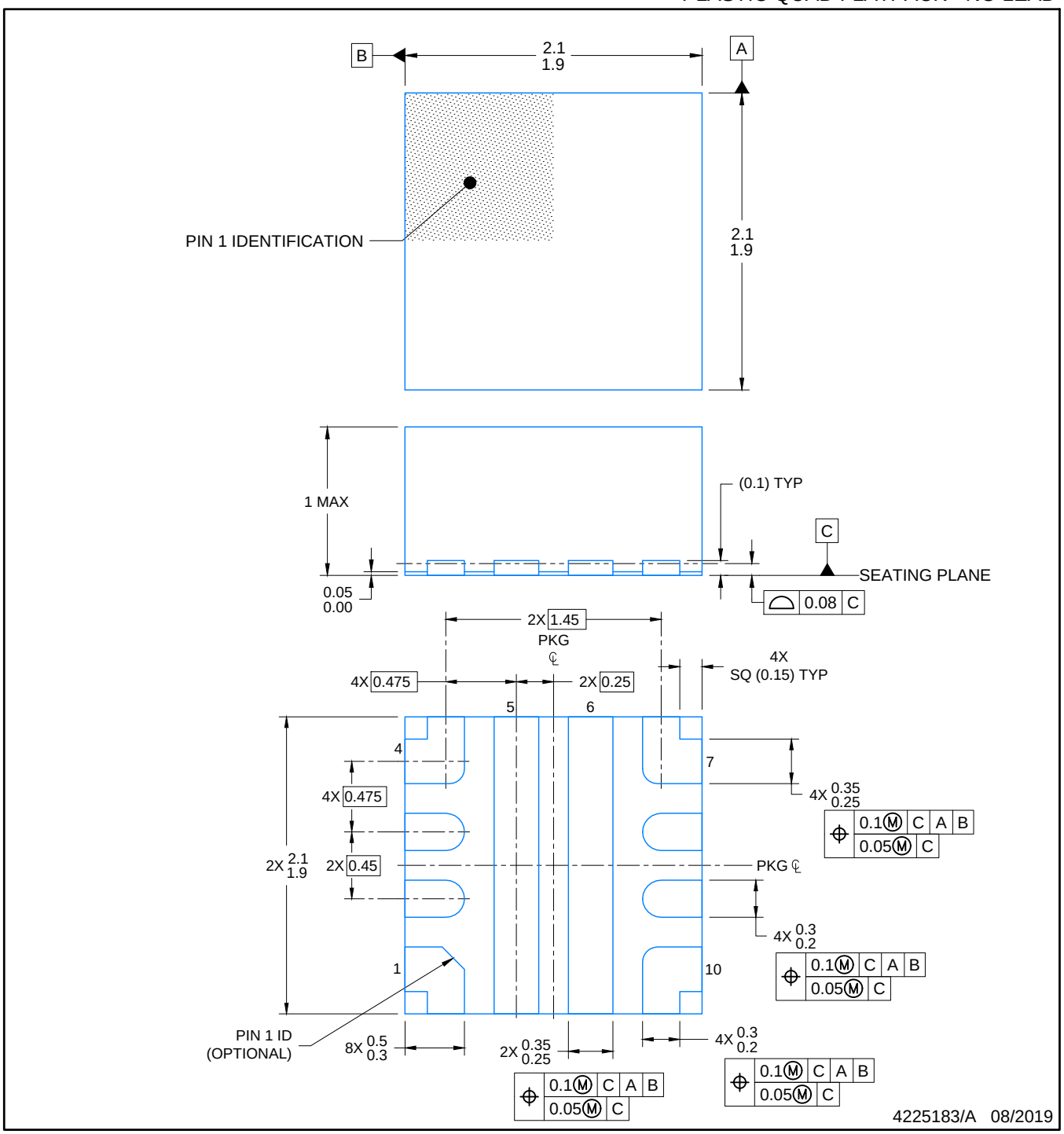
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25210ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25210LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

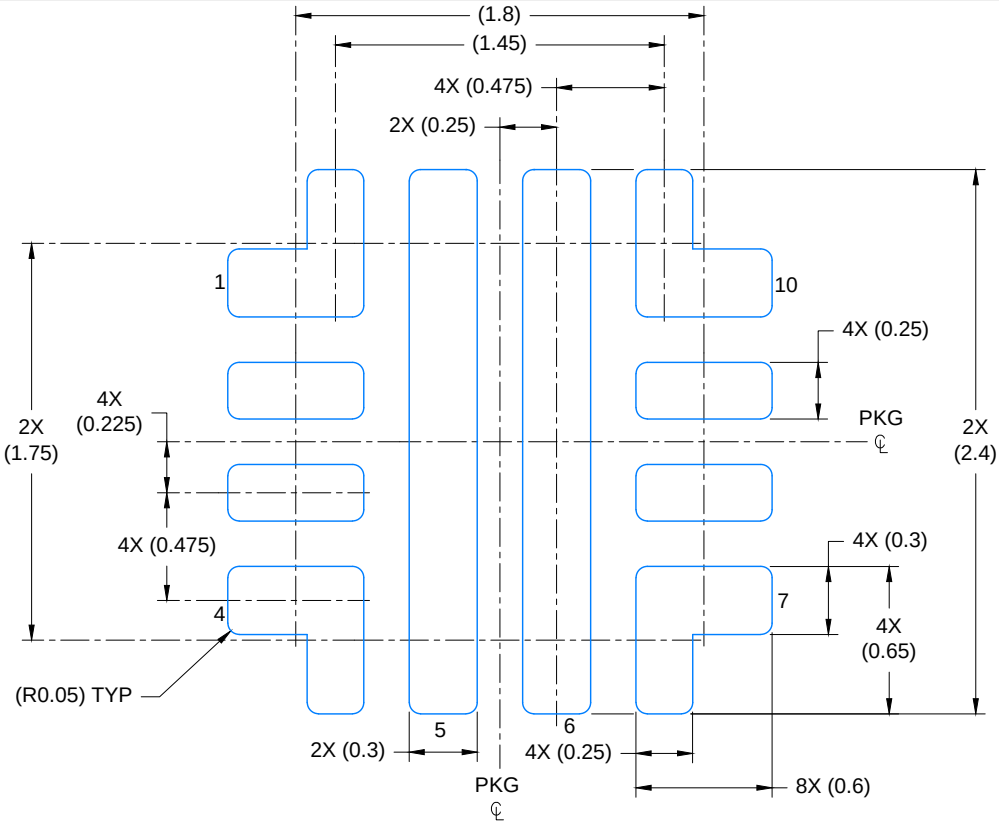
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



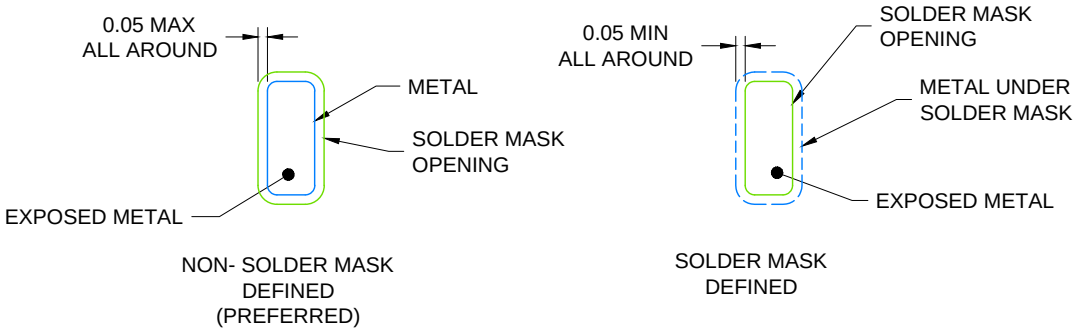
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



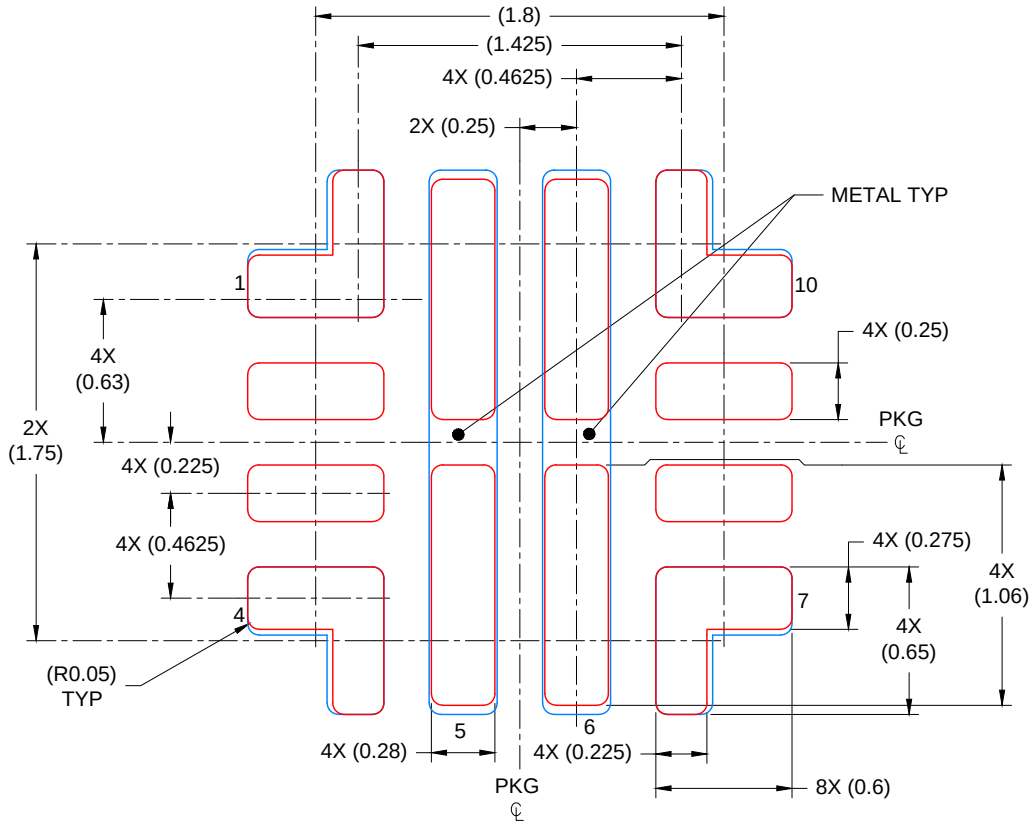
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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