2.5-V to 18-V High-Efficiency Adjustable Power-Limiting Hot-Swap Controller With Current Monitor and Overvoltage Protection

Check for Samples: TPS24720

FEATURES

- 2.5-V to 18-V Operation
- Accurate Current Limiting for Startup
- Programmable FET SOA Protection
- Adjustable Current Sense Threshold
- Programmable Fault Timer
- Power-Good Output
- Fast Breaker for Short-Circuit Protection
- Analog Load-Current Monitor Output
- Programmable UV and OV
- Low-current Standby Mode
- FET Fault Detection Flag
- 3-mm × 3-mm, 16-Pin QFN package

APPLICATIONS

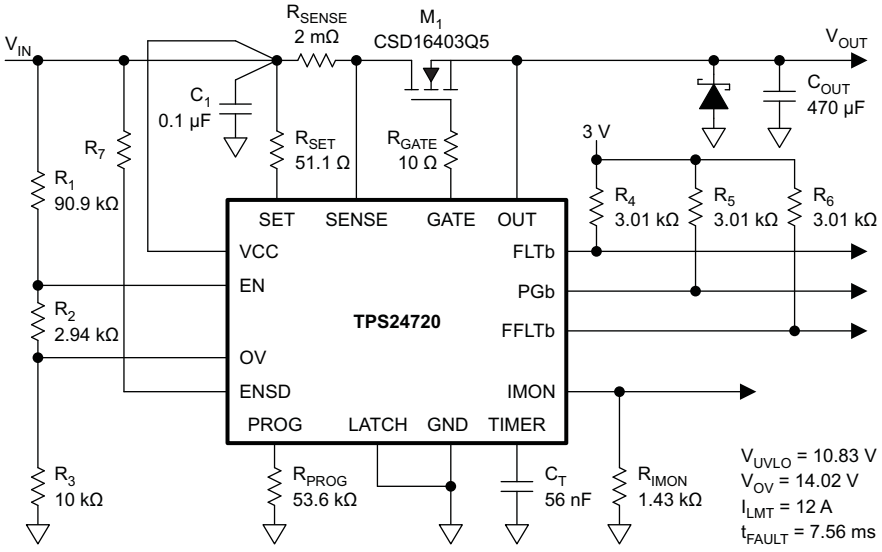
- Server Backplanes
- Storage Area Networks (SAN)
- Telecommunications Mezzanine Cards
- Medical Systems
- Plug-In Modules
- Base Stations

DESCRIPTION

The TPS24720 is an easy-to-use, full-featured protection device for 2.5-V to 18-V power rails. This hot-swap controller drives an external N-channel MOSFET, while protecting source, load and external MOSFET against multiple potentially damaging events. During startup, load current and MOSFET power dissipation are limited to user-selected values. After startup, currents above the user-selected limit will be allowed to flow until programmed timeout – except in extreme overload events when load is immediately disconnected from source.

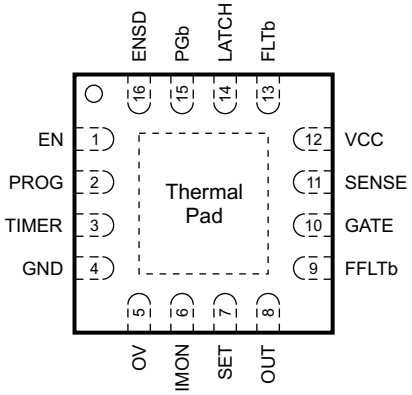
Programmable power limiting ensures the external MOSFET operates inside its safe operating area (SOA) at all times. This allows use of smaller FETs while improving system reliability. Power good, Fault, FET Fault, and current monitor outputs are provided for system status monitoring and downstream load control.

TYPICAL APPLICATION (12 V at 10 A)



PINOUT

RGT Package
(Top View)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

T_A	PACKAGE	PART NUMBER(1)	FUNCTION	MARKING
–40ºC to 85ºC	QFN-16	TPS24720	Latched or retry	24720

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)

			VALUE	UNIT
Input voltage range	EN, FFLTb(1), FLTb(1), GATE, OUT, PGb(1), SENSE, SET(1), VCC		–0.3 to 30	V
	ENSD, OV		–0.3 to 20	
	PROG(1)		–0.3 to 0.3	
	[SET, SENSE] to VCC		–0.3 to 0.3	
	IMON, LATCH, TIMER		–0.3 to 5	
Sink current	FFLTb, FLTb, PGb		5	mA
Source current	PROG		Internally limited	
	IMON		5	mA
ESD rating	Human-body model	All pins except PGb	2	kV
		PGb	0.5	
	Charged-device model		0.5	
Temperature	Maximum junction, T_J		Internally limited	°C

(1) Do not apply voltage directly to these pins.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS24720	UNIT
		QFN (16) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	47.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	63.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	20.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	ENSD, OV	0		16	V
	SENSE, SET(1), VCC	2.5		18	
	EN, FFLTb, FLTb, PGb, OUT	0		18	
Sink current	FFLTb, FLTb, PGb	0		2	mA
Source current	IMON	0		1	mA
Resistance	PROG	4.99		500	kΩ
External capacitance	TIMER	1			nF
	GATE(2)			1	µF
Operating junction temperature range, T_J		–40		125	°C

(1) Do not apply voltage directly to these pins.
(2) External capacitance tied to GATE should be in series with a resistor no less than 1 kΩ.

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 125°C, V_{CC} = 12 V, V_{EN} = 3 V, V_{ENSD} = 3 V, R_{SET} = 190 Ω, R_{IMON} = 5 kΩ, and R_{PROG} = 50 kΩ to GND.
All voltages referenced to GND, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC					
UVLO threshold, rising		2.2	2.32	2.45	V
UVLO threshold, falling		2.1	2.22	2.35	V
UVLO hysteresis(1)			0.1		V
Supply current	Enabled — I_{OUT} + I_{VCC} + I_{SENSE}		1	1.4	mA
	Disabled — EN = 0 V, I_{OUT} + I_{VCC} + I_{SENSE}		0.45		mA
	Shutdown — ENSD = 0 V, I_{OUT} + I_{VCC} + I_{SENSE}		1.7	10	µA
EN					
Threshold voltage, falling		1.2	1.3	1.4	V
Hysteresis(1)			50		mV
Input leakage current	0 V ≤ V_{EN} ≤ 30 V	–1	0	1	µA
Turnoff time	EN ↓ to V_{GATE} < 1 V, C_{GATE} = 33 nF	20	60	150	µs
Deglitch time	EN ↑	8	14	18	µs
Disable delay	EN ↓ to GATE ↓, C_{GATE} = 0, $t_{pff50–90}$, See Figure 1	0.1	0.4	1	µs
ENSD					
Threshold voltage	Rising or falling edge	0.3	0.7	1.4	V
Pullup current	V_{ENSD} = 5 V	0.5	1.2	2	µA
Disable delay	ENSD to GATE, $t_{pff50–90}$, See Figure 2		0.75	1	µs
OV					
Threshold voltage, rising		1.25	1.35	1.45	V
Hysteresis(1)			60		mV
Input leakage current	0 V ≤ V_{OV} ≤ 30 V	–1	0	1	µA
Deglitch time	OV rising	0.5	1.2	1.5	µs
FLTb					
Output low voltage	Sinking 2 mA		0.11	0.25	V
Input leakage current	V_{FLTb} = 0 V, 30 V	–1	0	1	µA
PGb					
Threshold	$V_{(SENSE – OUT)}$ rising, PGb going high	140	240	340	mV
Hysteresis(1)	Measured $V_{(SENSE – OUT)}$ falling, PGb going low		70		mV

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ T_J ≤ 125°C, V_{CC} = 12 V, V_{EN} = 3 V, V_{ENSD} = 3 V, R_{SET} = 190 Ω, R_{IMON} = 5 kΩ, and R_{PROG} = 50 kΩ to GND.

All voltages referenced to GND, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output low voltage	Sinking 2 mA		0.11	0.25	V
Input leakage current	V_{PGb} = 0 V, 30 V	–1	0	1	µA
Delay (deglitch) time	Rising or falling edge	2	3.4	6	ms
FFLTb					
V_{IMON} threshold	Measured V_{IMON} to GND	90	103	115	mV
Output low voltage	Sinking 2 mA		0.11	0.25	V
Input leakage current	FFLTb = 0 V, 30 V	–1	0	1	µA
Delay	FFLTb falling	60	115	140	ms
PROG					
Bias voltage	Sourcing 10 µA	0.65	0.678	0.7	V
Input leakage current	V_{PROG} = 1.5 V	–0.2	0	0.2	µA
TIMER					
Sourcing current	V_{TIMER} = 0 V	8	10	12	µA
Sinking current	V_{TIMER} = 2 V	8	10	12	µA
	V_{EN} = 0 V, V_{TIMER} = 2 V	2	4.5	7	mA
Upper threshold voltage		1.3	1.35	1.4	V
Lower threshold voltage		0.33	0.35	0.37	V
Timer activation voltage	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE - VCC)}$, V_{VCC} = 12 V	5	5.9	7	V
Bleed-down resistance	V_{ENSD} = 0 V, V_{TIMER} = 2 V	70	104	130	kΩ
IMON					
Summing threshold	Current limit in regulation	660	675	690	mV
OUT					
Input bias current	V_{OUT} = 12 V		16	30	µA
SET					
Input referred offset	Measure SET to SENSE	–1.5	0	1.5	mV
GATE					
Output voltage	V_{OUT} = 12 V	23.5	25.8	28	V
Clamp voltage	Inject 10 µA into GATE, measure $V_{(GATE - VCC)}$	12	13.9	15.5	V
Sourcing current	V_{GATE} = 12 V	20	30	40	µA
Sinking current	Fast turnoff, V_{GATE} = 14 V	0.5	1	1.4	A
	Sustained, V_{GATE} = 4 V to 23 V	6	11	20	mA
	In inrush current limit, V_{GATE} = 4 V to 23 V	20	30	40	µA
Pulldown resistance	Thermal shutdown or V_{ENSD} = 0 V	14	20	26	kΩ
Turn on delay	V_{VCC} rising to GATE sourcing, $t_{prr50-50}$, See Figure 3		100	250	µs
SENSE					
Input bias current	V_{SENSE} = 12 V, sinking current		30	40	µA
Current limit threshold	V_{OUT} = 12 V	22.5	25	27.5	mV
Power limit threshold	V_{OUT} = 7 V, R_{PROG} = 50 kΩ	10	12.5	15	mV
	V_{OUT} = 2 V, R_{PROG} = 25 kΩ	10	12.5	15	
Fast-trip threshold		52	60	68	mV
Fast-turnoff duration		8	13.5	18	µs
Fast-turnoff delay	$V_{(VCC - SENSE)}$ = 80 mV, C_{GATE} = 0 pF, $t_{prf50-50}$, See Figure 4		200		ns
LATCH					
Threshold, rising		0.3	0.9	1.4	V
Pullup current	V_{LATCH} = 0 V	7	10	13	µA

ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ T_J ≤ 125°C, V_{CC} = 12 V, V_{EN} = 3 V, V_{ENSD} = 3 V, R_{SET} = 190 Ω, R_{IMON} = 5 kΩ, and R_{PROG} = 50 kΩ to GND.

All voltages referenced to GND, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
OTSD					
Threshold, rising		130	140		°C
Hysteresis(2)			10		°C

(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

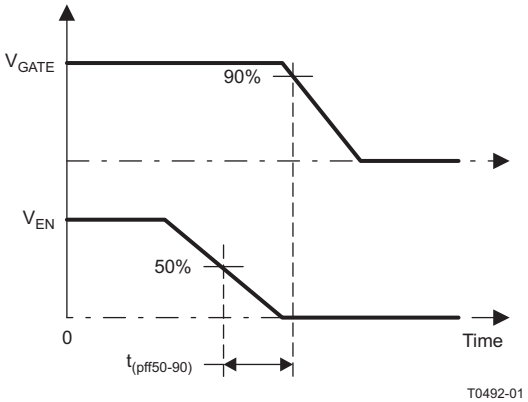


Figure 1. $t_{pff50–90}$ Timing Definition

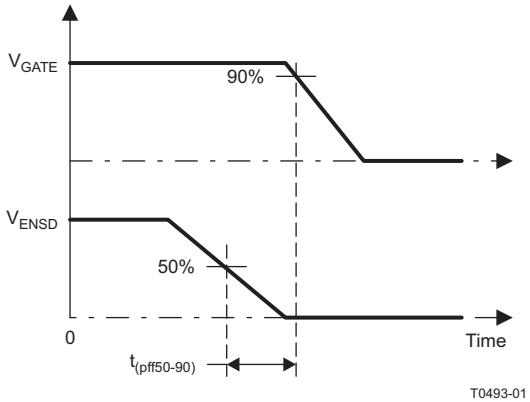


Figure 2. $t_{pff50–90}$ Timing Definition

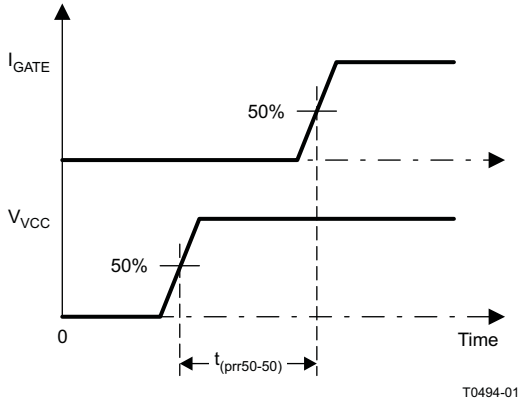


Figure 3. $t_{prr50–50}$ Timing Definition

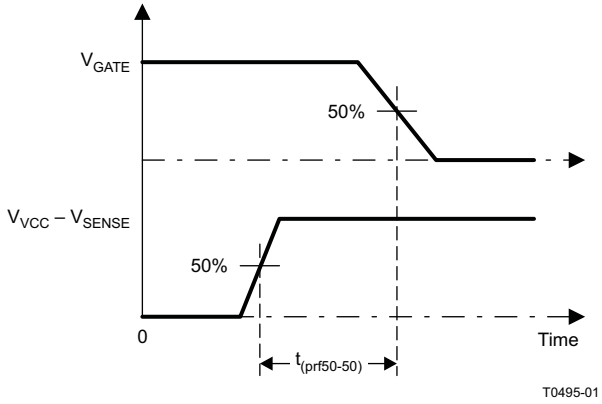


Figure 4. $t_{prf50–50}$ Timing Definition

FUNCTIONAL BLOCK DIAGRAM

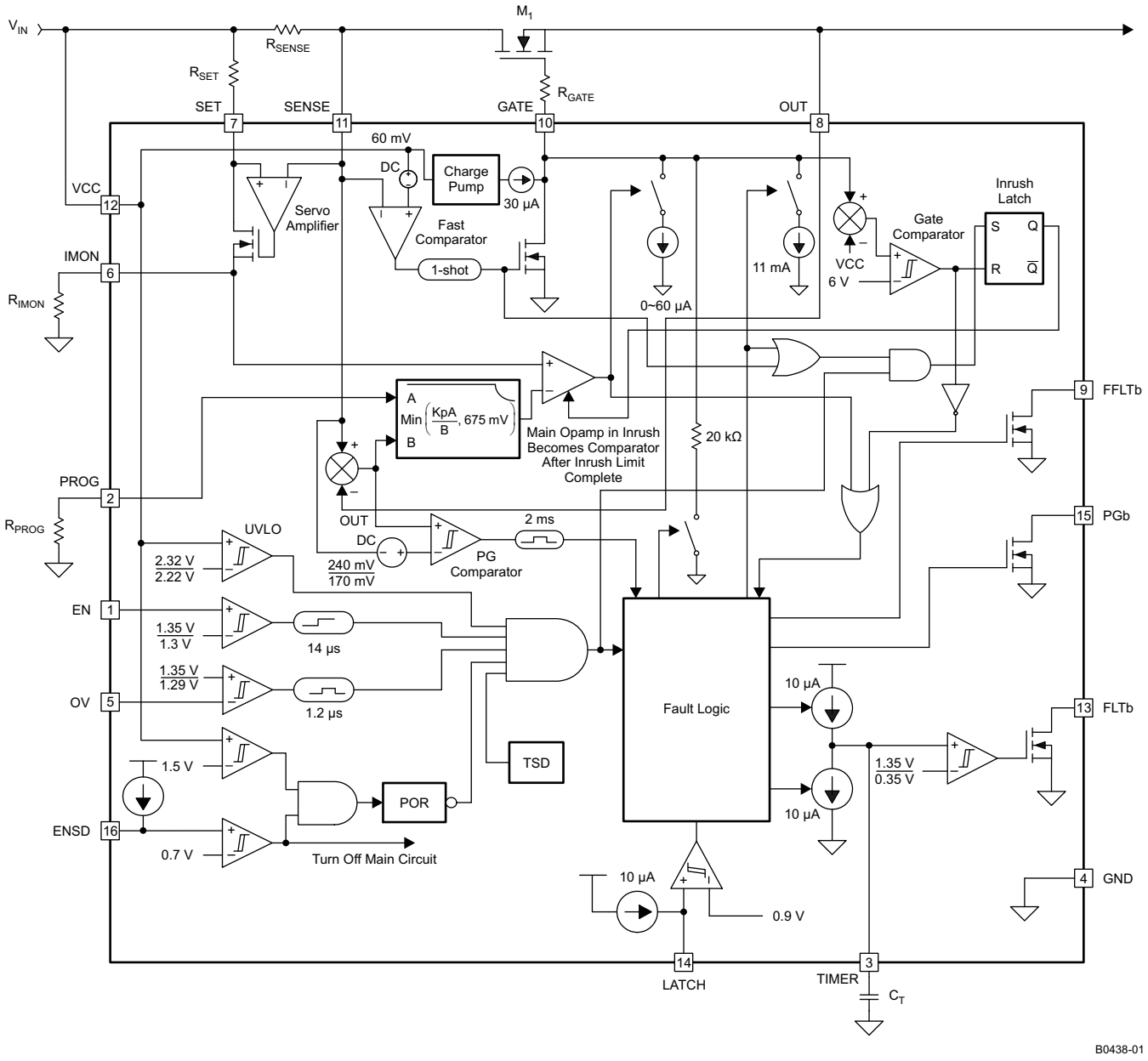


Figure 5. Block Diagram of the TPS24720

PIN FUNCTIONS

NAME	PIN	I/O	DESCRIPTION
EN	1	I	Active-high enable input. Logic input. Connects to resistor divider.
ENSD	16	I	Pull low to put device into low-current standby mode. Logic input.
FFLTb	9	O	Active-low, open-drain FET fault indicator. Indicates shorted MOSFET when output is off.
FLTb	13	O	Active-low, open-drain output indicates overload fault timer has turned MOSFET off.
GATE	10	O	Gate driver output for external MOSFET
GND	4	–	Ground
IMON	6	O	Analog load current limit program point. Connect R_{IMON} to ground.

PIN FUNCTIONS (continued)

NAME	PIN	I/O	DESCRIPTION
LATCH	14	I	Latch or retry mode select input. Latch when floating or connected to a logic-level voltage; retry when connected to GND.
OUT	8	I	Output voltage sensor for monitoring MOSFET power.
OV	5	I	Overvoltage comparator input. Connects to resistor divider. GATE is pulled low when OV exceeds the threshold.
PGb	15	O	Active-low, open-drain power-good indicator. Status is determined by the voltage across the MOSFET.
PROG	2	I	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the FET.
SENSE	11	I	Current-sensing input for resistor shunt from VCC to SENSE.
SET	7	I	Current-limit programming set pin. A resistor is connected from this pin to VCC.
TIMER	3	I/O	A capacitor connected from this pin to GND provides a fault timing function.
VCC	12	I	Input-voltage sense and power supply
Thermal pad	—	—	Tied to GND

DETAILED PIN DESCRIPTIONS

The following description relies on the typical application diagram shown on the front page of this data sheet, as well as the functional block diagram in Figure 5.

EN: Applying a voltage of 1.35 V or more to this pin enables the gate driver. The addition of an external resistor divider allows the EN pin to serve as an undervoltage monitor. Cycling EN low and then back high resets the TPS24720 that has latched off due to a fault condition. This pin should not be left floating.

ENSD: When this pin is pulled low, it shuts off all internal circuitry and thus places the device in a low-current standby mode. While in standby, the PGb, FLTb, and FFLTb outputs assume high-impedance states. A 20-kΩ resistor pulls GATE to GND in standby. This is a much weaker pulldown than the 11 mA drawn while the part is disabled (e.g., by EN, UVLO, OV, or overload fault current). Applications requiring rapid turnoff should disable the device using the EN pin before pulling ENSD low. This pin is preferably pulled up to a positive voltage from 2 V to 18 V, if not otherwise connected.

FFLTb: This active-low open-drain output pulls low if V_{VCC} is higher than the UVLO rising threshold and the voltage on the IMON pin exceeds 103 mV when EN is disabled. The presence of this voltage indicates that current continues to flow through the external circuitry even though the external MOSFET has been turned off. This presumably indicates a shorted MOSFET. FFLTb assumes a high impedance if one of the following conditions occurs:

- ENSD is pulled low.
- Temperature on the die exceeds the OTSD shutdown threshold.
- V_{VCC} drops below the UVLO falling threshold.

FFLTb also asserts if V_{VCC} is higher than the UVLO rising threshold, GATE is disabled by OV, and the voltage on the IMON pin exceeds 103 mV. This pin can be left floating when not used.

FLTb: This active-low open-drain output pulls low when the TPS24720 has remained in current limit long enough for the fault timer to expire. The behavior of the FLTb pin depends on the status of the LATCH pin. If the LATCH pin is held high or left floating, the TPS24720 operates in latch mode. If the LATCH pin is held low, the TPS24720 operates in retry mode. In latch mode, a fault timeout disables the external MOSFET and holds FLTb low. The latched mode of operation is reset by cycling EN, VCC, or ENSD. In retry mode, a fault timeout first disables the external MOSFET, next waits sixteen cycles of TIMER charging and discharging, and finally attempts a restart. This process repeats as long as the fault persists. In retry mode, the FLTb pin is pulled low whenever the external MOSFET is disabled by the fault timer. In a sustained fault, the FLTb waveform becomes a train of pulses. The FLTb pin does not assert if the external MOSFET is disabled by EN, ENSD, OV, overtemperature shutdown, or UVLO. This pin can be left floating when not used.

GATE: This pin provides gate drive to the external MOSFET. A charge pump sources 30 µA to enhance the external MOSFET. A 13.9-V clamp between GATE and VCC limits the gate-to-source voltage, because V_{VCC} is very close to V_{OUT} in normal operation. During start-up, a transconductance amplifier regulates the gate voltage of M_1 to provide inrush current limiting. The TIMER pin charges timer capacitor C_T during the inrush. Inrush current limiting continues until the $V_{(GATE - VCC)}$ exceeds the Timer Activation Voltage (6 V for V_{VCC} = 12 V). Then the TPS24720 enters into circuit-breaker mode. The Timer Activation Voltage is defined as a threshold voltage. When $V_{(GATE-VCC)}$ exceeds this threshold voltage, the inrush operation is finished and the TIMER stops sourcing current and begins sinking current. In the circuit-breaker mode, the current flowing in R_{SENSE} is compared with the current-limit threshold derived from the MOSFET power-limit scheme (see PROG). If the current flowing in R_{SENSE} exceeds the current limit threshold, then MOSFET M_1 is turned off. The GATE pin is disabled by the following three mechanisms:

1. GATE is pulled down by an 11-mA current source when
   - The fault timer expires during an overload current fault (V_{IMON} > 675 mV)
   - V_{EN} is below its falling threshold
   - V_{VCC} drops below the UVLO threshold
   - V_{OV} is above its rising threshold
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC - SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold or ENSD is pulled low.

GATE remains low in latch mode and attempts a restart periodically in retry mode.

If used, any capacitor connecting GATE and GND should not exceed 1 µF and it should be connected in series with a resistor of no less than 1 kΩ. No external resistor should be directly connected from GATE to GND or from GATE to OUT.

GND: This pin is connected to system ground.

IMON: A resistor connected from this pin to GND scales the current-limit and power-limit settings, as illustrated in Figure 5. The voltage present at this pin is proportional to the current flowing through sense resistor R_{SENSE}. This voltage can be used as a means of monitoring current flow through the system. The value of R_{IMON} can be calculated from Equation 3. This pin should not have a bypass capacitor or any other load except for R_{IMON}.

LATCH: This pin determines whether the TPS24720 operates in latch mode or retry mode. Applying a voltage of 2 V to 5 V to this pin or allowing it to float selects latch mode. Tying the pin to ground selects retry mode. In latch mode, an overload current fault disables the TPS24720 until EN, ENSD, or VCC is cycled. In retry mode, the TPS24720 automatically attempts a restart after every sixteen cycles of TIMER charging and discharging. In a sustained fault in retry mode, the external MOSFET conducts 3.93% of the time; i.e., the duty ratio is 0.0393. If the LATCH pin is allowed to float, then its open-circuit voltage is approximately 2.28 V.

OUT: This pin allows the controller to measure the drain-to-source voltage across the external MOSFET M_1. The power-good indicator (PGb) relies on this information, as does the power-limiting engine. The OUT pin should be protected from negative voltage transients by a clamping diode or sufficient capacitors. A Schottky diode of 3 A / 40 V in a SMC package is recommended as a clamping diode for high-power applications. The OUT pin should be bypassed to GND with a low-impedance ceramic capacitor in the range of 10 nF to 1 µF.

OV: This pin is used to program the device overvoltage level. A voltage of more than 1.35 V on this pin turns off the external MOSFET. A resistor divider connected from VCC to this pin provides overvoltage protection for the downstream load. This pin should be tied to GND when not used.

PGb: This active-low, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PGb pulls low after the drain-to-source voltage of the FET has fallen below 170 mV and a 3.4-ms deglitch delay has elapsed. It goes open-drain when V_{DS} exceeds 240 mV. PGb assumes high-impedance status after a 3.4-ms deglitch delay once V_{DS} of M_1 rises up, resulting from GATE being pulled to GND at any of the following conditions :

- An overload current fault occurs (V_{IMON} > 675 mV).
- A hard output short circuit occurs, leading to $V_{(VCC - SENSE)}$ greater than 60 mV, i.e., the fast-trip shutdown threshold has been exceeded.
- V_{EN} is below its falling threshold.

- V_{ENSD} is below its threshold.
- V_{VCC} drops below the UVLO threshold.
- V_{OV} is above its rising threshold.
- Die temperature exceeds the OTSD threshold.

This pin can be left floating when not used.

PROG: A resistor from this pin to GND sets the maximum power permitted in the external MOSFET M_1 during inrush. Do not apply a voltage to this pin. If the constant power limit is not desired, use a PROG resistor of 4.99 kΩ. To set the maximum power, use Equation 1,

$$P_{LIM} = \frac{3125}{R_{PROG} \times R_{SENSE}} \quad (1)$$

where P_{LIM} is the allowed power limit of MOSFET M_1. R_{SENSE} is the load-current-monitoring resistor connected between the VCC pin and the SENSE pin. R_{PROG} is the resistor connected from the PROG pin to GND. Both R_{PROG} and R_{SENSE} are in ohms and P_{LIM} is in watts. P_{LIM} is determined by the maximum allowed thermal stress of MOSFET M_1, given by Equation 2,

$$P_{LIM} < \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \quad (2)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature and $T_{C(MAX)}$ is the maximum case temperature prior to a start or restart. $R_{\theta JC(MAX)}$ is the junction-to-case thermal impedance of the pass MOSFET M_1 in units of °C/W. Both $T_{J(MAX)}$ and $T_{C(MAX)}$ are in °C.

SENSE: This pin connects to the negative terminal of R_{SENSE}. It provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the external FET. The current limit I_{LIM} is set by Equation 3.

$$I_{LIM} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}} \quad (3)$$

A fast-trip shutdown occurs when $V_{(VCC\ -\ VSENSE)}$ exceeds 60 mV.

SET: A resistor R_{SET} is connected from this pin to the positive terminal of R_{SENSE}. This resistor scales the current limit and power limit settings. It coordinates with R_{IMON} and R_{SENSE} to determine the current limit value. The value of R_{SET} can be calculated from Equation 3 (see SENSE).

TIMER: A capacitor C_T connected from the TIMER pin to GND determines the overload fault timing. TIMER sources 10 µA when an overload is present, and discharges C_T at 10 µA otherwise. M_1 is turned off when V_{TIMER} reaches 1.35 V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the external MOSFET is re-enabled. A minimum timing capacitance of 1 nF is recommended to ensure proper operation of the fault timer. The value of C_T can be calculated from the desired fault time t_{FLT}, using Equation 4.

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT} \quad (4)$$

As is explained in the description of the LATCH pin, either latch mode or retry mode occurs if the load current exceeds the current limit threshold or the fast-trip shutdown threshold, depending on the status of the LATCH pin. While in latch mode, the TIMER pin continues to charge and discharge the attached capacitor periodically. In retry mode, the external MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2-mA current source at the end of the 16th cycle of charging and discharging. The external MOSFET is then re-enabled. The TIMER pin capacitor, C_T, can also be discharged to GND during latch mode or retry mode in the following two ways:

1. A 2-mA current sinks TIMER whenever any of the following occurs:
   - V_{EN} is below its falling threshold.
   - V_{VCC} drops below the UVLO threshold.
   - V_{OV} is above its rising threshold.
2. A 100-kΩ resistor is connected to TIMER and discharges C_T at the moment when V_{ENSD} drops below its threshold.

TIMER is not affected when the die temperature exceeds the OTSD threshold.

VCC: This pin performs three functions. First, it provides biasing power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and undervoltage lockout (UVLO) functions. The VCC trace from the integrated circuit should connect directly to the positive terminal of R_{SENSE} to minimize the voltage sensing error. Bypass capacitor C_1, shown in the typical application diagram on the front page, should be connected to the positive terminal of R_{SENSE}. A capacitance of at least 10 nF is recommended.

TYPICAL CHARACTERISTICS

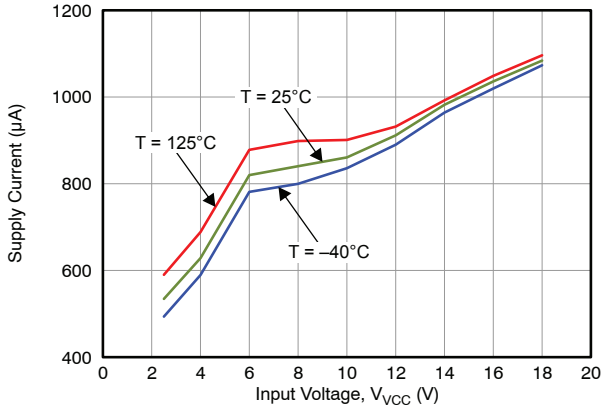


Figure 6. Supply Current vs Input Voltage at Normal Operation (EN = High)

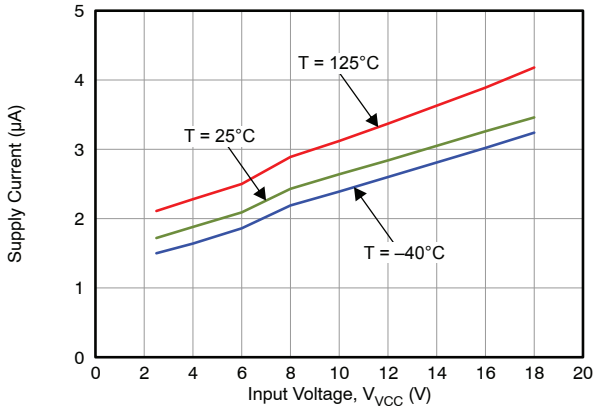


Figure 7. Supply Current vs Input Voltage at Shutdown (EN = 0 V)

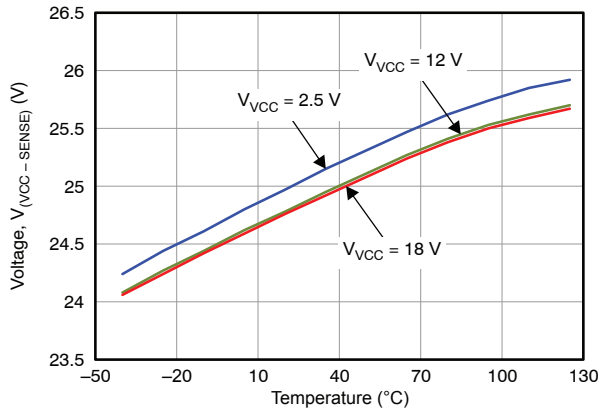


Figure 8. Voltage Across R_{SENSE} in Inrush Current Limiting vs Temperature

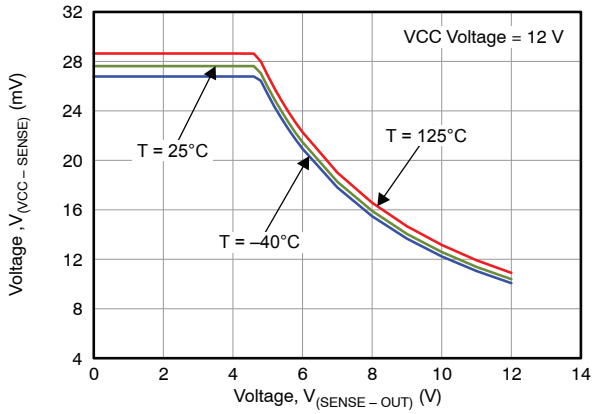


Figure 9. Voltage Across R_{SENSE} in Inrush Power Limiting vs V_{DS} of Pass MOSFET

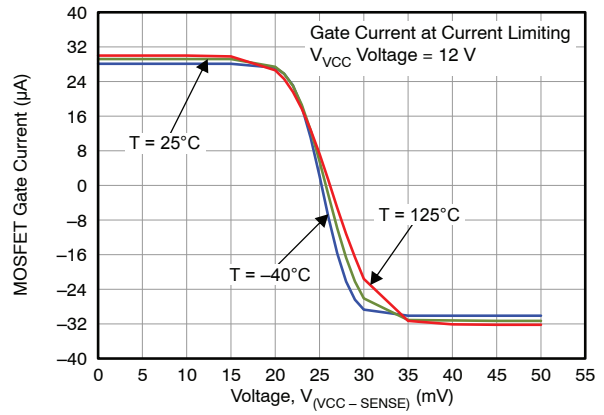


Figure 10. MOSFET Gate Current vs Voltage Across R_{SENSE} During Inrush Power Limiting

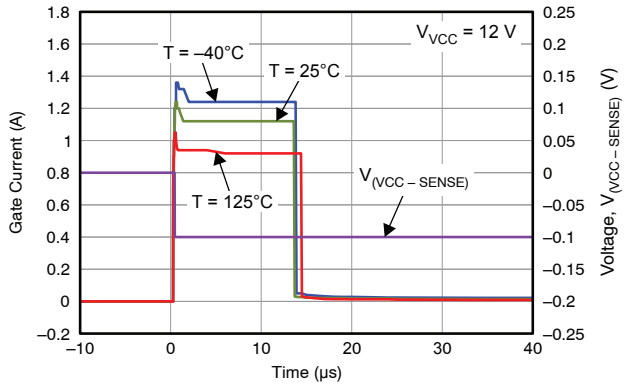


Figure 11. Gate Current During Fast Trip, V_{VCC} = V_{GATE} = 12 V

TYPICAL CHARACTERISTICS (continued)

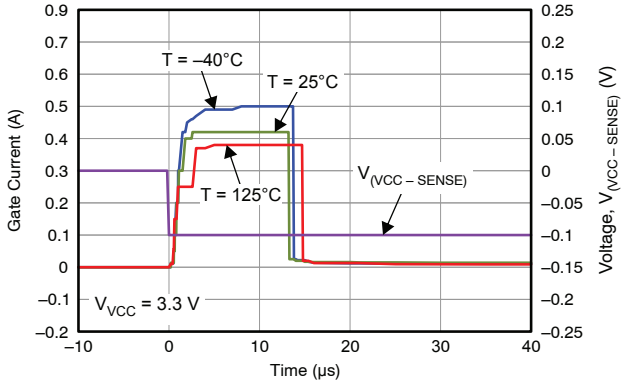


Figure 12. Gate Current During Fast Trip, V_{VCC} = V_{GATE} = 3.3 V

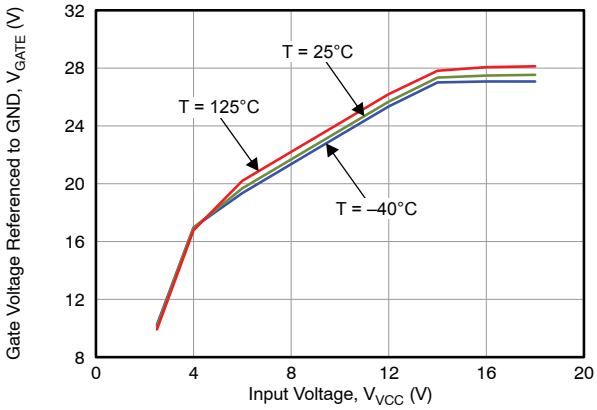


Figure 13. Gate Voltage With Zero Gate Current vs Input Voltage

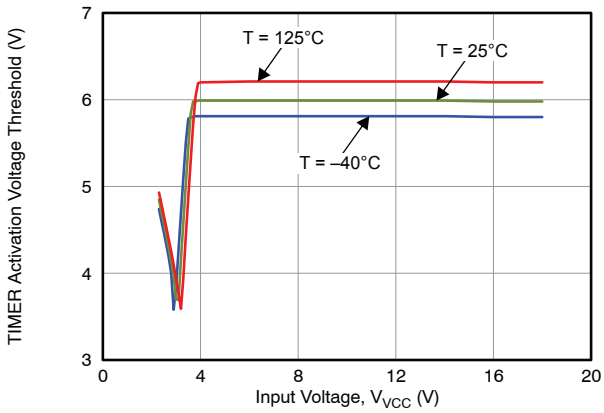


Figure 14. TIMER Activation Voltage Threshold vs Input Voltage at Various Temperatures

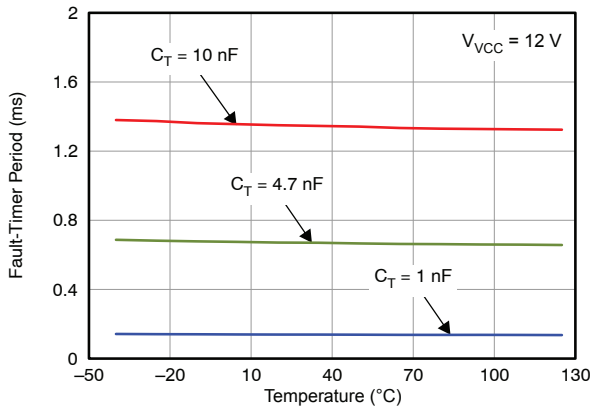


Figure 15. Fault-Timer vs Temperature With Various TIMER Capacitors

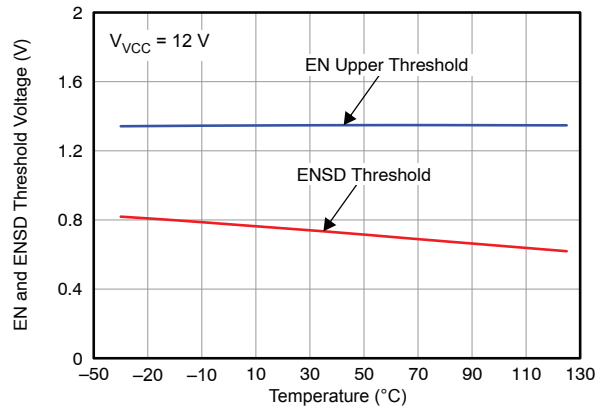


Figure 16. EN and ENSD Threshold Voltage vs Temperature

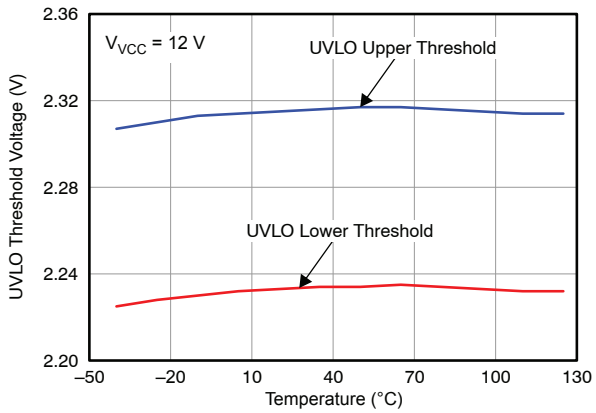


Figure 17. UVLO Threshold Voltage vs Temperature

TYPICAL CHARACTERISTICS (continued)

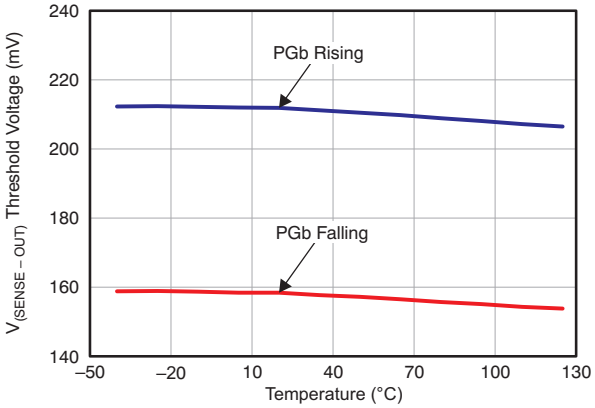


Figure 18. Threshold Voltage of V_{DS} vs Temperature, PGb Rising and Falling

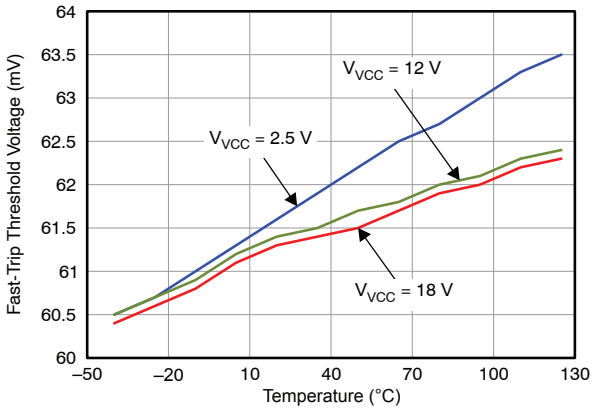


Figure 19. Fast-Trip Threshold Voltage vs Temperature

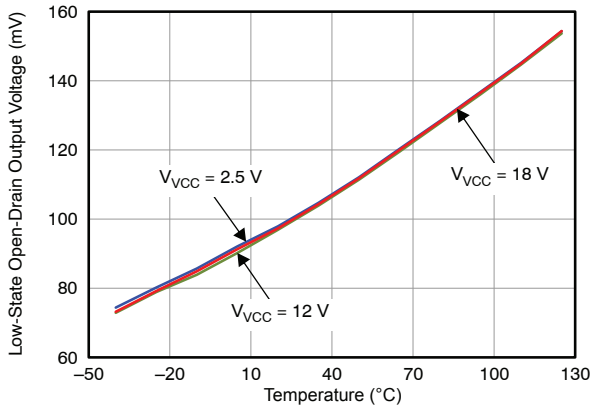


Figure 20. PGb Open-Drain Output Voltage in Low State

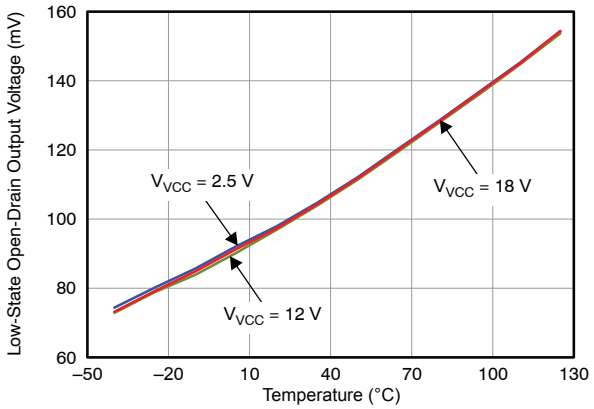


Figure 21. FLTb Open-Drain Output Voltage in Low State

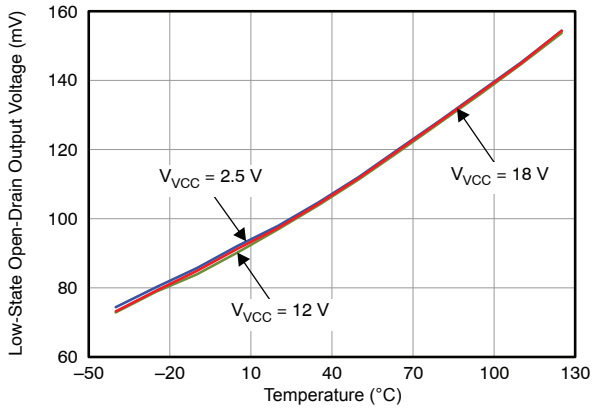


Figure 22. FFLTb Open-Drain Output Voltage in Low State

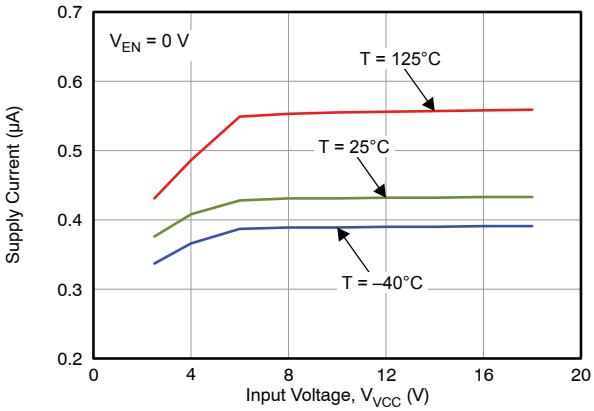


Figure 23. Supply Current vs Input Voltage at Various Temperatures When EN Pulled Low

TYPICAL CHARACTERISTICS (continued)

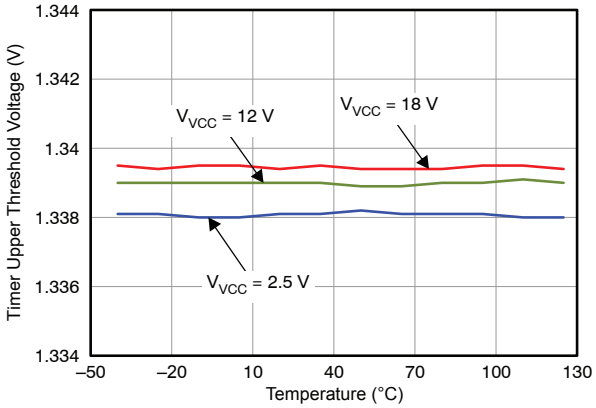


Figure 24. Timer Upper Threshold Voltage vs Temperature at Various Input Voltages

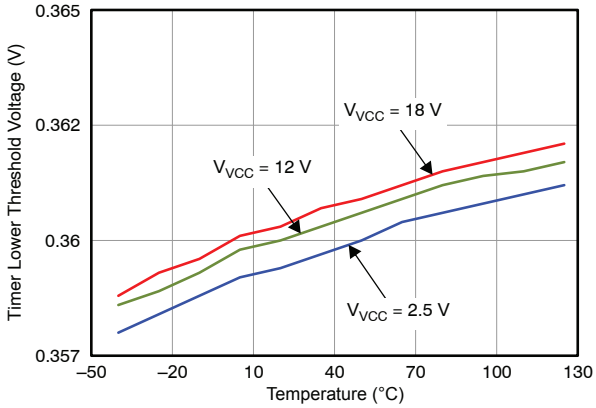


Figure 25. Timer Lower Threshold Voltage vs Temperature at Various Input Voltages

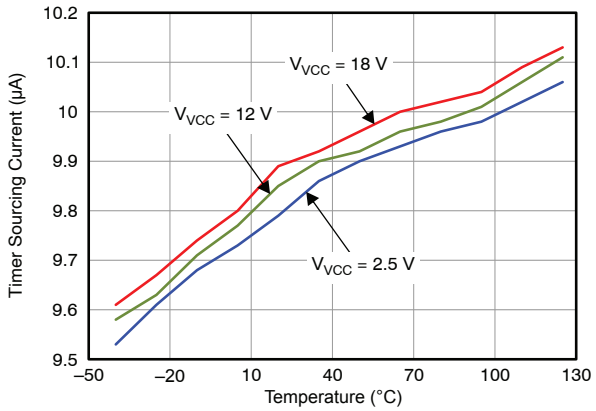


Figure 26. Timer Sourcing Current vs Temperature at Various Input Voltages

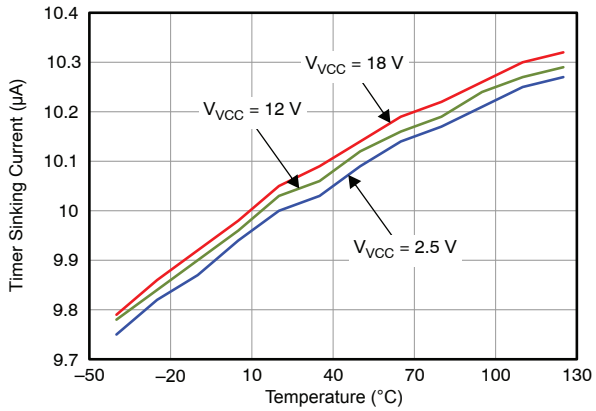


Figure 27. Timer Sinking Current vs Temperature at Various Input Voltages

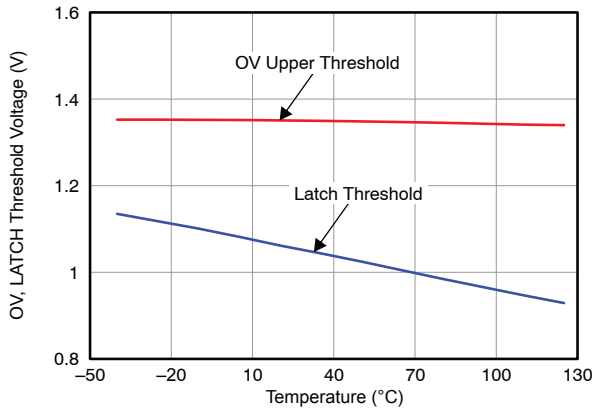


Figure 28. OV and LATCH Threshold Voltage vs Temperature

SYSTEM OPERATION

INTRODUCTION

The TPS24720 provides all the features needed for a positive hot-swap controller. These features include:

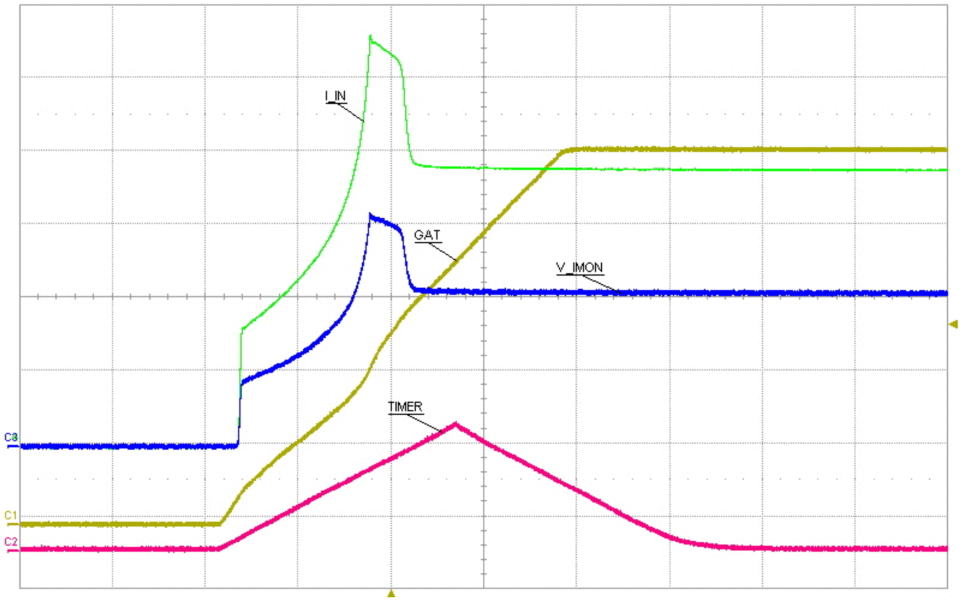
- Undervoltage lockout
- Adjustable (system-level) enable
- Turn-on inrush limiting
- High-side gate drive for an external N-channel MOSFET
- MOSFET protection by power limiting
- Adjustable overload timeout, also called an electronic circuit breaker
- Charge-complete indicator for downstream converter coordination
- A choice of latch or automatic restart mode
- A low-power disable mode accessed by holding ENSD low
- MOSFET short detection
- Load overvoltage protection

The typical application diagram, shown on the front page of this datasheet, and oscilloscope plots, shown in Figure 29 through Figure 31 and Figure 33 through Figure 36, demonstrate many of the functions described previously.

BOARD PLUG-IN

Figure 29 and Figure 30 illustrate the inrush current that flows when a hot swap board under the control of the TPS24720 is plugged into a system bus. Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS24720 is held inactive for a short period while internal voltages stabilize. In this short period, GATE, PROG, and TIMER are held low and PGb, FLTb, and FFLTb are held open-drain. When the voltage on the internal VCC rail exceeds approximately 1.5 V, the power-on reset (POR) circuit initializes the TPS24720 and a start-up cycle is ready to take place.

GATE, PROG, TIMER, PGb, FLTb and FFTb are released after the internal voltages have stabilized and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin to turn on MOSFET M_1. The TPS24720 monitors both the drain-to-source voltage across MOSFET M_1 and the drain current passing through it. Based on these measurements, the TPS24720 limits the drain current by controlling the gate voltage so that the power dissipation within the MOSFET does not exceed the power limit programmed by the user. The current increases as the voltage across the MOSFET decreases until finally the current reaches the current limit I_{LIM}.



I_IN: Input Current, 2 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_IMON: Voltage on IMON Pin, 200 mV/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C001

Figure 29. Inrush Mode at Hot-Swap Circuit Insertion

INRUSH OPERATION

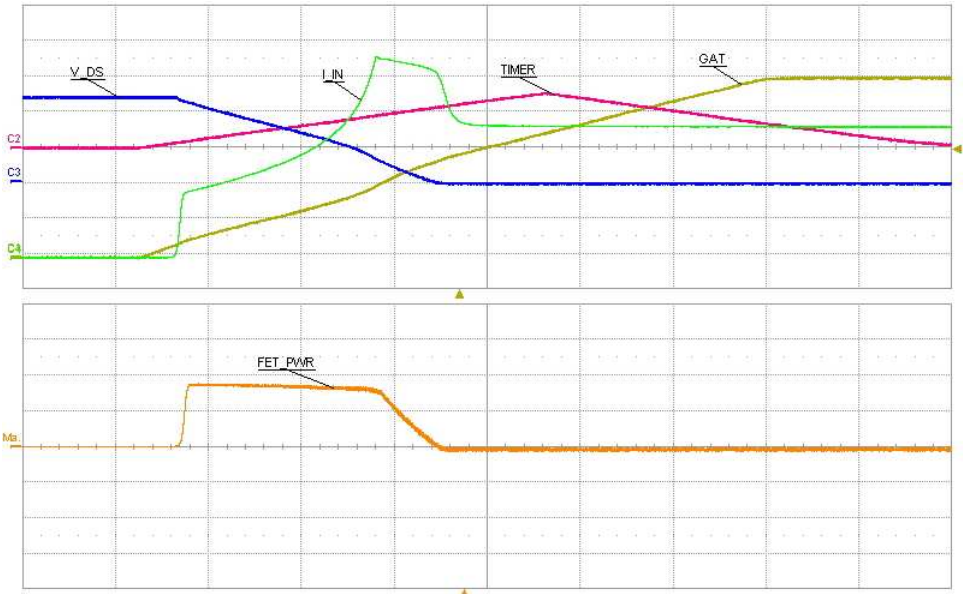
When the TPS24720 activates the MOSFET M_1, a current flows into the downstream bulk storage capacitors. When this current exceeds the limit set by the power-limit engine, the gate of the MOSFET is regulated by a feedback loop to make the MOSFET current rise in a controlled manner. This not only limits the capacitor-charging inrush current but it also limits the power dissipation of the MOSFET to safe levels. A more complete explanation of the power-limiting scheme is given in the section entitled *Action of the Constant Power Engine*. At the instant when the current in R_{SENSE} reaches the programmed limit, the TIMER pin begins to charge the timing capacitor C_T with a current of approximately 10 µA. The TIMER pin continues to charge C_T until $V_{(GATE - VCC)}$ reaches the timer activation voltage (6 V for V_{VCC} = 12 V). The TIMER then begins to discharge C_T with a current of approximately 10 µA. This indicates that the inrush mode is finished. If the TIMER exceeds its upper threshold of 1.35 V before $V_{(GATE - VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot-swap circuit enters either latch mode or auto-retry mode, depending upon the status of the LATCH pin (see LATCH in *Detailed Pin Descriptions*).

The power limit feature is disabled once the inrush operation is finished and the hotswap circuit becomes a circuit breaker. The TPS24720 will turn off the MOSFET M1 after a fault timer period once the load exceeds the current limit threshold.

ACTION OF THE CONSTANT-POWER ENGINE

Figure 30 illustrates the operation of the constant-power engine during start-up. The circuit used to generate the waveforms of Figure 30 was programmed to a power limit of 29.3 W by means of the resistor connected between PROG and GND. At the moment current begins to flow through the MOSFET, a voltage of 12 V appears across it (input voltage V_{VCC} = 12 V), and the constant-power engine therefore allows a current of 2.44 A (equal to 29.3 W divided by 12 V) to flow. This current increases in inverse ratio as the drain-to-source voltage diminishes, so as to maintain a constant dissipation of 29.3 W. The constant-power engine adjusts the current by altering the reference signal fed to the current limit amplifier. The lower part of Figure 31 shows the measured power

dissipated within the MOSFET, labeled *FET PWR*, remaining substantially constant during this period of operation, which ends when the current through the MOSFET reaches the current limit I_{LIM}. This behavior can be considered a form of foldback limiting, but unlike the standard linear form of foldback limiting, it allows the power device to operate near its maximum capability, thus reducing the start-up time and minimizing the size of the required MOSFET.



I_IN: Input Current, 2 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_DS: Drain-to-Source Voltage of M1, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
FET_PWR: Power on M1 (product of V_DS and I_IN), 19 W/div
Time: 10 ms/div

C002

Figure 30. Computation of M_1 Power Stress During Startup

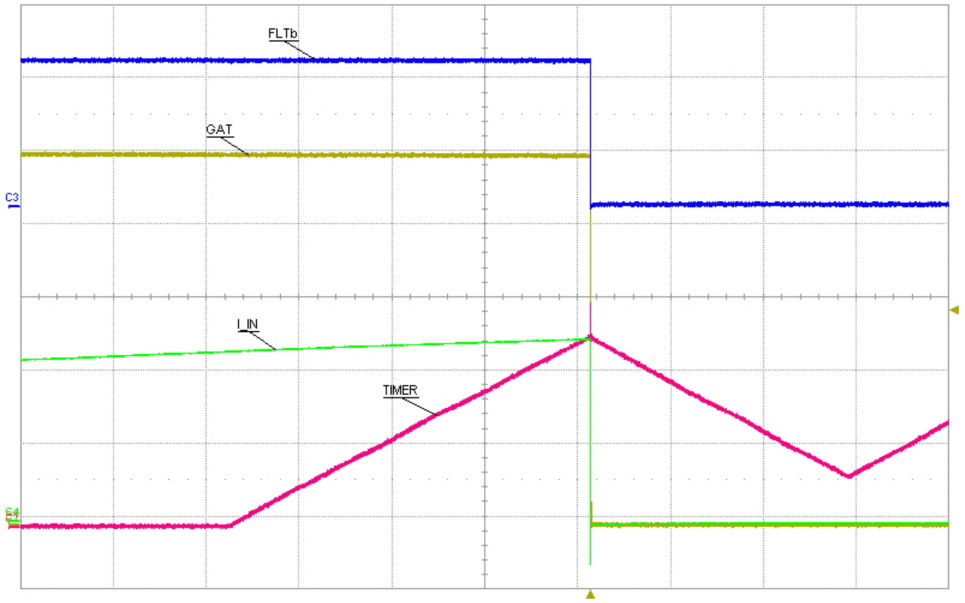
CIRCUIT BREAKER AND FAST TRIP

The TPS24720 monitors load current by sensing the voltage across R_{SENSE}. The TPS24720 incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold.

The functions of circuit breaker and fast-trip turn off are shown in Figure 31 through Figure 34.

Figure 31 shows the behavior of the TPS24720 when a fault in the output load causes the current passing through R_{SENSE} to increase to a value above the current limit but less than the fast-trip threshold. When the current exceeds the current-limit threshold, a current of approximately 10 µA begins to charge timing capacitor C_T. If the voltage on C_T reaches 1.35 V, then the external MOSFET is turned off. The TPS24720 either latches off or commences a restart cycle, depending upon the state of the LATCH pin. In either event, fault pin FLTb pulls low to signal a fault condition. Overload between the current limit and the fast-trip threshold is permitted for this period. This shutdown scheme is sometimes called an electronic circuit breaker.

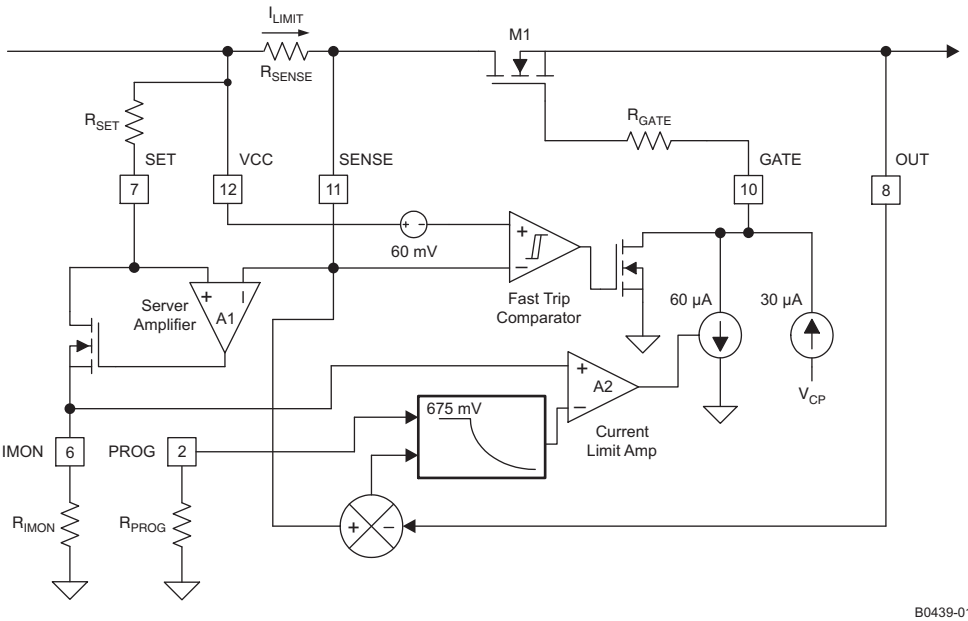
The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor R_{SENSE} exceeds the 60-mV fast-trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximately 1 A of current. This extremely rapid shutdown may generate disruptive transients in the system, in which case a low-value resistor inserted between the GATE pin and the MOSFET gate can be used to moderate the turn off current. The fast-trip circuit holds the MOSFET off for only a few microseconds, after which the TPS24720 turns back on slowly, allowing the current-limit feedback loop to take over the gate control of M_1. Then the hot-swap circuit goes into latch mode or auto-retry mode, depending on pre-determined conditions. Figure 33 and Figure 34 illustrate the behavior of the system when the current exceeds the fast-trip threshold.



I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
FLTb: Voltage on FLTb Pin, 2 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

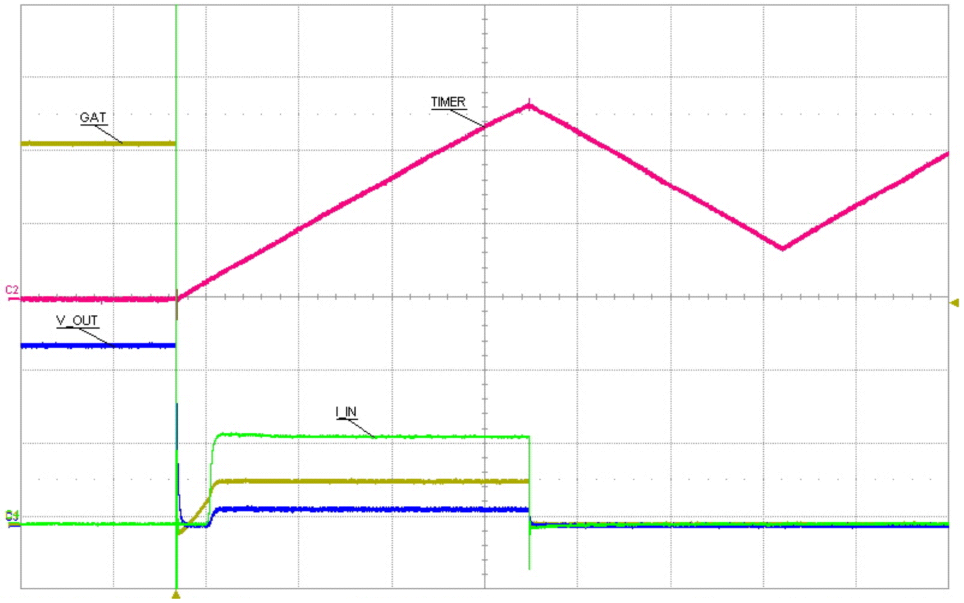
C003

Figure 31. Circuit-Breaker Mode During Overload Condition



B0439-01

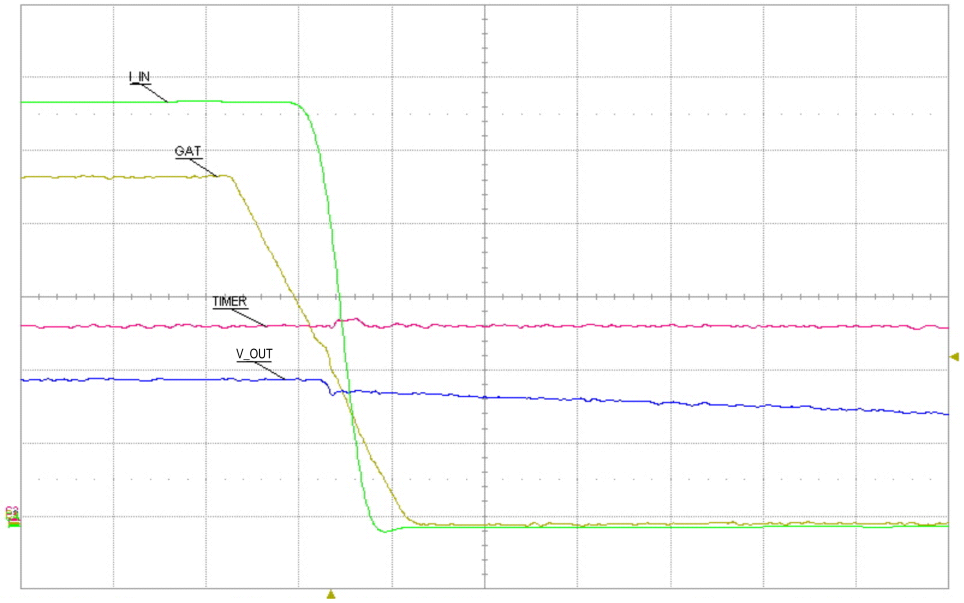
Figure 32. Partial Diagram of the TPS24720 With Selected External Components



I_IN: Input Current, 1 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C004

Figure 33. Current Limit During Output-Load Short-Circuit Condition (Overview)



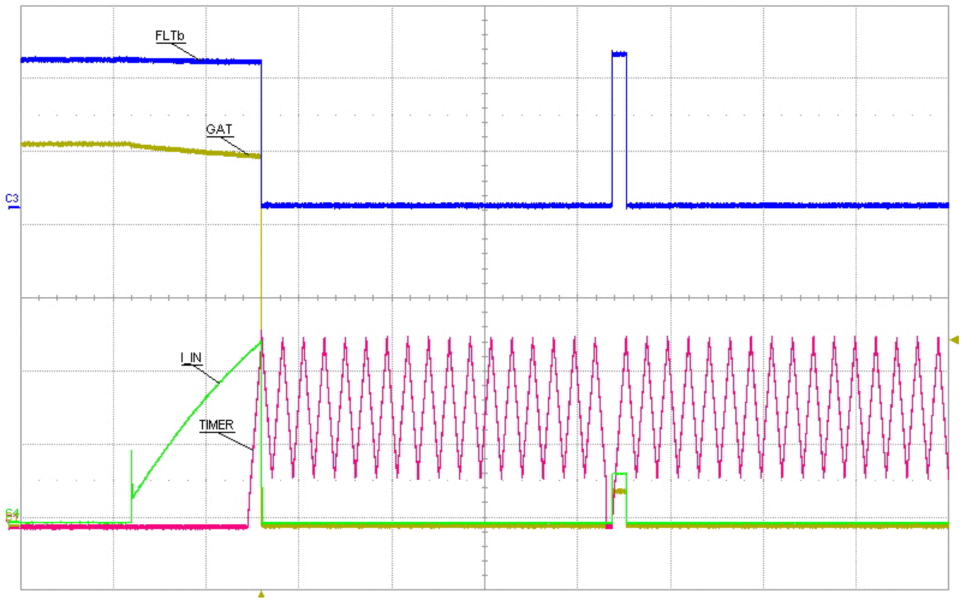
I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 10 µs/div

C005

Figure 34. Current Limit During Output-Load Short-Circuit Condition (Onset)

AUTOMATIC RESTART

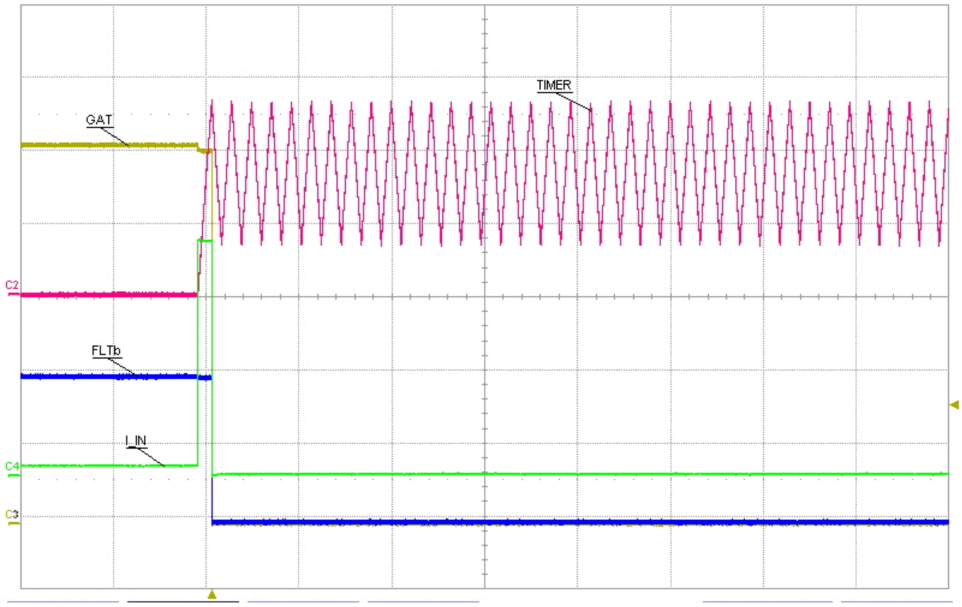
If LATCH is connected to GND, then the TPS24720 automatically initiates a restart after a fault has caused it to turn off the external MOSFET M_1. Internal control circuits use C_T to count 16 cycles before re-enabling M_1 as shown in Figure 35. This sequence repeats if the fault persists. The timer has a 1 : 1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0 V and rises to the upper threshold of 1.35 V and subsequently falls to 0.35 V before restarting. For the following 16 cycles, 0.35 V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.



I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
FLTb: Voltage on FLTb Pin, 2 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 50 ms/div

C006

Figure 35. Auto-Restart Cycle Timing



I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
FLTb: Voltage on FLTb Pin, 2 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 50 ms/div

C007

Figure 36. Latch After Overload Fault

PGb, FLTb, AND TIMER OPERATIONS

The open-drain PGb output provides a deglitched end-of-inrush indication based on the voltage across M_1. PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor C_{OUT} is still charging. PGb goes active-low about 3.4 ms after C_{OUT} is charged. This delay allows M_1 to fully turn on and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the power-limiting engine allows the MOSFET to conduct the full current set by the current limit I_{LIM}. Failure to observe this precaution may prevent the system from starting. The pullup resistor shown on the PGb pin in the typical application diagram on the front page is illustrative only; the actual connection to the converter depends on the application. The PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. Care should be taken to ensure that the MOSFET on-resistance is sufficiently small to ensure that the voltage drop across this transistor is less than the minimum power-good threshold of 140 mV. After the hot-swap circuit successfully starts up, the PGb pin can return to a high-impedance status whenever the drain-to-source voltage of MOSFET M_1 exceeds its upper threshold of 340 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, input overvoltage, higher die temperature, or the GATE shutdown by UVLO, EN or ENSD.

FLTb is an indicator that the allowed fault-timer period during which the load current can exceed the programmed current limit (but not the fast-trip threshold) expires. The fault timer starts when a current of approximately 10 µA begins to flow into the external capacitor, C_T, and ends when the voltage of C_T reaches TIMER upper threshold, i.e., 1.35 V. FLTb pulls low at the end of the fault timer. Otherwise, FLTb assumes a high-impedance state.

The fault-timer state requires an external capacitor C_T connected between the TIMER pin and GND pin. The duration of the fault timer is the charging time of C_T from 0 V to its upper threshold of 1.35 V. The fault timer begins to count under any of the following three conditions:

1. In the inrush mode, TIMER begins to source current to the timer capacitor, C_T, when MOSFET M_1 is enabled. TIMER begins to sink current from the timer capacitor, C_T when $V_{(GATE - VCC)}$ exceeds the timer activation voltage (see the *Inrush Operation* section). If $V_{(GATE - VCC)}$ does not reach the timer activation voltage before TIMER reaches 1.35 V, then the TPS24720 disables the external MOSFET M_1. After the MOSFET turns off, the timer goes into either latch mode or retry mode, depending on the LATCH pin status.
2. In an overload fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode or retry mode, depending on the LATCH pin status.
3. In output short-circuit fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits following a fast-trip shutdown of M_1. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode or retry mode, depending on the LATCH pin status.

If the fault current drops below the programmed current limit within the fault timer period, V_{TIMER} decreases and the pass MOSFET remains enabled.

The behaviors of TIMER are different in the latch mode and retry mode. If the timer capacitor reaches the upper threshold of 1.35 V, then:

- In latch mode, the TIMER pin continues to charge and discharge the attached capacitor periodically until TPS24720 is disabled by UVLO, EN, ENSD, or OV, as shown in Figure 36.
- In retry mode, TIMER charges and discharges C_T between the lower threshold of 0.35 V and the upper threshold of 1.35 V for sixteen cycles before the TPS24720 attempts to re-start. The TIMER pin is pulled to GND at the end of the 16^{th} cycle of charging and discharging and then ramps from 0 V to 1.35 V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the TPS24720 is disabled by UVLO, EN, ENSD, or OV.

OVERTEMPERATURE SHUTDOWN

The TPS24720 includes a built-in overtemperature shutdown circuit designed to disable the gate driver if the die temperature exceeds approximately 140°C. An overtemperature condition also causes the FLTb, FFLTb and PGb pins to go to high-impedance states. Normal operation resumes once the die temperature has fallen approximately 10°C.

START-UP OF HOT-SWAP CIRCUIT BY VCC OR EN

The connection and disconnection between a load and the input power bus are controlled by turning on and turning off the MOSFET, M_1.

The TPS24720 has two ways to turn on MOSFET M_1:

- Increasing V_{VCC} above UVLO upper threshold while EN is already higher than its upper threshold sources current to the GATE pin. After an inrush period, the TPS24720 fully turns on MOSFET M_1.
- Increasing EN above its upper threshold while V_{VCC} is already higher than the UVLO upper threshold sources current to the GATE pin. After an inrush period, the TPS24720 fully turns on MOSFET M_1.

The EN pin can be used to start up the TPS24720 at a selected input voltage V_{VCC}.

To isolate the load from the input power bus, the GATE pin sinks current and pulls the gate of MOSFET M_1 low. The MOSFET can be disabled by any of the following conditions: UVLO, EN, ENSD, load current above the current-limit threshold, hard short at load, OV, or OTSD. Three separate mechanisms pull down the GATE pin:

1. GATE is pulled down by an 11-mA current source when any of the following occurs.
   - The fault timer expires during an overload current fault (V_{IMON} > 675 mV).
   - V_{EN} is below its falling threshold.
   - V_{VCC} drops below the UVLO threshold.
   - V_{OV} is above its rising threshold.
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC - SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold or ENSD is pulled low.

MINIMIZATION OF POWER DISSIPATION AT STANDY BY ENSD

The ENSD pin enables the use of TPS24720 in applications requiring a low-power standby mode. When this pin is pulled below its threshold voltage, all the internal circuitry is switched off and the GATE pin is discharged to GND through a 20-kΩ resistor. Thus, the MOSFET is disabled and power consumption is kept to a minimum. The correct procedure to go into standby mode is first to shut down the TPS24720 by using the EN pin and then to pull the ENSD pin low.

FAULT DETECTION OF MOSFET SHORT WITH FFLTb

One of the salient features of the TPS24720 is the detection of short-circuited MOSFETs by the FFLTb pin. The FFLTb is pulled low to indicate a FET short if all the following conditions occur.

- EN is below its threshold voltage.
- V_{VCC} is above the UVLO threshold.
- V_{IMON} > 103 mV.

The fact that GATE is turned off but current is still flowing through R_{SENSE} indicates a drain-to-source short.

DESIGN EXAMPLE: POWER-LIMITED START-UP

This design example assumes a 12-V system voltage with an operating tolerance of ±2 V. The rated load current is 10 A, corresponding to a dc load of 1.2 Ω. If the current exceeds 12 A, then the controller should shut down and then attempt to restart. Ambient temperatures may range from 20°C to 50°C. The load has a minimum input capacitance of 470 µF. Figure 37 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of MOSFET M_1 under both static and transient conditions by proper selection of package, cooling, $r_{DS(on)}$, current limit, fault timeout, and power limit. The design procedure further assumes that a unit running at full load and maximum ambient temperature experiences a brief input power interruption sufficient to discharge C_{OUT}, but short enough to keep M_1 from cooling. A full C_{OUT} recharge then takes place. Adjust this procedure to fit the application and design criteria.

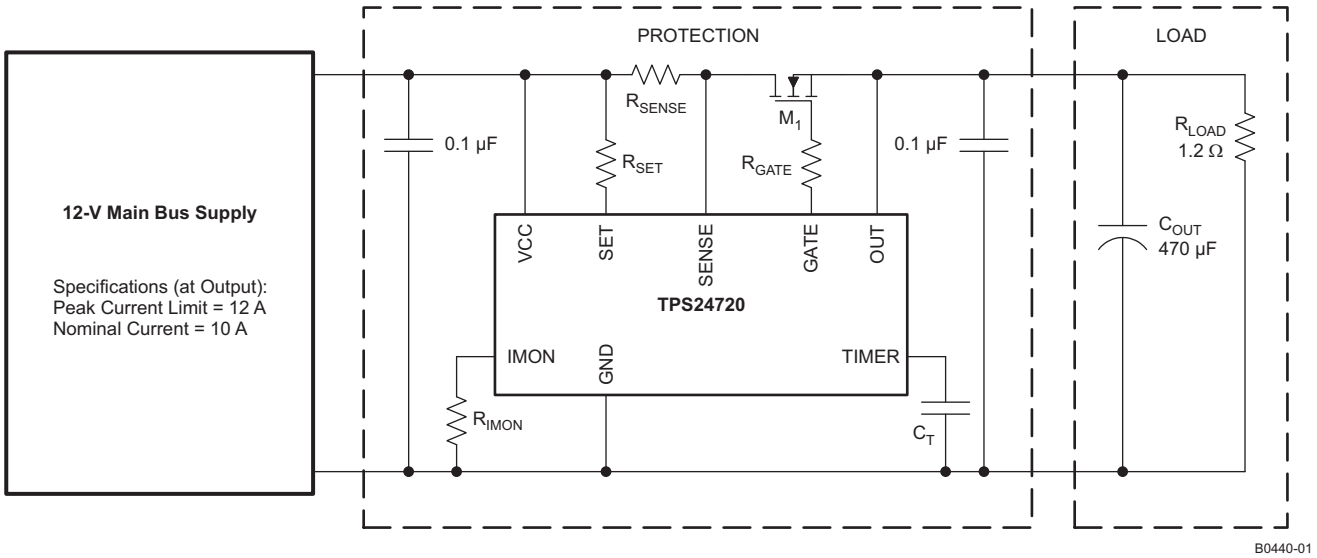


Figure 37. Simplified Block Diagram of the System Constructed in the Design Example

STEP 1. Choose R_{SENSE}, R_{SET}, and R_{IMON}

The recommended range of the current-limit threshold voltage, $V_{(VCC - SENSE)}$, extends from 10 mV to 42 mV. Values near the low threshold of 10 mV may be affected by system noise. Values near the upper threshold of 42 mV may be too close to the minimum fast-trip threshold voltage of 52 mV. Values near the middle of this range help minimize both concerns.

To achieve high efficiency, the power dissipation in R_{SENSE} must be kept to a minimum. A R_{SENSE} of 2 mΩ develops a voltage of 24 mV at the specified peak current limit of 12 A, while dissipating only 200 mW at the rated 10-A current. This represents a 0.17% power loss.

For best performance, a current of approximately 0.5 mA (referring to the RECOMMENDED OPERATING CONDITIONS table) should flow into the SET pin and out of the IMON pin when the TPS24720 is in current limit. The voltage across R_{SET} nominally equals the voltage across R_{SENSE}, or 24 mV. Dividing 24 mV by 0.5 mA gives a recommended value of R_{SET} of 48 Ω. A 51.1-Ω, 1% resistor was chosen. Using Equation 3, the value of R_{IMON} must equal 1437 Ω, or as near as practically possible. A 1.43-kΩ, 1% resistor was chosen.

$$R_{IMON} = \frac{0.675\ V \times R_{SET}}{I_{LIM} \times R_{SENSE}},$$

therefore,

$$R_{IMON} = \frac{0.675\ V \times 51.1\ \Omega}{12\ A \times 2\ m\Omega} = 1437\ \Omega \quad (5)$$

STEP 2. Choose MOSFET M_1

The next design step is to select M_1. The TPS24720 is designed to use an N-channel MOSFET with a gate-to-source voltage rating of 20 V.

Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected so as to limit the maximum gate-to-source voltage the transistor sees.

The next factor to consider is the drain-to-source voltage rating, $V_{DS(MAX)}$, of the MOSFET. Although the MOSFET only sees 12 V dc, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff that occurs during a fast trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice the nominal input power-supply voltage is recommended regardless of whether a TVS is used or not.

Next select the on-resistance of the transistor, $r_{DS(on)}$. The maximum on-resistance must not generate a voltage greater then the minimum power-good threshold voltage of 140 mV. Assuming a current limit of 12 A, a maximum $r_{DS(on)}$ of 11.67 mΩ is required. Also consider the effect of $r_{DS(on)}$ on the maximum operating temperature $T_{J(MAX)}$ of the MOSFET. Equation 6 computes the value of $r_{DS(on)(MAX)}$ at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $r_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. Compute the maximum allowable on-resistance, $r_{DS(on)(MAX)}$, using Equation 6.

$$r_{DS(on)(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{I_{MAX}^2 \times R_{\theta JA}},$$

therefore,

$$r_{DS(on)(MAX)} = \frac{150°C - 50°C}{(12\ A)^2 \times 51°C/W} = 13.6\ m\Omega \quad (6)$$

Taking these factors into consideration, the TI CSD16403Q5 was selected for this example. This transistor has a $V_{GS(MAX)}$ rating of 16 V, a $V_{DS(MAX)}$ rating of 25 V, and a maximum $r_{DS(on)}$ of 2.8 mΩ at room temperature. During normal circuit operation, the MOSFET can have up to 10 A flowing through it. The power dissipation of the MOSFET equates to 0.24 W and an 9.6°C rise in junction temperature. This is well within the data sheet limits for the MOSFET. The power dissipated during a fault (e.g., output short) is far larger than the steady-state power. The power handling capability of the MOSFET must be checked during fault conditions.

STEP 3. Choose Power-Limit Value, P_{LIM}, and R_{PROG}

MOSFET M_1 dissipates large amounts of power during inrush. The power limit P_{LIM} of the TPS24720 should be set to prevent the die temperature from exceeding a short-term maximum temperature, $T_{J(MAX)2}$. The short-term $T_{J(MAX)2}$ could be set as high as 150°C while still leaving ample margin to the usual manufacturer's rating of 175°C. Equation 7 is an expression for calculating P_{LIM},

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2} - \left[\left(I_{MAX}^2 \times r_{DS(on)} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}},$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{130°C - \left[\left((12\ A)^2 \times 0.002\ \Omega \times (51°C/W - 1.8°C/W)\right) + 50°C\right]}{1.8°C/W} = 29.3\ W \quad (7)$$

where $R_{\theta JC}$ is the junction-to-case thermal resistance of the MOSFET, $r_{DS(on)}$ is the its resistance at the maximum operating temperature, and the factor of 0.8 represents the tolerance of the constant-power engine. For an ambient temperature of 50°C, the calculated maximum P_{LIM} is 29.3 W. From Equation 1, a 53.6-kΩ, 1% resistor is selected for R_{PROG} (see Equation 8).

$$R_{PROG} = \frac{3125}{P_{LIM} \times R_{SENSE}},$$

therefore,

$$R_{PROG} = \frac{3125}{29.3\ W \times 0.002\ \Omega} = 53.15\ k\Omega \quad (8)$$

STEP 4. Choose Output Voltage Rising Time, t_{ON}, and Timing Capacitor C_T

The maximum output voltage rise time, t_{ON}, set by timer capacitor C_T must suffice to fully charge the load capacitance C_{OUT} without triggering the fault circuitry. Equation 9 defines t_{ON} for two possible inrush cases. Assuming that only the load capacitance draws current during startup,

$$t_{ON} = \begin{cases} \dfrac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}^2} + \dfrac{C_{OUT} \times V_{VCC(MAX)}^2}{2 \times P_{LIM}} - \dfrac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} < I_{LIM} \times V_{VCC(MAX)} \\ \dfrac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} > I_{LIM} \times V_{VCC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\ \mu F \times 29.3\ W}{2 \times (12\ A)^2} + \frac{470\ \mu F \times (12\ V)^2}{2 \times 29.3\ W} - \frac{470\ \mu F \times 12\ V}{12\ A} = 0.614\ ms \tag{9}$$

The next step is to determine the minimum fault-timer period. In Equation 9, the output rise time is t_{ON}. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the TPS24720 is still in inrush limit. The fault timer continues to run until V_{GS} rises 6 V (for V_{VCC} = 12 V) above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault time can be calculated using Equation 10,

$$t_{FLT} = t_{ON} + \frac{6\ V \times C_{ISS}}{I_{GATE}},$$

therefore,

$$t_{FLT} = 0.614\ ms + \frac{6\ V \times 2040\ pF}{20\ \mu A} = 1.23\ ms \tag{10}$$

where C_{ISS} is the MOSFET input capacitance and I_{GATE} is the minimum gate sourcing current of TPS24720, or 20 µA. Using the example parameters and the CSD16403Q5 data sheet in Equation 10 leads to a minimum fault time of 1.23 ms. This time is derived considering the tolerances of C_{OUT}, C_{ISS}, I_{LIM}, P_{LIM}, I_{GATE}, and $V_{VCC(MAX)}$. The fault timer must be set to a value higher than 1.23 ms to avoid turning off during start-up, but lower than any maximum fault time limit determined by the device SOA curve.

There is a maximum time limit set by the SOA curve of the MOSFET. Referring to Figure 38, which shows the CSD16403Q5 SOA curve at T_J = 25°C, the MOSFET can tolerate 12 A with 12 V across it for approximately 20 ms. If the junction temperature T_J is other than 25°C, then the pulse time should be scaled by a factor of (150°C – T_J) / (150°C – 25°C). Therefore, the fault timer should be set between 1.23 ms and 20 ms. For this example, we will select 7 ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation 11 as 52 nF. Selecting the next-highest standard value, 56 nF, yields a 7.56-ms fault time.

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT},$$

therefore,

$$C_T = \frac{10\ \mu A}{1.35\ V} \times 7\ ms = 52\ nF \tag{11}$$

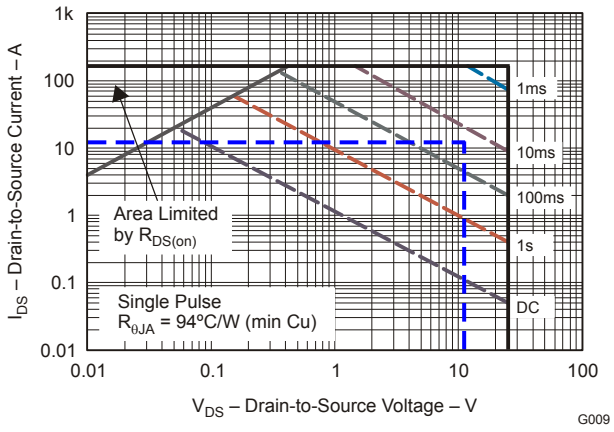


Figure 38. CSD16403Q5 SOA Curve

STEP 5. Calculate the Retry-Mode Duty Ratio

In retry mode, the TPS24720 is on for one charging cycle and off for 16 charge/discharge cycles, as can be seen in Figure 35. The first C_T charging cycle is from 0 V to 1.35 V, which gives 7.56 ms. The first C_T discharging cycle is from 1.35 V to 0.35 V, which gives 5.6 ms. Therefore, the total time is 7.56 ms + 33 x 5.6 ms = 192.36 ms. As a result, the retry mode duty ratio is 7.56 ms/192.36 ms = 3.93%.

STEP 6. Select R_1, R_2, and R_3 for UV and OV

Next, select the values of the OV and UV resistors, R_1, R_2, and R_3, as shown in the typical application diagram on the front page. From the TPS24720 electrical specifications, $V_{OVTHRESH}$ = 1.35 V and $V_{ENTHRESH}$ = 1.35 V. V_{OV} is the overvoltage trip voltage, which in this case is 14 V. V_{UV} is the undervoltage trip voltage, which for this example equals 10.8 V.

$$V_{ENTHRESH} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \tag{12}$$

$$V_{UVTHRESH} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \tag{13}$$

Assume R_3 is 1 kΩ and use Equation 12 to solve for (R_2 + R_3). Use Equation 13 and the (R_2 + R_3) from Equation 12 to solve for R_2 and finally for R_3. From Equation 12, (R_2 + R_3) = 9370.4 Ω. From Equation 13, R_2 = 296 Ω and R_1 = 9.074 kΩ. Scaling all three resistors by a factor of ten to use less supply current for these voltage references and using standard 1% resistor values gives R_1 = 90.9 kΩ, R_2 = 2.94 kΩ, and R_3 = 10 kΩ.

STEP 7. Choose R_{GATE}, R_4, R_5, R_6, and C_1

In the typical application diagram on the front page, the gate resistor, R_{GATE}, is intended to suppress high-frequency oscillations. A resistor of 10 Ω serves for most applications, but if M_1 has a C_{ISS} below 200 pF, then 33 Ω is recommended. Applications with larger MOSFETs and very short wiring may not require R_{GATE}. R_4, R_5, and R_6 are required only if PGb, FLTb, and FFLTb are used; these resistors serve as pullups for the open-drain output drivers. The current sunk by each of these pins should not exceed 2 mA (referring to the RECOMMENDATION OPERATING CONDITIONS table). C_1 is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended.

ALTERNATIVE DESIGN EXAMPLE: GATE CAPACITOR (dV/dt) CONTROL IN INRUSH MODE

The TPS24720 can be used in applications that expect a constant inrush current. This current is controlled by a capacitor connected from the GATE terminal to GND. A resistor of 1 kΩ placed in series with this capacitor prevents it from slowing a fast-turnoff event. In this mode of operation, M_1 operates as a source follower, and the slew rate of the output voltage approximately equals the slew rate of the gate voltage (see Figure 39).

To implement a constant-inrush-current circuit, choose the time to charge, Δt, using Equation 14,

$$\Delta t = \frac{C_{OUT} \times V_{VCC}}{I_{CHG}} \tag{14}$$

where C_{OUT} is the output capacitance, V_{VCC} is the input voltage, and I_{CHG} is the desired charge current. Set P_{LIM} to a value greater than $V_{VCC} \times I_{CHG}$ to prevent power limiting from affecting the desired current.

To select the gate capacitance use Equation 15.

$$C_{GATE} = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{ISS} \quad (15)$$

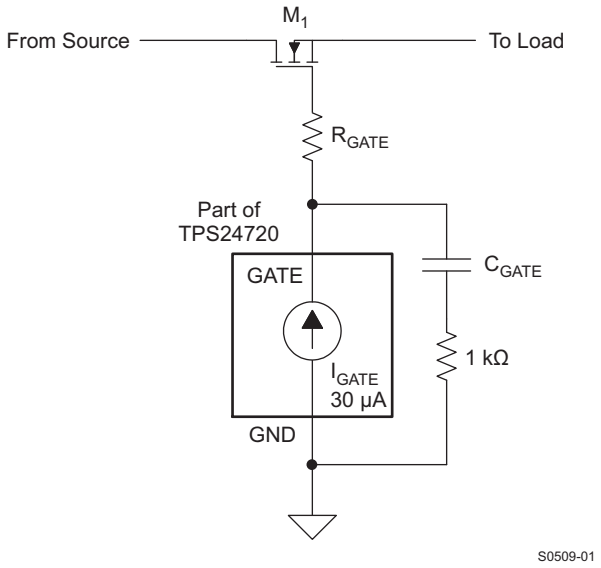


Figure 39. Gate Capacitor (dV/dt) Control Inrush Mode.

ADDITIONAL DESIGN CONSIDERATIONS

Use of PGb

Use the PGb pin to control and coordinate a downstream dc/dc converter. If this is not done, then a long time delay is needed to allow C_{OUT} to fully charge before the converter starts. An undesirable latch-up condition can be created between the TPS24720 output characteristic and the dc/dc converter input characteristic if the converter starts while C_{OUT} is still charging; using the PGb pin is one way to avoid this.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current-limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode should be selected to control the negative voltage at the full short-circuit current. Schottky diodes are generally recommended for this application.

Gate Clamp Diode

The TPS24720 has a relatively well-regulated gate voltage of 12 V–15.5 V with a supply voltage V_{VCC} higher than 4 V. A small clamp Zener from gate to source of M_1 is recommended if V_{GS} of M_1 is rated below 12 V. A series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground.

High-Gate-Capacitance Applications

Gate voltage overstress and abnormally large fault-current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M_1 exceeds about 4000 pF. When gate capacitor dV/dt control is used, a 1-kΩ resistor in series with C_{GATE} is recommended (see Figure 39). If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then a Zener is not necessary .

Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10 nF to 1 µF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low-impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (e.g., 10 nF to 0.1 µF) are often tolerable in these systems.

Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

Layout Considerations

TPS24720 applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces should be as short as possible, but the following list deserves first consideration:

- Decoupling capacitors on VCC pin should have minimal trace lengths to the pin and to GND.
- Traces to SET and SENSE must be short and run side-by-side to maximize common-mode rejection. Kelvin connections should be used at the points of contact with R_{SENSE} (see Figure 40).
- SET runs must be short on both sides of R_{SET}.
- Power path connections should be as short as possible and sized to carry at least twice the full-load current, more if possible.
- Connections to GND and IMON pins should be minimized after the previously described connections have been placed.
- The device dissipates low power, so soldering the thermal pad to the board is not a requirement. However, doing so improves thermal performance and reduces susceptibility to noise.
- Protection devices such as snubbers, TVS, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode shown in the typical application diagram on the front page of the data sheet should be physically close to the OUT pin.

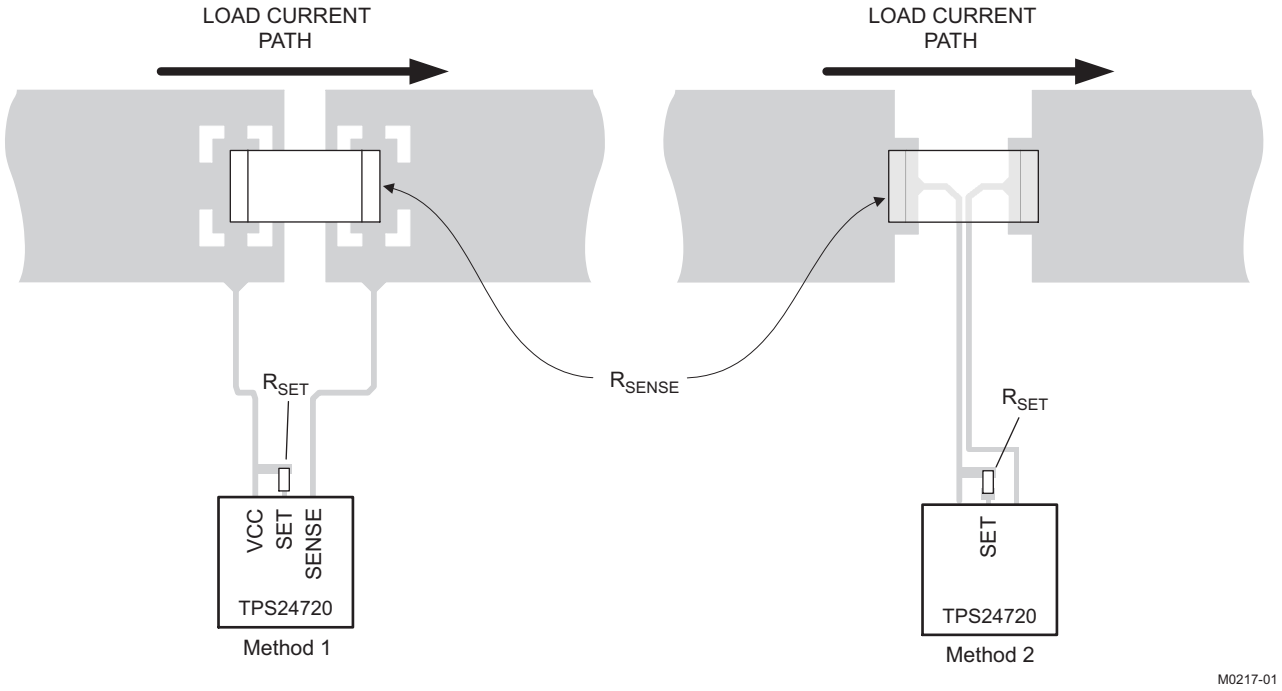


Figure 40. Recommended R_{SENSE} Layout

REVISION HISTORY

Changes from Revision A (April 2011) to Revision B **Page**

- Changed voltages in PGb pin description from 140 mV and 340 mV to 170 mV and 240 mV. 8
- Changed R_{IMON} equation 24

Changes from Revision Original (March 2011) to Revision A **Page**

- Corrected voltages shown in the block diagram 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS24720RGT	PREVIEW	QFN	RGT	16		TBD	Call TI	Call TI	
TPS24720RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS24720RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

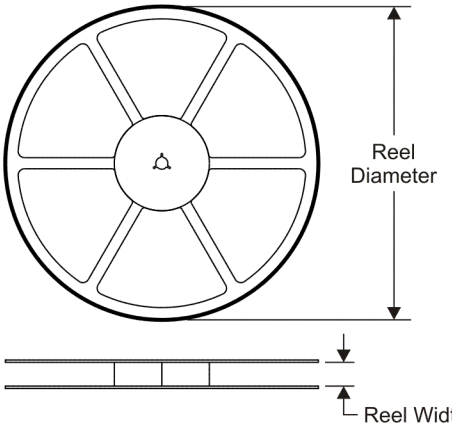
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

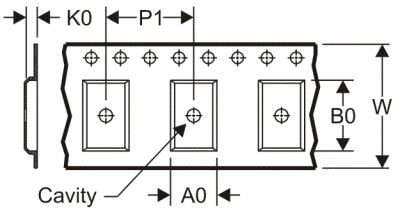
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

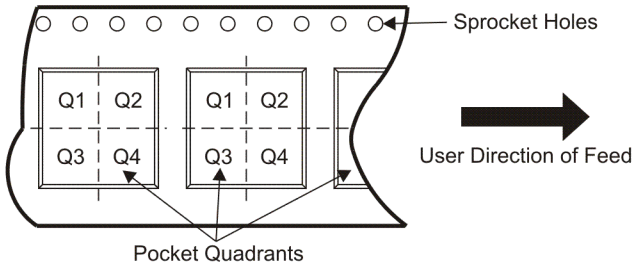


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

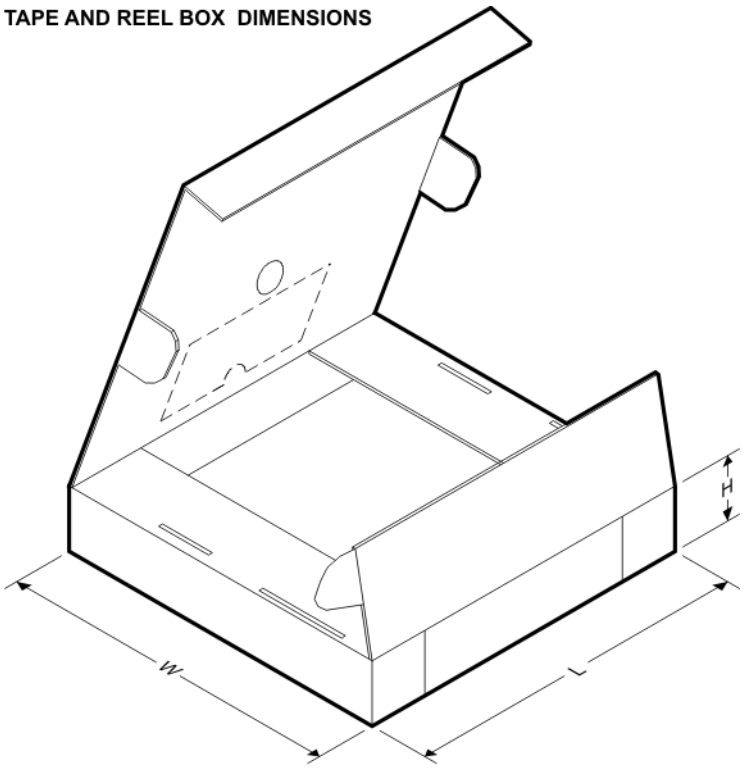
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24720RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS24720RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

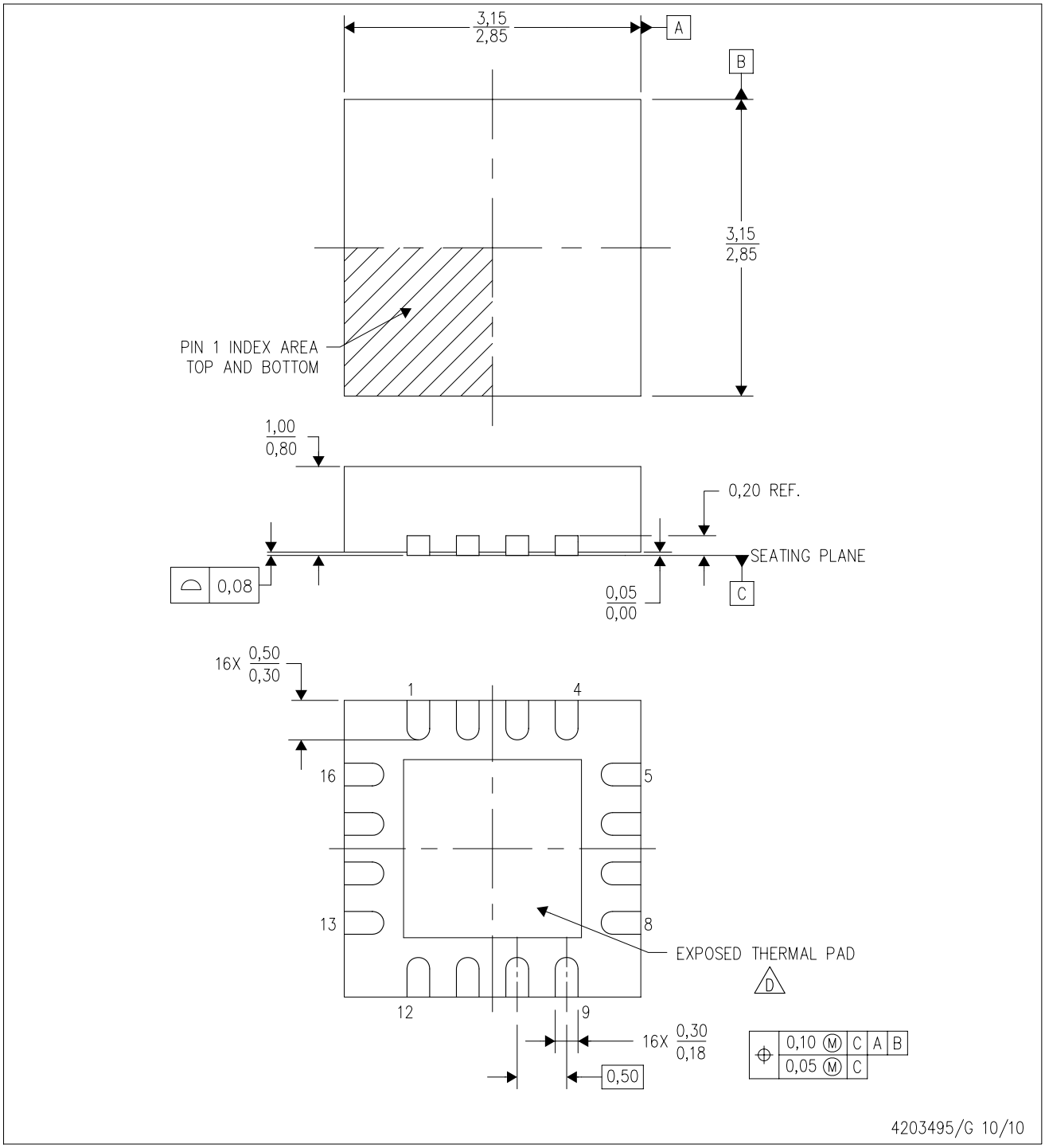
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24720RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
TPS24720RGTT	QFN	RGT	16	250	190.5	212.7	31.8

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

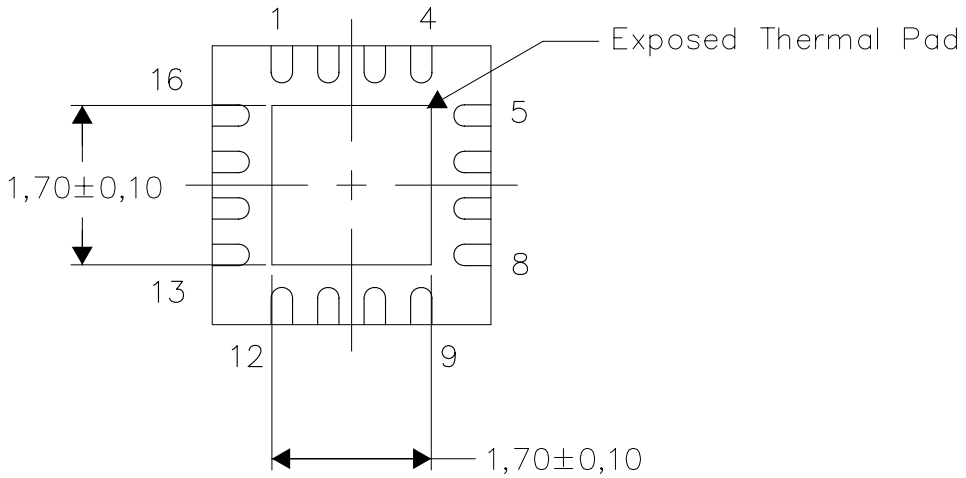
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



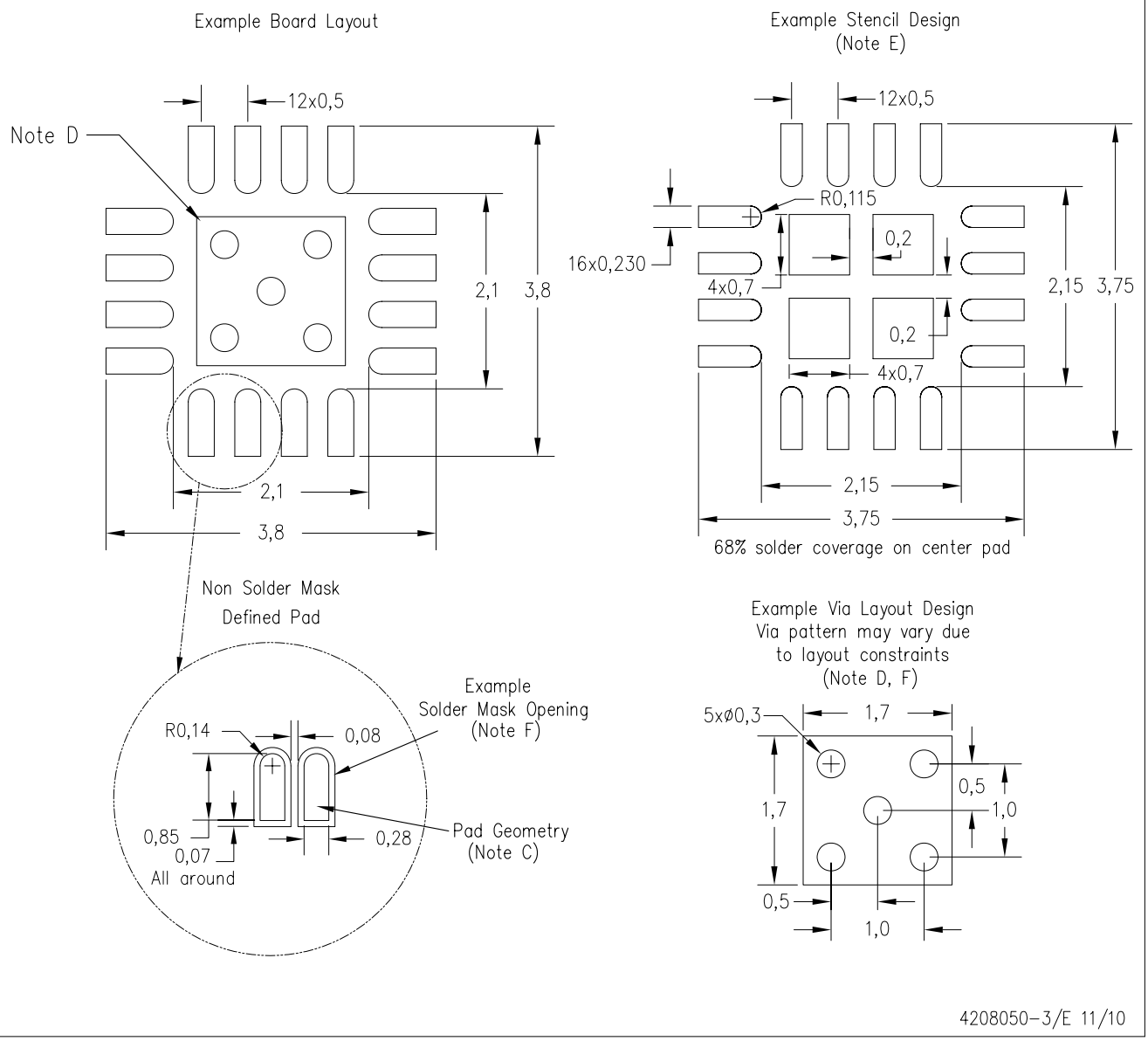
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/0 11/10

NOTE: A. All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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